MimoStar3
User Manual

MimoStar2 User Manual

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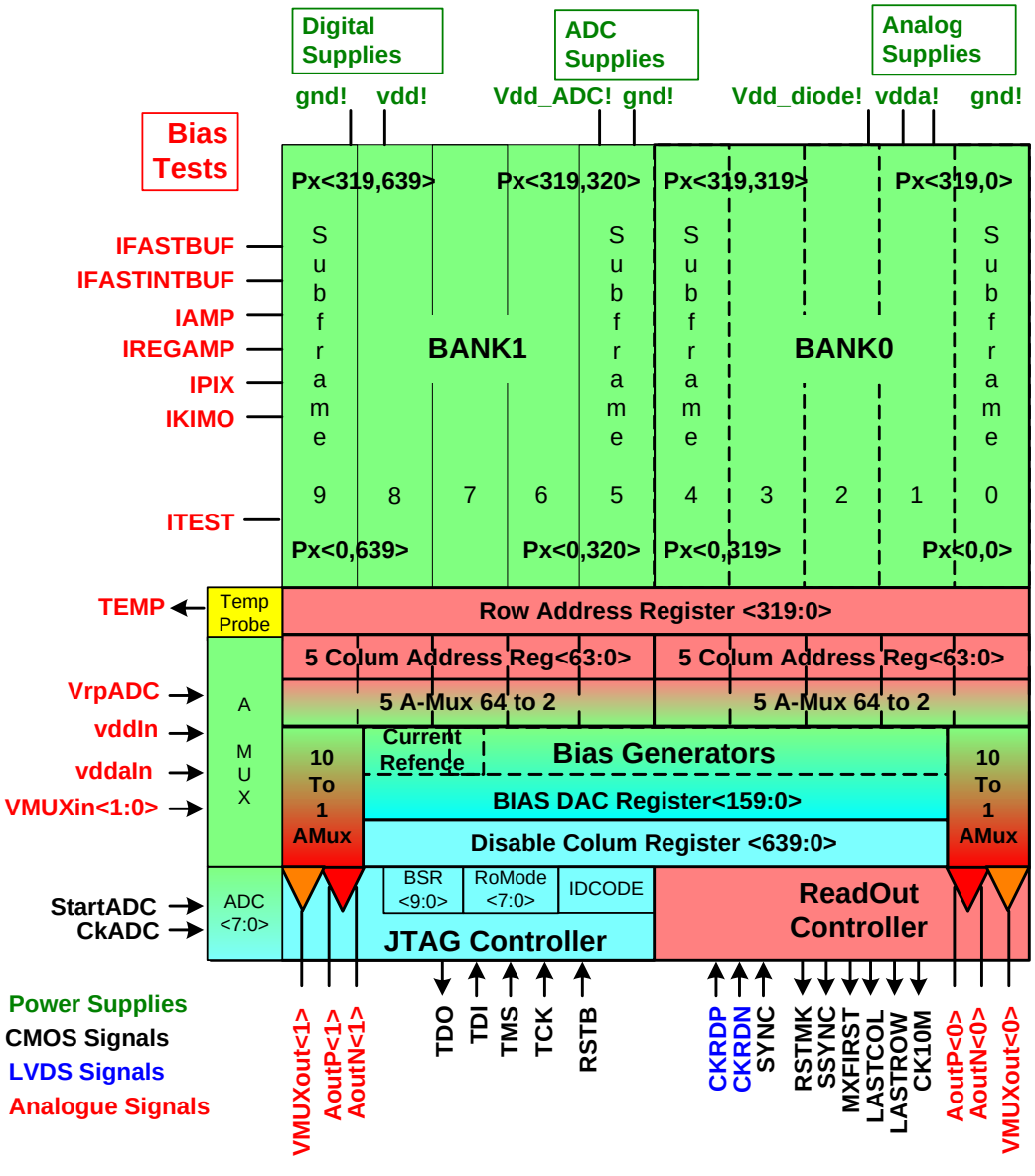
Mimo★

Document history		
Version	Date	Description
1.0	March 2007	Based on MimoStar2 Version

MimoStar chip		
Version	Date	Description
3	Submitted June 06	AMS 035 Opto Version, 640 x 320 pixels
2	Submitted:June 05	AMS 035 Opto Version, 128 x 128 pixels
1	Submitted July 04	TSMC 025 Version

1 Introduction

Mimostar3, the third version of the MimoStar family, has been designed in C35B4O1, the AMS 0.35 µm opto process. Like MimoStar 1 and 2, it is a Monolithic Active Pixel Sensor prototype dedicated to vertex particle tracking in a future update of the STAR vertex detector. The matrix is composed by 320 x 640 pixels of 30 µm pitch and based on self biased diode architectures. It is organised in 10 matrices, or subframes, of 320 lines x 64 columns, accessed in parallel during the readout. The individual pixel architecture, should meet the radiation tolerance and the low leakage current requirements. Actually Mimostar3 prototype has the half size of the final circuit which is foreseen with 640 lines.
The addressing of each subframe is sequential and starts from the upper left pixel up to the lower right pixel. The beginning of each subframe row is stamped by 2 pixels acting as makers and having programmable levels.
The 10 subframes are gathered in 2 banks. Each bank has its own analogue serial output, a differential current output buffer running up to 50 MHz allowing a readout time of 2 ms/frame.



MimoStar3 is very simple to operate:

- Power On Reset or Reset on RSTB pad
- Setup of the chip
  It is performed with programmable registers accessed via an embedded slow control interface. It consists to:
  - Load the DACs which bias the analogue blocks

    - If necessary, load the ReadOut Register with a specific configuration. The default setup on power on reset allows a normal readout once the biases have been set.
- Readout of the chip
    - The chip is driven by a 50 MHz clock. The readout starts when the input "SYNC" token has its falling signal sampled by the internal 5 MHz clock. It happens at the first falling edge of the internal clock which follows the SYNC falling edge.
    - Readout synchronisation is achieved by the digital marker MxFirst which becomes active when the analogue signal of the first pixel appears
    - Other digital makers are available for the control of the readout process
    - Pixels are sequentially read out in a specific order explained later in the document
    - Successive pixel frames are read until the readout clock is stopped

A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

In addition some test features have been implemented in this version:

- 2 single-ended voltage output buffers, one per bank, allows a simpler readout at low frequency. The purpose is to verify coarse parameters, like analogue baseline, directly on the wafer with a probe card.
- An 8 bit ADC running at 100 kHz/word allows some parameter measurements like voltage supplies and current consumption.
- An embedded temperature probe provides its analogue output via 2 output pads.

2 Control Interface

The control interface of MimoStar3 complies with the Boundary Scan, JTAG, IEEE 1149.1 Rev 1999 standard. It allows the access to the internal registers of the chip like the bias register and the readout mode selection register.
On Power-On-Reset, an internal reset for the control interface is generated. The finite state machine of the Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the ID register is selected.

2.1 *JTAG Instruction Set*

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	**5 Bit Code$_{16}$**	**Selected Register**	**Notes**
EXTEST	01	BSR	JTAG mandatory instruction
HIGHZ	02	BYPASS	JTAG optional instruction
INTEST	03	BSR	JTAG optional instruction
CLAMP	04	BYPASS	JTAG optional instruction
SAMPLE_PRELOAD	05	BSR	JTAG mandatory instruction
ID_CODE	0E	ID register	JTAG optional instruction
BIAS_GEN	0F	BIAS register	User instruction
DIS_COL	10	Disable Columns	User instruction
ADC_SEL	11	AnalogIn Select reg	User instruction
ADC_ROR	12	ReadOut Register	User instruction
NU1	13		Reserved, Not Used
NU2	14		Reserved, Not Used
NU3	15		Reserved, Not Used
NU4	16		Reserved, Not Used
NU5	17		Reserved, Not Used
NU6	18		Reserved, Not Used
NU7	19		Reserved, Not Used
NU8	1A		Reserved, Not Used
NU9	1B		Reserved, Not Used
NU10	1C		Reserved, Not Used
RO_MODE1	1D	Read Out Mode1	User instruction
RO_MODE0	1E	Read Out Mode0	User instruction
BYPASS	1F	BYPASS	JTAG mandatory instruction

2.2 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
BYPASS	1	R Only	
BSR	11	R/W	
ID_CODE	32	R Only	Pattern fixed at 0xFFFF0001
BIAS_GEN (20 DACs)	160	R/W	Previous value shifted out during write
DIS_COL	640	R/W	Previous value shifted out during write
ADC_SEL	20	R/W	Previous value shifted out during write
ADC_ROR	11	R Only	Previous ADC value shifted
RO_MODE1	8	R/W	Previous value shifted out during write
RO_MODE0	8	R/W	Previous value shifted out during write
NU1, …, NU10	0		Not implemented. For future use

2.2.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register of MimoStar2 is 5 bits long. On reset, it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

X	**X**	**X**	**1**	**0**

2.2.2 Bypass Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

2.2.3 Boundary Scan Register

The Boundary Scan Register, according with the JTAG instructions, tests and set the IO pads. The MimoStar3 BSR is 11 bits long and allows the test of the following input and output pads

Bit #	Corresponding Pad	Type	Signal	Notes
10	LVDS CkRdP/CkRdN	Input	CkRd	Resulting CMOS signal after LVDS Receiver
9	ASync	Input	Sync	
8	CkADC	Input	CkADC	
7	StartADC	Input	StarADC	
6	SSync	Output	SSync	
5	Ck5M	Output	Ck5M	
4	Ck10M	Output	Ck10M	
3	RstMk	Output	RstMk	
2	LastRow	Output	LastRow	
1	LastCol	Output	LastCol	
0	MxFirst	Output	MxFirst	

2.2.4 ID_CODE Register

The Device Identification register is implemented is this third version. It is 32 bits long and has fixed value hardwired into the chip. When selected by the ID_CODE instruction or after the fixed value is shifted via TDO, the JTAG serial output of the chip.

Mimostar3 ID_CODE register value is **0xFFFF0001**

2.2.5 DIS_COL Register

The DIS_COL register is 640 bit wide. The purpose of this register is to disable the column current sources if a short circuit is suspected on a specific column. During the readout, even if a current source is disabled the corresponding column is selected, i.e. no columns are skipped. Obviously, the signal of the corresponding pixel has not signification.
The default value of the DIS_COL register is 0; it means that all current sources can be activated by the readout logic. Setting a bit to 1 disables the corresponding current source. In MimoStar2, the column<639> is on the left hand side while column<0> is on the right hand side. The organisation of the chip in 10 subframes of 64 columns has no matter to do with the DIS_COL register.

640 (Msb)	**0 (Lsb)**
DisCol<639>	**DisCol<0>**

2.2.6 RO_Mode Register0

The RO_Mode registers are 8 bits large; they allow the user to select specific features of the chip. MimoStar3 only use RO_Mode Register0.

Bit #	**Bit Name**	**Purpose**	**Default value**	
7	SelJtagCk	Select TCK as the ADC clock in place of the external CkADC signal	0	Ext CkADC selected
6	SelFull	Set the row shift register to 640 in place of 320 bits. This option is designed to emulate a 640 x 640 pixel matrix.	0	Normal mode, 320 row shift register selected
5	DisLVDS	Disable LVDS, readout clock is not active anymore.	0	LVDS selected
4	SelMux	On MxFirst output, select MuxFirst signal or First_Pixel_of_First_Frame signal	1	MuxFirst Signal, active See § 3.4 Readout
3	EnaGain3	Select gain 3 for the serial differential output buffer	0	Gain 5
2	Not used		-	
1	BufCopy			
0	EnaTstCol	Test Mode: Select the 2 Test Levels, IVTEST1 and IVTEST0, which emulate a pixel output	0	Normal mode

2.2.7 BIAS_DAC Register

The BIAS_DAC register is 160 bits large; it sets simultaneously the 20 DAC registers.
As show bellow these 8-bit DACs set voltage and current biases.
After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit.
The current values of the DACs are read while the new values are downloaded during the access to the register.
The image of the value of some critical biases can be measured on corresponding test pads.

Bit range	**DAC #**	**DAC Internal Name**	**DAC purpose**	**Corresponding Test Pad**
159-152	DAC19	IKIMO	External circuit monitoring	IKIMO
151-144	DAC18	I4PIX	Pixel source follower bias. DAC with positive slope (0 to 255 µA; 1 µA step)	IPIX
143-136	DAC17	V4TEST1	Test Level, emulates a pixel output. DAC with positive slope (0 to 2.55V; 10 mV step). Marker1	No pad
135-128	DAC16	V4TEST0	IDEM. Marker0	No pad
127-120	DAC15	V4REG9	Regulator voltage bias for the column amplifier (Gain 3 &5). DAC with negative slope ((3.3 to 0.75 V by step of 10 mV)	No pad
119-112	DAC14	V4REG8	Idem	No pad
111-104	DAC13	V4REG7	Idem	No pad
103- 96	DAC12	V4REG6	Idem	No pad
95- 88	DAC11	V4REG5	Idem	No pad

87- 80	DAC10	V4REG4	Idem	No pad
79- 72	DAC9	V4REG3	Idem	No pad
71- 64	DAC8	V4REG2	Idem	No pad
63- 56	DAC7	V4REG1	Idem	No pad
55- 48	DAC6	V4REG0	Idem	No pad
47- 40	DAC5	I4REG1	Idem	IREGAMP
39- 32	DAC4	I4AMP	Bias of column amplifier. DAC with positive slope (0 to 255 µA; 1 µA step)	IAMP
31- 24	DAC3	I4INTBUF	Bias of the Intermediate Buffer. DAC with positive slope (0 to 255 µA; 1 µA step)	IFASTINTBUF
23- 16	DAC2	V4BUF1	Bias of the differential current Output Buffer. DAC with positive slope (0 to 2.55 V by step of 10 mV)	No pad
15- 8	DAC1	V4BUF0	Idem	No pad
7- 0	DAC0	I4BUF	Bias of the two differential current output buffers. DAC with positive slope (0 to 255 µA; 1 µA step)	IFASTBUF

3 Running MimoStar3

The following steps describe how to operate Mimostar3

3.1 After reset

On RSTB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_COL is set to 0, i.e. all columns are selected
- RO_Mode is set to 0
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias register has to be loaded.
The same for the RO_MODE0 and DIS_COL registers if the running conditions differ from defaults.
Finally the readout can be performed either in normal mode or in test mode.

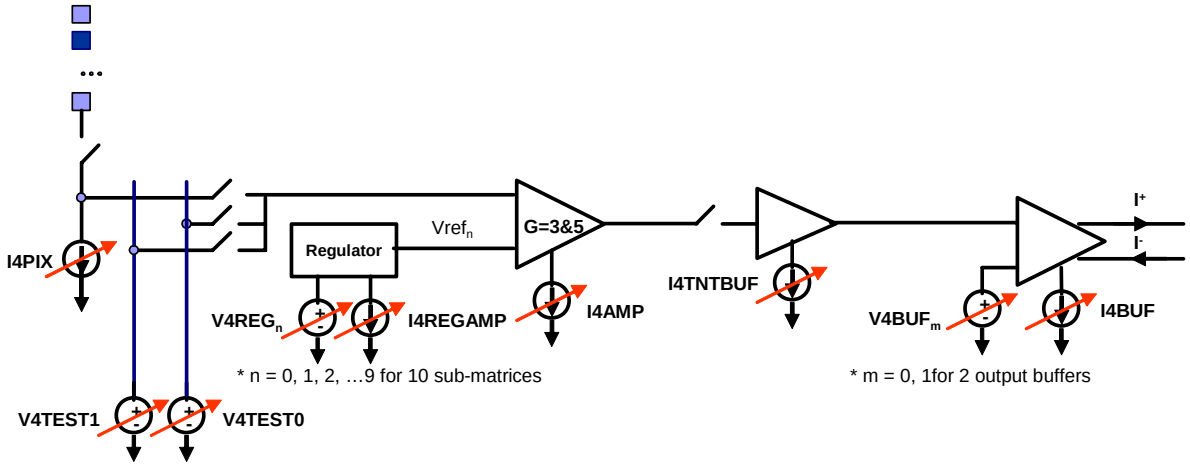
3.2 Biasing MimoStar3

The BIAS_DAC register has to be loaded before operating MimoStar3.
The 20 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	**Simulation**			**Resolution**	**Range**	**Experimental (1)**
	$Code_{16}$ - $Code_{10}$	**DacInternal current-µA**	**Output value**			**$Code_{16}$ - $Code_{10}$**
IKIMO	64-100	100	1 V	10 mV	From 0 up to 2.55 V	0-0
I4PIX	1E-30	30	30 µA	1 µA	From 0 up to 255 µA	1-1
V4TEST1	C3–195	195	1.95 V	10 mV	From 0 up to 2.55 V	FA-250
V4TEST0	B9–185	185	1.85 V	10 mV	From 0 up to 2.55 V	E6-230
V4REG 9-0	23–35	35	2.95 V	10 mV	From 3.3 down to 0.75 V	**80-128**
I4REG1	21–33	33	33 µA	1 µA	From 0 up to 255 µA	**1-1**
I4AMP	64–100	100	100 µA	1 µA	From 0 up to 255 µA	**80-128**
I4INTBUF	64–100	100	100 µA	1 µA	From 0 up to 255 µA	**3-3**
V4BUF1-0	5C–92	92	0.92 V	10 mV	From 0 up to 2.55 V	
I4BUF	28–40	40	40 µA	1 µA	From 0 up to 255 µA	

Note 1: The HRES polysilicon, used in the bias block, is missing for this submission. Experimental values correspond to the recalculated parameters that allow nevertheless the chip be operated. A new submission of the chip is in progress.

Bias synthetic block diagram



Note1: Vrefn ~= V4REGn – 1V

3.3 Setting the Readout_Mode Register

If the desired operating mode does not correspond to the default one, set the Readout_Mode register following the §2.2.6.

3.4 Readout

3.4.1 Signal protocol

Ones JTAG registers have been loaded, the readout of MimoStar3 may initiate with the following signal protocol:

- The readout clock is started. This allows the CK10M output pad to generate a 10 MHz clock. This clock follows the input clock with a 1/10 ratio if the 100 MHz is selected.
- The SYNC signal is set.
- The readout starts at the first rising edge of CK10M of after SYNC signal disappears.
- Signal markers allow the readout monitoring and the analogue data sampling:
  - RstMk maker confirms the internal reset of the readout logic.
  - SSync marker shows that the readout starts.
  - 4 extra CK10M clock cycles, after SYNC sampling, are necessary before the first pixel analogue signal appears on the selected output(s).
  - The MxFirst digital signal helps for a better sampling of the analogue output signals. The way it acts is set by the RO_Mode[4] bit.
    - RO_Mode[4] = 0: MxFirst is active only on the first pixel oft the frame
    - RO_Mode[4] = 1: MxFirst is active on each pixel change on the parallel analogue output i.e. it is a10 MHz periodic signal.
      Used with the 100 MHz serial mode (see serial data format bellow), its period shows when one pixel index has been read in all the subframes (2 real + 8 virtual).
  - LastCol is active when the last column of the current row is selected
  - LastRow is active when the last row of the frame is selected

3.4.2 Successive frames and resynchronisation

Successive pixel frames are read until the readout clock is stopped.
A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

3.5 Analogue Data Format

Two types of signal can be generated on the serial analogue outputs

- Normal pixel signal
- Test signal

3.5.1 Normal mode data format

In order to improve the readout speed Mimostar3 is organized in subframes, i.e. 10 subframes for this prototype. During the readout, the 10 subframes are accessed in parallel. For each subframe the addressing is done row by row, each pixel is accessed sequentially from the left side to right side. Each row contains 2 makers (acting as dummy pixels), and 64 active pixels. One can use the adjustable level of the 2 markers as a pattern recogniser. If the pixel coordinate format is specified as Px<Line, Column>, then for each subframe, the upper left pixel is Px<319, 63> while the lower right is Px<0, 0> and the markers of each beginning row are named Mk1 and Mk0. The 10 subframes are themselves gathered in 2 banks. The two banks are readout in parallel; each one has its own analogue serial output. Thus in each bank, the readout consists to access successively one pixel of each of the 5 subframes and then turning back to the first subframe in order to read its next pixel.

For Mimostar3 the left hand side subframe is named Sf9 and the right hand side is Sf0.
Thus the normal data stream format for the bank1 on the analogue output<1> is:

```
Sf9Mk1       ,Sf8Mk1       ,Sf7Mk1       ,Sf6Mk1       ,Sf5Mk1       ,
Sf9Mk0       ,Sf8Mk0       ,Sf7Mk0       ,Sf6Mk0       ,Sf5Mk0       ,
Sf9Px<319,63>,Sf8Px<319,63>,Sf7Px<319,63>,Sf6Px<319,63>,Sf5Px<319,63>,
Sf9Px<319,62>,Sf8Px<319,62>,Sf7Px<319,63>,Sf6Px<319,62>,Sf5Px<319,62>,
. . . . . .
Sf9Px<319, 0>,Sf8Px<319, 0>,Sf7Px<319, 0>,Sf6Px<319, 0>,Sf5Px<319, 0>,
Sf9Mk1       ,Sf8Mk1       ,Sf7Mk1       ,Sf6Mk1       ,Sf5Mk1,
Sf9Mk0       ,Sf8Mk0       ,Sf7Mk0       ,Sf6Mk0       ,Sf5Mk0,
Sf9Px<318,63>,Sf8Px<318,63>,Sf7Px<318,63>,Sf6Px<318,63>,Sf5Px<318,63>,
Sf9Px<318,62>,Sf8Px<318,62>,Sf7Px<318,63>,Sf6Px<318,62>,Sf5Px<318,62>,
. . . . . .
Sf9Px<318, 0>,Sf8Px<318, 0>,Sf7Px<318, 0>,Sf6Px<318, 0>,Sf5Px<318, 0>,
Sf9Mk1       ,Sf8Mk1       ,Sf7Mk1       ,Sf6Mk1       ,Sf5Mk1       ,
Sf9Mk0       ,Sf8Mk0       ,Sf7Mk0       ,Sf6Mk0       ,Sf5Mk0       ,
Sf9Px<  0,63>,Sf8Px<  0,63>,Sf7Px<  0,63>,Sf6Px<  0,63>,Sf5Px<  0,63>,
Sf9Px<  0,62>,Sf8Px<  0,62>,Sf7Px<  0,63>,Sf6Px<  0,62>,Sf5Px<  0,62>,
. . . . . .
Sf9Px<  0, 0>,Sf8Px<  0, 0>,Sf7Px<  0, 0>,Sf6Px<  0, 0>,Sf5Px<  0, 0>,
```

For bank0 the format on the analogue output<0> is:

```
Sf4Mk1       ,Sf3Mk1       ,Sf2Mk1       ,Sf1Mk1       ,Sf0Mk1       ,
Sf4Mk0       ,Sf3Mk0       ,Sf2Mk0       ,Sf1Mk0       ,Sf0Mk0       ,
Sf4Px<319,63>,Sf3Px<319,63>,Sf2Px<319,63>,Sf1Px<319,63>,Sf0Px<319,63>,
Sf4Px<319,62>,Sf3Px<319,62>,Sf2Px<319,63>,Sf1Px<319,62>,Sf0Px<319,62>,
. . . . . .
Sf4Px<319, 0>,Sf3Px<319, 0>,Sf2Px<319, 0>,Sf1Px<319, 0>,Sf0Px<319, 0>,
Sf4Mk1       ,Sf3Mk1       ,Sf2Mk1       ,Sf1Mk1       ,Sf0Mk1,
Sf4Mk0       ,Sf3Mk0       ,Sf2Mk0       ,Sf1Mk0       ,Sf0Mk0,
Sf4Px<318,63>,Sf3Px<318,63>,Sf2Px<318,63>,Sf1Px<318,63>,Sf0Px<318,63>,
Sf4Px<318,62>,Sf3Px<318,62>,Sf2Px<318,63>,Sf1Px<318,62>,Sf0Px<318,62>,
. . . . . .
Sf4Px<318, 0>,Sf3Px<318, 0>,Sf2Px<318, 0>,Sf1Px<318, 0>,Sf0Px<318, 0>,
Sf4Mk1       ,Sf3Mk1       ,Sf2Mk1       ,Sf1Mk1       ,Sf0Mk1       ,
Sf4Mk0       ,Sf3Mk0       ,Sf2Mk0       ,Sf1Mk0       ,Sf0Mk0       ,
Sf4Px<  0,63>,Sf3Px<  0,63>,Sf2Px<  0,63>,Sf1Px<  0,63>,Sf0Px<  0,63>,
Sf4Px<  0,62>,Sf3Px<  0,62>,Sf2Px<  0,63>,Sf1Px<  0,62>,Sf0Px<  0,62>,
. . . . . .
Sf4Px<  0, 0>,Sf3Px<  0, 0>,Sf2Px<  0, 0>,Sf1Px<  0, 0>,Sf0Px<  0, 0>,
```

3.5.2 Test mode data format

During the test mode the pixel matrix is not connected to the multiplexing electronic. In place of it, two test levels V4TEST1 (V1), V4TEST0 (V0) are available. . They emulate the readout shift from one column of pixel to the other column of pixel.. Actually these levels correspond to those of Marker 1 and Marker 0. They are adjustable via 2 DACs. Even and odd columns amplifiers are alternatively connected to one of them. The V1 and V1 levels are connected to the multiplexing electronic with a specific patter. This pattern allows seeing the output signal changing Thus the test data stream has the following format:

Analogue output <1> format:

```
Sf9V1, Sf8V0, Sf7V1, Sf6V0, Sf5V1, Sf9V0, Sf8V1, Sf7V0, Sf6V1, Sf5V0,
Sf9V0, Sf8V1, Sf7V0, Sf6V1, Sf5V0, Sf9V1, Sf8V0, Sf7V1, Sf6V0, Sf5V1,
. .  . . . . . . . . .
```

Analogue output <0> format:

```
Sf4V0, Sf3V1, Sf2V0, Sf1V1, Sf0V0, Sf4V1, Sf3V0, Sf2V1, Sf1V0, Sf0V1
Sf4V1, Sf3V0, Sf2V1, Sf1V0, Sf0V1, Sf4V0, Sf3V1, Sf2V0, Sf1V1, Sf0V0
. .  . . . . . . . . .
```

3.6 MimoStar3 Chronograms

The following chronograms describe typical access to the chip; Reset, JTAG download sequence and then the readout. This one starts with the initialisation phase followed by the successive row readouts as showed in the zoom.

3.6.1 Normal Readout

Figure 1 show the beginning of a typical normal data readout mode. After Reset and JTAG settings, one can see the initialisation phase of the readout of the first pixel row. The LastCol signal is active meanwhile the last pixel of a row is read. The last row of the frame makes the LastRow signal to be active. The 2 serial analogue outputs are showed. One can distinguish the 2 makers placed at the beginning of each row.

3.6.1.1 Readout synchronisation

The simplest way to get a readout synchronisation on the analogue data is to use the MxFirst signal in "First_Pixel_of_Frame" mode which becomes active when the first pixel is ready on the analogue output. It makes the data acquisition independent of the latency which exists between the start of the readout (Sync) and the appearance of the data.

Nevertheless if it is impossible for the user to use MxfFirst, the synchronisation on the analogue data is possible by counting the number of the CK10M cycles. The latency between the Sync signal falling edge and the rising edge of the MxFirst signal is: **Latency = ((Ck10Count +1) modulo 2) + 6**

Where:

- Latency is given in CK10M cycles. It begins at the first Ck10M rising edge which follows the Sync falling edge
- Ck10Count is the value of a CK10M counter at the falling edge of SYNC

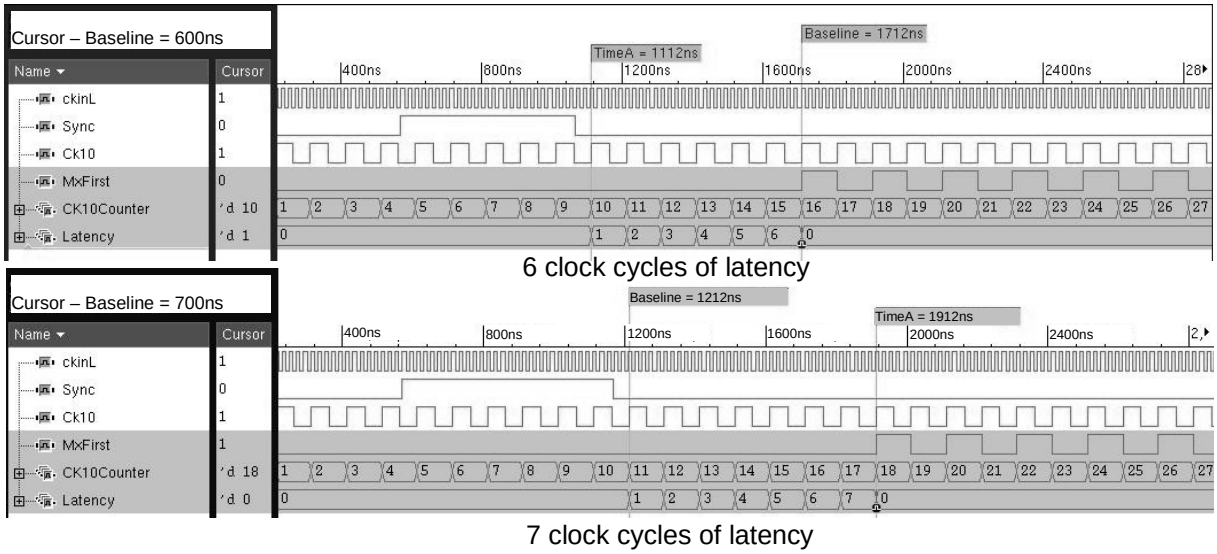


Figure 2 zoom on the readout start. After a latency of 6 or 7 CK10M cycles, Mxfirst goes active and the analogue signal generated in respect with the serial format.
Figure 3 zoom on the transition between 2 consecutive rows of the same frame. The markers are clearly showed.
Figure 4 shows the end of the last row readout followed by the first row of the next frame.

Figure 5 show the alternate option of the MxFirst signal. It is permanently running, being active high on the first maker. This option is set via the RoMode register.

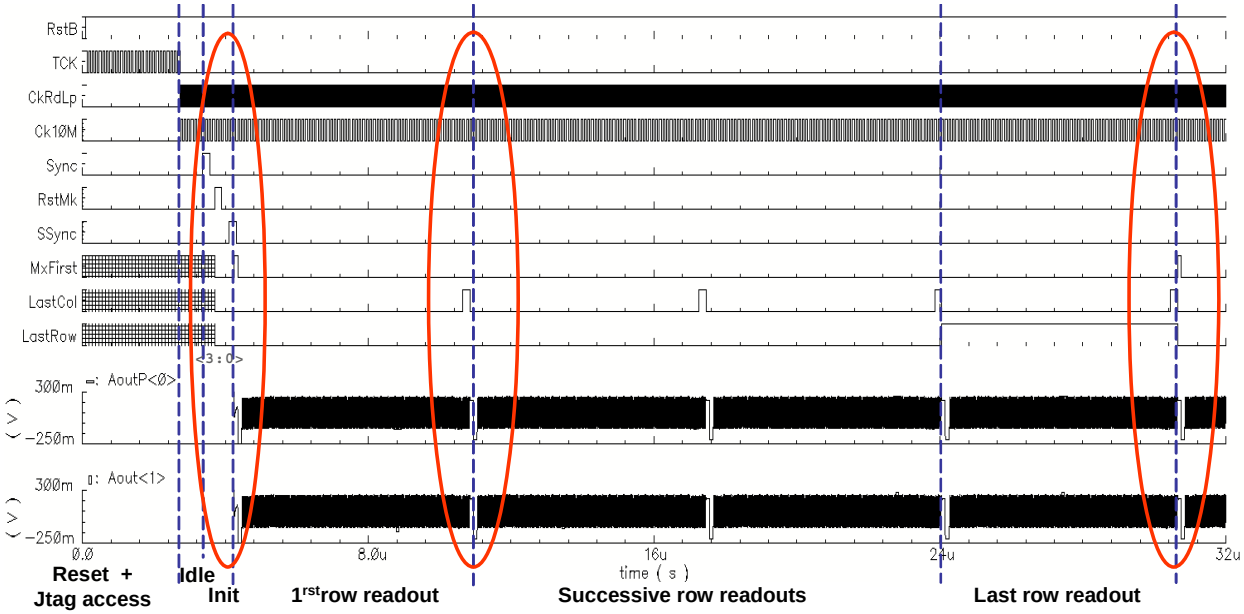


Figure 1

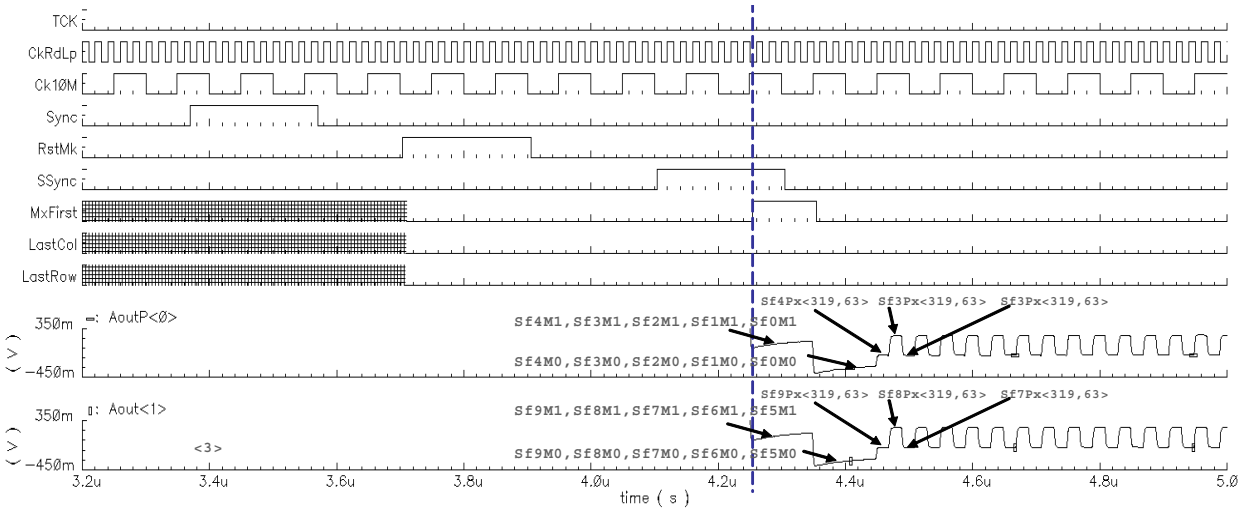


Figure 2

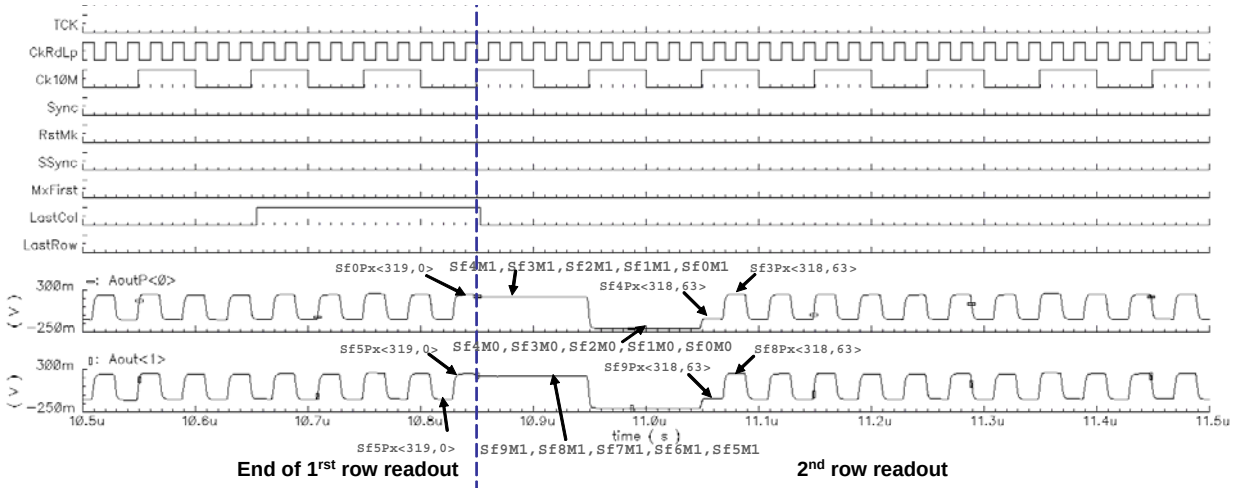


Figure 3

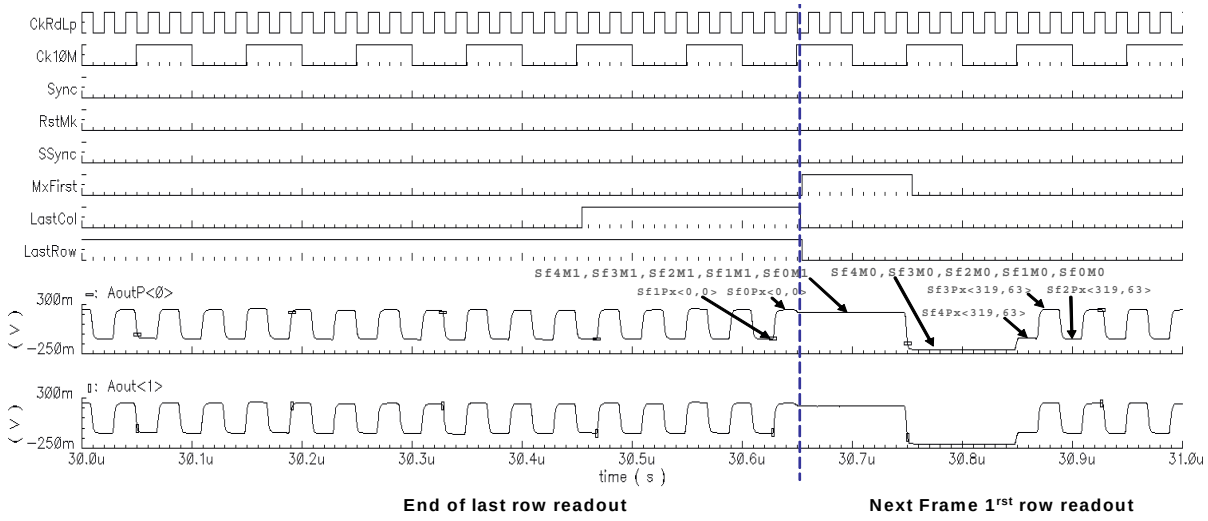


Figure 4

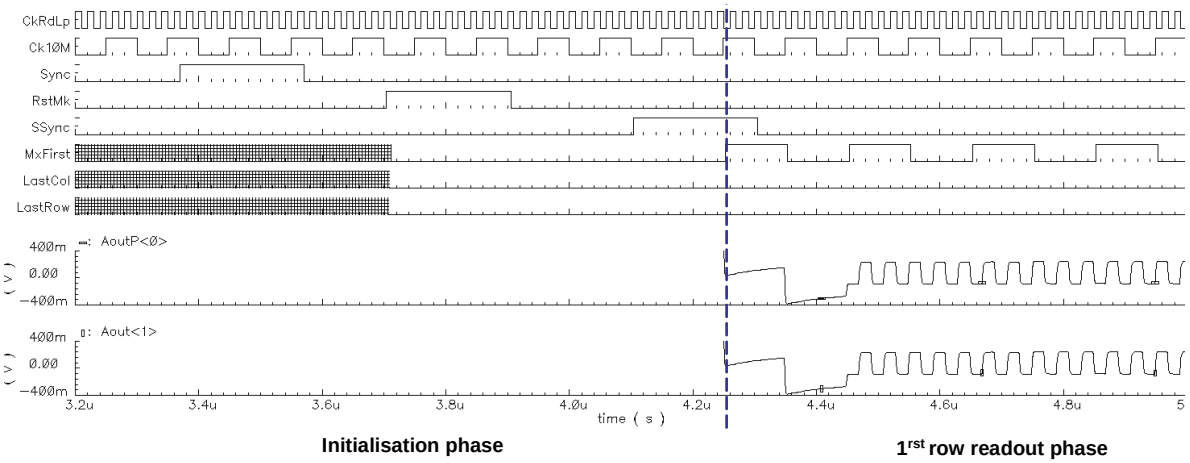
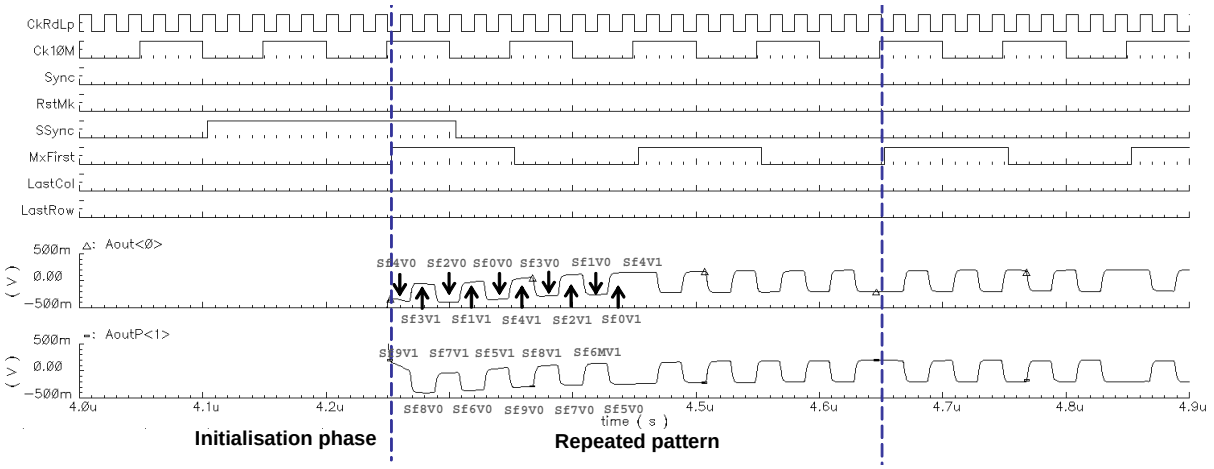


Figure 5

3.6.2 Test mode readout

The initialisation phase if the test mode is the same than in the normal mode. But it has to be noticed than the LastCol and LastRow makers are unavailable because the test mode has nothing to deal with the matrix and its line and column addressing registers. For the same reason the MxFirst maker is unavailable in the “First Pixel of frame mode” but only continuous mode.



3.6.3 Main Signal Specifications

	Parameter	Typical Value	Notes
INIT	RSTB Pulse Width	>1 µS	Active Low, Asynchronous Power on Reset
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	~10 nS	Boundary Scan Control Signal
	TDI Setup/Hold Time	~10 nS	Boundary Scan Serial Data In
READOUT	CKRD Frequency	Up to 50 MHz	Readout Clock LVDS signal
	CKRD Duty Cycle	50%	
	SYNC Setup/Hold Time	5 nS	Chip Initialisation, CMOS signal. Starts after falling edge on 1rst CKRD sampling
Differential Current Buffer (1)	Input Dynamic range	0.7 up to 1.2 V	
	Rise time	5 nS	@ 10-90%, for fully input dynamic range Simulated with Z_{load} = 2*100 Ohm and 2*5pF
	Fall time	5 nS	
	Bandwidth	245 MHz	@ -3 dB
	Transconductance gain	5.8 mS	
	Output Current Range	-2.2; 2.2 mA	

Note 1: The differential current output buffer can be modelled as an ideal current source. Its performances in terms of raising and falling times are limited by its load's time constant (R_{load} x C_{load})

Note 2: Simple source follower

3.7 ADC

3.7.1 ADC_SEL register

Bit #			Selected signal for the measure	
19			DAC V4FASTBUF1	
18			DAC V4FASTBUF0	
17			DAC V4REG9	
16			DAC V4REG8	
15			DAC V4REG7	
14			DAC V4REG6	
13			DAC V4REG5	
12			DAC V4REG4	
11			DAC V4REG3	
10			DAC V4REG2	
9			DAC V4REG1	
8			DAC V4REG0	
7			DAC VTEST1	

6			DAC VTEST0	
5			VDDA chip Supply	
4			VDDA IN Pad	
3			VDDD Chip supply	
2			VDDD IN Pad	
1			VMUX<1> Pad	
0			VMUX<0> Pad	

4 Pad Ring

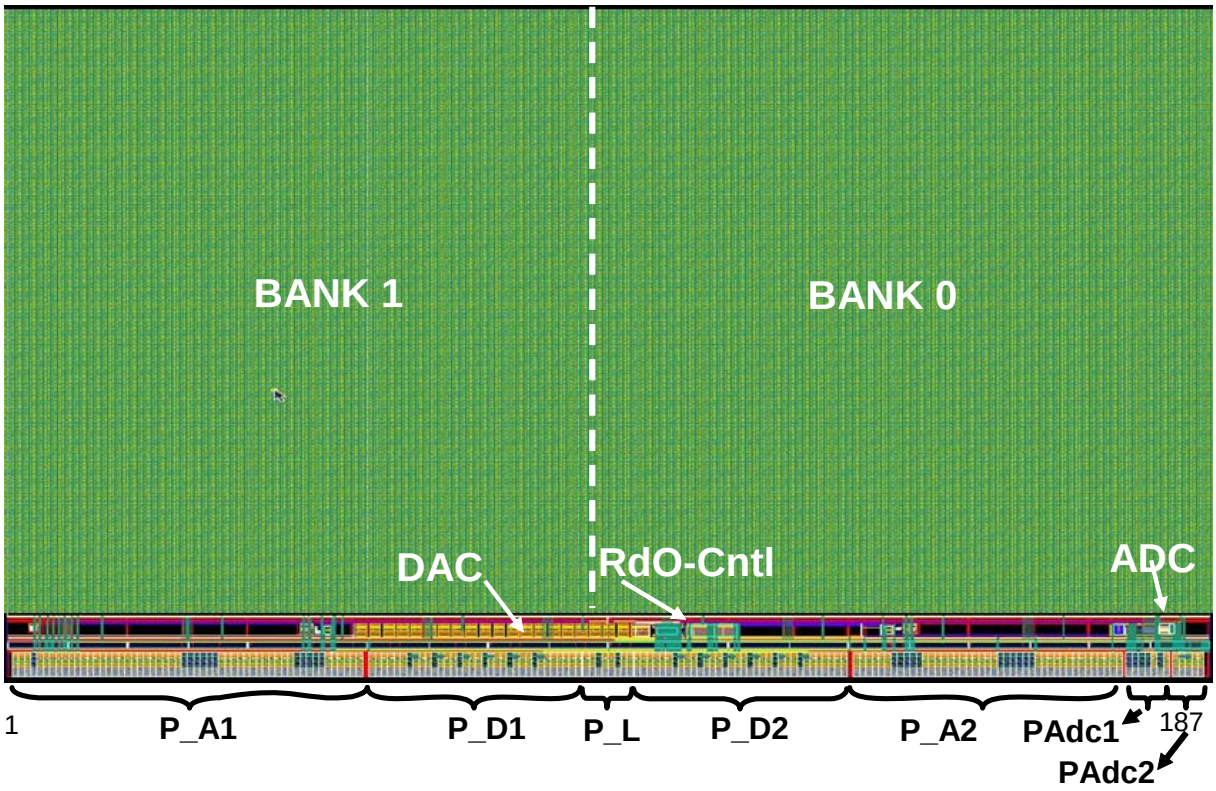
The pad ring of the chip is build with

- Pads full custom designed for some of the analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies

The pad ring is split in 7 functional independent parts

- Read out analogue output<1> & analogue supplies
- CMOS JTAG & digital supplies
- LVDS read out drivers
- Digital read out control & digital supplies
- Read out analogue output<0> & analogue supplies
- Test ADC input signals
- Test ADC control signals & supplies

4.1 MimoStar3 Pad Ring and Floor Plan View



Foundry submission information

Mimostar3 has been designed in AMS C35B4O1 CMOS 0.35 µm epitaxial and opto process with 2 poly and 4 metal layers.
The Process Design Kit V3.70 has been provided by CMP
CAD tools are CADENCE DFII 5.0 with DIVA and ASSURA rules
The chip has been submitted in an engineering run via CMP the June 2006

4.2 Pad List

Pad ring segment 1 – P_A1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
1	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
2	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
3	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
4	TEMP	Direct Pad, no protections	DIRECTPAD	Temperature probe output
5	IFASTBUF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Out, Test Purpose Only
6	IFASTINBUF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Out, Test Purpose Only
7	IAMP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Out, Test Purpose Only
8	IREGAMP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Out, Test Purpose Only
9	IPIX	Analog I/O pad, 0 Ω serial	APRIOP	DAC Out, Test Purpose Only
10	IKIMO	Analog I/O pad, 0 Ω serial	APRIOP	Gen Purpose DAC Output
11	ITEST	Analog I/O pad, 0 Ω serial	APRIOP	Internal Current Ref Source
12	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
13	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
14	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
15	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
16	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
17	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
18	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
19	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
20	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
21	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
22	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
23	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
24	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
25	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
26	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
27	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
28	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
29	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
30	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
31	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
32	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
33	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
34	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
35	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
36	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
37	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
38	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
39	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
40	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
41	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
42	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
43	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
44	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
45	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
46	Aout1P(pb)	Simple metal for probing	Full Custom	
47	Aout1P	Empty pad with embedded buffer	Full Custom	Differential parallel output<1>
48	Aout1N	Empty pad with embedded buffer	Full Custom	Differential parallel output<1>
49	Aout1N(pb)	Simple metal for probing	Full Custom	Probing
50	VMUXout<1>	Direct Pad, no protections	DIRECTPAD	Analogue out, test purpose only
51	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
52	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
53	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core

54	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
55	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
56	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core

Pad ring segment 2 – P_D1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
57	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
58	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
59	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
60	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
61	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
62	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
63	RSTB(pb)	Simple metal for probing	Full Custom	Probing
64	RSTB	Schmitt-Trigger Input Buffer, Pull Up	ISUP	Asynchronous Active Low Reset
65	vddd	Output buffer supply	VDD3OP	Output buffer supply
66	vddd	Output buffer supply	VDD3OP	Output buffer supply
67	TMS(pb)	Simple metal for probing	Full Custom	Probing
68	TMS	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
69	vddd	Output buffer supply	VDD3OP	Output buffer supply
70	vddd	Output buffer supply	VDD3OP	Output buffer supply
71	TDI(pb)	Simple metal for probing	Full Custom	Probing
72	TDI	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
73	vddd	Output buffer supply	VDD3OP	Output buffer supply
74	vddd	Output buffer supply	VDD3OP	Output buffer supply
75	TCK(pb)	Simple metal for probing	Full Custom	Probing
76	TCK	CMOS Clock Input Buffer, 2 mA	ICCK2P	JTAG Clock
77	gnd	Output buffer ground	GND3OP	Output buffer ground
78	gnd	Output buffer ground	GND3OP	Output buffer ground
79	TDO(pb)	Simple metal for probing	Full Custom	Probing
80	TDO	Tri-State Output Buffer, 4 mA	BT4P	JTAG Serial Data Out
81	gnd	Output buffer ground	GND3OP	Output buffer ground
82	gnd	Output buffer ground	GND3OP	Output buffer ground
83	RSTMK(pb)	Simple metal for probing	Full Custom	Probing
84	RSTMK	Tri-State Output Buffer, 2 mA	BT2P	Readout Reset Marker
85	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
86	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
87	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
88	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
89	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
90	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core

Pad ring segment 3 – P_L				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
91	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
92	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
93	CKRN(pb)	Simple metal for probing	Full Custom	Probing
94	CKRN	LVDS In -	Full Custom	Readout Clock Signal
95	CKRP	LVDS In +		
96	CKRP(pb)	Simple metal for probing	Full Custom	Probing
97	vddd	Analogue Pad Supply	AVDDALLP	Supply periphery & core
98	vddd	Analogue Pad Supply	AVDDALLP	Supply periphery & core

Pad ring segment – P_D2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
99	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
100	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
101	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
102	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
103	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
104	vddd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
105	LastRow(pb)	Simple metal for probing	Full Custom	Probing
106	LastRow	Tri-State Output Buffer, 2 mA	BT2P	Last Row Maker
107	vddd	Output buffer supply	VDD3OP	Output buffer supply
108	vddd	Output buffer supply	VDD3OP	Output buffer supply
109	LastCol(pb)	Simple metal for probing	Full Custom	Probing
110	LastCol	Tri-State Output Buffer, 2 mA	BT2P	Last Column Marker
111	vddd	Output buffer supply	VDD3OP	Output buffer supply
112	vddd	Output buffer supply	VDD3OP	Output buffer supply
113	CK10M(pb)	Simple metal for probing	Full Custom	Probing
114	CK10M	Tri-State Output Buffer, 2 mA	BT2P	20 MHz Clock Out
115	gnd	Output buffer ground	GND3OP	Output buffer ground
116	gnd	Output buffer ground	GND3OP	Output buffer ground
117	MxFirst(pb)	Simple metal for probing	Full Custom	Probing
118	MxFirst	Tri-State Output Buffer, 2 mA	BT2P	First pixel maker
119	gnd	Output buffer ground	GND3OP	Output buffer ground
120	gnd	Output buffer ground	GND3OP	Output buffer ground
121	Ssync(pb)	Simple metal for probing	Full Custom	Probing
122	Ssync	Tri-State Output Buffer, 2 mA	BT2P	Readout Synchro. Start Marker
123	gnd	Output buffer ground	GND3OP	Output buffer ground
124	gnd	Output buffer ground	GND3OP	Output buffer ground
125	Sync(pb)	Simple metal for probing	Full Custom	Probing
126	Sync	CMOS Input Buffer	ICP	Readout Input token
127	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
128	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
129	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
130	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
131	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
132	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core

Pad ring segment – P_A2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
133	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
134	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
135	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
136	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
137	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
138	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
139	VMUX0	Direct Pad, no protections	DIRECTPAD	Analogue out, test purpose only
140	Aout0N(pb)	Simple metal for probing	Full Custom	
141	Aout0N	Empty pad with embedded buffer	Full Custom	Differential parallel output<0>
142	Aout0P	Empty pad with embedded buffer	Full Custom	Differential parallel output<0>
143	Aout0P(pb)	Simple metal for probing	Full Custom	Probing
144	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
145	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
146	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
147	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core

148	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
149	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
150	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
151	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
152	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
153	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
154	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
155	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
156	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
157	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
158	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
159	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
160	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
161	vdd_diode	Direct Pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
162	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
163	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
164	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
165	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
166	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
167	gnd	Analogue Pad Supply	AGNDALLP	Ground periphery & core
168	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
169	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
170	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
171	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
172	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
173	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
174	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core
175	vdda	Analogue Pad Supply	AVDDALLP	Supply periphery & core

Pad ring segment 3 – P_Adc1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
176	vddain		DIRECTPAD	ADC input
177	vdddin		DIRECTPAD	ADC input
178	VMUXin1		DIRECTPAD	ADC input
179	VMUXin0		DIRECTPAD	ADC input
180	vdd_ADC	Analogue Pad Supply	AVDDALLP	ADC supply
181	vrpADC		DIRECTPAD	ADC input
182	gnd	Analogue Pad Supply	AGNDALLP	ADC gnd

Pad ring segment 3 – P_Adc2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
183	vdd	Analogue Pad Supply	AVDDALLP	ADC supply
184	CkADC	CMOS Clock Input Buffer, 2 mA	ICCK2P	ADC Clock
185	StartADC	CMOS Input Buffer, Pull Down	ICDP	ADC start conversion
186	gnd	Analogue Pad Supply	AGNDALLP	ADC gnd
187	gnd	Analogue Pad Supply	AGNDALLP	ADC gnd