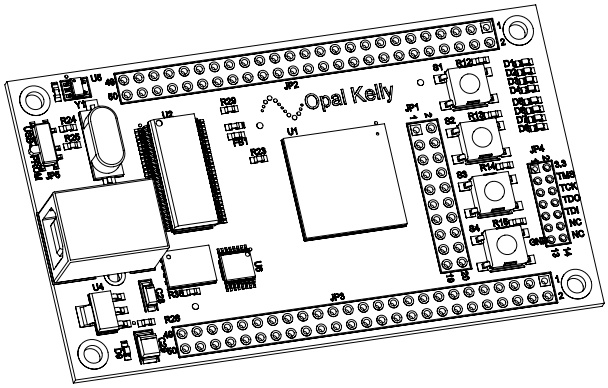
Opal Kelly



XEM6001 User's Manual

A business-card sized (3.5'' x 2.0'') experimentation board featuring the Xilinx Spartan-6 FPGA.

The XEM6001 is a small, business-card sized FPGA board featuring the Xilinx Spartan-6 FPGA. Designed as a bare-bones system, the XEM6001 is an excellent experimenting or prototyping system which provides access to nearly all I/O pins on the 256-pin Spartan-6 device. The USB 2.0 interface provides fast downloads and easy access with FrontPanel software. An on-board PLL provides flexible clock generation for a variety of applications and on-board pushbuttons and LEDs allow simple user interfacing when FrontPanel components don't suit the purpose. Dozens of pins at 0.1" spacing are provided and easily fit onto a standard prototyping board with 0.1" hole spacing.

Software, documentation, samples, and related materials are

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Revision History:

Date	Description
20101001	Initial release.
20140331	Replace pin list tables with reference to Pins.
20150303	Added additional Pins information.

Contents

Introducing the XEM6001

The XEM6001 is a small, business-card sized (3.5'' x 2.0'') FPGA board featuring the Xilinx Spartan-6 FPGA. Designed as a full-featured starter system, the XEM6001 provides access to most of the I/O pins on the 256-pin Spartan 6 device. The XEM6001 is ideally suited to experiments based on the FrontPanel virtual instrumentation platform, integration into prototype development, or as a quick and easy way to add USB capability to an existing device.

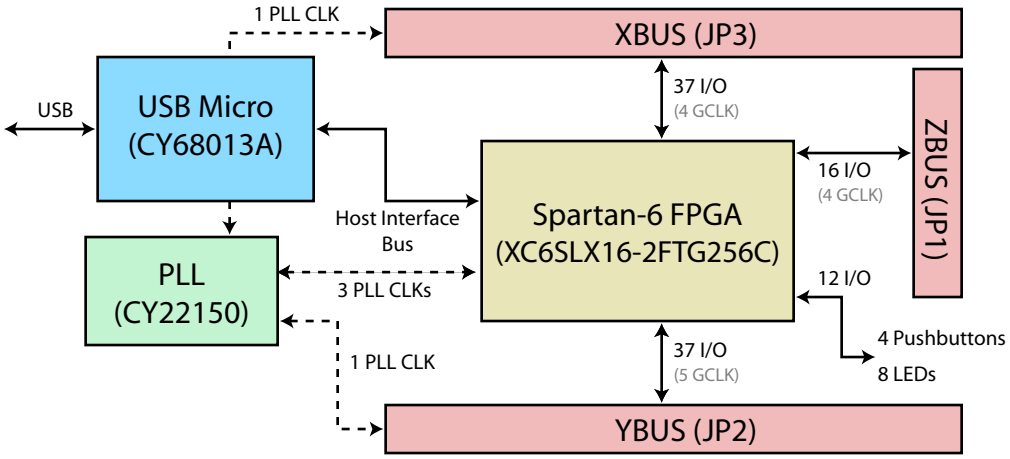
The XEM6001 has been designed to be pin- and footprint-compatible to its Spartan-3 predecessor, the XEM3001.

PCB Footprint

A mechanical drawing of the XEM6001 is provided at the end of this document. The PCB is 3.5" x 2.0" (88.9mm x 50.8mm) with four mounting holes spaced as shown in the figure. These mounting holes are electrically isolated (disconnected).

The three FPGA-access ports JP1, JP2, and JP3 are located on a 0.1" grid so that the entire board may be attached to a standard prototyping board. The JTAG header JP4 is also on this grid.

Functional Block Diagram



Power Supply

The XEM6001 is a bus-powered device in its default configuration (R26 resistor inserted). That is, it takes power from the 5-v USB power and generates the voltages it needs from there. To do so, the XEM6001 has small linear regulators for 3.3v, and 1.2v. External power may be applied to any of the 3.3-v pins on JP1, JP2, or JP3 as long as R26 is removed. In this case, the 5-v USB power is not required and the device consumes very little bus current.

Computers and USB hubs often have USB ports that do not provide bus power. These are called unpowered ports. In order to be operated as a bus-powered device, the XEM6001 must be connected to a USB port that provides bus power. You should check with the hub or computer manufacturer to verify that the port provides bus power.

The XEM6001 may also be self-powered by removing resistor R26. This 0-ohm resistor connects the 3.3-v regulator to the 3.3-v supply plane on the board. By removing this resistor, the 3.3-v supply as well as the derived 1.2-v supply are disconnected from bus power. 3.3 volts must be supplied externally -- to at least one of the 3.3-V pins on JP1, JP2, or JP3.

> IMPORTANT NOTE: Under normal operating conditions and with an unconfigured FPGA, the XEM6001 draws approximately 125 mA from the 3.3-V node. FPGA current draw is impossible to predict because it strongly depends on the implemented design, clock rates, and I/O usage. Current requirements of the FPGA can be estimated using Xilinx power estimation tools and should be considered if you think you may be getting close to USB limits. The current can be measured by removing R26 and placing a current meter across the leads. If you need to exceed the 500 mA limit, make sure to apply external power and remove R26.

USB 2.0 Interface

The XEM6001 uses a Cypress CY7C68013A FX2 USB microcontroller to make the device a USB 2.0 peripheral. As a USB peripheral, the module is instantly recognized as a plug and play peripheral on millions of PCs. More importantly, FPGA downloads happen blazingly fast, virtual instruments under FrontPanel update quickly, and data transfers are much faster than the parallel port interfaces common on many FPGA experimentation boards.

The USB interface also allows the XEM to be bus-powered which means it is ultra-portable requiring just a USB cable and the proper drivers to connect to any supporting PC, including laptops.

On-board Peripherals

The XEM6001 is designed as a low-cost, barebones device. However, a few key peripherals have been added for convenience.

EEPROM

A small serial EEPROM is attached to the USB microcontroller on the XEM6001, but not directly available to the FPGA. The EEPROM is used to store boot code for the microcontroller as well as PLL configuration data and a device identifier string.

The PLL configuration data is loaded from EEPROM and used to reconfigure the PLL each time a new configuration file is loaded to the FPGA. Therefore, stable and active clocks will be present on the FPGA pins as soon as it comes out of configuration. The stored PLL configuration may be changed at any time using FrontPanel's PLL Configuration Dialog.

The EEPROM also stores a device identifier string which may be changed at any time using FrontPanel. The string serves only a cosmetic purpose and is used when multiple XEM devices are attached to the same computer so you may select the proper active device.

Cypress CY22150 PLL

A multi-output, single-VCO PLL can provide up to five clocks, three to the FPGA and another two to the expansion connectors JP2 and JP3. The PLL is driven by a 48-MHz signal output from the USB microcontroller. The PLL can output clocks up to 150-MHz and is configured through the FrontPanel software interface or the FrontPanel API.

32 Mb SPI Flash

A serial flash device is available to the FPGA for configuration booting and post-configuration usage as general-purpose non-volatile memory.

LEDs and Pushbuttons

Eight LEDs and four pushbuttons are available for general use as debug inputs and outputs.

Expansion Connectors

Three 0.1"-spaced expansion connectors (JP1, JP2, JP3) are available to connect the module to your devices. These connectors provide 3.3v power, ground, PLL outputs, and 90 FPGA pins for general I/O. Of the 90 FPGA pins, 13 are FPGA GCLK pins which can be used for global clock inputs to the fabric. All expansion connectors are on a 0.1" grid so that the entire module can piggy-back onto a standard 0.1" PCB protoboard.

> NOTE: The expansion connectors are not installed at the factory to provide you the flexibility of installing your choice of expansion -- directly soldering wires, or using stacking or right-angle connectors.

FrontPanel Support

The XEM6001 is fully supported by Opal Kelly's FrontPanel software. FrontPanel augments the limited peripheral support with a host of PC-based virtual instruments such as LEDs, hex displays, pushbuttons, toggle buttons, and so on. Essentially, this makes your PC a reconfigurable I/O board and adds enormous value to the XEM6001 as an experimentation or prototyping system.

Programmer's Interface

In addition to complete support within FrontPanel, the XEM6001 is also fully supported by the FrontPanel programmer's interface (API), a powerful C++ class library available to Windows and Linux programmers allowing you to easily interface your own software to the XEM.

In addition to the C++ library, wrappers have been written for Java and Python making the API available under those languages as well. Java and Python extensions are available under Windows and Linux.

Complete documentation and several sample programs are installed with FrontPanel.

FPGA Pin Connections

Host Interface

There are 27 pins that connect the on-board USB microcontroller to the FPGA. These pins comprise the host interface on the FPGA and are used for configuration downloads. After configuration, these pins are used to allow FrontPanel communication with the FPGA.

If the FrontPanel okHostInterface module is instantiated in your design, you must map the interface pins to specific pin locations using Xilinx LOC constraints. This may be done using the Xilinx constraints editor or specifying the constraints manually in a text file.

A template constraints file (`xem6001.ucf`) is located in the Samples directory of the FrontPanel installation. This file lists all the XEM6001 pins and maps them to the appropriate FPGA pins using LOC (location) constraints. You can use this template to quickly get the pin locations correct on a new design.

MUXSEL

MUXSEL is a signal on the XEM6001 which selects the signal path to the FPGA programming signals D0 and CCLK. When low (deasserted), the FPGA and USB microcontroller are connected. When high (asserted), the FPGA and Flash are connected.

In normal USB-programmed operation, JP5 is positioned at "USB" and pulls MUXSEL low, connecting the FPGA and USB microcontroller at all times. This allows USB-based programming of the FPGA and subsequent USB communication with the FPGA design after configuration.

In order to allow the Flash to configure the FPGA, JP5 is positioned at "PROM." In order to deassert MUXSEL post-configuration, your design must deassert MUXSEL. This allows the FPGA

design to properly startup and allows for communication over USB even after the Flash has configured it.

The end result is that your FPGA design should always tie HI_MUXSEL to 0. This is the case regardless of how the design was configured (via Flash or USB). For example, in Verilog:

```
assign hi_muxsel = 1'b0;
```

LEDs and Pushbuttons

There are eight LEDs and four pushbuttons on the XEM6001. Each is wired directly to the FPGA as shown in the tables below.

LED	FPGA Pin
D1	A4
D2	C5
D3	B5
D4	A5
D5	C6
D6	B6
D7	A6
D8	A7

Button	FPGA Pin
BTN1	D5
BTN2	D6
BTN3	D8
BTN4	D9

The LED anodes are connected to a pull-up resistor to +3.3VDD and the cathodes wired directly to the FPGA. To turn ON an LED, the FPGA pin should be brought low. To turn OFF an LED, the FPGA pin should be brought high.

The pushbuttons are connected between their respective FPGA pin and DGND. The FPGA side of the connection has a pull-up resistor to +3.3VDD. Therefore, in the pressed state, the FPGA pin will be at DGND (low) and in the unpressed state, the FPGA pin will be at +3.3VDD (high). Note that the pushbuttons are not debounced on the XEM6001. In order to deglitch the signals from the pushbuttons, proper debouncing should be done inside the FPGA.

PLL Connections

The PLL contains six output pins, one of which is left unconnected. The other five are labelled SYS_CLK1 through SYS_CLK5. SYS_CLK4 connects to JP3 and SYS_CLK5 connects to JP2. The other three pins are connected directly to the FPGA. The table below illustrates the PLL connections.

PLL Pin	Clock Name	Connection
LCLK1	SYS_CLK1	FPGA - T8
LCLK2	SYS_CLK2	FPGA - K12
LCLK3	SYS_CLK3	FPGA - H4
LCLK4	SYS_CLK4	JP3 - Pin 48
CLK5	SYS_CLK5	JP2 - Pin 3
CLK6	N/A	

SPI Flash

The SPI flash on the module is a Numonyx M25P32-VME6G or equivalent. It can be programmed (using the FlashLoader sample) with an FPGA configuration bitfile to configure the FPGA on boot. To boot the FPGA from flash, the switch JP5 must be slid to the "PROM" position. To boot the FPGA using FrontPanel, the switch must be slid to the "USB" position. In both cases, FrontPanel communication is available after configuration completes.

Flash Pin	FPGA Pin
C	M9
S	T3
D	R9
Q	T9

FlashLoader Sample

The FlashLoader sample is installed with your FrontPanel installation. It is a simple command-line utility that you can use to program the SPI flash with an FPGA configuration file. Please see the Samples directory for more information.

You can also load a configuration file to the Flash using your own HDL, of course. There is nothing special about the way our FlashLoader sample loads the configuration file into the Flash.

Expansion Connectors

The XEM6001 has locations for three expansion connectors in addition to a JTAG connector. All I/O banks on the FPGA are tied to +3.3VDD.

Opal Kelly Pins is an interactive online reference for the expansion connectors on all Opal Kelly FPGA integration modules. It provides additional information on pin capabilities, pin characteristics, and PCB routing. Additionally, Pins provides a tool for generating constraint files for place and route tools. Pins can be found at the URL below.

http://www.opalkelly.com/pins

JP4 - JTAG Connector

JP4 is the 14-pin 2-mm JTAG connector on-board and is connected only to the FPGA. The connector pinout is compatible with the Xilinx JTAG cable for JTAG configuration and ChipScope. The JP4 pins are connected as shown below:

JP4 Pin	Signal
2	+3.3VDD
4	TMS
6	TCK
8	TDO
10	TDI
12	NC

JP4 Pin	Signal
14	NC
1,3,5,7,9, 11,13	DGND

JP1

JP1 is a 20-pin dual-row 100-mil header, four pins of which are dedicated to power supply. The other 16 pins connect directly to the Spartan 6 on bank 1. Pins 17 and 18 of the header connect to global clock pins on the FPGA and can therefore be used as clock inputs to the internal clock network. All 16 FPGA pins may be used as general-purpose input/output.

JP2

JP2 is a 50-pin dual-row 100-mil header providing access to FPGA bank 3. Several pins of this header are dedicated to power supply (+3.3VDD and DGND). Pin 4 of this header is connected to a global clock input on the FPGA and can therefore be used as an input to the global clock network.

Pin 3 on this header is SYSCLK5 and is directly connected to LCLK5 (pin 14) on the Cypress CY22150 PLL. Using FrontPanel's PLL Configuration Dialog, you can configure the clock signal present on this pin.

JP3

JP3 is a 50-pin dual-row 100-mil header providing access to FPGA bank 1. Several pins of this header are dedicated to power supply (+3.3VDD and DGND). Pin 47 of this header is connected to a global clock input on the FPGA and can therefore be used as an input to the global clock network.

Pin 48 on this header is SYSCLK4 and is directly connected to LCLK4 (pin 12) on the Cypress CY22150 PLL. Using FrontPanel's PLL Configuration Dialog, you can configure the clock signal present on this pin.

Pins

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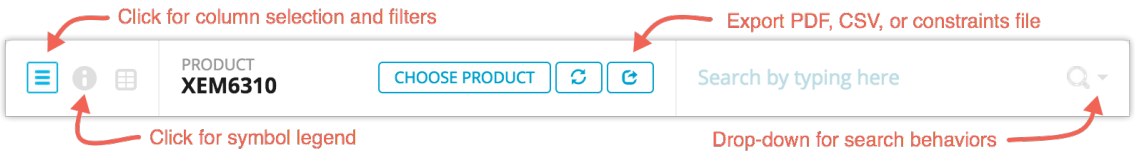
Toolbar

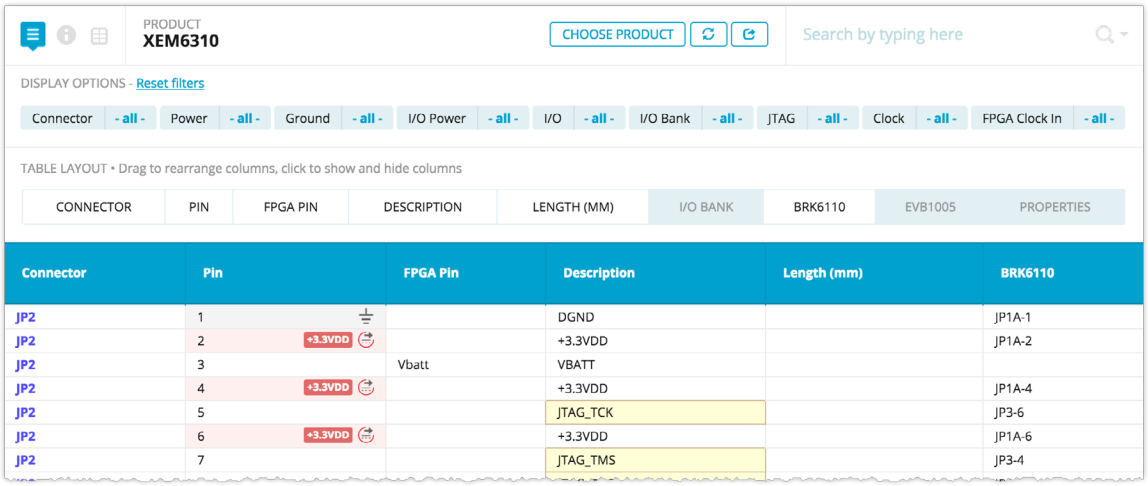
The toolbar at the top of a Pins product page has a number of features. Explore a bit; you won't break it.



Pin Lists

As the primary reference for Opal Kelly integration module expansion connectors, Pin Lists contain a comprehensive table of the FPGA-to-Connector data including connector pin, FPGA pin, signal description, routed length (when applicable), breakout board pin mapping, FPGA I/O bank, and other properties.

By default, not all data columns are visible. Click on the "Toggle Filters" icon at the top-left to select which columns to show. Depending on the specific module, several additional columns may be shown. The data in these columns is always exported when you export the pin list to CSV.



Filters

You can hide or show the additional information associated with each signal by clicking on the icon at the top left ("Toggle Filters"). Use these filters to limit the visible pin listing to particular subsets of signals you are interested in.

Search

You can search the pin list using the search entry at the top-right. Click on the magnifying glass drop-down to adjust the function of the search to one of:

- Highlight - Highlights search results only.
- Hide Matching - Hides rows where search matches are found.
- Show Only Matching - Shows only rows where a search match is found.

Export (PDF, CSV, Constraints Files)

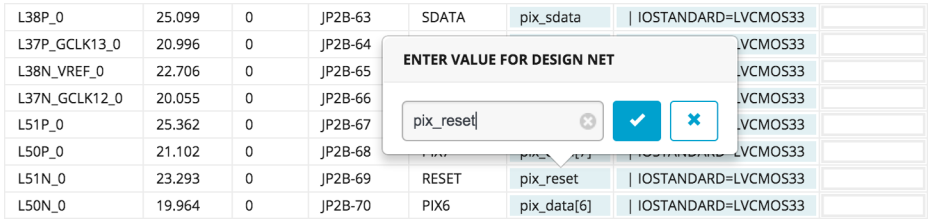
The export button near the search entry allows you to export the pin list in several formats. PDFs can be viewed or printed. CSV can be loaded into a spreadsheet application or manipulated with scripts. Constraints files can be used as inputs to Xilinx and Altera synthesis and mapping tools.

The constraints files include additional mapping information for other peripherals on the module such as memory, clock oscillators, and LEDs.

Peripherals

A Pins Peripheral is a project definition where you can enter your top-level HDL design nets to have Pins generate a complete constraint file for you.

When you create a Peripheral, you will select a target integration module. The Peripheral is paired to this module so that the design parameters match the features and expansion capabilities of the module.



Specifying Net Names

The Pin List view for a Peripheral includes three additional, editable columns:

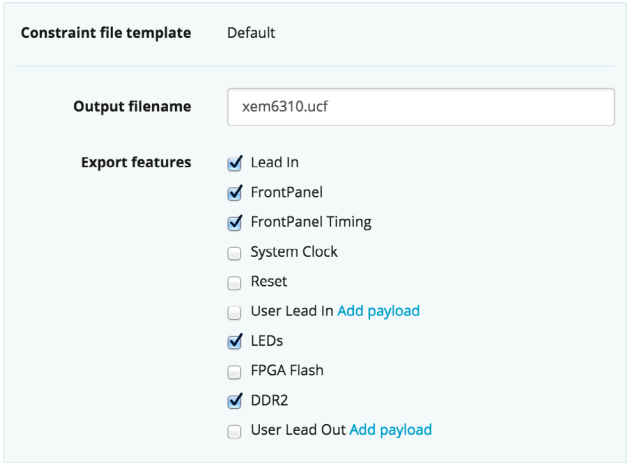
- Design Net - The name of the signal as it appears in your top-level HDL.
- Constraints - Text that is inserted into the constraints file for that signal.
- Comment - Additional comment text that is added to the constraints file.

These additional data are merged with the default Pin List constraints file prior to export. The result is a constraints file complete with net names that can be used with your FPGA development flow.

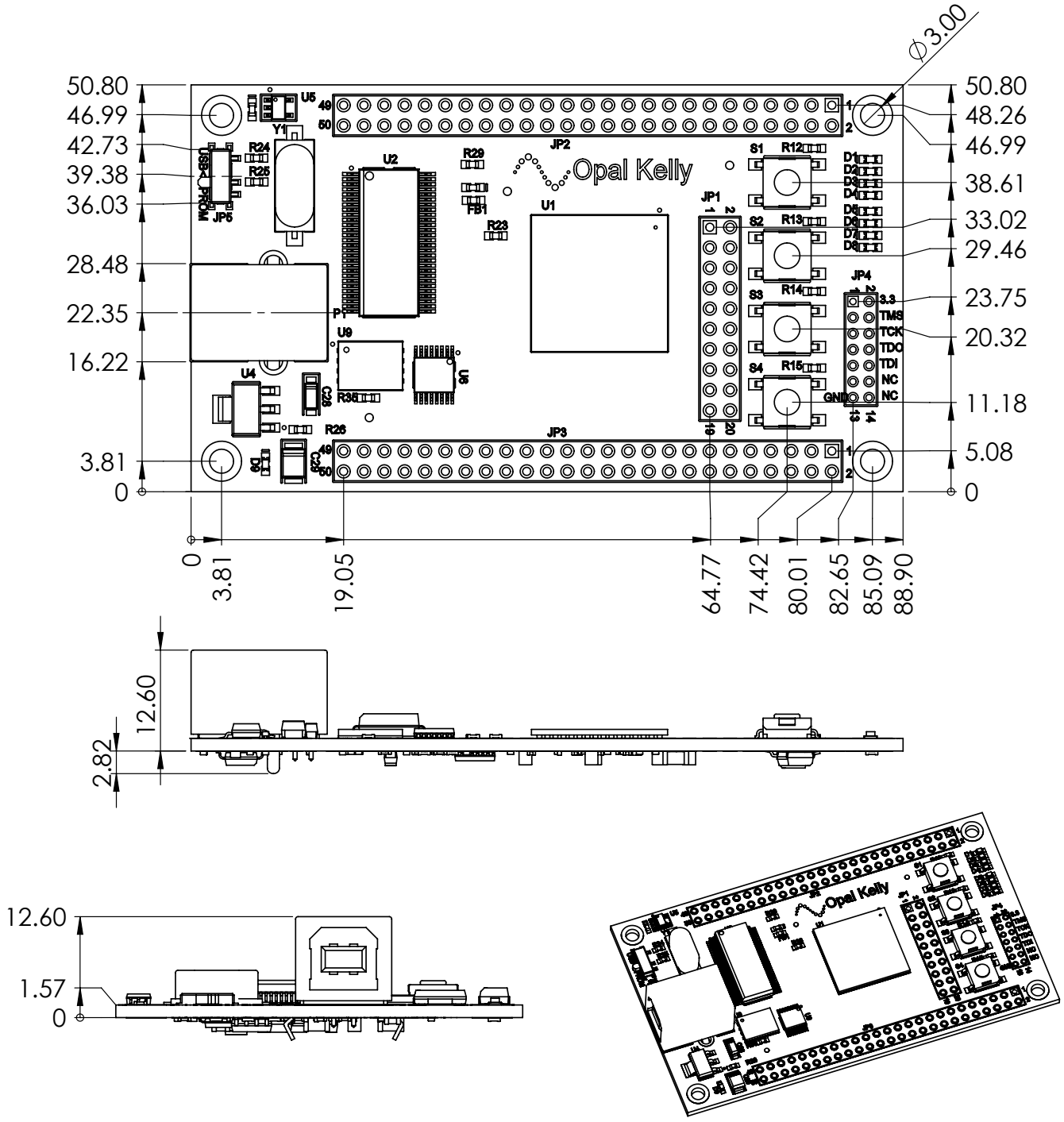
Export Features

Enable the specific module features you would like to appear in the exported constraints file. When a feature is enabled, Pins will export the constraints appropriate to that feature such as pin locations. When a feature is disabled, Pins will skip that portion.

The User Lead In and User Lead Out sections allow you to add custom payloads (your own constraints) that will be added to the exported constraints file. Additional timing constraints or comments can be added here.



XEM6001 Mechanical Drawing



All dimensions in mm