Laboratory Experiment 6

EE348L

Spring 2005

B. Madhavan

Spring 2005

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6 Experiment #6: MOSFETs Continued

6.1 Introduction

Laboratory experiment 5 introduced the MOSFET canonic cells used in MOSFET amplifier design. The ac small-signal model was presented for each canonic cell, and was used to discuss its performance. What the previous lab didn't clearly present are the limitations of the canonic cells. These limitations are one reason why circuits don't comprise of just a single stage that incorporates a single canonic cell. An integrated circuit amplifier doesn't consist on just one common-source amplifier. To be sure, a common-source canonic cell(s) may be used in the amplifier topology, but other elements and canonic cells are also used to address the performance limitations of the amplifier. Another example is the voltage buffer. A voltage buffer in an integrated circuit design doesn't consist of a single common-drain (source follower) canonic cell. As you probably discovered in the pervious lab, the gain of a common-drain (source follower) amplifier is less than unity, and depending on the MOS technology used, it can be considerably less than one. This lab will present ways to combine the canonic cells in order to overcome certain inherent limitations of a single cell. The design strategies and topologies presented here are not comprehensive of all the possible solutions known to overcome the limitations of MOSFET amplifiers. However, they should give you insight into how to approach practical problems in MOSFET analog integrated circuit design.

6.2 Common-source Amplifier

A common occurrence a circuit designer faces is get more gain out of a common-source amplifier. One reason is the relatively low transconductance associated with a MOSFET, as compared to a bipolar transistor. A common-source amplifier is shown below in **Figure 6-1**. Note that the circuitry necessary to establish the proper operating point of the MOSFET M_1 is not shown. Only the ac circuit schematic is shown.
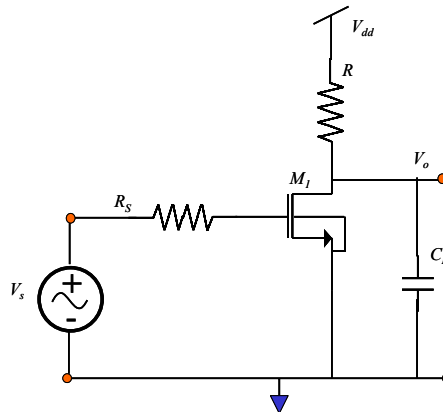
Figure 6-1 V_s Schematic diagram of a common-source amplifier. Bias circuitry is not shown.

From the previous lab, it was shown that a common-source amplifier has gain

$$A_V = \frac{V_o}{V_s} = -g_m R \qquad (6.1)$$

This is assuming that the drain to source resistance, r_{ds}, of the MOSFET is much greater than R. If it isn't, than the net effective resistance is the parallel combination of the resistor R and the drain-source resistance of the device. The transconductance, g_m, of a MOSFET is defined as:

$$g_m = \sqrt{2k_n\left(\frac{W}{L}\right)I_{DQ}} \qquad (6.2)$$

From these equations it can be seen that the only gain variables that a circuit designer has control over are the load resistance, R, the drain bias current, I_{DQ}, and the gate aspect ratio (or size) of the transistor, W/L.

In integrated circuit design, a resistor is not usually a passive element as depicted in **Figure 6-1**. Active devices usually realize resistances. Large on-chip passive resistance takes up much more area than a resistance realized by using an active device. In the case of the common-source amplifier shown in **Figure 6-1**, a PMOS device would be biased in saturation with a dc bias voltage at its gate terminal specified by the designer, to achieve the desired resistance. Ideally, you would like that PMOS to act like a dc current source, shown in **Figure 6-2**. At low frequency, this would maximize the small-signal gain due to the very large (ideally infinite) resistance associated with a dc current source.
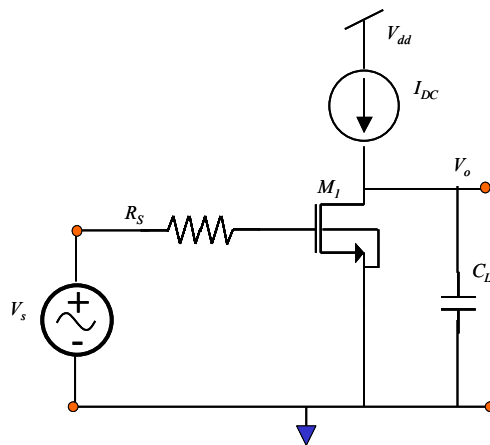
Figure 6-2: An Ideal Common-source Configuration. Bias circuitry is not shown.

We can attempt to maximize the amount of gain that can be realistically obtained from the circuit topology in **Figure 6-2**, by making the small-signal resistance as large as possible. In most MOSFET integrated circuits, this is achieved by replacing the DC current source in **Figure 6-2** with a PMOS version of the current mirror that was presented in laboratory experiment 5, as shown below in **Figure 6-3**. **Note**: It can be seen in **Figure 6-3** that the PMOS current mirror uses a passive resistor R_1 to establish the reference current, I_{ref}, needed to bias the common-source amplifier. As in **Figure 6-1**, this resistance is usually realized with a MOSFET. Normally, another NMOS transistor that is either diode-connected or biased with a dc voltage is used to present the required amount of resistance. For the purposes of this explanation, it will be left as an effective resistance, R_{eff}. **Figure 6-3** doesn't show the bias circuitry that establishes a dc bias voltage at the gate of MOSFET M_1. It is assumed that the input signal, V_s, has the appropriate amount of DC offset to ensure that MOSFET M_1 is biased in the saturation region. Note that the current mirror formed by PMOS transistors M_2 and M_3 are correctly biased by appropriate choice of current I_{ref}, resistor R_{eff} and device sizes (if applicable) of M_2 and M_3.

One may recognize that the small-signal output resistance of the topology feature in **Figure 6-3**, R_{out}, is nothing more than the parallel combination of the output resistance of MOSFET M_2 and that of MOSFET M_1. This derivation is left as a pre-lab exercise.

As stated before, a passive on-chip resistor consumes a great deal of area and its resistance is proportional to that area. Thus, high-value on-chip passive resistors are extremely inefficient from a layout area standpoint. The gain of the common-source canonic cell **Figure 6-1** was increased by using the low frequency, small-signal resistance of a MOSFET current mirror as

shown in **Figure 6-3**, which is much higher than the resistance that can be realized with a typical on-chip passive resistor. However, this assumes that the drain-to-source (or output) resistance, r_{ds}, of a MOSFET is very large. As device geometries become smaller, this assumption begins to fail. This next section will deal with what is known as a cascode configuration, which is a cascade of the common-source and common-gate canonic cells that increases the drain-to-source resistance of a MOSFET.
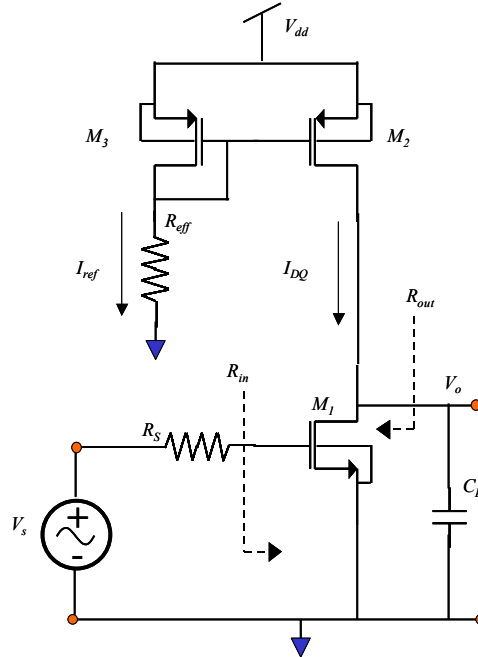

Figure 6-3: A common-source with a current mirror load. Bias circuitry is not shown.

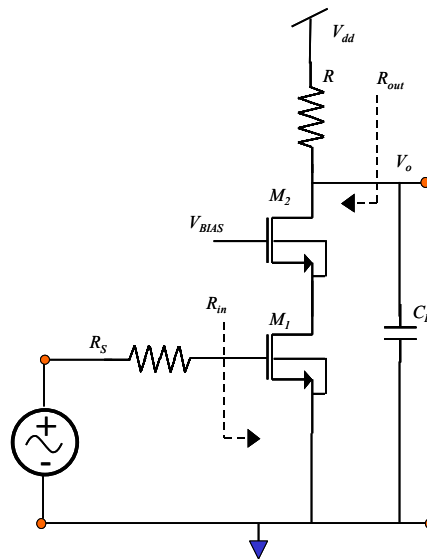## 6.3   Cascode configuration

Figure 6-4: Common-source cascode. Bias circuitry is not shown.

The cascode configuration is shown in **Figure 6-4**. Going back to laboratory experiment 5, one can see that this cascode configuration is nothing more than a common gate that has been stacked on top of the common-source amplifier. Since we have derived the small-signal transfer-function of each canonic cell, we should be able to calculate the small-signal transfer function of the overall amplifier by inspection. The new output resistance should be calculated by replacing each transistor with its ac small-signal model. Both of the above are left as pre-lab exercises.

The cascode configuration has a couple of advantages over the traditional common-source amplifier. As you should find out in the pre-lab, the output resistance, R_{out} in **Figure 6-4** is increased (especially for short-channel devices with gate length < 1μm). Consequently, the gain of the overall circuit is increased. Another benefit is achieved from a speed perspective. The common-gate stage reduces the Miller multiplication of the gate-to-drain capacitance, C_{gd}, of transistor M_1, seen by the source Vs.

The Miller Effect occurs when a capacitor is connected between two nodes, one of which experiences inverting gain with respect to the other. This effectively increases the effective capacitance seen at the input by a factor of one plus the gain. In a traditional common-source configuration such as **Figure 6-1**, there isn't an explicit capacitor between the gate and drain terminals of the MOSFET M_1. The MOSFET small-signal model has a parasitic gate-drain capacitance, C_{gd}, associated with it. Also from laboratory experiment 5, it is known that a common-source amplifier has a transconductance gain of $-g_m$ between the gate and drain. The effective capacitance seen by the input to the common-source amplifier **Figure 6-1** is

$$C_{eff} = C_{gd}(1 + g_m R_L) \qquad (6.3)$$

where R_L is the effective load resistance at the drain. Hence, one can now see that the time constant associated with this node has increased, and will effectively slow the circuit down. This could also potentially render the amplifier unstable if the dominate pole criteria is violated. Bipolar transistors have a much larger g_m associated with them, which increases the Miller Effect when doing IC design with BJTs.
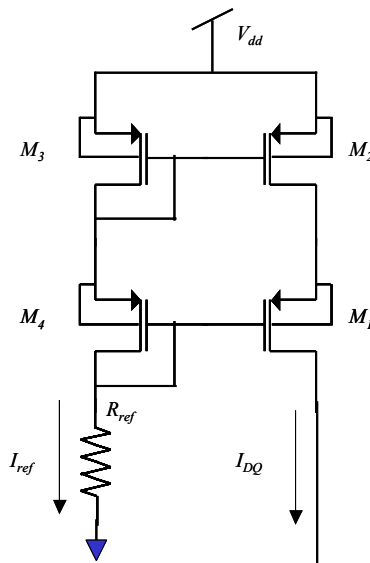
Figure 6-5: Cascode current mirror.

It was stated above that one of the main benefits of the cascode was to increase the output resistance of the common-source amplifier, thus increasing the gain. This modification was successful because the assumption of very large drain-source of the traditional common-source resistance is no longer valid when dealing with small geometry devices. In **Figure 6-4**, the load is symbolized by an effective resistance, R_{eff}, but it is assumed that this effective resistance would

be replaced by some sort of active circuitry such as a current mirror, as shown in **Figure 6-3** Now if the assumption of large drain-to-source resistance is not valid for the traditional common-source, then it may not be valid for the devices in the current mirror either. **Figure 6-5** shows how to increase the output resistance by applying the cascode configuration to the current mirror. The output resistance is derived by replacing all the transistors with their ac small-signal model, followed by a small-signal analysis at the output. This is left as a pre-lab exercise. *See page 649 of the textbook, "Microelectronic Circuits" by Sedra and Smith.*

6.4   A systematic procedure for biasing a source-follower amplifier

In the laboratory experiment 5 biasing supplement, we developed a systematic biasing procedure for a common-source amplifier with a source-degeneration resistor. After making some design choices, we related the ac small-signal gain of the amplifier to the dc-bias voltages of the amplifier. We then used HSpice simulation to determine the drain current, I_D, and transconductance, g_m, of the MOSFET corresponding to the dc bias point for a desired ac small-signal gain. The simulated ac small-signal gain of the complete amplifier, and the gain observed from transient simulation of the amplifier were found to be in excellent agreement with the initial calculations.

In this section, we repeat the procedure for a source-follower (common-drain) amplifier. Before doing this we motivate the need for a source-follower amplifier by looking at the limitation of the common source amplifier whose schematic is shown in **Figure 6-6**. We note that the discrete n-channel MOSFET that we use is 2N7000, whose datasheet may be found at (http://www.supertex.com).
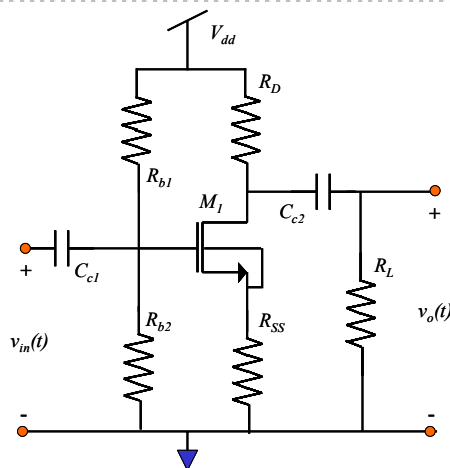
Figure 6-6: Common-source amplifier with variable load impedance R_L. The signal source is not shown.

If the small-signal drain-to-source resistance of MOSFET M_1 is denoted by r_{ds}, the effective load impedance seen by MOSFET M_1 in the frequency range of interest when ac-coupling capacitor C_{c2} is a short is given by $R_D \parallel r_{ds} \parallel R_L$. R_L does not affect the gain of the amplifier in **Figure 6-6** as long as it is larger than $R_D \parallel r_{ds}$. However, as R_L becomes comparable or smaller than $R_D \parallel r_{ds}$, the ac small-signal gain of the amplifier in **Figure 6-6** begins to decrease. The ac small-signal gain is given by

$$A_v = -\left(\frac{g_m (R_D \parallel r_{ds} \parallel R_L)}{1 + g_m R_{ss}} \right)$$ (6.4)

In the laboratory experiment 5 biasing supplement, the design values for the common-source amplifier in **Figure 6-6**, with a small-signal gain close to 20, were found to be
   1. $V_D = 3V$

2. $V_G = 1.475V$
3. $V_S = 0.225V$
4. $I_D = 5.29$ mA
5. $r_{ds} = 9.97$ KΩ
6. $g_m = 29.72$ mS
7. $R_{ss} = 42.53$ Ω
8. $R_D = 1323$ Ω

The revised gain for different values of R_L are shown in the table below, which shows excellent agreement between calculated and simulated values. The influence of varying load resistance R_L on the frequency response of the common-source amplifier in **Figure 6-6** can be seen in **Figure 6-7**, which shows the HSpice simulation of the common-source amplifier in **Figure 6-6** with the design values and MOSFET operating piont developed in the laboratory experiment 5 biasing supplement.

Table 6-1   Relationship between R_L and $|A_v|$

R_L	$R_D||r_{ds}||R_L$	$|A_v|$	$|A_v|$ (dB), calculated	$|A_v|$ (dB), simulated
100	92.114	1.21	1.65	1.65
1000	538.75	7.07	16.99	17.21
10000	1045.85	13.73	22.75	22.24
100000	1154.52	15.16	23.6	24.15
1000000	1166.63	15.31	23.7	24.25

Figure 6-7: Gain variation of the common-source amplifier in **Figure 6-6** due to variation in the R_L.
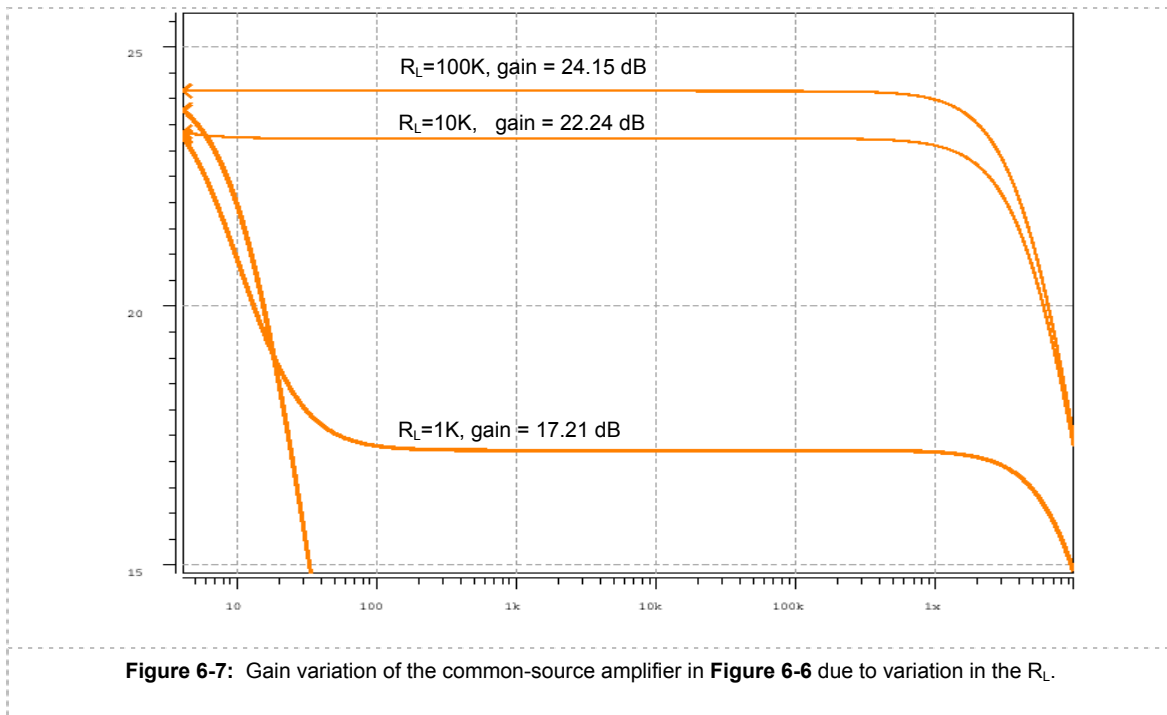
In order to reduce the impact of varying load resistance on the small-signal gain of the common-source amplifier in **Figure 6-6**, we need to insert a buffer stage between the drain of MOSFET M_1 and the load resistance R_L. The output impedance of the buffer needs to be low, so that the variation in R_L does not affect the output impedance of the buffer. Since the output of the common-source amplifier in **Figure 6-6** is a voltage signal, the buffer stage is a voltage-in,

voltage-out stage, with high input impedance and low output impedance. The canonic cell that has these characteristics is the source-follower amplifier, whose output impedance is approximately $1/g_m$, but suffers from a gain that is at best close to 1, but always less than 1.

A schematic of a source-follower (common-drain) amplifier is shown in **Figure 6-8**. *Note that the source and bulk terminals of M_2 are tied together, which is typical of most discrete MOSFET devices, unless specified otherwise*. M_2 is a discrete n-channel MOSFET device such as the 2N7000 used in this lab experiment. resistor connected between the power supply, V_{dd}, and the drain terminal of M_2. R_{b3} and R_{b4} establish a dc-bias voltage, V_{G2}, at the gate terminal of M_2. V_{D2} is the dc-bias voltage at the drain terminal of M_2. V_{S2} (not shown in the figure) is the dc-bias voltage at the source terminal of M_2. The function of resistor R_{D2} is to limit the voltage at the drain of MOSFET M_2 so that it does not enter into breakdown. For low values of V_{dd}, R_{D2} can be eliminated from the circuit schematic.

The ac small-signal gain of the source-follower amplifier in **Figure 6-8** is given by

$$A_v = \left(\frac{g_{m2}R_{SS2}}{1 + g_{m2}R_{SS2}} \right) \tag{6.5}$$

where g_{m2} is the transconductance of MOSFET M_2, which is biased in saturation.

Figure 6-8: Source-follower amplifier schematic with dc-blocking capacitors C_{c1} and C_{c2} isolating the dc-potentials at the gate and drain terminals of M_1 from that of the signal source and that of the load. The signal source and load impedance are not shown.
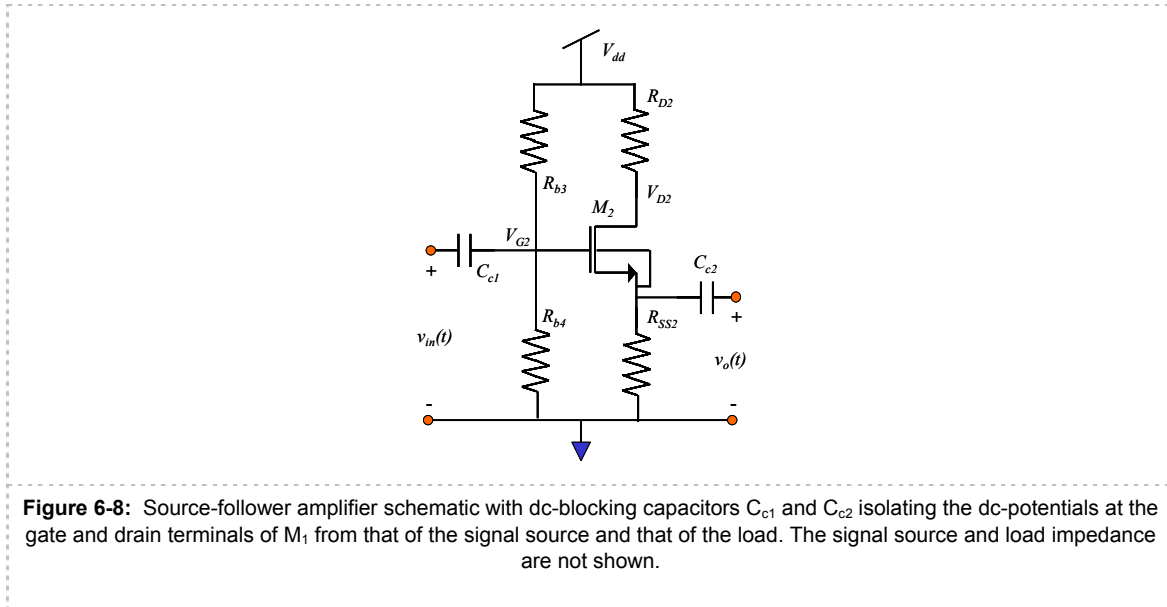
The dc drain-current, $I_{D2,}$ of MOSFET M_2, which is assumed to be in the saturation region of operation is

$$I_{D2} = \frac{K}{2}\left(V_{GS2} - V_{tn}\right)^2 \tag{6.6}$$

$$K = \frac{K_n W}{L} \tag{6.7}$$

The expression for the transconductance g_{m2} (equation 5.10) of MOSFET M_2 is given by

$$g_{m2} = K\left(V_{GS2} - V_{tn}\right) = \sqrt{2KI_{D2}} \tag{6.8}$$

where V_{GS2}, $I_{D2,}$ and V_{tn} are the dc gate-to-source potential, the dc drain current and the threshold voltage of MOSFET M_2 in **Figure 6-8**.

To bias MOSFET M_2 in **Figure 6-8** in the saturation region, we make the following design choices, where V_{D2} is the dc-bias voltage at the drain terminal of M_2, V_{S2} is the dc-bias voltage at the source terminal of M_2, and V_{G2} is the dc-bias voltage at the gate terminal of M_2.
  1. $(V_{GS2} - V_{tn})$ is chosen to be 0.25 V.

2. The above means that $V_{DS2} > 2V$ is sufficient to ensure that MOSFET M_2 is in saturation under reasonable variations of temperature and device parameters.

Using the above design choices, we get

$$I_{D2} = \frac{K}{32} \tag{6.9}$$

$$g_{m2} = \frac{K}{4} \tag{6.10}$$

$$R_{D2} = \frac{V_{dd} - V_{D2}}{I_{D2}} = \frac{32}{K}\left(V_{dd} - V_{D2}\right) \tag{6.11}$$

$$R_{SS2} = \frac{V_{S2}}{I_D} = \frac{32}{K}V_{S2} \tag{6.12}$$

Substituting the above into the expression for the magnitude of the small-signal gain, $|A_v|$, we get

$$|A_v| = \frac{\frac{K}{4}(V_{S2})\frac{32}{K}}{1 + \left(\frac{K}{4}\right)\left(\frac{32V_{S2}}{K}\right)} = \frac{8V_{S2}}{1 + 8V_{S2}} \tag{6.13}$$

The magnitude of the ac small-signal gain of the source-follower amplifier in **Figure 6-7** is detailed in **Table 6-2** for different values of V_{S2}. It can be seen for that $V_{S2} > 2$, the increase in the magnitude of the gain of the source-follower is very small. Based on the results in **Table 6-2**, we choose $V_{S2} = 2.25V$. This implies that with the design choice of $(V_{GS2} - V_{tn}) = (V_{GS2} - 1V) = 0.25$ V, $V_{G2} = 3.5V$.

Table 6-2   Relationship between V_{S2} and $|A_v|$

V_{S2}	$|A_v|$
0.90	0.878
1.00	0.89
1.50	0.923
1.75	0.9333
2.00	0.94
2.25	0.95
2.50	0.952

HSpice dc-simulations of a 2N7000 MOSFET, as was done in the biasing supplement of laboratory experiment 5, with gate-to-source voltage of 0.25V, source and bulk terminals at the same potential, drain-to-source voltage of 3V (ensuring that MOSFET M_2 remains in saturation), gives a dc drain current of 5 mA and a transconductance of 29.42 mS. Therefore, $I_{D2} = 5.18mA$ and $g_{m2} = 29.42$ mS. This gives $R_{ss2} = 2.25V/5.18mA = 434.4\ \Omega$.

Since we chose $V_{S2} = 2.25V$ based on the results in **Table 6-2**, and separately chose $V_{DS2} = 3V$ to ensure that MOSFET M_2 remains in saturation, $V_{D2} = 5.25V$. Since $V_{dd} = 10V$ (as in the biasing supplement of laboratory experiment 5), $R_{D2} = 5.25V/5.18mA = 1013.5\ \Omega$.

The design point of the source-follower amplifier is
- $V_{S2} = 2.25$ V
- $V_{G2} = 3.50$ V
- $V_{D2} = 5.25$ V
- $I_{D2} = 5.18$ mA
- $g_{m2} = 29.42$ mS
- $V_{dd} = 10V$

- R_{ss2} = 2.25V/5.18mA = 434.4 Ω
- R_{D2} = 5.25V/5.18mA = 1013.5 Ω

We want to cascade the common-source amplifier that we designed in the biasing supplement of laboratory experiment 5, with the source-follower amplifier that we have just designed as shown in **Figure 6-9**. We note that the ac-coupling capacitor C_{c2}, the biasing resistors R_{b3} and R_{b4} in **Figure 6-9** can be removed if we directly connect the gate terminal of MOSFET M_2 to the drain terminal of MOSFET M_1. However, the drain terminal of MOSFET M_1 in the common-source amplifier is at 3V, and gate terminal of MOSFET M_2 in the source-follower amplifier is at 3.5V (design point V_{G2} = 3.50V, see above).

Figure 6-9: Cascade of common-source amplifier with source-follower amplifier schematic with dc-blocking capacitors C_{c1}, C_{c2} and C_{c3}. The signal source and its impedance are not shown.
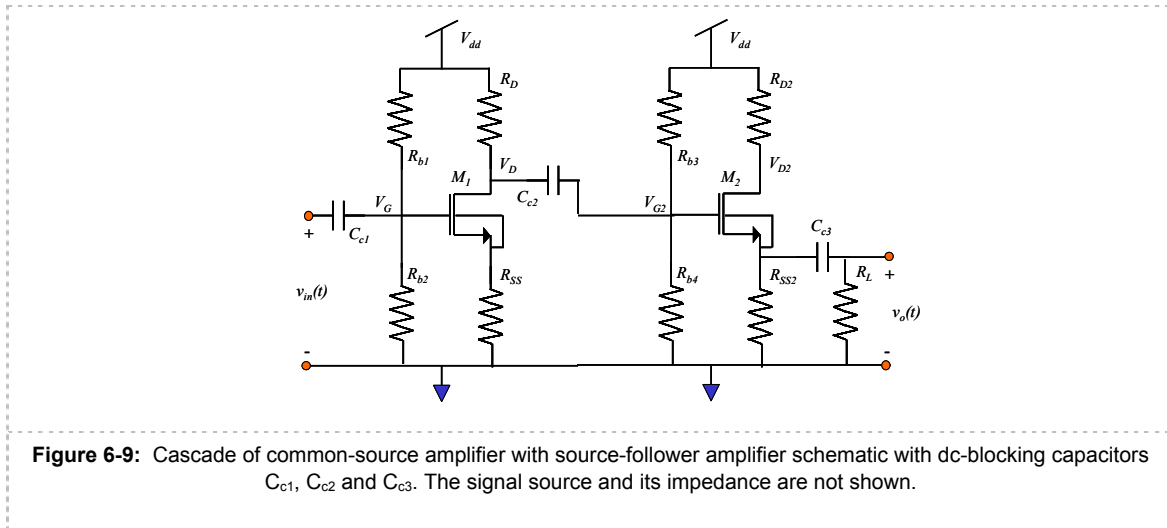
Therefore, we have two choices. We can adjust the drain voltage of MOSFET M_1 from 3.0V to 3.5V or change the gate voltage of MOSFET M_2 from 3.5V to 3.0V.

Choice 1: Changing the drain voltage of MOSFET M_1 from 3.0V to 3.5V
Changing the drain voltage of MOSFET M_1 from 3.0V to 3.5V requires us to change the value of R_D from 1323 Ω to (10V – 3.5V)/5.29mA = 1229 Ω. Assuming that this small change (0.5V) in drain voltage does not change I_D, g_m, and r_{ds} of MOSFET M_1, the ac small-signal gain of the common-source amplifier changes from 15.31 (**Table 6-1**, assuming that RL > 1E6 Ω and that r_{ds} = 9.97 KΩ) to 14.35 (assuming that RL > 1E6 Ω and that r_{ds} = 9.97 KΩ). From **Table 6-2**, the gain of the source-follower amplifier, A_v = 0.95, for our design choice of V_{S2} = 2.25V. The overall gain of the cascade of common-source followed by the source-follower amplifier is the product of the individual gains = 14.35 x 0.95 = 13.633 = 22.69dB.

Choice 2: Changing the gate voltage of MOSFET M_2 from 3.5V to 3.0V
Changing the gate voltage of MOSFET M_2 from 3.5V to 3.0V requires that we change the design value of V_{S2} = 2.25V to V_{S2} = 1.75V to preserve the gate-to-source overdrive = $(V_{GS2} – V_{tn})$ = (3V – 1.75V – 1V) = 0.25V. From **Table 6-2**, the gain of the source-follower amplifier, A_v = 0.9333, for our design choice of V_{S2} = 1.75V. The overall gain of the cascade of common-source followed by the source-follower amplifier is the product of the individual gains = 15.31 x 0.933 = 14.29 = 23.1dB.

☞ **Very Important Point**

Since the source and bulk terminals of MOSFET M_2, which is a discrete device, are tied together and at the same potential, there is no change in the drain current and transconductance of MOSFET M_2, when the gate voltage is changed from 3.5V to 3.0V and the gate-to-source

voltage, V_{GS2}, remains unchanged. Therefore, the output impedance of the source-follower amplifier remains unchanged in this particular case.

This is not the case when the bulk terminal of the n-channel MOSFET (namely M_1 and M_2) are tied to the lowest potential in the circuit, as one might be required to do if this design were to be fabricated on an integrated circuit.

6.4.1 Verification of the systematic procedure for biasing a common-source amplifier

☞ **Very Important Point**

See pages 4-18 to 4-20 of the HSpice user manual, version 2001.4, December 2001;page 8-14 for the general MOSFET model statement, pages 8-21 to 8-26 for the MOSFET equivalent circuits, 8-59 to 8-101 for MOSFET capacitance models, and pages 9-20 to 9-33 for the Level 3 MOSFET model deck, in the HSpice Device Models Reference Manual, version 2001.4, December 2001

```
AC-coupled Common-Source amplifier with Source Degeneration Resistor
*This file has been used for cs + source-follower amplifier
*Written March 3, 2005 for EE348L by Bindu Madhavan.
*****************************************************
**** options section
*****************************************************
.options post=1 brief nomod alt999 accurate acct=1 opts
.options unwrap dccap=1
.param capop=4
*****************************************************
**** circuit description
*****************************************************
rb1 vdd  gate 8.525K
rb2 gate vss  1.475K
m1 drain gate source source nmos_2N7000 W=0.8E-2 L=2.5E-6
rs source vss 'srcres' $500
rd vdd drain 'drainres' $1500
cc1 gatec gate  10uF

*source-follower amplifier, dc-coupled
rd2 vdd drain2 1014
m2  drain2 drain source2 source2 nmos_2N7000 W=0.8E-2 L=2.5E-6
rs2 source2 vss 435

cc2 source2 drainc 10uF
rl drainc vss 'loadres'
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**** parameters section
*****************************************************
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.param srcres=42.53
.param loadres=100K
*****************************************************
**** sources section
*****************************************************
v1       vdd     vss 10V
vgate    gatec   vss ac 1 sin(0V 10mV 100k)
v2       vss     0   0V
*****************************************************
**** analysis section
*****************************************************
* see page 8-63 and 8-66 of HSpice user manual
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```

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.probe ac vgsov      = par('(v(gate)-v(source)-lv9(m1))')
.probe ac vds        = par('(v(drain)-v(source))')
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**** specify nominal temperature of circuit in degrees C
********************************************************
.TEMP=27
********************************************************
**** analysis section
********************************************************
.ac dec 100 1 1G sweep loadres poi 5 100 1K 10K 100K 1X
********************************************************
**** models section
********************************************************
*(this Model is from supertex.com)
.MODEL nmos_2N7000   NMOS
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+DELTA=0.1      KAPPA=0.0506    TPG=1           CGDO=3.1716E-9
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+NFS=6.6E10     TOX=1.0E-7      LD=1.698E-9     UO=862.425
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.END
```

Figure 6-10: HSpice netlist of the cascade of common-source and source-follower amplifiers in **Figure 6-9**.

Table 6-3   Relationship between R_L and $|A_v|$

R_L	Common Source $|A_v|$ (dB), calculated	Common Source $|A_v|$ (dB), simulated	Common Source + Source Follower $|A_v|$ (dB), simulated
100	1.65	1.65	20.32
1000	16.99	17.21	22.61
10000	22.75	22.24	22.88
100000	23.6	24.15	22.905

| 1000000 | 23.7 | 24.25 | 22.908 |

The simulation results of the frequency response of the cascade of common-source and source-follower amplifiers in **Figure 6-9** using the netlist in **Figure 6-10** are summarized in **Table 6-3** and **Figure 6-11** for values of RL varying from 100 Ω to 1E6 Ω. The results in **Table 6-3**, compare the mid-band gain of the common-source and the cascaded common-source source-follower amplifier. The variation in gain due to variation in R_L is reduced from 22.6 dB to less than 2.6 dB.

Figure 6-11: Gain variation of the common-source, source-follower amplifier cascade in **Figure 6-6** due to variation in the load resistor, R_L.
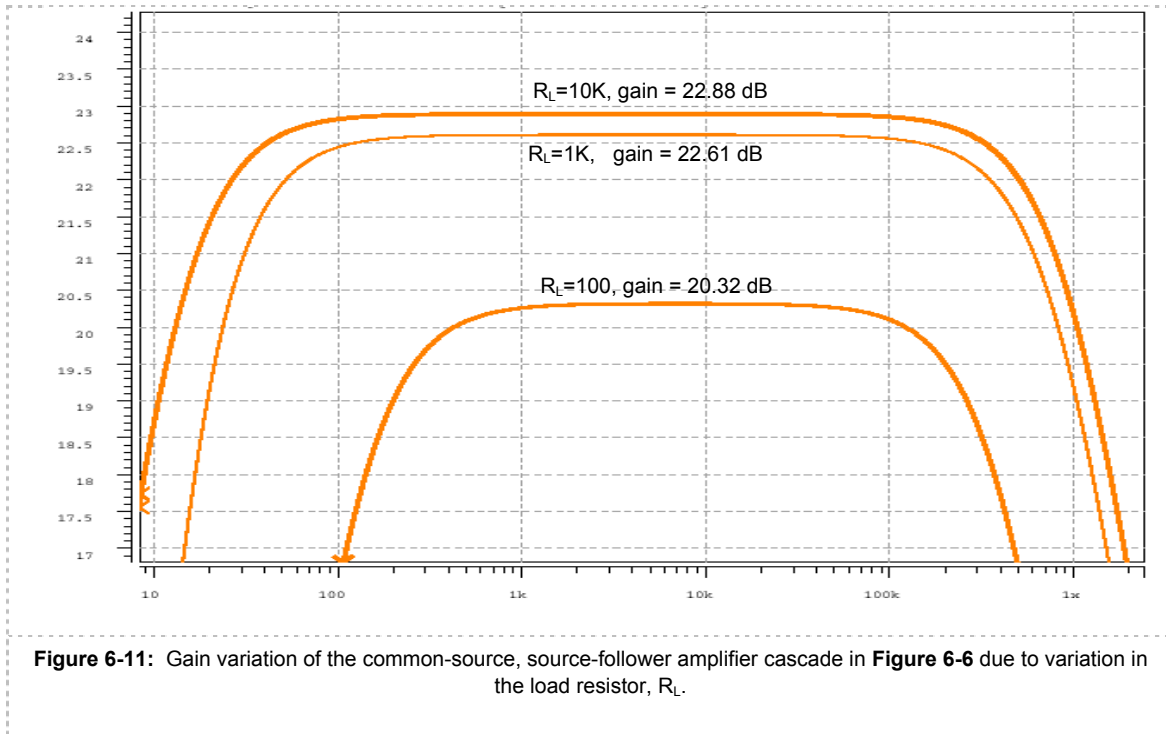
6.5 HSpice simulation of discrete p-channel MOSFET, BS250P

Figure 6-12 is an example of a netlist that can be used to plot the i_D-v_{DS} characteristics of the MOSFET BS250P, specified by the subcircuit named BS250P in **Figure 6-12**. We use a subcircuit definition because we do not have a properly characterized model deck for the BS250P from the manufacturer that accounts for all aspects of its behavior. The drain to source voltage, V_{DS}, is swept from 0V through 10V in steps of 0.01V at gate to source voltages, V_{GS} of 2 V-10 V = -8V, 4V-10V = -6V, and 6V-10V = -4V. The HSpice simulation results are shown in **Figure 6-13**. Refer to Laboratory experiment 3 or the HSpice user manual, version 2001.4, December 2001 for help on plotting using mwaves/awaves.

```
PMOSFET I-V characteristic for BS250P
*This file has been used to generated figures for lab6
*Written Mar 4, 2005 for EE348L by Bindu Madhavan.
*****************************************************
**** options section
*****************************************************
.options post=1 brief nomod alt999 accurate acct=1 opts
.options unwrap dccap=1 numdgt=9
.param capop=4
*****************************************************
**** subcircuit definition
*****************************************************
```
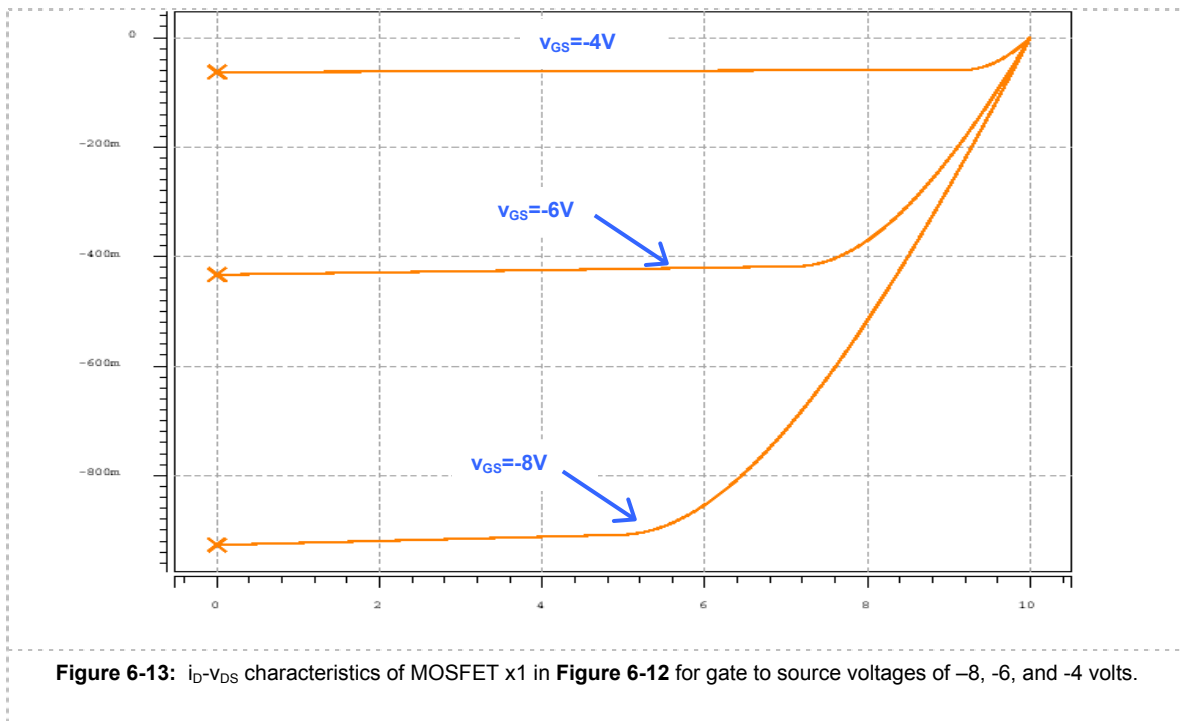
```
.SUBCKT BS250P drain gate source
M1 drain gate1 source source MBS250
RG gate   gate1   160
RL drain source 1.2E8
C1 gate1 source 47E-12
C2 gate1 drain   10E-12
D1 drain source DBS250
.MODEL MBS250 PMOS
+VTO=-3.193       RS=2.041 RD=0.697 IS=1E-15 KP=0.277
+CBD=105E-12      PB=1 LAMBDA=1.2E-2
.MODEL DBS250 D IS=2E-13 RS=0.309
.ENDS BS250P
*******************************************************
**** circuit description
*******************************************************
x1 drain gate source BS250P
*******************************************************
**** sources section
*******************************************************
vdrain  drain  vss     3.0V
vsource source vss     10.0V
vgate   gate   vss     4.0V
v2      vss    0       0.0V
*******************************************************
**** analysis section
*******************************************************
* see page 8-63 and 8-66 of HSpice user manual
.probe dc idrain     = par('id(x1.m1)')
.probe dc cgd        = par('-lx19(x1.m1)')
.probe dc cgs        = par('-lx20(x1.m1)')
.probe dc cgtotal    = par('lx18(x1.m1)')
.probe dc vthreshold = par('lv9(x1.m1)')
.probe dc vdsat      = par('lv10(x1.m1)')
.probe dc gm         = par('lx7(x1.m1)')
.probe dc gmbs       = par('lx9(x1.m1)')
.probe dc gds        = par('lx8(x1.m1)')
.probe dc rds        = par('1/lx8(x1.m1)')

*******************************************************
**** specify nominal temperature of circuit in degrees C
*******************************************************
.TEMP=27
*******************************************************
**** analysis section
*******************************************************
.dc vdrain 0 10.0 0.01 sweep vgate poi 3 2V 4V 6V

.END
```

Figure 6-12: HSpice netlist for obtaining I-V characteristic of an n-channel MOSFET, 2N7000.

Figure 6-13: i_D-v_{DS} characteristics of MOSFET x1 in **Figure 6-12** for gate to source voltages of –8, -6, and -4 volts.

6.6 Conclusion

The MOS canonic cells were presented in laboratory experiment 5. These cells are the fundamental building blocks of analog integrated circuit design. This lab focused on using the canonic cells in combination to overcome their inherent limitations when used as a single cell. Thus when doing circuit analysis, one may always break down a circuit topology into the canonic cells in order to obtain insight into the design of a circuit. An advanced understanding of these basic building blocks will allow a circuit designer to effectively use canonic cells to overcome their individual limitations, and satisfy the largest possible subset of circuit design specifications.

6.7 MOSFET Spice model for PMOS transistor BS250P

Note that the spice model for the discrete p-channel MOSFET used in this laboratory experiment, BS250P, utilizes a subcircuit definition, which includes a first-order PMOS model deck.

```
.SUBCKT BS250P drain gate source
M1 drain gate1 source source MBS250
RG gate  gate1  160
RL drain source 1.2E8
C1 gate1 source 47E-12
C2 gate1 drain  10E-12
D1 drain source DBS250
.MODEL MBS250 PMOS
+VTO=-3.193      RS=2.041 RD=0.697 IS=1E-15 KP=0.277
+CBD=105E-12     PB=1 LAMBDA=1.2E-2
.MODEL DBS250 D IS=2E-13 RS=0.309
.ENDS BS250P
```

In order to use this device in an HSpice netlist, the above subcircuit is defined before the start of the circuit description. Then, a subcircuit call is used to instantiate the BS250P in the HSPice netlist, as shown below.
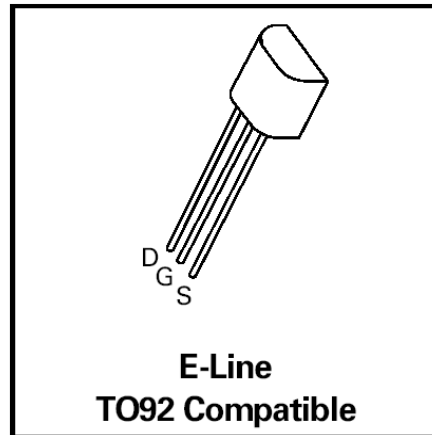
```
X1 drain gate source BS250P
```


Figure 6-14: Pin diagram of the BS250P (Courtesy of Zetex).

6.8 Revision History

This laboratory experiment is a modified version of the laboratory experiment 7 (MOSFET Dynamic circuitsII) created by Jonathan Roderick.

6.9 References

[1]   Bindu Madhavan, Laboratory Experiment 5 biasing supplement, EE348L, Spring 2005

[2]   Avant! HSpice User Manual, Version 2001.4, December 2001, posted on EE348L class web site.

[3]   Avant! HSpice Device Models Reference Manual, Version 2001.4, December 2001, posted on EE348L class web site.

[4]   Bindu Madhavan, EE348L Laboratory Experiment 3, Spring 2005.

[5]   Adel Sedra and K. C. Smith, *Microelectronic Circuits*, fifth edition, Oxford University Press.

[6]   Ben G. Streetman. *Solid State Electronic Devices*. Prentice-Hall Inc., Englewood Cliffs, New Jersey, 1990.

[7]   Richard C. Jaeger. *Introduction to Microelectronic Fabrication*. Addison-Wesley Publishing Company, Reading, Massachusetts, 1993.

[8]   S. M. Sze. *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., New York, 1981.

[9]   Paul R. Gray & Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Inc., New York, 1993.
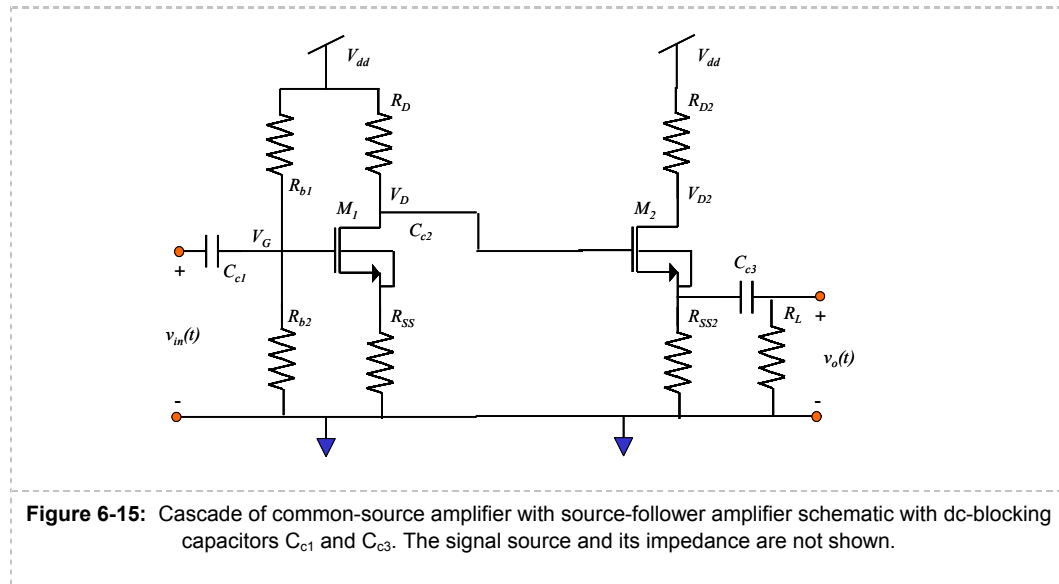
6.10 Pre-lab Exercises

<u>**Note:**</u>
- For HSpice simulations, use the model deck for 2N7000 in **Figure 6-10** and the model deck for BS250P in **Figure 6-12**.
- See HSpice guidelines in Laboratory Experiment 3 and Laboratory Experiment 5.
- Read Laboratory Experiment 5 biasing supplement carefully.
- Submit plots relevant to each question in your lab report.

- **Note**: The 2N7000 and BS250P are not small geometry devices, so the approximation of large small-signal, drain-to-source resistance in the saturation region, r_{ds}, is normally valid.
- **Device Specifications:**
  Caution: Never exceed the device maximum limitations during design.
2N7000	Idmax=200mA	Vdsmax=60V	Vth$\approx$0.8V
BS250P	Idmax=-250mA	Vdsmax=-45V	Vth$\approx$-1V

Figure 6-15: Cascade of common-source amplifier with source-follower amplifier schematic with dc-blocking capacitors C_{c1} and C_{c3}. The signal source and its impedance are not shown.

1) Following the systematic procedure for biasing a common-source amplifier outlined in laboratory experiment 5 biasing supplement, design a common-source amplifier (**Figure 6-8**) in HSpice, with source degeneration resistance which has the following specifications:
   a. Supply voltage of 10 V (bonus points if you achieve specification with lower supply voltage between 5V and 8V)
   b. small-signal gain > 25 dB between 0˚C and 125˚C for an ac-coupled load resistance R_L=100 KΩ, in the frequency range of 1000 Hz to 1E5 Hz.
   c. small-signal gain > 20 dB at 27˚C for R_L(min) = 1 KΩ, in the frequency range of 1000 Hz to 1E5 Hz.
   Your answer should indicate
   i) how you arrived at the dc-operating point of the common-source amplifier
   ii) how the component values were chosen.
   iii) Show that the calculated small-signal gain is in good agreement with that obtained from your HSpice simulations.
   iv) As shown in **Table 6-1**, tabulate the variation in mid-band (frequency range of 1000 Hz to 1E5 Hz) small-signal gain due to variation in load-resistance, R_L for 100 Ω, 1 KΩ, 10KΩ, 100 KΩ, and 1E6 Ω.
   v) Submit the results of a transient simulation with a 20mV peak-to-peak sinusoidal input at 10 KHz. Does the gain inferred from the transient simulation agree with the gain obtained from the frequency response (small-signal) simulation in HSpice ? Why or Why not ?

2) Modify your design in pre-lab question 1 as shown in **Figure 6-15** so that the variation in mid-band small-signal gain due to variation in load-resistance R_L, from 100 Ω to 1E6 Ω is no more than 5 dB.
   Your answer should indicate

i) how you arrived at the dc-operating point of the common-source amplifier
ii) how the component values were chosen.
iii) Show that the calculated small-signal gain is in good agreement with that obtained from your HSpice simulations.
iv) As shown in **Table 6-3**, tabulate the variation in mid-band (frequency range of 1000 Hz to 1E5 Hz) small-signal gain due to variation in load-resistance, R_L for 100 Ω, 1 KΩ, 10KΩ, 100 KΩ, and 1E6 Ω.
v) Submit the results of a transient simulation with a 20mV peak-to-peak sinusoidal input at 10 KHz. Does the gain inferred from the transient simulation agree with the gain obtained from the frequency response (small-signal) simulation in HSpice ? Why or Why not ?

3) Derive the small-signal output resistance of the common-source amplifier featured in **Figure 6-3**, taking into account the small-signal MOSFET drain-to-source resistance, r_{ds}.

4) Derive the small-signal gain and output resistance of the common-source cascode in **Figure 6-4**, taking into account the small-signal MOSFET drain-to-source resistance, r_{ds}.

5) Neglecting the load, but taking into account the small-signal MOSFET drain-to-source resistance, r_{ds}.how much greater is the common-source cascode output resistance as compared to the traditional common-source amplifier (This means the output resistance, R_{out}, looking down the drain of the MOSFET M_2 for the cascode in **Figure 6-4**, and MOSFET M_1 for the traditional common-source amplifier in **Figure 6-1**).

6) Calculate the small signal output resistance of the cascode current mirror shown in **Figure 6-5**, taking into account the small-signal MOSFET drain-to-source resistance, r_{ds}.. How much larger is it compared to the traditional current mirror? *See pages 563-564 of the textbook, "Microelectronic Circuits" by Sedra and Smith for basic current mirrors and page 649 for cascaded current mirrors. Also see laboratory experiment 5.*

7) One drawback of using cascode topologies is that the maximum achievable signal swing is reduced. Replace R_{eff} in **Figure 6-4** with the cascode current mirror in **Figure 6-5** and derive an expression for maximum AC signal swing (i.e. $V_o$max < V_o < $V_o$min) that can be achieved. It should be in terms of device DC biasing voltages (i.e. V_{gs} and V_{ds}) and guarantees that all devices operate in saturation. (*What are the maximum and minimum voltages at the output that will allow all MOSFET devices to be in the saturation region?*)

6.11 Lab Exercises

- use the model deck for 2N7000 in **Figure 6-10**
- use the model deck for BS250P in **Figure 6-12**.
- Submit plots relevant to reach question in your lab report.
- Use the supply voltage that you used in your pre-lab HSpice simulations for this lab.
- **Take care that you look up the manufacturer's datasheet to determine the threshold voltage range (minimum, typical, and maximum values) of the particular discrete MOSFET device that you are using**.

1) Build the common-source amplifier you designed in pre-lab question 1. Verify your results for load resistances of 1 KΩ, 10KΩ, and100 KΩ. Does your gain remain the same for sine wave inputs at 10 KHz, with peak-to-peak values of 20mV, 100mV, 200mV and 400mV? Tabulate the output peak-to-peak values obtained. Calculate the gain observed from your transient signal measurement as the ratio of the output peak-to-peak voltage to the input peak-to-peak voltage. Do your results agree with you HSpice results? Why or why not?

2) Using the results from pre-lab question 2, build the amplifier in **Figure 6-15**. Verify your results for load resistances of 1 KΩ, 10KΩ, and100 KΩ. Does your gain remain the same for sine wave inputs at 10 KHz, with peak-to-peak values of 20mV, 100mV, 200mV and 400mV? Tabulate the output peak-to-peak values obtained. Calculate the gain observed from your transient signal measurement as the ratio of the output peak-to-peak voltage to the input peak-to-peak voltage. Do your results agree with you HSpice results? Why or why not?

3) **Bonus Question:** Build the circuit from pre-lab question 7. Note that your job is to correctly bias the circuit for maximum signal swing, while making sure all devices are in saturation. Measure the maximum signal swing you can achieve by adjusting the amplitude of a 5 KHz sine wave. Do these results agree with what you derived in the pre-lab? Why or why not?

6.12 General Report Format Guidelines

1. Data
   Present all data taken during the lab. It should be organized and easy to read.
2. Discussion
   Answer all the questions in the lab. For each laboratory exercise, make sure that you discuss the significance of the results you obtained. How do they help your investigation? Explain the meaning, the numbers alone aren't good enough.
3. Conclusion
   Wrap up the report by giving some comments on the lab. Do the results clearly agree with what the lab was trying to teach? Did you have any problems? Suggestions?