Hardware User Manual

CM-BF561 V2.0

Tinyboards from Bluetechnix
www.bluetechnix.com

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Information
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Warnings
Due to technical requirements components may contain dangerous substances.

The Core Modules and development systems contain ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused Core Modules and Development Boards should be stored in the protective shipping package.

BLACKFIN Products

Core Modules:

CM-BF533:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF533 processor; up to 600MHz, 32MB RAM, 2MB Flash, 120 pin expansion connector and a size of 36.5x31.5mm
CM-BF537E:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 600MHz, 32MB RAM, 4MB Flash, integrated TP10/100 Ethernet physical transceiver, 120 pin expansion connector and a size of 36.5x31.5mm
CM-BF537U:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 600MHz, 32MB RAM, 4MB Flash, integrated USB 2.0 Device, 120 pin expansion connector and a size of 36.5x31.5mm (will be replaced by CM-BF527).
TCM-BF537:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 500MHz, 32MB RAM, 8MB Flash, 28x28mm, 120 pin expansion connector, Ball Grid Array or Border Pads for reflow soldering, industrial temperature range -40°C to +85°C.
CM-BF561:	Blackfin Processor Module powered by Analog Devices dual core ADSP-BF561 processor; up to 2x 600MHz, 64MB RAM, 8MB Flash, 120 pin expansion connector and a size of 36.5x31.5mm.
CM-BF527:	The new Blackfin Processor Module is powered by Analog Devices single core ADSP-BF527 processor; key features are USB OTG 2.0 and Ethernet. The 2x60 pin expansion connectors are backwards compatible with other Core Modules.
CM-BF548:	The new Blackfin Processor Module is powered by Analog Devices single core ADSP-BF548 processor; key features are 64MB DDR SD-RAM 2x100 pin expansion connectors.

Development Boards:

EVAL-BF5xx:	Low cost Blackfin processor Evaluation Board with one socket for any Bluetechnix Blackfin Core Module. Additional peripherals are available, such as an SD-Card.
DEV-BF5xxDA-Lite:	Get ready to program and debug Bluetechnix Core Modules with this tiny development platform including a USB Based Debug Agent. The DEV-BF5xxDA-Lite is a low cost starter development system including VDSP++ Evaluation Software License.

DEV-BF5xx-FPGA: Blackfin Development Board with two sockets for any combination of Blackfin Core Modules. Additional peripherals are available, such as SD-Card, Ethernet, USB host, multi-port JTAG including a USB based Debug Agent, connector for an LCD-TFT Display and connector for a digital camera system. A large on-board SPARTAN-3 FPGA and Soft IPs make this board the most flexible Blackfin development platforms ever developed.

DEV-BF548DA-Lite: Get ready to program and debug Bluetechnix CM-BF548 Core Module with this tiny development platform including a USB Based Debug Agent. The DEV-BF548DA-Lite is a low cost starter development system including VDSP++ Evaluation Software License.

EXT-Boards: The following Extender Boards are available: EXT-BF5xx-Audio, EXT-BF5xx-Video, EXT-BF5xx-Camera, EXT-BF5xx-Exp, EXT-BF5xx-ETH-USB, EXT-BF5xx-AD/DA. Additional boards based on customer request are also available.

Software Support:

BLACKSheep: The BLACKSheep VDK is a multithreaded framework for the Blackfin processor family from Analog Devices that includes driver support for a variety of hardware extensions. It is based on the real-time VDK kernel included within the VDSP++ development environment.

LabVIEW: LabVIEW embedded support for the CM-BF537E, CM-BF537U and TCM-BF537 Core Modules is based upon the BLACKSheep VDK driver Framework.

uClinux: All the Core Modules are fully supported by uClinux. The required boot loader and uClinux can be downloaded from: http://blackfin.uClinux.org.

Upcoming Products and Software Releases:

Keep up-to-date with all the changes to the Bluetechnix product line and software updates at: www.bluetechnix.com

BLACKFIN Design Service

Based on more than five years of experience with Blackfin, Bluetechnix offers development assistance as well as custom design services and software development.

1 Introduction

The CM-BF561 is an outstanding high performance and low power dual core processor module incorporating Analog Devices Blackfin family of processors. The module allows easy integration into high demanding very space and power limited applications.

1.1 Overview

The Core Module CM-BF561 consists of the following components:

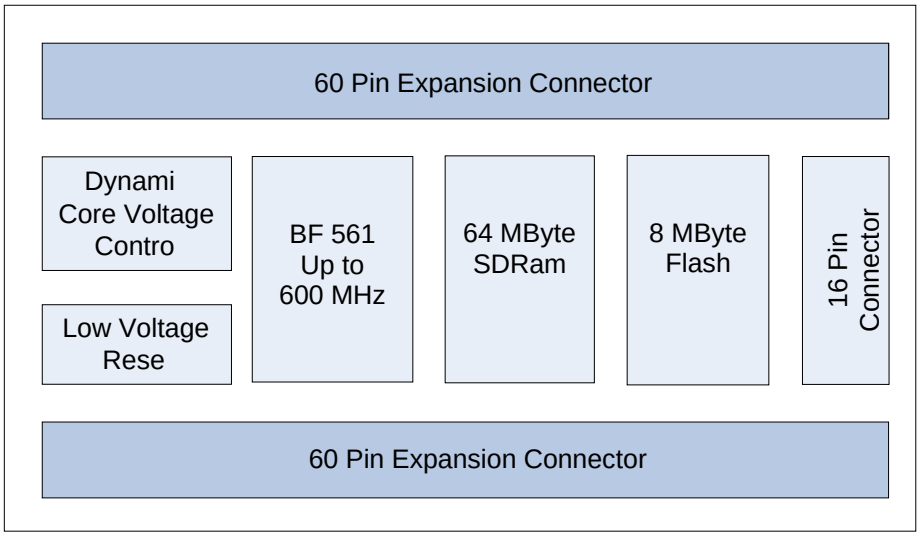

Figure 1-1: Main components of the CM-BF561 module

- **Analog Devices Blackfin Processor BF561**
  - ADSP-BF561SKBCZ600
- **64 MB SDRAM**
  - SDRAM Clock up to 133MHz
  - 2x MT48LC16M16A2BG-75IT:D (16Mx16, 256Mbit at 3.3V)
- **8 MB of Byte Addressable Flash**
  - PF48F2000P0ZBQ0 (4Mx16, 64Mbit at 3.3V; all 8MByte addressable)
  - Additional flash memory can be connected through the expansion board as parallel Flash using asynchronous chip select lines or as a SPI flash.
- **Dynamic Core Voltage Control**
  - Core voltage can be adjusted by setting software registers on the Blackfin processor
  - Core voltage range: 0.8 – 1.2V

- **Low Voltage Reset Circuit**
    - Resets module if power supply goes below 2.93V for at least 140ms
- **Connector P1**
    - SPORT 0
    - JTAG
    - UART
    - SPI
    - PPI-1 (Parallel Port Interface 1)
    - GPIO's
- **Connector P2**
    - Data Bus
    - Address Bus, Control Signals
    - PPI-2 (Parallel Port Interface 2)
    - Power Supply
- **Expansion Connector P3**
    - SPORT 1
    - PF Flags

1.2 Differences between Board Versions V1.x

Version 2.0 and higher differ from Version 1.x in the amount of RAM and FLASH. Both versions are size and PIN Compatible! An additional expansion connector P3 has been provided. The V1.x hardware is not supported any longer. Changes include the removal of the BGA pads and the increase in RAM memory (2x 32MB Chips, providing a total of 64MB) and FLASH memory (Intel P30 8MB instead of Intel J3 4MB)

This document contains information of Version 2.x hardware only. See Chapter 7 for Software Changes.

1.3 Key Features

- The CM-BF561 is very compact and measures only 36.5x31.5 mm
- Allows quick prototyping of product that comes very close to the final design
- Reduces development costs, faster time to market
- Very cost effective for small and medium volumes

1.4 Target Applications

- Generic high performance signal processor module
- High performance web camera
- Robotics: Tiny processor module for mobile robots

1.5 Further Information

Further information, and document updates are available on the product homepage: http://www.bluetechnix.com/goto/cm-bf561

2 Specification

2.1 Functional Specification

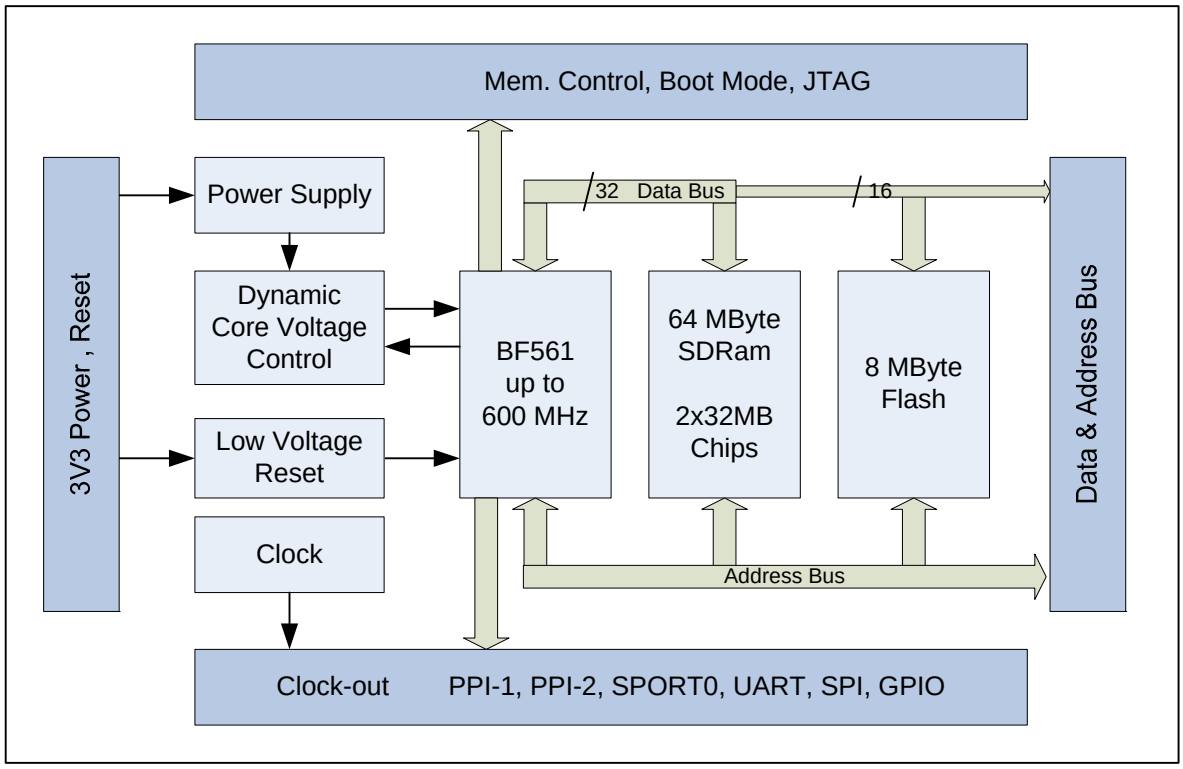

Figure 2-1: Detailed Block Diagram

Figure 2-1 shows a detailed block diagram of the CM-BF561 module. Beside the SDRAM control pins the CM-BF561 has all other pins of the Blackfin processor at its two main 60 pin connectors.
A special feature of the CM-BF561 module is the availability of two parallel port interfaces (PPI) for different applications such as the simultaneous use of one camera and one display interface; the use of one stereo camera interface; or the use of two separate ports for bandwidth-hungry ADC and DAC interfaces.
Dynamic voltage control allows the reduction of power consumption to a minimum by adjusting the core voltage and the clock frequency dynamically in accordance to the required processing power.
A low voltage reset circuit guarantees a power on reset and resets the system when the input voltage drops below 2.93V.

2.2 Boot Mode

By default the Boot Mode is set to 01 (BMODE0 pin = HIGH, BMODE1 pin = LOW). In this configuration the BMODE0 pin and the BMODE1 pin have an on-board pull-down resistor (Figure 3-4, resistor R10 and R11 are mounted) and BMODE0 has an additional 0R resistor connected to 3.3V (Figure 3-4, resistor R8 is mounted). For setting the BMODE1 pin HIGH a 0R resistor must be mounted at R9. For Boot Mode 00 remove R8.

2.3 Memory Map

Memory Type	Start Address	End Address	Size	Comment
FLASH *)	0x20000000	0x207FFFFF	8MB	Intel PF48F2000P0ZBQ0
SDRAM	0x00000000	0x03FFFFFF	64MB	32Bit Bus, 2x Micron MT48LC16M16A2BG

Table 2-1: Memory Map

*) Please be aware that you have to unlock the flash before starting an erase process!

2.4 Electrical Specification

2.4.1 Supply Voltage

- 3.3V DC +/-10%

2.4.2 Supply Voltage Ripple

- 100mV peak to peak 0-20 MHz

2.4.3 Input Clock Frequency

- 25MHz

2.4.4 Supply Current

- Maximum supply current: 550mA at 3.3V and 1.2V Core Voltage
- Operating conditions:
    - Both core CPUs running at 600MHz, Core Voltage 1.21V, SDRAM 20% bandwidth utilization @ 120MHz: ca. 470mA
    - Both core CPUs running at 300MHz, Core Voltage 0.8V SDRAM 20% bandwidth utilization @ 100MHz: ca. 160mA
    - One core CPUs running at 500MHz, Core Voltage 1.16V SDRAM 20% bandwidth utilization @ 125MHz, other core idle: ca. 330mA

  All measurements done at an environmental temperature of 25°C.

2.4.5 Core Voltage and Frequency Requirements

Core voltage: 1.21V

Core clock frequency: 500 MHz (default setting)

Be aware that the core voltage set in the VR_CTL register doesn't match exactly with the effective core voltage measured. There is a difference of about 50mV, which is caused by the processor itself.
Don't operate the core module higher than these ratings without cooling otherwise there is a risk of overheating!

2.5 Environmental Specification

2.5.1 Temperature

- Operating at full 500MHz:: 0 to + 70° C
- Industrial temperature range on request only

Please be aware to operate the CM-BF561 in an environment with enough cooling. If you mount the core module in an enclosure please be aware that there is enough air flow. If an adequate air flow cannot be guaranteed we recommend the use of a heat sink or to reduce the core voltage and/or the core clock frequency.

2.5.2 Humidity

- Operating: 10% to 90% (non condensing)

3 CM-BF561

3.1 Mechanical Outline

Figure 3-1 shows the bottom view of the mechanical outline of the CM-BF561 Core Module. All dimensions are given in millimeters!

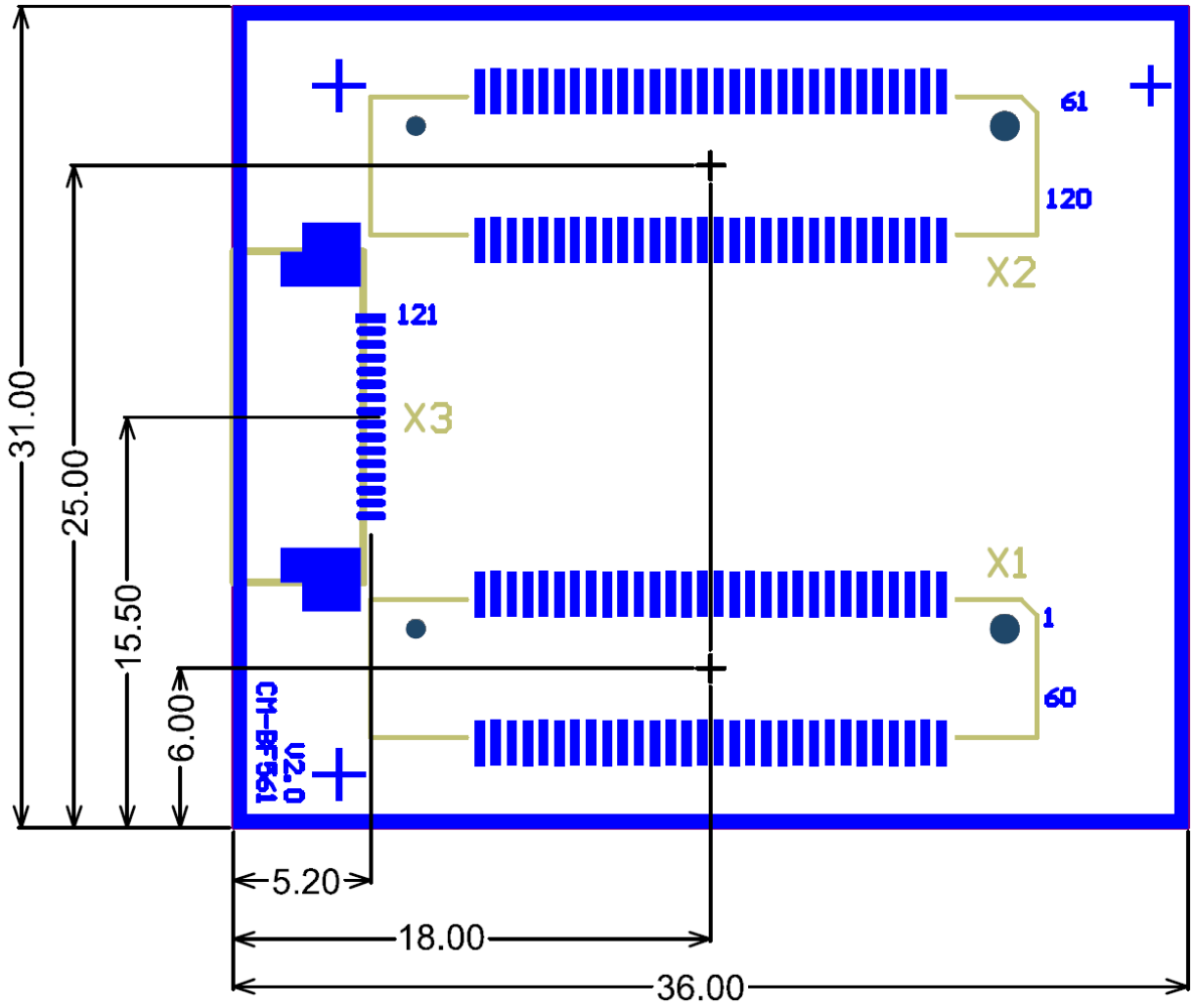

Figure 3-1: Mechanical outline and Bottom Connectors (**bottom view**)

The mechanical outline represents a bottom view of the connectors placed at the bottom of the core board.

The connectors on the CM-BF561 are of the following type:

Part	Manufacturer	Manufacturer Part No.
X1, X2	Hirose 3mm height	FX8-60P-SV(21)
X3	Molex FCC/FPC Connector	527451696

Table 3-1: Core Module Connector Types

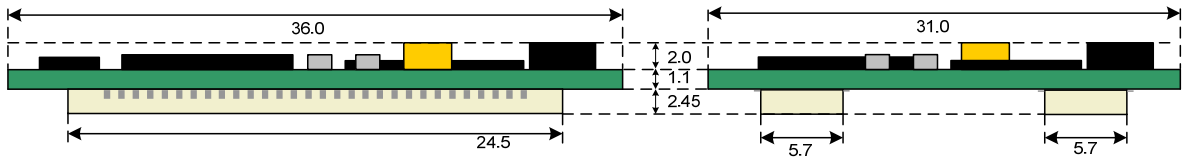

Figure 3-2: Side view with connector mounted

The total minimum mounting height including receptacle at the motherboard is 6.1mm.

3.1.1 Footprint

The optional 16 pole extension connector may be omitted if there is no need for the additional GPIO pins (see chapter 3.5).

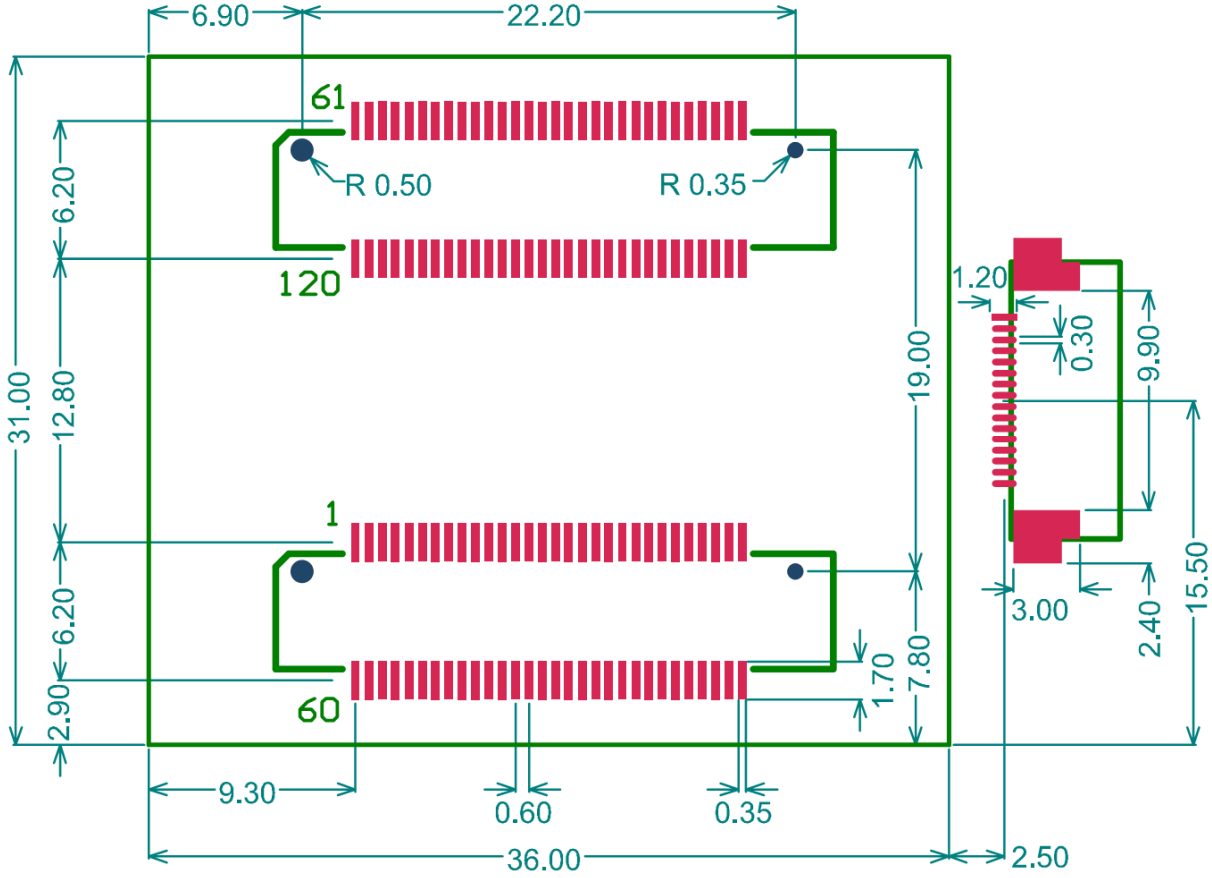

Figure 3-3: Recommended footprint and spacing (**top view**)

For the base board the following connectors have to be used.

Matching Connector	Manufacturer	Manufacturer Part No.
X1,X2	Hirose	FX8-60S-SV
X3	Molex FCC/FPC Connector	527451696

Table 3-2: Base Board Connector Types

Info: A Library of the Baseboards module for the Altium Designer 6.x can be obtained from Bluetechnix upon request.

3.1.2 Top Mounted Components

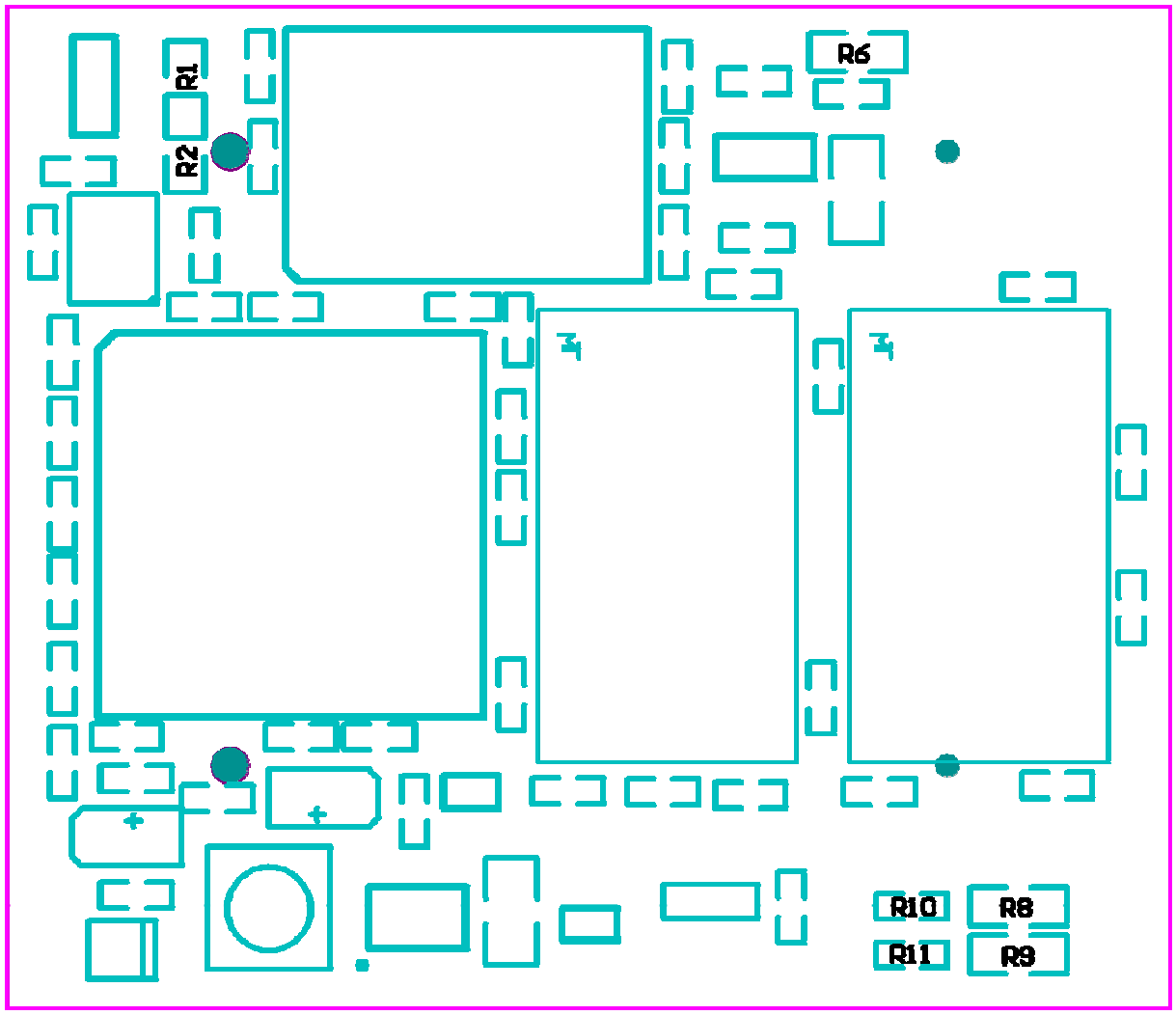

Figure 3-4: Top Overlay (**top view**)

See section 2.2 for the Boot Mode settings.

The resistors R1 and R2 switch between Clk_out (R1 mounted, default) and PF11 (R2 mounted) on pin 5 of the Core Module.

By mounting a 0R resistor at R6 you can write-protect the on-board flash.

3.2 Schematic Symbol (Signals of P1 and P2)

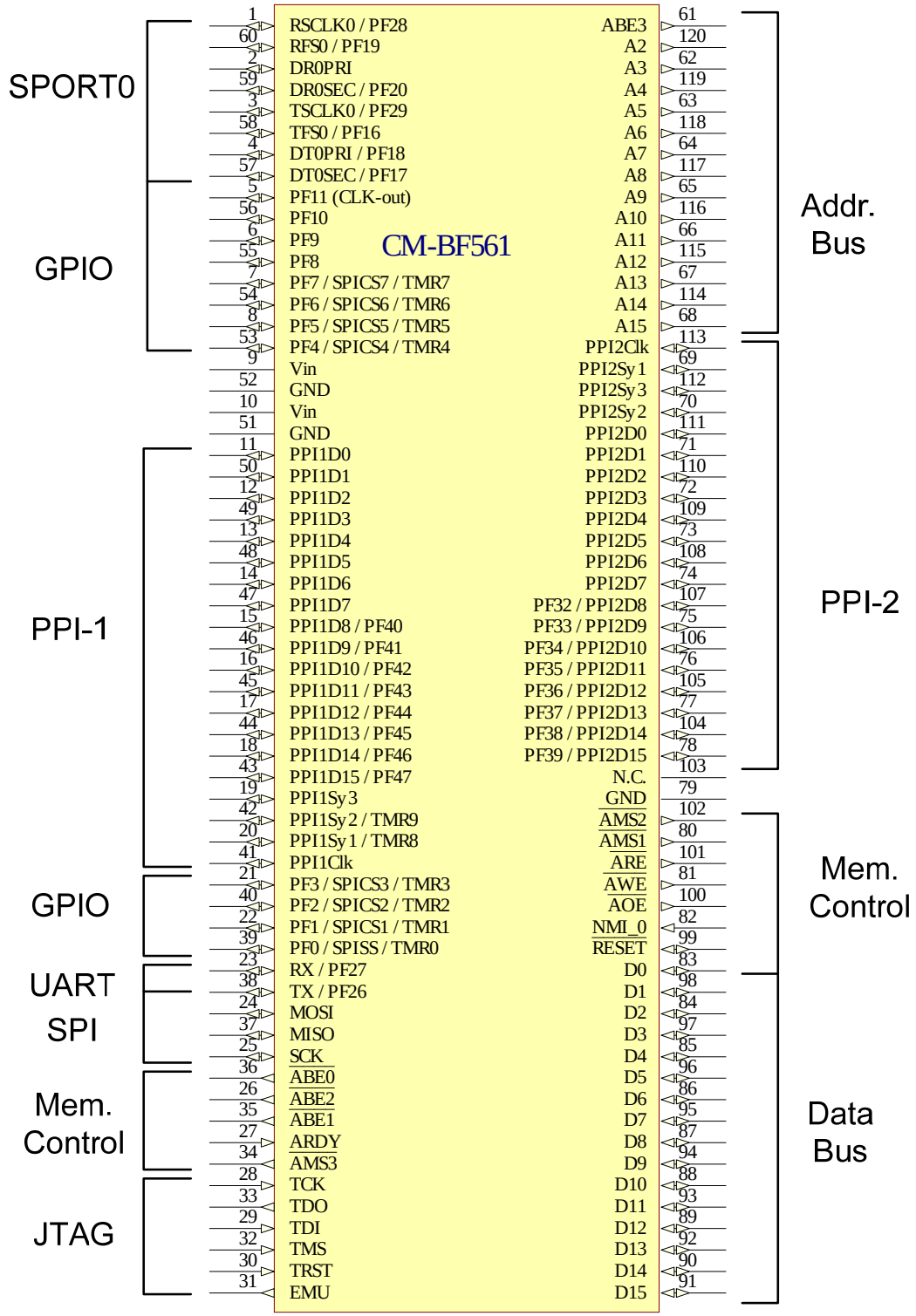

Figure 3-5: Schematic Symbol of the CM-BF561 Module

3.3 Connector X1 – (1-60)

Please mind the mounted pull up and pull down resistors on the Core Module (see the third column).

Pin No.	Signal	Signal Type.
1	RSCLK0 / PF28	I/O
2	DR0PRI	I
3	TSCLK0 / PF29	I/O
4	DT0PRI / PF18	I/O
5	PF11(Clk_out)*	I/O
6	PF9	I/O
7	PF7 / SPISEL7 / TMR7	I/O
8	PF5 / SPISEL5 / TMR5	I/O
9	Vin 3V3	PWR
10	Vin 3V3	PWR
11	PPI1D0	I/O
12	PPI1D2	I/O
13	PPI1D4	I/O
14	PPI1D6	I/O
15	PPI1D8 / PF40	I/O
16	PPI1D10 / PF42	I/O
17	PPI1D12 / PF44	I/O
18	PPI1D14 / PF46	I/O
19	PPI1SYNC3	I/O
20	PPI1SYNC1 / TMR8	I/O
21	PF3 / SSEL3 / TM3	I/O
22	PF1 / SSEL1 / TMR1	I/O
23	RX / PF27	I/O – 100k pull up
24	MOSI	I/O
25	SCK	I/O
26	$\overline{\text{ABE2}}$ / SDQM2	O
27	ARDY	I – 10k pull up
28	TCK	I – 10k pull up
29	TDI	I – 10k pull up
30	$\overline{\text{TRST}}$	I – 4k7 pull down
31	$\overline{\text{EMU}}$	O
32	TMS	I – 10k pull up
33	TDO	O
34	$\overline{\text{AMS3}}$	O
35	$\overline{\text{ABE1}}$/SDQM1	O
36	$\overline{\text{ABE0}}$/SDQM0	O
37	MISO	I/O
38	TX / PF26	I/O
39	PF0/SPISS/TMR0	I/O
40	PF2/SSEL2/TMR2	I/O
41	PPI1CLK	I
42	PPI1SYNC2 / TMR9	I/O

43	PPI1D15 / PF47	I/O
44	PPI1D13 / PF45	I/O
45	PPI1D11 / PF43	I/O
46	PPI1D9 / PF41	I/O
47	PPI1D7	I/O
48	PPI1D5	I/O
49	PPI1D3	I/O
50	PPI1D1	I/O
51	GND	PWR
52	GND	PWR
53	PF4/SPISEL4/TMR4	I/O
54	PF6/SPISEL6/TMR6	I/O
55	PF8	I/O
56	PF10	I/O
57	DT0SEC / PF17	O
58	TFS0 / PF16	I/O
59	DR0SEC / PF20	I
60	RFS0 / PF19	I/O

Table 3-3: Connector P1 Pin Assignment

All pin names of the connectors correspond to the names found in the Blackfin BF561 datasheet from Analog Devices.

*Mount option R1 and R2:
Default is R2 mounted - PF11 at the pin 5 of the connector; unmounting R2 and mounting to position R1 outputs the buffered clock on pin 5 of the connector. (See Figure 3-4)

3.4 Connector X2 – (61-120)

Please mind the mounted pull up and pull down resistors on the Core Module (see the third column).

Pin No.	Signal	Signal Type.
61	$\overline{\text{ABE3}}$/SDQM3	O
62	A3	O
63	A5	O
64	A7	O
65	A9	O
66	A11	O
67	A13	O
68	A15	O
69	PPI2SYNC1	I/O
70	PPI2SYNC2	I/O
71	PPI2D1	I/O
72	PPI2D3	I/O
73	PPI2D5	I/O
74	PPI2D7	I/O

75	PPI2D9 / PF33	I/O
76	PPI2D11 / PF35	I/O
77	PPI2D13 / PF37	I/O
78	PPI2D15 / PF39	I/O
79	GND	PWR
80	$\overline{\text{AMS1}}$	O
81	$\overline{\text{AWE}}$	O
82	NMI_0	I - 10k pull down
83	D0	I/O
84	D2	I/O
85	D4	I/O
86	D6	I/O
87	D8	I/O
88	D10	I/O
89	D12	I/O
90	D14	I/O
91	D15	I/O
92	D13	I/O
93	D11	I/O
94	D9	I/O
95	D7	I/O
96	D5	I/O
97	D3	I/O
98	D1	I/O
99	$\overline{\text{RESET}}$	I – see chapter 3.6
100	$\overline{\text{AOE}}$	O
101	$\overline{\text{ARE}}$	O
102	$\overline{\text{AMS2}}$	O
103	N.C.	-
104	PPI2D14 / PF38	I/O
105	PPI2D12 / PF36	I/O
106	PPI2D10 / PF34	I/O
107	PPI2D8 / PF32	I/O
108	PPI2D6	I/O
109	PPI2D4	I/O
110	PPI2D2	I/O
111	PPI2D0	I/O
112	PPI2SYNC3	I/O
113	PPI2CLK	I
114	A14	O
115	A12	O
116	A10	O
117	A8	O
118	A6	O
119	A4	O
120	A2	O

Table 3-4: Connector P2 Pin Assignment

3.5 Optional Expansion Connector X3 – (1-16)

There is an optional expansion connector mounted on the bottom side of the Core Module. He makes accessible some more GPIO pins via a 16 pol FFC (flat flex cable). See the following Symbol and Table for detail information.

Pin No.	Signal	Signal Type.
121	GND	PWR
122	SCLK0	I/O
123	GND	PWR
124	RSCLK1/PF30	I/O
125	RFS1/PF24	I/O
126	DR1PRI	I/O
127	DR1SEC/PF25	I/O
128	TSCLK1/PF31	I/O
129	TFS1/PF21	I/O
130	DT1PRI/PF23	I/O
131	DT1SEC/PF22	I/O
132	PF15/EXTCLK	I/O
133	PF14	I/O
134	PF13	I/O
135	PF12	I/O
136	GND	PWR

Table 3-5: Optional Connector X3 Pin Assignment

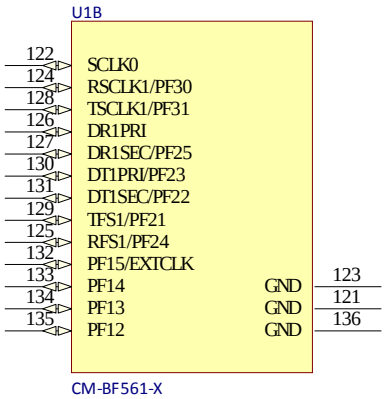

Figure 3-6: Optional Extension Connector Symbol

3.6 Reset circuit

The reset of the flash and the processor are connected to a power monitoring IC. The output can be used as power on reset for external devices, see Figure 3-7.

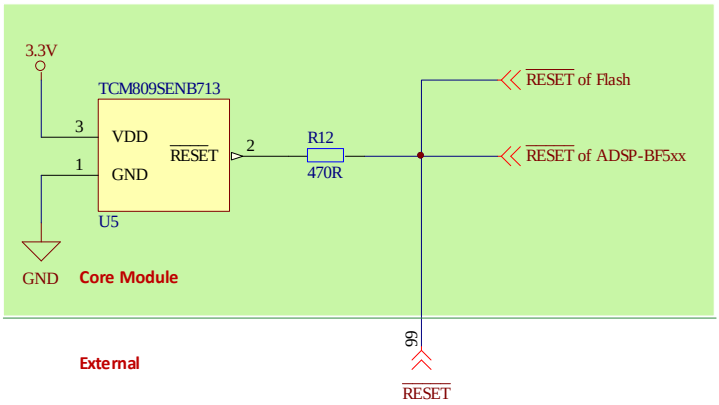

Figure 3-7: Schematic of reset circuit on the Core Module

4 Application Examples

4.1 Sample Application

In this sample application the Core Module is used as a high performance SPI based co-processor module.

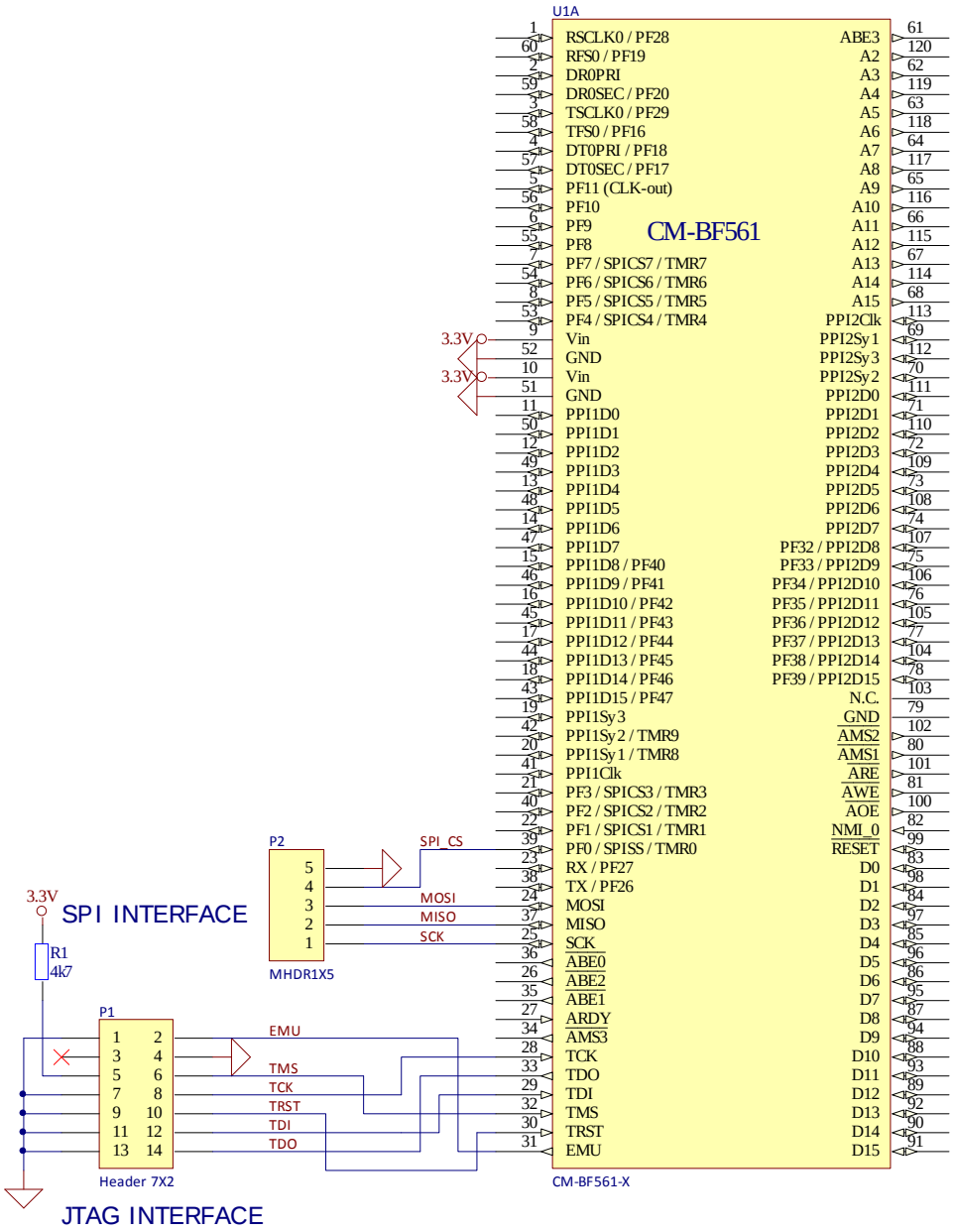

Figure 4-1: Sample Application with SPI and JTAG Connector, no more pins required.

4.2 Stereo Camera System

Figure 4-2: Image Recognition System with Stereo Cameras

4.3 High Performance Symmetric Processing System

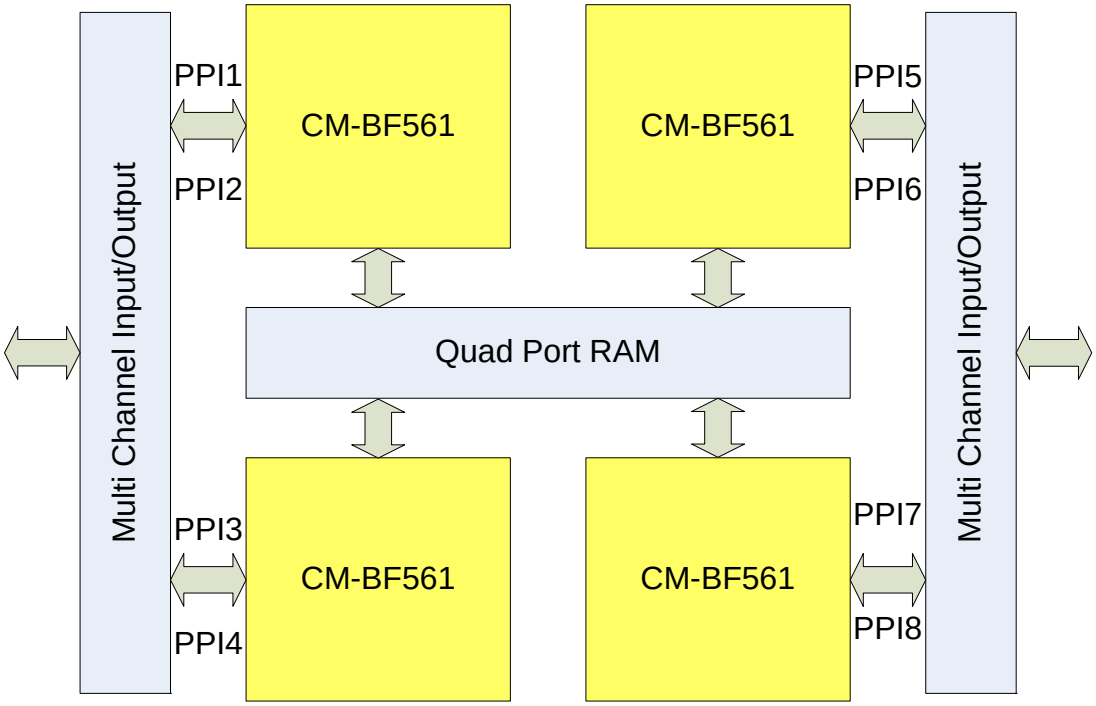

Figure 4-3: Block Diagram: Symmetric Processing System

4.4 Video Processing System

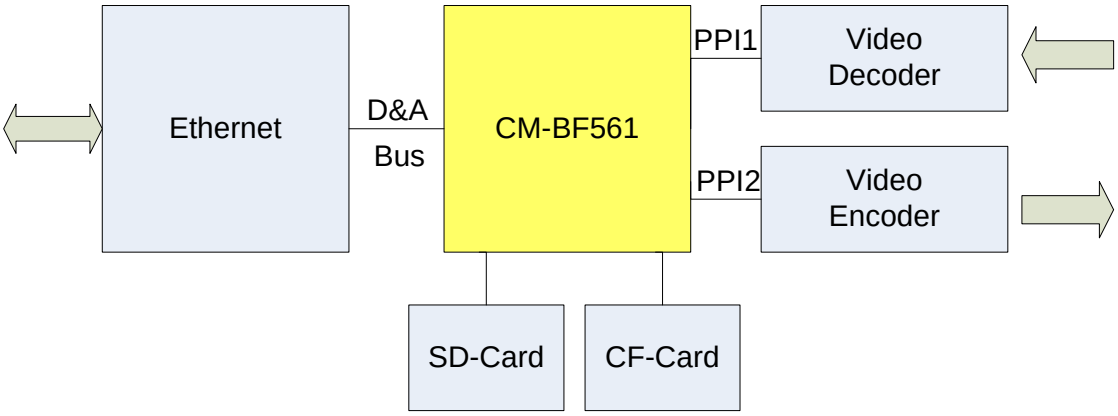

Figure 4-4: Real-time Video Processing System

4.5 Design Services

Bluetechnix offers custom design services and software development.

5 Software Support

5.1 BLACKSheep

The Core Module is delivered with a pre-flashed basic version of the BLACKSheep VDK multithreaded framework. It contains a boot-loader for flashing the Core Module via the serial port.

Please mind the software development documents.

5.2 uClinux

The Core Module is fully supported by the open source platform at http://blackfin.uclinux.org. Since the Core Modules are pre-flashed with BLACKSheep you have to flash uBoot first. To flash uBoot you can use the BLACKSheep boot-loader.

6 Anomalies

For the latest information regarding anomalies for this product, please consult the product home page:

http://www.bluetechnix.com/goto/cm-bf561

7 Production Report for CM-BF561 (100-1211)

Version	Component	Type
V1.2	Processor	ADSP-BF561SKBCZ600 (Rev 0.3) (Analog Devices)
	RAM	MT48LC16M16A2BG-75IT:D (Micron)
	FLASH	PF48F2000P0ZBQ0 (Intel)
V2.0 R20-1000 to R20-2999	Processor	ADSP-BF561SKBCZ600 (Rev 0.3)
	RAM	MT48LC16M16A2BG-75IT:D (Micron)
	FLASH	PF48F2000P0ZBQ0 (Intel)
V2.0 R20-3000 to R20-3210	Processor	ADSP-BF561SKBCZ600 (Rev 0.5) (Analog Devices)
	RAM	MT48LC16M16A2BG-75IT:D (Micron)
	FLASH	PF48F2000P0ZBQ0 (Intel)
V2.0.5	Processor	ADSP-BF561SKBCZ600 (Rev 0.5) (Analog Devices)
	RAM	MT48LC16M16A2BG-75IT:D (Micron)
	FLASH	PF48F2000P0ZBQ0 (Intel)

Table 7-1: Production Report CM-BF561

8 Product Changes

For the latest product change information please consult the product web-page at:

http://www.bluetechnix.com/goto/cm-bf561

Version	Changes
V1.x to V2.0	64 Mbit Flash, 64MB RAM instead of 32Mbit Flash and 32MB RAM
	Additional optional bottom FFC connector with 13 Processor pins

Table 8-1: Product Changes

How do these changes affect the Software developed for V1.x Modules?

Flash chip:

The flash chip has changed on CM-BF561V2 to an Intel P30 Flash.
If you use write accesses to the flash now you have to unlock the appropriate sectors first by using the unlock command as shown in the c-code segment below:

```
nFlashAddr = (unsigned short *)(FLASH_START_ADDRESS + pa_nSectorAddr);
*nFlashAddr = 0x0050; //reset statusregister
asm("ssync;");
*nFlashAddr = 0x0060;  // unlock command
asm("ssync;");
*nFlashAddr = 0x00d0;  // confirm unlock command
```

Also be aware that the flash is a bottom Boot which means the first 4 sectors have 32kByte then all sectors have 128kByte as in the J3 Flash.
This probably won't affect your application at all, since you may have read only code in these sections anyway.

SDRAM:

The SDRAM size on V2 is 64MByte (32Mbyte on V1). If you want to be able to use the upper 32MByte you have to change an entry in the SDRAM BANK CONTROL REGISTER to enable the upper 32MByte:
For CM-BF561-V2 (64MByte):

```
EBIU_SDBCTL = 0x0015
For version 1 (32MByte):
EBIU_SDBCTL = 0x0013
```

If 32Mbytes is enough you can leave your V1.x software unchanged.

9 Document Revision History

Version	Date	Document Revision
11	2008-02-19	NMI pull down added
10	2008-12-02	Pull up/down information added Reset circuit added
9	2008-09-03	Footprint and mechanical drawings updated
8	2008-09-03	Footprint and mechanical drawings updated
7	2008-08-14	English checked for spelling, grammar and clarity
6	2008-04-30	Chapter 2.2, boot mode settings
5	2007-10-01	P3 numbering – picture and table,
4	2007-05-31	Flash and SD RAM hints + Chip numbers
3	2007-05-23	Updated Fig.1 changed Ra, Rb to R1 R2 in Figures
2	2007-05-15	Added Chapter 7 description of possible software changes
1	2007-04-11	First release V1.0 of the Document

Table 9-1: Revision History

A List of Figures and Tables

Figures

Tables