DRS4 Evaluation Board User's Manual

Board Revision 2.0
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Revision History

Date	Modification
2 March 09	Initial Revision
27 April 09	Mention input range, added timing calibration description

Table of Contents

1. Introduction

The DRS4 chip, which has been designed at the Paul Scherrer Institute, Switzerland by Stefan Ritt and Roberto Dinapoli is a Switched Capacitor Array (SCA) capable of digitizing eight channels at sampling speeds up to 6 GSPS. This chip is available through the PSI technology transfer program for other institutes and organizations. In order to simplify the design process to integrate the DRS4 chip into custom electronics, an evaluation board has been designed, which demonstrates the basic operation of the chip. It has SMA connectors for four input channels CH1 to CH4, an USB 2.0 connector and a LEMO trigger input (Figure 1). The board is powered through the USB port and contains an on-board trigger logic. It comes with MS Windows® and Linux drivers and two application programs. It is basically equivalent to a four channel 5 GSPS digital oscilloscope.

This manual describes the software installation, the usage of the application programs, and gives hints for developers seeking to build new electronics around the DRS4 chip.

1.1. Board description

Since the DRS4 chip has differential inputs, the board uses four transformers (ADT1-1WT from Mini-Circuits®) to converted the 50-Ohm terminated single ended inputs into differential signals. The transformers are followed by analog switches (ADG936 form Analog Devices®). These switches allow the multiplexing of the DRS4 inputs between the input connectors and a reference voltage generated by the on-board 16-bit DAC for calibration purposes. The four analog inputs ar AC coupled and have a input range of 1 V peak-to-peak. The absolute maximum input voltage range is -0.5V to +2.8V. The DRS4 is read out with a 14-bit ADC (AD9245 from Analog Devices®) and a FPGA (Xilinx® Spartan 3). The USB connection is implemented with a micro controller (Cypress® CY2C68013A). The high speed modus of the USB 2.0 bus allows for data transfer rates of more than 20 MB/sec.

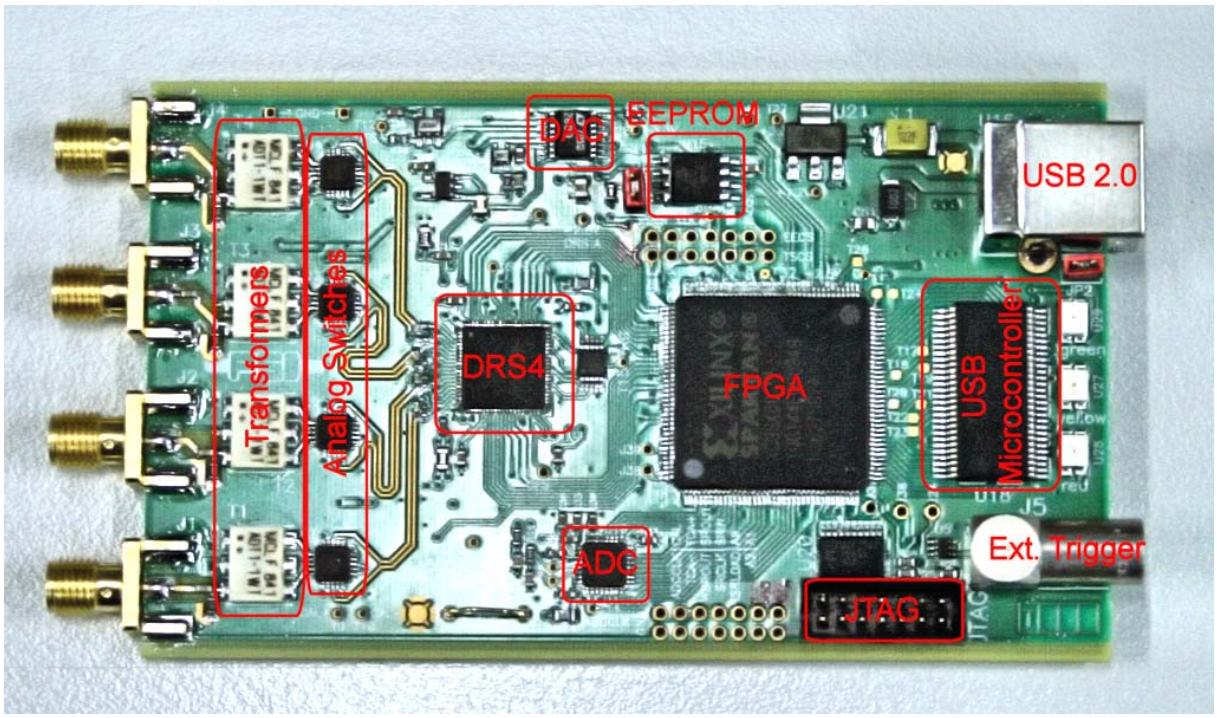


Figure 1: Picture of the DRS4 Evaluation Board with different components

For trigger purposes, a 50 Ω terminated TTL compatible input is implemented (Lemo connector). Since the input is 50 Ω terminated, care has to be taken that the trigger source is able to drive at least 2.2 V into 50 Ω.

A on-board discriminator with programmable level allows for self triggering on any of the four input channels. An 1 MBit EEPROM (25LC1025 from Microchip®) is used to store the board serial number and calibration information. Two 14-pin headers carry all important logical signals which allow easy debugging with a logic analyzer or oscilloscope. A JTAG adapter can be used to update the FPGA firmware through a Xilinx® Platform Cable Adapter.

The specifications of the board inputs is summarized in following table:

Analog inputs		
Termination	50 Ω	
Input range	1 V p-p	AC coupled
Maximum allowed input voltage	-0.5 V to +2.8 V	
Trigger input		
Termination	50 Ω	
Maximum allowed input voltage	-0.5 V to +5.5 V	5 V TTL compatible
High Level Input Voltage	2.2 V (max)	

1.2. Firmware Description

Both the Windows and the Linux distribution contain a subdirectory "firmware" which contains the FPGA and Microcontroller firmware for the DRS4 Evaluation Board. The FPGA firmware is written in pure VHDL, thus making it easy to port it to other FPGA devices such as Altera® or Lattice®. Only a few Xilinx® basic components such as clock managers and I/O blocks have been instantiated and must be adapted when another FPGA manufacturer than Xilinx® is chosen. The FPGA source code is contained in several files with following contents:

`src/drs4_eval1.vhd`	Top level entity. Routing of clock signals, global reset signal, LEDs and LEMO input
`src/drs4_eval1_app.vhd`	Main file containing state machines for DRS4 readout, serial interface to DAC, EEPROM and temperature sensor, trigger logic and reference clock generation
`src/usb_dpram.vhd`	Instantiates block ram for waveform storage
`src/usb_racc.vhd`	Interface to CY2C68013A microcontroller in slave FIFO mode. Implements a set of status and control registers through which the main application can be controlled
`src/usr_clocks.vhd`	Generates 66 MHz, 132 MHz, 264 MHz and a phase shifted 66 MHz clock out of the 33 MHz quartz input frequency via the Xilinx® Digital Clock Managers (DCM)
`ucf/drs4_eval1.ucf`	Constraint file. Assigns package pins and defines clock constraints
`3s400/drs4_eval1.ise`	Xilinx® ISE 9.2i project file
`3s400/drs4_eval1.bit`	Compiled firmware image directly for Spartan 3s400 FPGA

3s400/drs4_eval1.mcs	Compiled firmware image for FPGA EEPROM XCF02S
3s400/drs4_eval1.ipf	Xilinx® Impact project file to program FPGA via download cable

The firmware for the USB microcontroller from Cypress® is written in C and must be compiled with the Keil® 8051 C compiler. It contains the standard include and library files from the Cypress EZ-USB® development kit plus some DRS specific files:

CY7C68013A/drs_eval.c	Main micro controller firmware file
CY7C68013A/dscr.a51	USB descriptor tables
CY7C68013A/drs_eval.hex	Compiled firmware file (Intel HEX format)
CY7C68013A/drs_eval1.iic	Compiled firmware file (For Cypress EZ-USB Console download)
CY7C68014A/*	Remaining files are standard files from EZ-USB development kit

The FPGA firmware implements a set of control and status registers, through which the DRS4 can be controlled and read out. The mapping of the control registers is as follows:

#	Ofs.	Bit	Name	Comment
0	0x00	0	start_trig	Write a "1" to start the domino wave
0	0x00	1	reinit_trig	Write a "1" to stop & reset the DRS chip
0	0x00	2	soft_trig	Write a "1" to stop the DRS chip & read the data to RAM
0	0x00	3	eeprom_write_trig	Write contents of RAM into EEPROM (32kB page)
0	0x00	4	eeprom_read_trig	Read contents of EEPROM into RAM (32kB page)
0	0x02	18	led	1=on, 0=blinks once at beginning of DRS chip readout
0	0x02	19	tcal_en	Switch on (1) / off (0) 264 MHz calib. sig. for DRS chips
0	0x02	20	tcal_source	System clock (0) or separate quartz (1) clock source
0	0x02	21	transp_mode	1=send DRS inputs to outputs ("transparent mode")
0	0x02	22	enable_trigger1	Write a "1" to enable external trigger (LEMO)
0	0x02	23	readout_mode	0:start from first bin, 1:start from domino stop
0	0x02	24	neg_trigger	1=trigger on high to low transition
0	0x02	25	acalib	Write "1" to enable amplitude calibration
0	0x02	27	dactive	0:stop domino wave during readout, 1:keep it running
0	0x02	28	standby	1: put chip in standby mode
0	0x02	29	trigger_source1	Analog trigger source bits CH1-CH4
0	0x02	30	trigger_source2	Analog trigger source bits CH1-CH4
0	0x02	31	enable_trigger2	Write a "1" to enable analog trigger
1	0x04	31..16	DAC0	Set DAC 0 (=A, ROFS)
1	0x06	15..0	DAC1	Set DAC 1 (=B, CMOFS)
2	0x08	31..16	DAC2	Set DAC 2 (=C, CAL-)
2	0x0A	15..0	DAC3	Set DAC 3 (=D, CAL+)
3	0x0C	31..16	DAC4	Set DAC 4 (=E, BIAS)
3	0x0E	15..0	DAC5	Set DAC 5 (=F, TLEVEL)
4	0x10	31..16	DAC6	Set DAC 6 (=G, O-OFS)
4	0x12	15..0	DAC7	Set DAC 7 (=H, -)

5	0x14	31..24	configuration	Bit0: DMODE, Bit1: PLLEN, Bit2: WSRLOOP
5	0x14	23..16	channel_config	1=1x8k,0x11=2x4k,0x33=4x2k,0xFF=8x1k
5	0x16	7..4	first_chn	First channel address to read out (0..9)
5	0x16	3..0	last_chn	Last channel address to read out (1..9)
6	0x18	31..16	trigger_delay	Trigger delay in ticks of roughly 0.56 ns
6	0x1A	15..0	sampling_freq	Sampling frequency in ticks (=1024/f_{samp}*0.120-2)
7	0x1C	31..16	zero_supp_thresh	Not yet implemented
8	0x1E	15..0	eeprom_page	Page number for EEPROM communication

While the mapping of the status registers is like this:

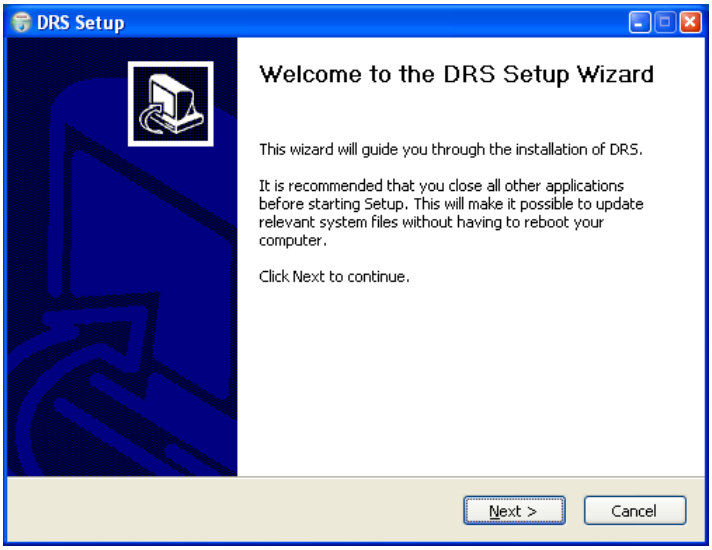
#	Ofs.	Bits	Name	Comment
0	0x00	31..16	board_magic	0xC0DE, Magic number for DRS board identification
0	0x02	15..8	board_type	5 for DRS4 USB Evaluation Board 1.1
0	0x02	7..0	drs_type	4 for DRS4
1	0x04	0	running	"1" while domino wave running or readout in progress
2	0x08	31..16	stop_cell	position of cell where sampling stopped at last trigger
8	0x20	31..16	temperature	temperature in 0.0625 deg. C units
9	0x24	31..16	serial_cmc	Serial number CMC board
9	0x26	15..0	version_fw	firmware version (SVN revision)

All registers are implemented as 32-bit registers, so they can be mapped easily into some VME address space for example if one decides to build a VME board containing the DRS4.

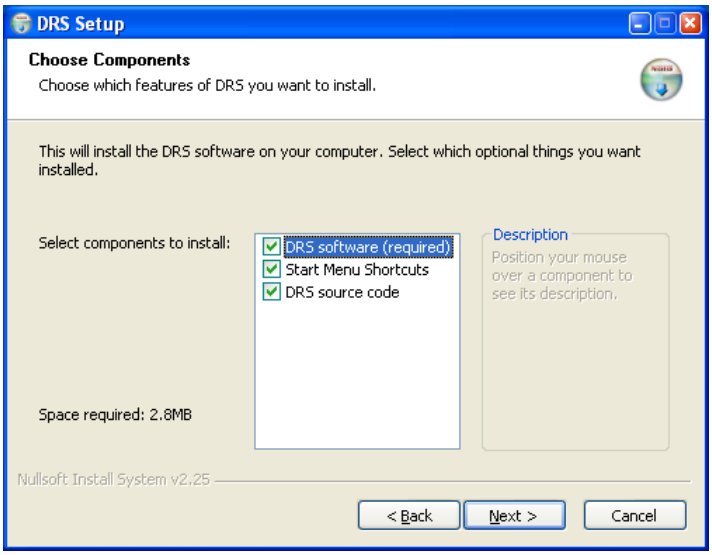
2. Installation

2.1. Windows XP

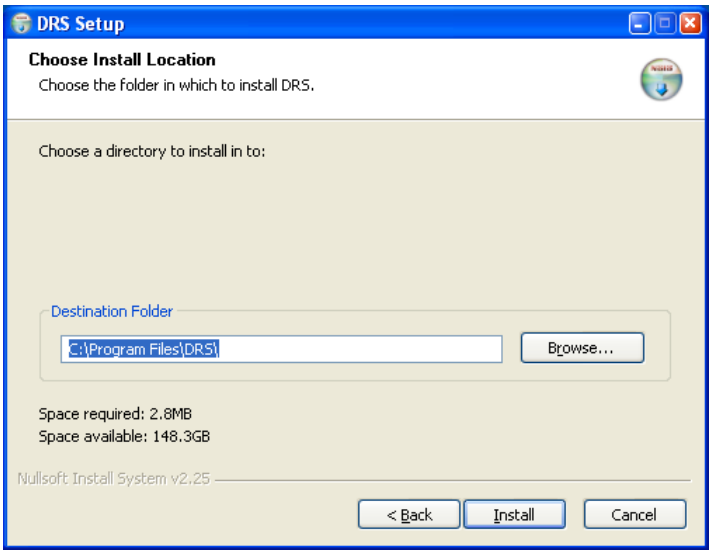
Under MS Windows® it is important to install the necessary driver before connection the DRS4 Evaluation Board with the PC. The current distribution can be downloaded from http://drs.web.psi.ch/download . The Windows version contains a single program **`drs-xx.exe`** (where **`xx`** is the version) which can be executed to install the driver, applications, documentation and source code. Executing this file starts the installer:



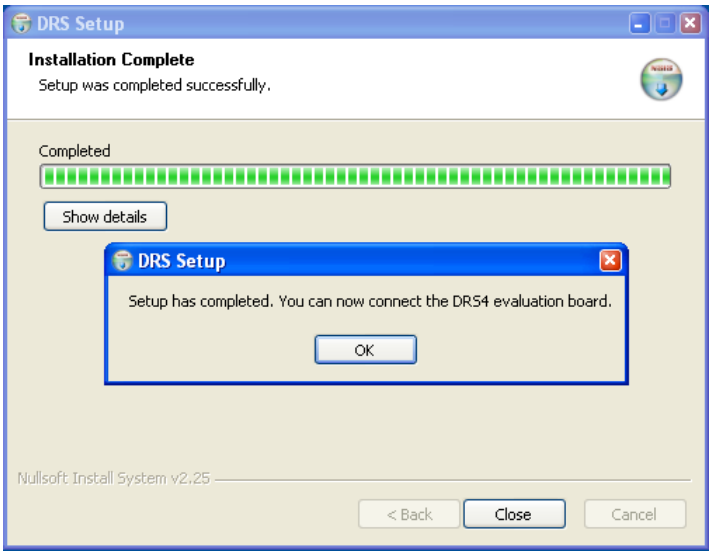
You can select which components to be installed:



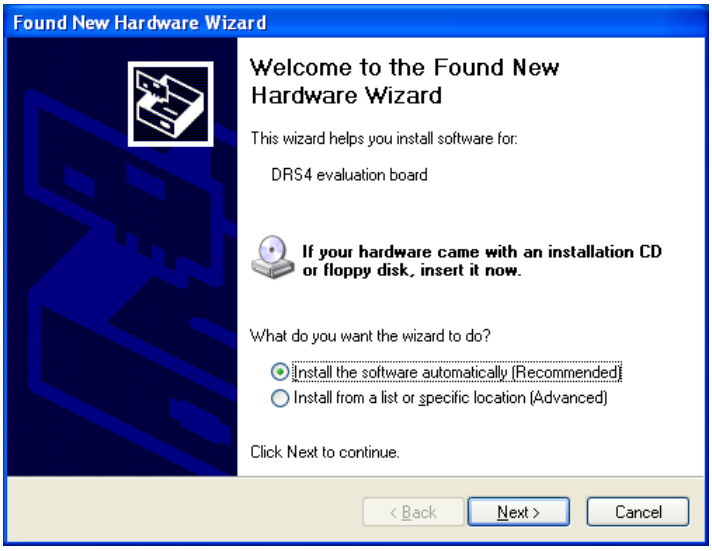
Then you can select the installation directory:



After the installer has finished, you can connect the DRS4 Evaluation Board to the Computer:



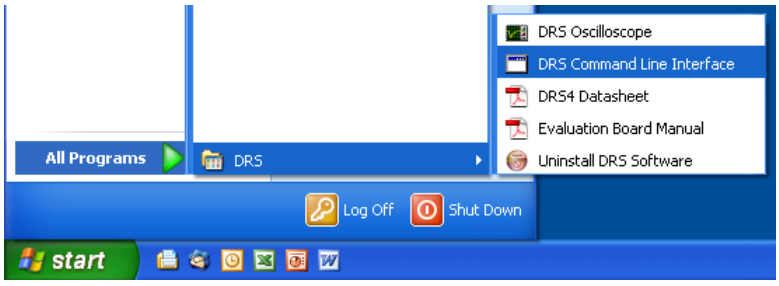
Now you will see the "Found New Hardware" dialog:



Where you can click "Install the software automatically" and then click "Next".

After successful installation of the driver, you will see the following window:

And a new group in your Start Menu:



The software comes with two applications, a command line interface and an oscilloscope. These applications are explained in section 3.

2.2. Linux

The drivers and applications are distributed for Linux in source code and must be compiled on each system. First untar the tar ball:

```
[/usr/local]$ tar -xzvf drs-1.0.tar.gz
drs-1.0/
drs-1.0/doc/
drs-1.0/doc/DRS4_rev06.pdf
drs-1.0/doc/manual.pdf
drs-1.0/include/
drs-1.0/include/ConfigDialog.h
drs-1.0/include/DOFrame.h
drs-1.0/include/DOScreen.h
. . .
```

Then change the directory and do a „make". Note that to compile the oscilloscope application it is necessary to have the wxWidgets package version 2.8.9 or later installed. You can obtain this package in source form from http://www.wxwidgets.org/downloads/. If this package is present, you can change to the drs directory and issue a make:

```
[/usr/local]$ cd drs-1.0
[/usr/local/drs-1.0]$ make
g++ -g -O2 -Wall -Wuninitialized -fno-strict-aliasing -Iinclude -DOS_LINUX
-DHAVE_LIBUSB -c src/musbstd.c
g++ -g -O2 -Wall -Wuninitialized -fno-strict-aliasing -Iinclude -DOS_LINUX
-DHAVE_LIBUSB -c src/mxml.c
...
```

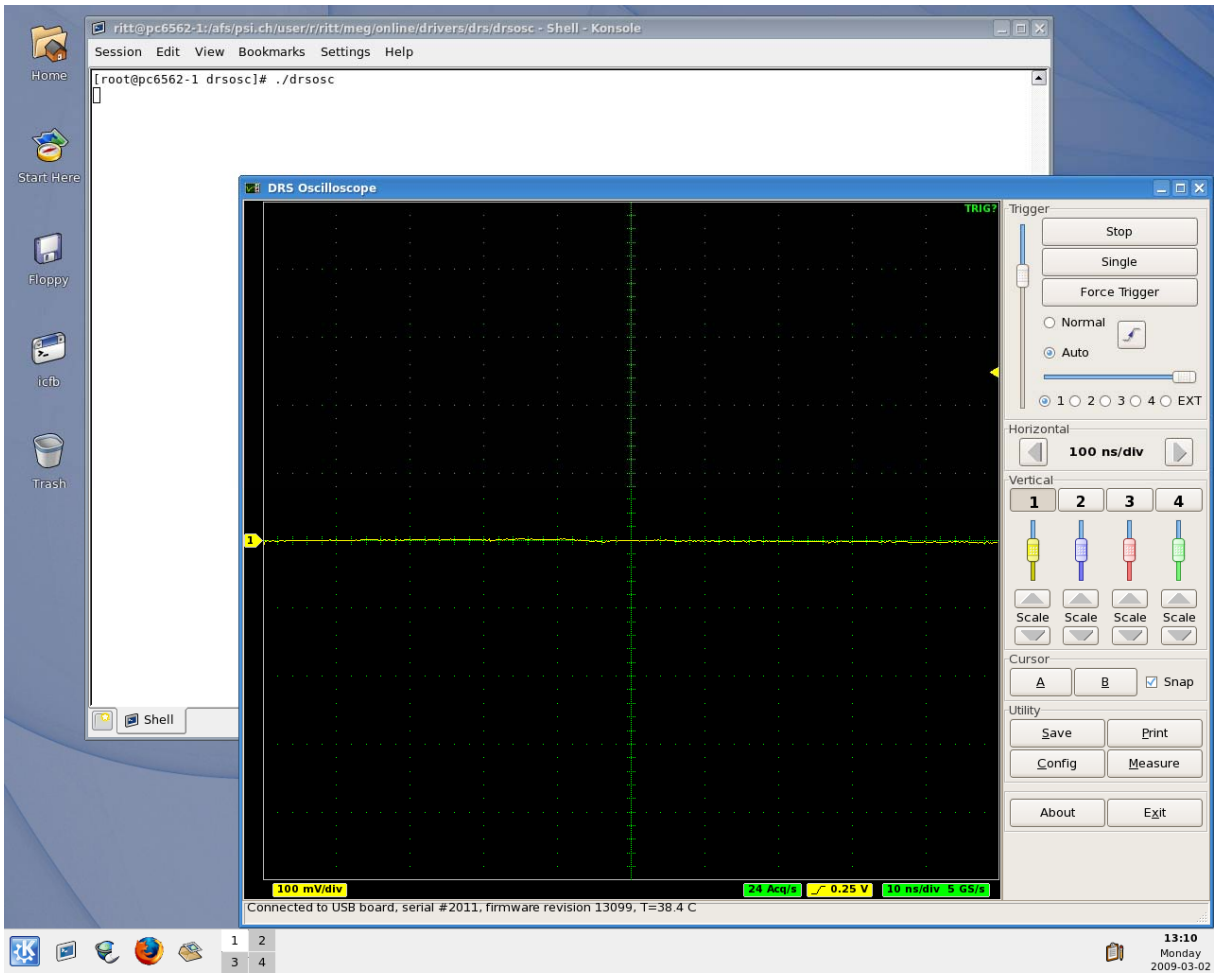
Now you can connect the DRS4 board to the PC. On systems where the "lsusb" tool is installed, one should be able to find the DRS4 evaluation board after connecting it with following command:

```
[/usr/local/drs-1.0]$ /sbin/lsusb -d 04b4:1175 –v

Bus 005 Device 005: ID 04b4:1175 Cypress Semiconductor Corp.
Device Descriptor:
  bLength                18
  bDescriptorType         1
  bcdUSB               2.00
  bDeviceClass            0 (Defined at Interface level)
  bDeviceSubClass         0
  bDeviceProtocol         1
  bMaxPacketSize0        64
  idVendor           0x04b4 Cypress Semiconductor Corp.
  idProduct          0x1175
  bcdDevice            0.01
  iManufacturer           1 S. Ritt PSI
  iProduct                2 DRS4 Evaluation Board
  iSerial                 3 REV1
  bNumConfigurations      1
  Configuration Descriptor:
    bLength                 9
    bDescriptorType         2
    wTotalLength           46
    bNumInterfaces          1
    bConfigurationValue     1
    iConfiguration          0
    bmAttributes         0x80
    MaxPower              500mA
...
```

If the board is correctly recognized, one can access it with the command line program. Under most Linux distributions however, only the "root" user can directly access USB devices. Some systems can be configured to allow non-root access via the "udev" system, but the exact instructions vary from distribution to distribution and can therefore not be given here.

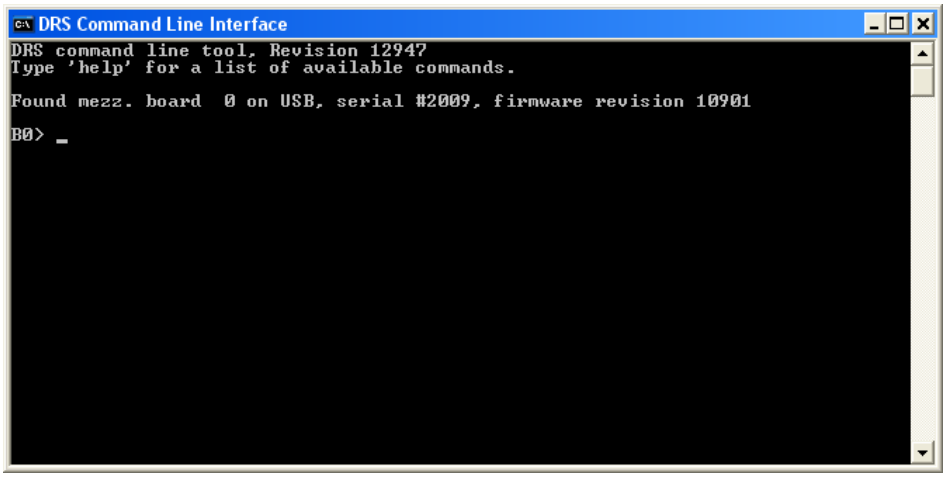
If the command line program works, the oscilloscope application "drsosc" can be started. It will open a X window and show exactly the same functionality as its Windows counterpart:



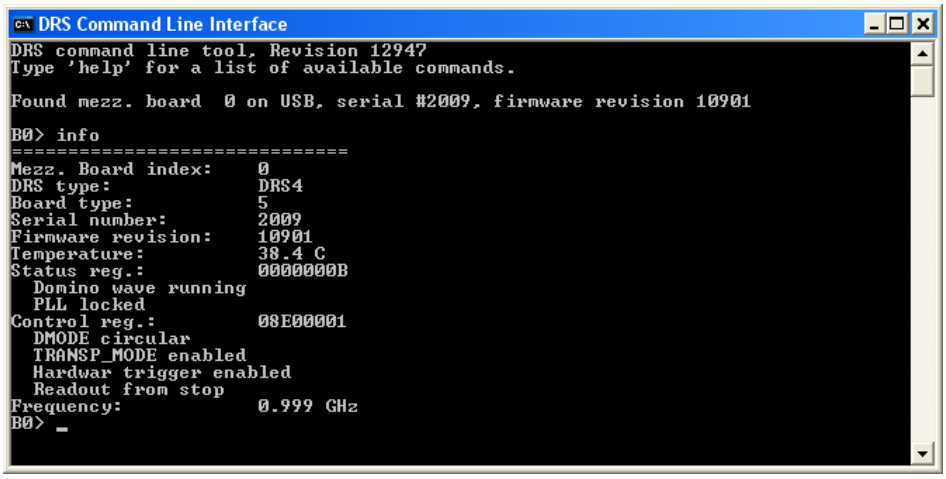
3. Running the Board

3.1. Command line Interface "drscl"

Clicking on „DRS Command Line Interface" (Windows) or entering "drscl" (Linux) will start a simple application which connects to the DRS4 Evaluation Board. If it finds the board, it displays the board serial number and the firmware revision as on the following screen shot:

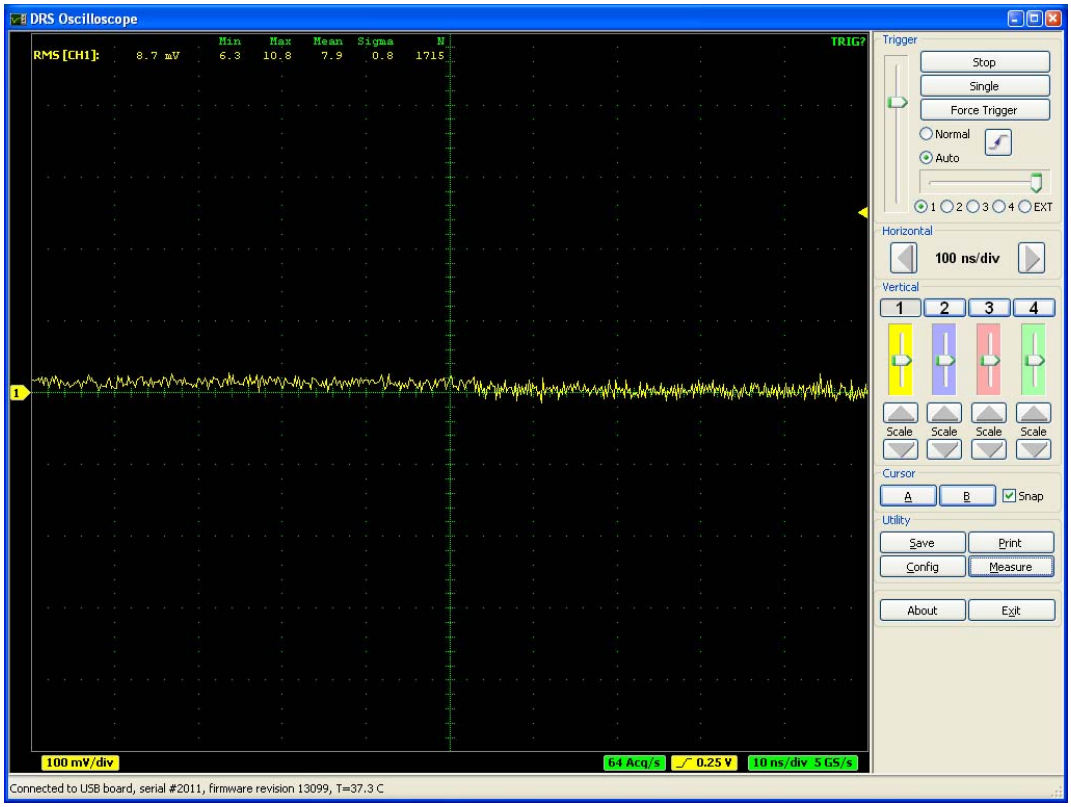


Now you are ready to issue your first command "info" which shows some more information, like the current board temperature. The temperature sensor is on the bottom side just below the DRS4 chip. If you keep issuing "info" commands and touch that sensor with your finger, you should see the temperature increase.

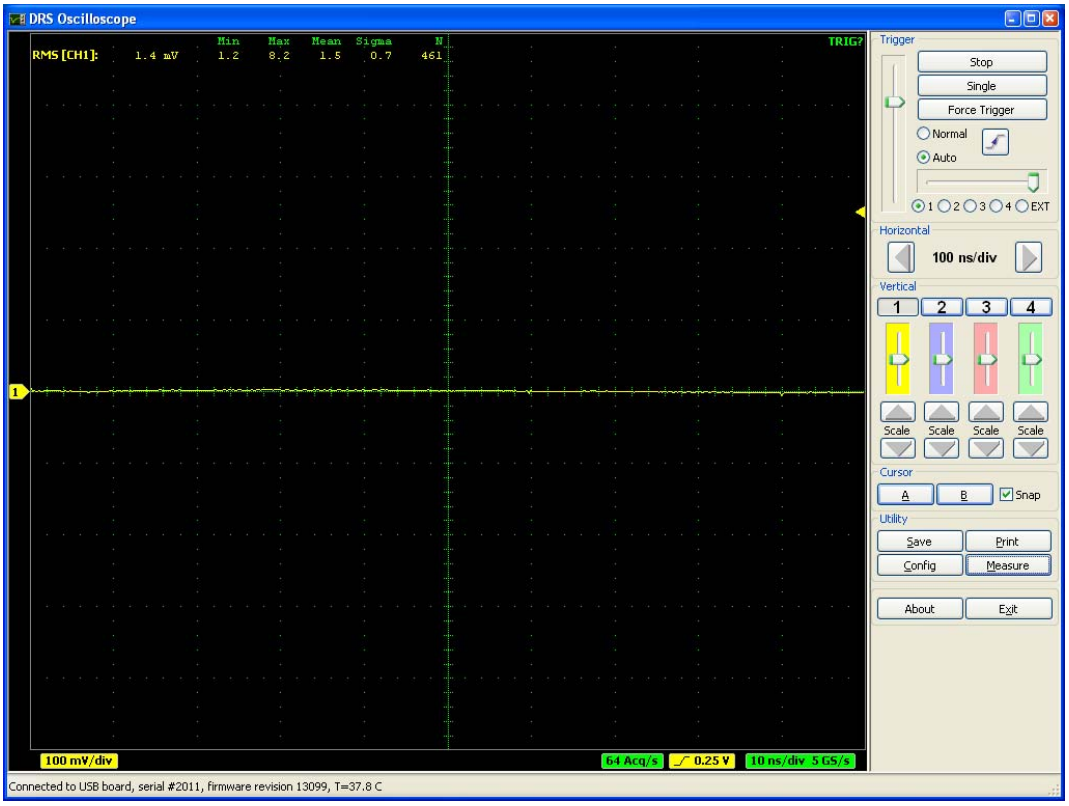


Oscilloscope application

The second application is an oscilloscope-like program, which connects to the DRS4 board and works pretty much like a normal oscilloscope. You can select the trigger mode, trigger level and trigger source. On Rev. 1.1 of the DRS4 evaluation board, only CH1 can be selected as trigger source. You enable a channel by clicking on the number "1" to "4". There are two cursors and a few utilities.

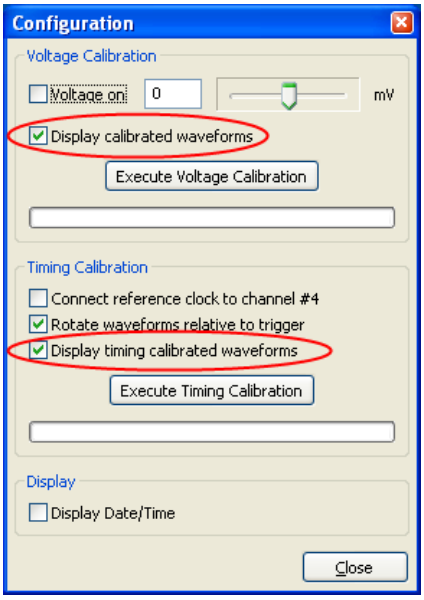


The picture above shows an un-calibrated evaluation board, which shows a noise level of about 8 mV RMS. After offset and gain calibrations, the noise level is reduced significantly:



The evaluation board Rev. 2.0 still shows some small random spikes originating probably from the USB interface. It is expected that future versions will improve this and reduce the noise level further.

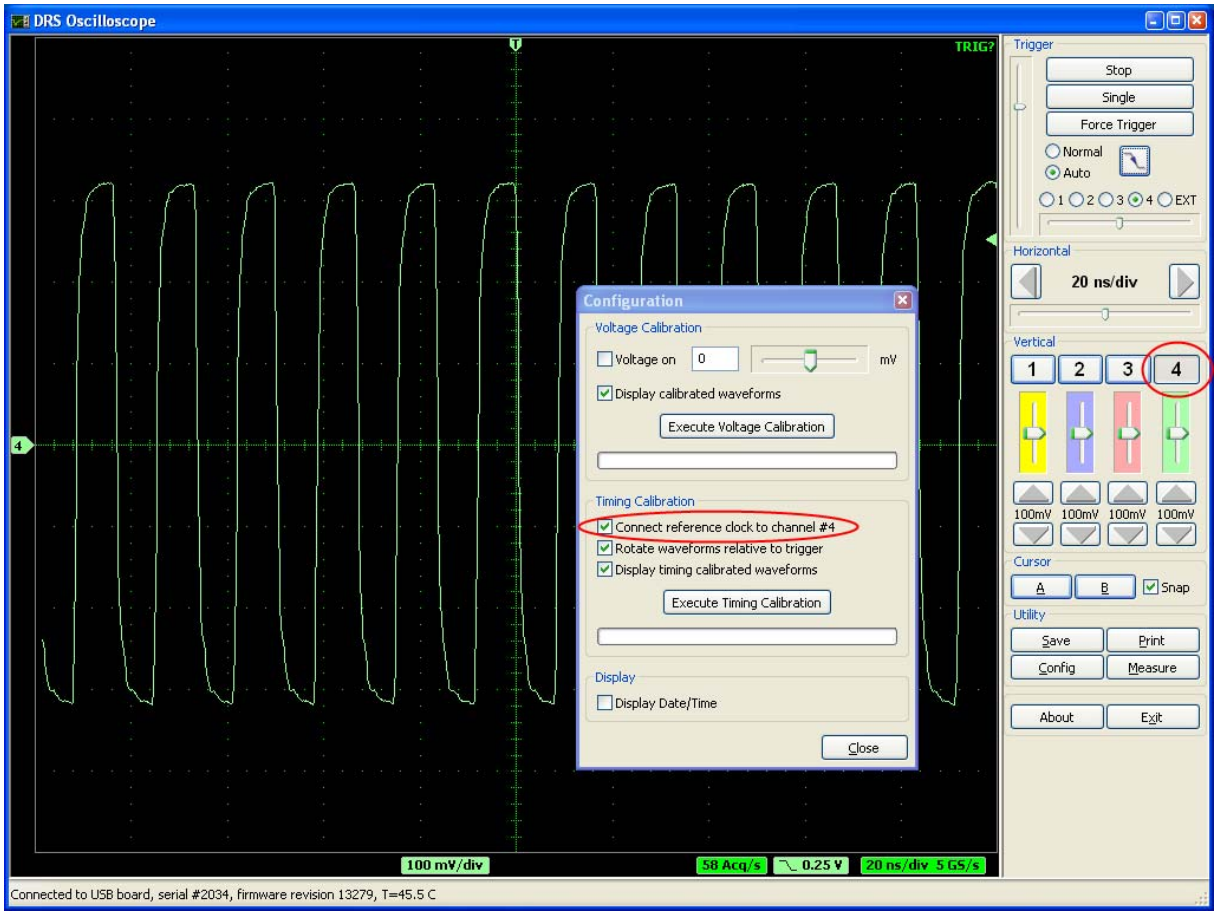
The DRS4 evaluation board is shipped pre-calibrated in amplitude and time. This calibration can be turned on or off using the check boxes "Display calibrated waveforms" and "Display timing calibrated waveforms" in the "Config" Dialog:



The calibration can be re-done any time by clicking on the "Execute Voltage Calibration" and "Execute Timing Calibration" buttons. For the voltage calibration, the inputs are switched to a calibration voltage generated by a DAC. Three calibration points (-0.4V, 0V, +0.4V) are taken and an offset and gain is evaluation. For the timing calibration, a 240 MHz clock is sampled in one channel and the deviation from the expected period to the measured period is used to determine the effective width of each cell.

This calibration data both for voltage and timing is then stored in the EEPROM on the evaluation board, from where it is obtained each time the oscilloscope is started.

For test purposes, an internal 60 MHz reference clock signal can be connected to channel #4 via the "Config" menu. To do so, activate channel #4, then select the "Config" menu and click on "Connect reference clock to channel #4":



The effect of the timing calibration can be tested by turning the timing calibration on and off via the "Display timing calibrated waveforms" check box.

You can save a waveform in an ASCII and a binary format by pressing the "Save" button. After you open a file, each trigger will write the waveform of the active channel(s) to that file. When you are continuously running, the file will grow very quickly. If the file has the extension ".xml" it will be written in ASCII form using XML encoding, otherwise a raw binary file will be written with following contents:

Byte	**Contents**
0 (LSB) 1 (MSB)	First cell first channel 16-bit value (0 = -0.5 V, 65535 = +0.5V)
2 (LSB) 3 (MSB)	Second cell first channel 16-bit value
…	
2048 (LSB)	First cell second channel 16-bit value

4. Development Hints

The idea behind the evaluation board is to make first steps in using the DRS4 chip, but then develop your own custom electronics around the chip. The first thing to do there is to study carefully the DRS4 data sheet, which can be obtained from http://drs.web.psi.ch/datasheets. Then have a look at the DRS4 Evaluation Board Reference Design, which schematics is supplied at the end of this document. When you start to design your own electronics, there are however some important points, which are not necessarily obvious from the data sheet or from the reference design. These points together with some design tips are explained in this section.

4.1. Power Supply

As with any analog design, the quality of the power supply is very important, since it has an influence of the noise level measured by the DRS4 chip. Low noise linear regulators together with the usual decoupling capacitors are recommended for all power supplies. The analog power supply AV_{DD} powers only the domino circuit of the DRS4 chip and directly influences the jitter of the sampling frequency. Long term variations in this power supply (seconds…) are regulated by the on-chip PLL, but high frequency noise in the MHz region leads directly to an increase of the PLL jitter. Therefore the evaluation board contains two separate 2.5V linear regulators for the DRS4 chip, one for the AV_{DD} power and one for the DV_{DD} power. Although the DV_{DD} power is called "digital power", it powers also the analog output buffers of the DRS4 chip and needs the same good quality than the AV_{DD} power in order to minimize the noise of the board.

The DRS4 chip also contains two grounds AGND and DGND. They can be either routed separately on the board and be connected at the power source, or they can be directly connected to an overall dedicated ground plane of the PCB. Tests have been shown that the latter choice gives slightly less noise.

The bottom of the QFN76 package of the DRS4 has an exposed paddle connected to the internal DGND. It is recommended that this paddle is matched by a PCB pad of similar size connected to analog ground to achieve the best electrical and thermal performance of the DRS4. The copper plane should have several vias to achieve a good heat dissipation to flow through the PCB as shown in Figure 2:

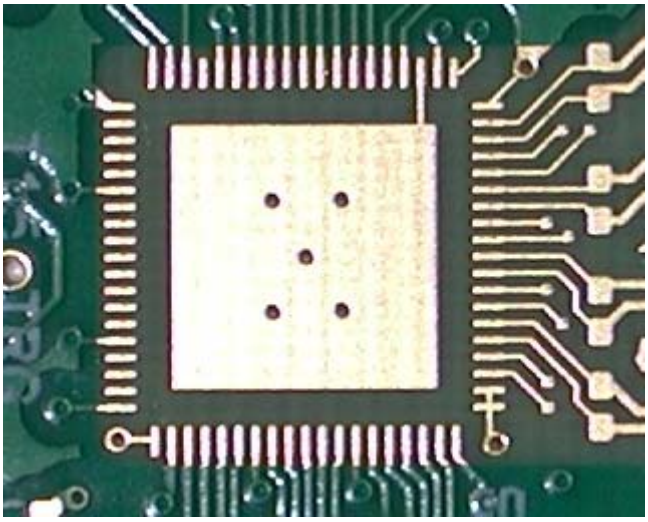


Figure 2: PCB pad under the DRS4 chip

These vias should be solder-filled or plugged. The maximum power dissipation of the DRS4 chip is not critical (350 mW), but an improved thermal stability helps the performance of any analog chip. To maximize the coverage and adhesion between the DRS4 and the PCB, the copper plane could be partitioned into several uniform sections, providing several tie points during the reflow process.

4.2. Analog Input

If non-differential signals should be digitized with the DRS4 chip, they must be converted into differential signals for the DRS4 inputs. The simplest solution is to connect the IN- inputs to AGND and to connect the signals directly to the IN+ inputs. This method has however the disadvantage that the crosstalk and noise immunity of the DRS4 chip are worsened. The evaluation board uses passive transformers ADT1-1WT from Mini-Circuits® for this purpose. While this is a good solution to reduce the power consumption of the board, such that it can be powered from the USB power (500 mA @ 5V), it has the disadvantage that it reduces the analog bandwidth of the system to about 200 MHz (-3 dB). The reason for this is the dynamic capacitive load of the DRS4 inputs, which must be driven by the signal source. Since the input impedance of the DRS4 becomes very small at high frequencies, the signal height drops if only driven passively. Better performance is achieved with active differential drivers. Tests have been made with the THS4513 from Texas Instruments® giving a bandwidth of 450 MHz and the ADA4937 from Analog Devices® giving 700 MHz. A small bypass capacitor (1pF) in the feedback loop of the buffer adds a high frequency pole, which shows up as a peak in the response function, but then pushes the bandwidth to 750 MHz. The peaking can be reduced by adding a series resistor of a few Ohm between the buffer output and the DRS4 input.

The usual design rules like proper termination and matched impedance PCB traces apply as in any high frequency analog design.

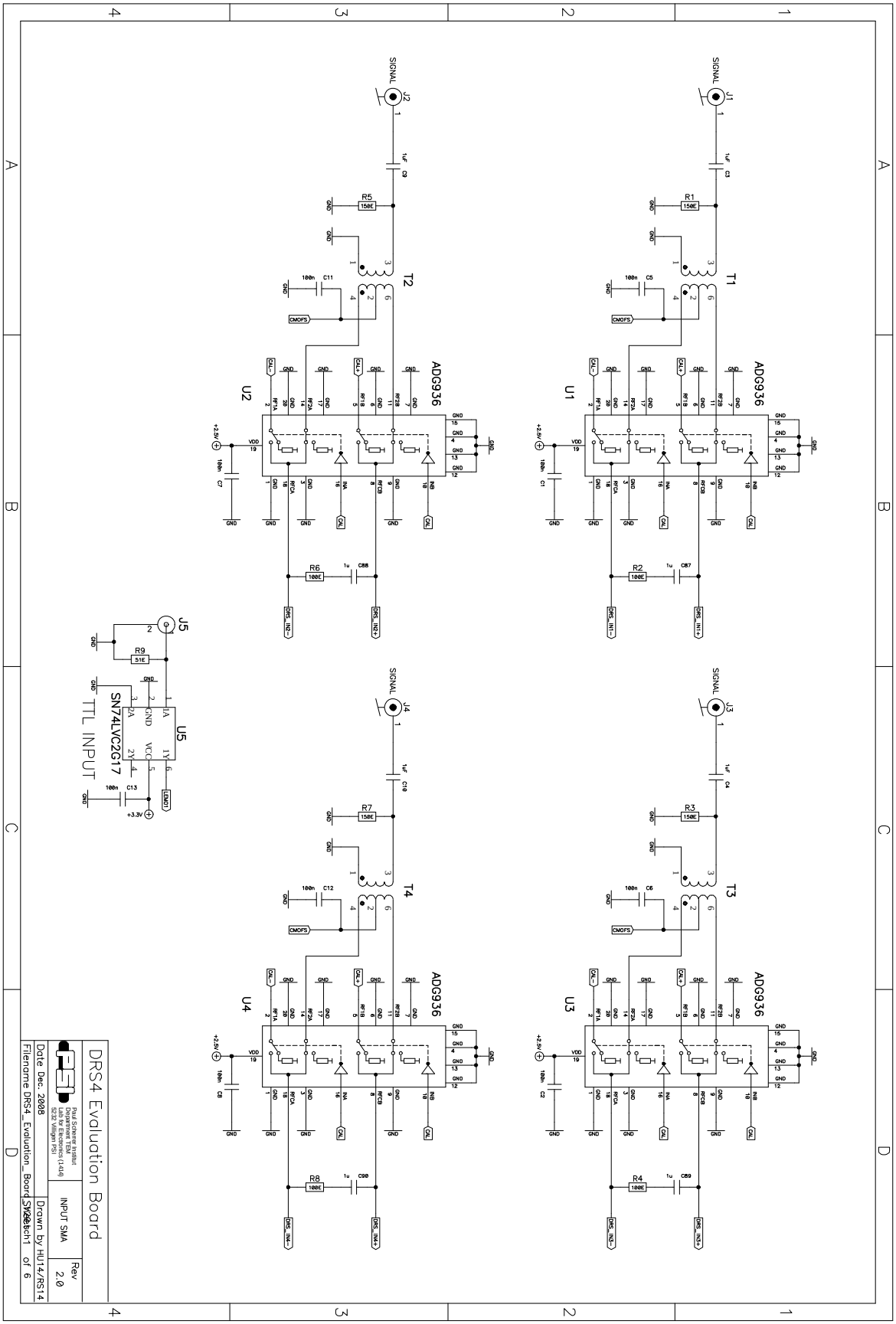
4.3. Control Voltages

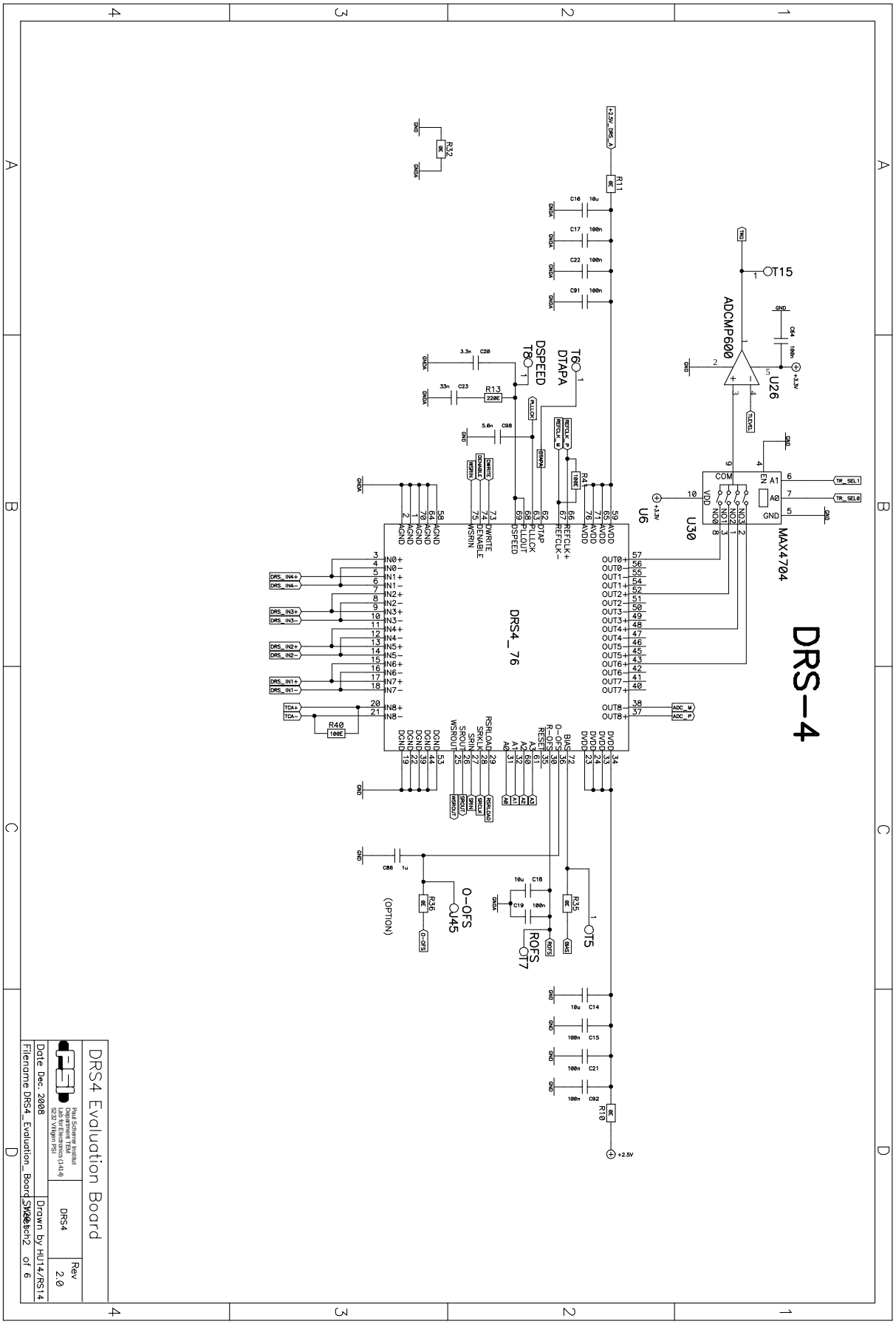
The DRS4 chip requires certain control voltages: ROFS, O-OFS and BIAS. The latter two are generated internally with some default voltage, but can be "overwritten" by an external low impedance source. It is recommended to connect these lines to an external 16-bit DAC, so that the DRS4 input range can be fine-tuned on a board-by-board basis, to compensate for chip variations. The ROFS signal should be driven by a high speed low noise buffer. If this signal would be directly connected to the DAC output, the signal height would change slightly during the chip readout and the measurement would show a varying baseline level.

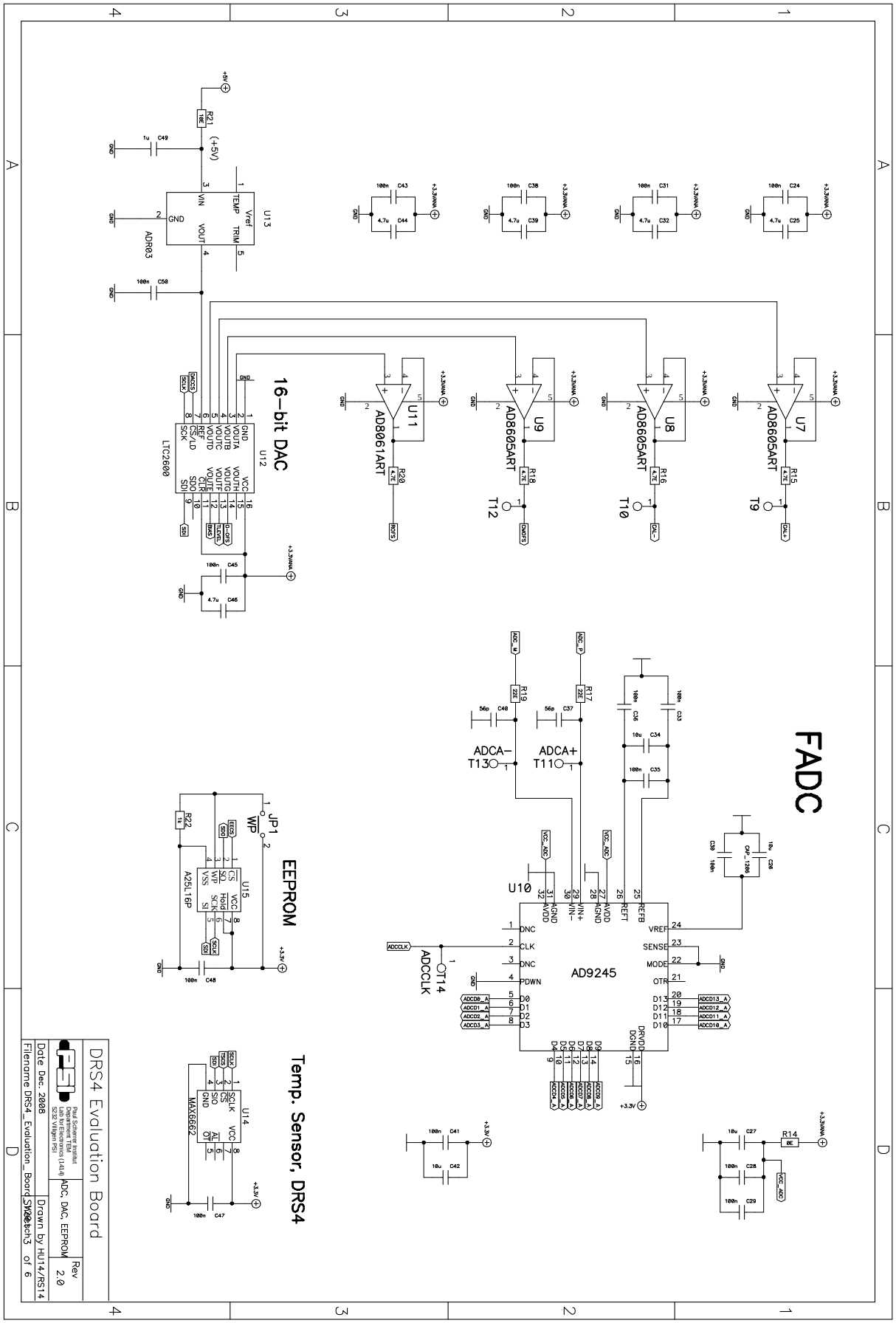
4.4. ADC Clock

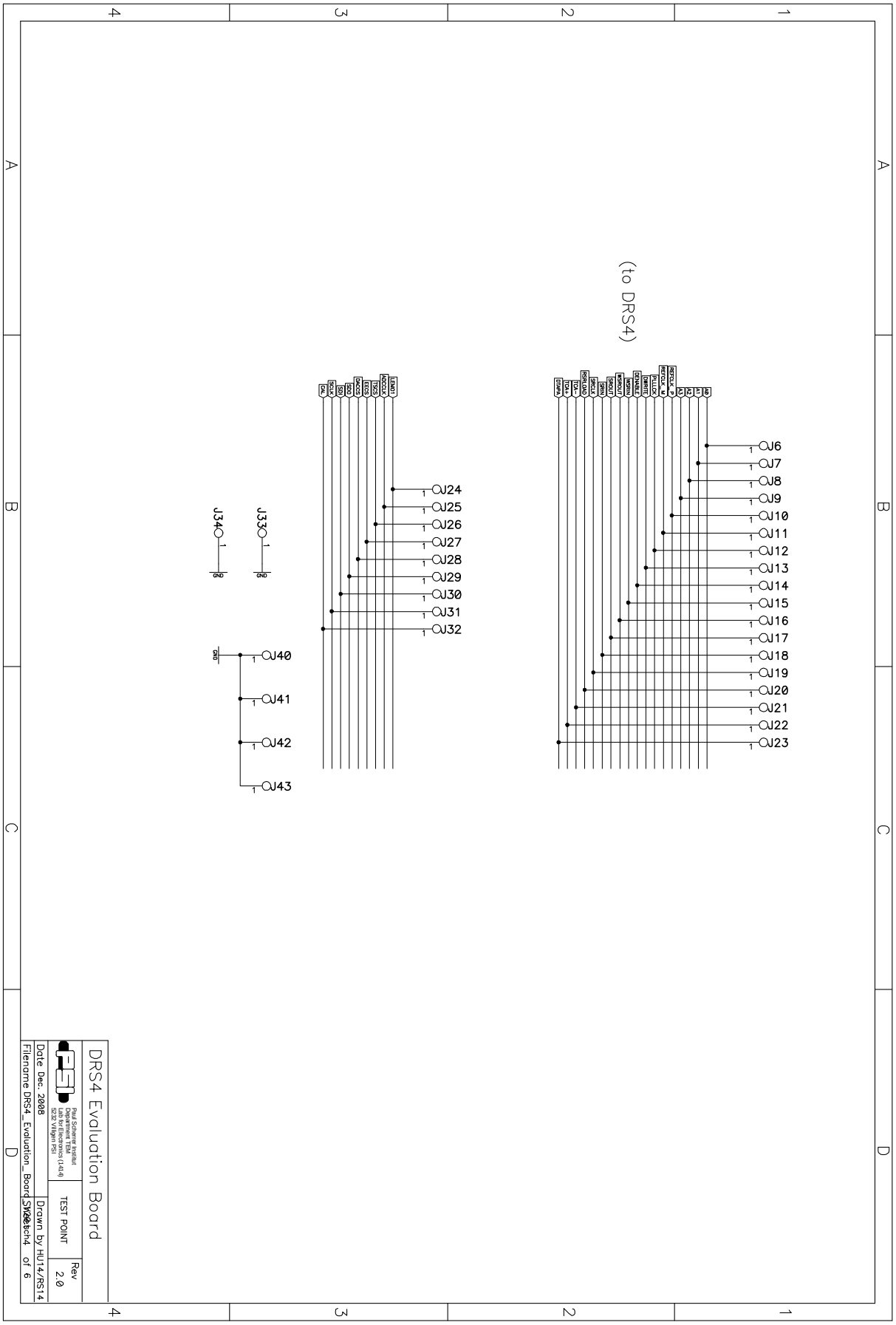
There is a very strict relation between the DRS4 output shift register clock SRCLK and the ADC clock (see DRS4 data sheet WAVEFORM READOUT). In order to reduce the noise due to aperture jitter, the phase shift between these two clocks must be fixed and contain very small jitter (~10ps). The easiest way to generate this phase shift is to use the digital clock managers (DCM) in the FPGA, as it is done on the evaluation board Rev. 1.1. Since the DCMs have however an inherent phase jitter of ~150ps, this introduces some noise in form of a baseline variation when sampling a DC signal in the order of up to a few mV. If this becomes a problem, it is recommended to generate the phase shift between these two clocks with a low jitter delay circuit.

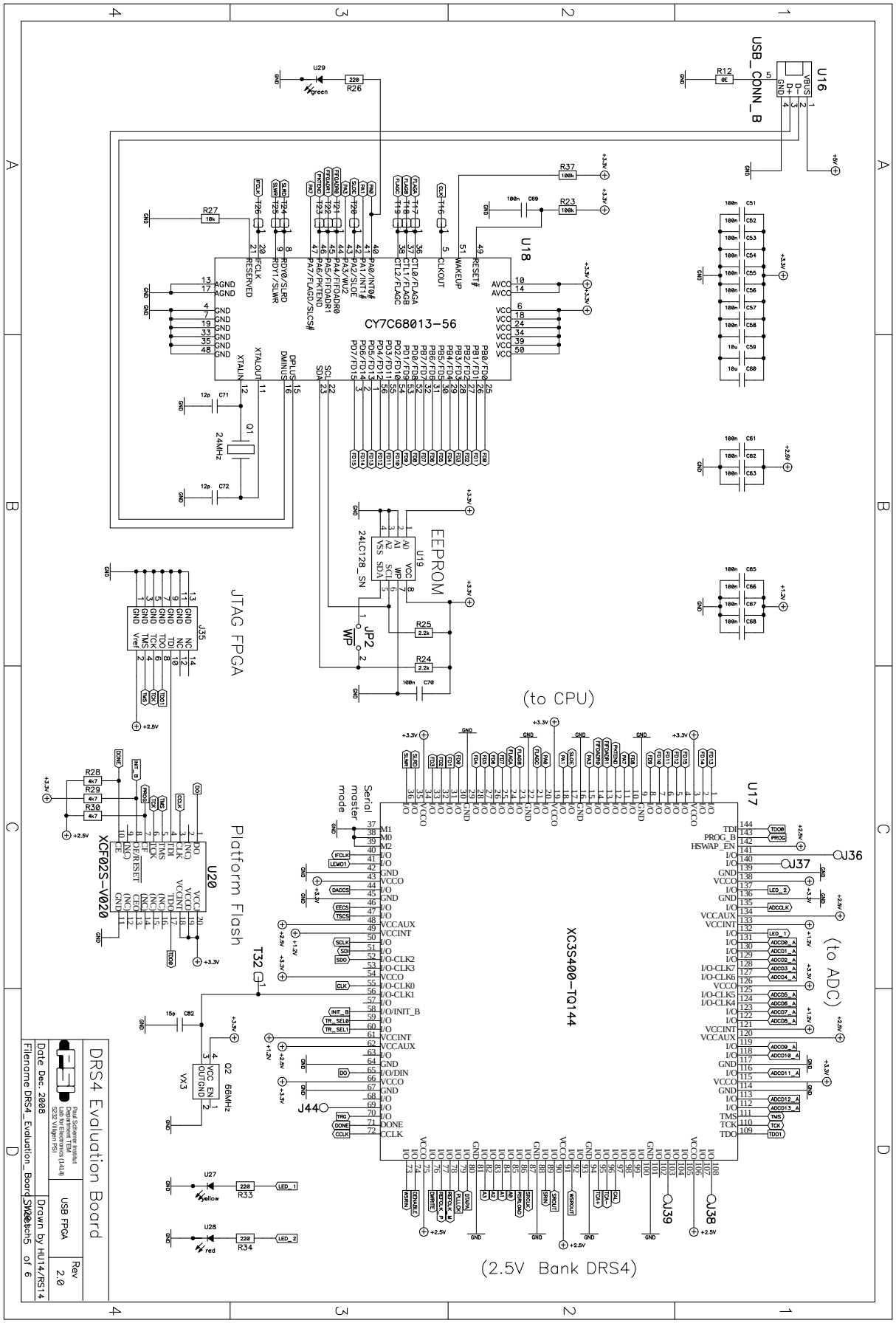
5. DRS4 Evaluation Board Schematics

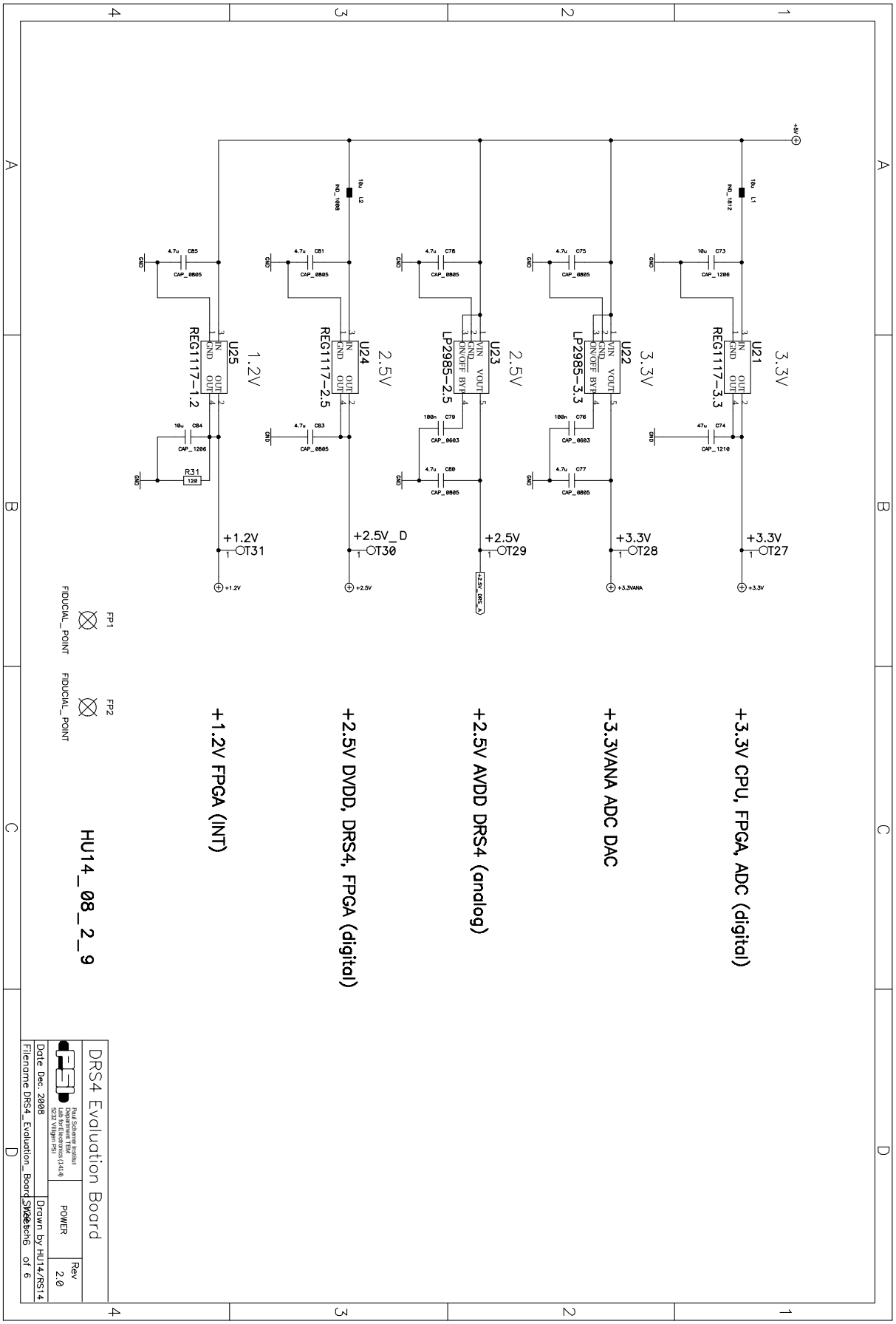



DRS-4
DRS4_76
ADCMP600
U26
MAX4704
U30
U6
T15
T5
T7
T8
T6
DSPEED
DTAPA
O-OFS
U45
ROFS
(OPTION)
DRS4 Evaluation Board
Paul Scherrer Institut
Laboratory for Electronics (LEA)
5232 Villigen PSI
Date Dec. 2008
DRS4
Rev 2.0
Drawn by HU14/RS14
Filename DRS4_Evaluation_Board_Sch2.sch
Sheet 2 of 6


16-bit DAC
EEPROM
Temp. Sensor, DRS4
FADC
ADCA-
ADCA+
AD9245
ADCCLK
DRS4 Evaluation Board
ADC, DAC, EEPROM
Rev 2.0
Drawn by HU14/RS14
Date Dec. 2008
Filename DRS4_Evaluation_Board_Sch.sch
Sheet 3 of 6


(to DRS4)
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
J16
J17
J18
J19
J20
J21
J22
J23
J24
J25
J26
J27
J28
J29
J30
J31
J32
J33
J34
J40
J41
J42
J43
GND
DRS4 Evaluation Board
Paul Scherrer Institut
Labor für Elektronik (LEL)
5232 Villigen PSI
TEST POINT
Rev
2.0
Date Dec. 2008
Drawn by HU14/RS14
Filename DRS4_Evaluation_Board_Sch2.sch
Sheet 4 of 6


USB_CONN_B
U16
CY7C68013-56
U18
EEPROM
24LC128_SN
U19
JTAG FPGA
Platform Flash
XCF02S-V020
U20
XC3S400-TQ144
U17
(to CPU)
(to ADC)
(2.5V Bank DRS4)
DRS4 Evaluation Board
USB FPGA
Rev 2.0
Drawn by HU14/RS14
Date Dec. 2008
Filename DRS4_Evaluation_Board_Sheet5.sch
Sheet 5 of 6


+3.3V CPU, FPGA, ADC (digital)
+3.3VANA ADC DAC
+2.5V AVDD DRS4 (analog)
+2.5V DVDD, DRS4, FPGA (digital)
+1.2V FPGA (INT)
HU14_08_2_9
DRS4 Evaluation Board
Paul Scherrer Institut
Labor für Elektronik (14-4)
5232 Villigen PSI
POWER
Rev 2.0
Date Dec. 2008
Drawn by HU14/RS14
Filename DRS4_Evaluation_Board_Sheet6.sch
Sheet 6 of 6
REG1117-3.3
REG1117-2.5
REG1117-1.2
LP2985-3.3
LP2985-2.5
+3.3V
+2.5V
+2.5V_D
+1.2V

6. DRS4 Evaluation Board Bill of Materials

Count	ComponentName	RefDes	PatternName	Value	Description	Producer
1	24LC128_SN	U19	SO-G8		EEPROM 16kx8	MICROCHIP
1	44.021.0547	J5	CONN_PSI2		Lemo 00 90°	Lemo
1	AT45DB161D	U15	SO-8-SM	16Mbit	Data-Flash	ATMEL
1	AD8061ART	U11	SOT23-5		Amplifier	ANALOG DEVICES
3	AD8605ART	U7	SOT23-5		Amplifier	ANALOG DEVICES
	AD8605ART	U8	SOT23-5		Amplifier	ANALOG DEVICES
	AD8605ART	U9	SOT23-5		Amplifier	ANALOG DEVICES
1	AD9245	U10	LFCSP_VQ_32		ADC	ANALOG DEVICES
1	ADCMP600	U26	SOT23-5		Comparator	ANALOG DEVICES
4	ADG936	U1	PQFP-N20			ANALOG DEVICES
	ADG936	U2	PQFP-N20			ANALOG DEVICES
	ADG936	U3	PQFP-N20			ANALOG DEVICES
	ADG936	U4	PQFP-N20			ANALOG DEVICES
1	ADR03	U13	SC70-5	2.5V		ANALOG DEVICES
4	CAP_0402	C87	0402	1u	Capacitor	
	CAP_0402	C88	0403	1u	Capacitor	
	CAP_0402	C89	0404	1u	Capacitor	
	CAP_0402	C90	0405	1u	Capacitor	
6	CAP_0603	C49	0603	1u	Capacitor	
	CAP_0603	C86	0603	1u	Capacitor	
	CAP_0603	C3	0603	1u	Capacitor	
	CAP_0603	C9	0603	1u	Capacitor	
	CAP_0603	C10	0603	1u	Capacitor	
	CAP_0603	C4	0603	1u	Capacitor	
1	CAP_0603	C20	0603	3.3n	Capacitor	
1	CAP_0603	C98	0603	5.6n	Capacitor	
2	CAP_0603	C71	0603	12p	Capacitor	
	CAP_0603	C72	0603	12p	Capacitor	
1	CAP_0603	C82	0603	15p	Capacitor	
1	CAP_0603	C23	0603	33n	Capacitor	
2	CAP_0603	C37	0603	56p	Capacitor	
	CAP_0603	C40	0603	56p	Capacitor	
50	CAP_0603	C1	0603	100n	Capacitor	
	CAP_0603	C2	0603	100n	Capacitor	
	CAP_0603	C5	0603	100n	Capacitor	
	CAP_0603	C6	0603	100n	Capacitor	
	CAP_0603	C7	0603	100n	Capacitor	
	CAP_0603	C8	0603	100n	Capacitor	
	CAP_0603	C11	0603	100n	Capacitor	
	CAP_0603	C12	0603	100n	Capacitor	
	CAP_0603	C13	0603	100n	Capacitor	
	CAP_0603	C15	0603	100n	Capacitor	
	CAP_0603	C17	0603	100n	Capacitor	
	CAP_0603	C19	0603	100n	Capacitor	
	CAP_0603	C21	0603	100n	Capacitor	
	CAP_0603	C22	0603	100n	Capacitor	
	CAP_0603	C24	0603	100n	Capacitor	
	CAP_0603	C28	0603	100n	Capacitor	
	CAP_0603	C29	0603	100n	Capacitor	
	CAP_0603	C30	0603	100n	Capacitor	
	CAP_0603	C31	0603	100n	Capacitor	

	CAP_0603	C33	0603	100n	Capacitor
	CAP_0603	C35	0603	100n	Capacitor
	CAP_0603	C36	0603	100n	Capacitor
	CAP_0603	C38	0603	100n	Capacitor
	CAP_0603	C41	0603	100n	Capacitor
	CAP_0603	C43	0603	100n	Capacitor
	CAP_0603	C45	0603	100n	Capacitor
	CAP_0603	C47	0603	100n	Capacitor
	CAP_0603	C48	0603	100n	Capacitor
	CAP_0603	C50	0603	100n	Capacitor
	CAP_0603	C51	0603	100n	Capacitor
	CAP_0603	C52	0603	100n	Capacitor
	CAP_0603	C53	0603	100n	Capacitor
	CAP_0603	C54	0603	100n	Capacitor
	CAP_0603	C55	0603	100n	Capacitor
	CAP_0603	C56	0603	100n	Capacitor
	CAP_0603	C57	0603	100n	Capacitor
	CAP_0603	C58	0603	100n	Capacitor
	CAP_0603	C61	0603	100n	Capacitor
	CAP_0603	C62	0603	100n	Capacitor
	CAP_0603	C63	0603	100n	Capacitor
	CAP_0603	C64	0603	100n	Capacitor
	CAP_0603	C65	0603	100n	Capacitor
	CAP_0603	C66	0603	100n	Capacitor
	CAP_0603	C67	0603	100n	Capacitor
	CAP_0603	C68	0603	100n	Capacitor
	CAP_0603	C70	0603	100n	Capacitor
	CAP_0603	C76	0603	100n	Capacitor
	CAP_0603	C79	0603	100n	Capacitor
	CAP_0603	C91	0603	100n	Capacitor
	CAP_0603	C92	0603	100n	Capacitor
12	CAP_0805	C25	0805	4.7u	Capacitor
	CAP_0805	C32	0805	4.7u	Capacitor
	CAP_0805	C39	0805	4.7u	Capacitor
	CAP_0805	C44	0805	4.7u	Capacitor
	CAP_0805	C46	0805	4.7u	Capacitor
	CAP_0805	C75	0805	4.7u	Capacitor
	CAP_0805	C77	0805	4.7u	Capacitor
	CAP_0805	C78	0805	4.7u	Capacitor
	CAP_0805	C80	0805	4.7u	Capacitor
	CAP_0805	C81	0805	4.7u	Capacitor
	CAP_0805	C83	0805	4.7u	Capacitor
	CAP_0805	C85	0805	4.7u	Capacitor
11	CAP_1206	C14	1206	10u	Capacitor
	CAP_1206	C16	1206	10u	Capacitor
	CAP_1206	C18	1206	10u	Capacitor
	CAP_1206	C26	1206	10u	Capacitor
	CAP_1206	C27	1206	10u	Capacitor
	CAP_1206	C34	1206	10u	Capacitor
	CAP_1206	C42	1206	10u	Capacitor
	CAP_1206	C59	1206	10u	Capacitor
	CAP_1206	C60	1206	10u	Capacitor
	CAP_1206	C73	1206	10u	Capacitor
	CAP_1206	C84	1206	10u	Capacitor
1	CAP_1206	C69	1206	100n	Capacitor

1	CAP_1210	C74	1210	47u	Capacitor	
1	CONN_MOLEX	J35	DIL14P_2MM		JTAG	MOLEX
1	CY7C68013-56	U18	SSO-G56		UP	CYPRESS
1	DRS4_76	U6	QFN-76		DRS4	PSI
1	IND_1008	L2	1008	10u	Inductor	EPCOS
1	IND_1812	L1	1812	10u	Inductor	EPCOS
2	JMP2MM	JP1	TP50MIL	~WP	Jumper	
	JMP2MM	JP2	TP50MIL	~WP	Jumper	
1	LED_PLCC-4	U29	PLCC-4	green		AVAGO
1	LED_PLCC-4	U28	PLCC-4	red		AVAGO
1	LED_PLCC-4	U27	PLCC-4	yellow		AVAGO
1	LP2985-2.5	U23	SOT23-5		150mA Low Dropout	National
1	LP2985-3.3	U22	SOT23-5		150mA Low Dropout	National
1	LTC2600	U12	SSOP16		DAC	LINEAR
1	MAX4704	U30	MSOP-10		MUX	MAXIM
1	MAX6662	U14	SO-G8			MAXIM
1	QUARZ_NKS7	Q1	QUARZ_NKS7	24MHz	JXS75-12-30/30	
1	REG1117-1.2	U25	SOT223		800mA Low Dropout	
1	REG1117-2.5	U24	SOT223		800mA Low Dropout	
1	REG1117-3.3	U21	SOT223		800mA Low Dropout	
4	RES_0402	R2	0402	100E	Resistor	
	RES_0402	R4	0402	100E	Resistor	
	RES_0402	R6	0402	100E	Resistor	
	RES_0402	R8	0402	100E	Resistor	
1	RES_0603	R35	0603	0E	Resistor	
1	RES_0603	R22	0603	1k	Resistor	
2	RES_0603	R24	0603	2.2k	Resistor	
	RES_0603	R25	0603	2.2k	Resistor	
3	RES_0603	R28	0603	4k7	Resistor	
	RES_0603	R29	0603	4k7	Resistor	
	RES_0603	R30	0603	4k7	Resistor	
4	RES_0603	R15	0603	4.7E	Resistor	
	RES_0603	R16	0603	4.7E	Resistor	
	RES_0603	R18	0603	4.7E	Resistor	
	RES_0603	R20	0603	4.7E	Resistor	
1	RES_0603	R21	0603	10E	Resistor	
1	RES_0603	R27	0603	10k	Resistor	
2	RES_0603	R17	0603	22E	Resistor	
	RES_0603	R19	0603	22E	Resistor	
2	RES_0603	R40	0603	100E	Resistor	
	RES_0603	R41	0603	100E	Resistor	
2	RES_0603	R23	0603	100k	Resistor	
	RES_0603	R37	0603	100k	Resistor	
4	RES_0603	R1	0603	150E	Resistor	
	RES_0603	R3	0603	150E	Resistor	
	RES_0603	R5	0603	150E	Resistor	
	RES_0603	R7	0603	150E	Resistor	
4	RES_0603	R26	0603	220E	Resistor	
	RES_0603	R33	0603	220E	Resistor	
	RES_0603	R34	0603	220E	Resistor	
	RES_0603	R13	0603	220E	Resistor	
2	RES_0805	R10	0805	0E	Resistor	

	RES_0805	R11	0805	0E	Resistor	
4	RES_0805	R12	0805	0E	Resistor	
	RES_0805	R14	0805	0E	Resistor	
	RES_0805	R32	0805	0E	Resistor	
	RES_0805	R36	0805	0E	Resistor	
1	RES_1206	R9	1206	51E	Resistor	
1	RES_1206	R31	1206	120E	Resistor	
4	RF-TRAFO	T1	RF-TRAFO	75Ohm		Mini-Circuits
	RF-TRAFO	T2	RF-TRAFO	75Ohm		Mini-Circuits
	RF-TRAFO	T3	RF-TRAFO	75Ohm		Mini-Circuits
	RF-TRAFO	T4	RF-TRAFO	75Ohm		Mini-Circuits
4	SMA_SMD	J1	SMA_SMD		SMA Connector	Johnson
	SMA_SMD_S	J2	SMA_SMD		SMA Connector	Johnson
	SMA_SMD_S	J3	SMA_SMD		SMA Connector	Johnson
	SMA_SMD_S	J4	SMA_SMD		SMA Connector	Johnson
1	SN74LVC2G17	U5	SC-70		Dual schmitt-trigger	TI
1	USB_CONN_B	U16	USB_CONN_B			Lumberg
1	Oszillator VX3	Q2	VX3	66MHz	Oszillator VX3	
1	XC3S400-TQ144	U17	TQFP144		FPGA	XILINX
1	XCF02S-V020	U20	TSSOP20		EEPROM	XILINX