NEC

MOS INTEGRATED CIRCUIT
μPD78P083

8-BIT SINGLE-CHIP MICROCOMPUTER

The μPD78P083 is a member of the μPD78083 subseries, which is part of the 78K/0 Series. It includes an on-chip 24-Kbyte one-time programmable (OTP)ROM or EPROM.

Because this device can be programmed by users, it is ideally suitable for application system evaluation in development stages, small-scale production of many different devices, and quick product release to a hot market.

For specific functions and other detailed information, consult the following user's manuals. These manuals are required reading for design work.

μPD78083 Subseries User's Manual : IEU-1407

78K/0 Series Users Manual — Instruction — : IEU-1372

Features

- Pin-compatible with mask ROM versions (except for V_{PP} pin)
- Internal PROM: 24 Kbytes **Note**
  - μPD78P083DU : reprogrammable (suitable for system evaluation)
  - μPD78P083CU and μPD78P083GB : one-time programmable (suitable for small-scale production)
- Internal high-speed RAM: 512 bytes **Note**
- Operates over the same power supply voltage range as for mask ROM versions: 2.0 to 5.5 V

Note Internal PROM and internal high-speed RAM capacities can be changed with the internal memory switching register.

This product differs from mask ROM versions in the following respects.

Memory mapping is different. To get the same memory mapping as mask ROM versions, the internal memory switching register should be set.

Ordering Information

Part No.	Package	Internal ROM
μPD78P083CU	42-pin plastic shrink DIP (600 mil)	One-Time PROM
μPDD78P083GB-3B4	44-pin plastic QFP (10 × 10 mm)	One-Time PROM
μPD78P083DU	42-pin ceramic shrink DIP (with window)(600 mil)	EPROM

In this document, all ROM descriptions common to one-time PROM and EPROM are referred to as PROM.

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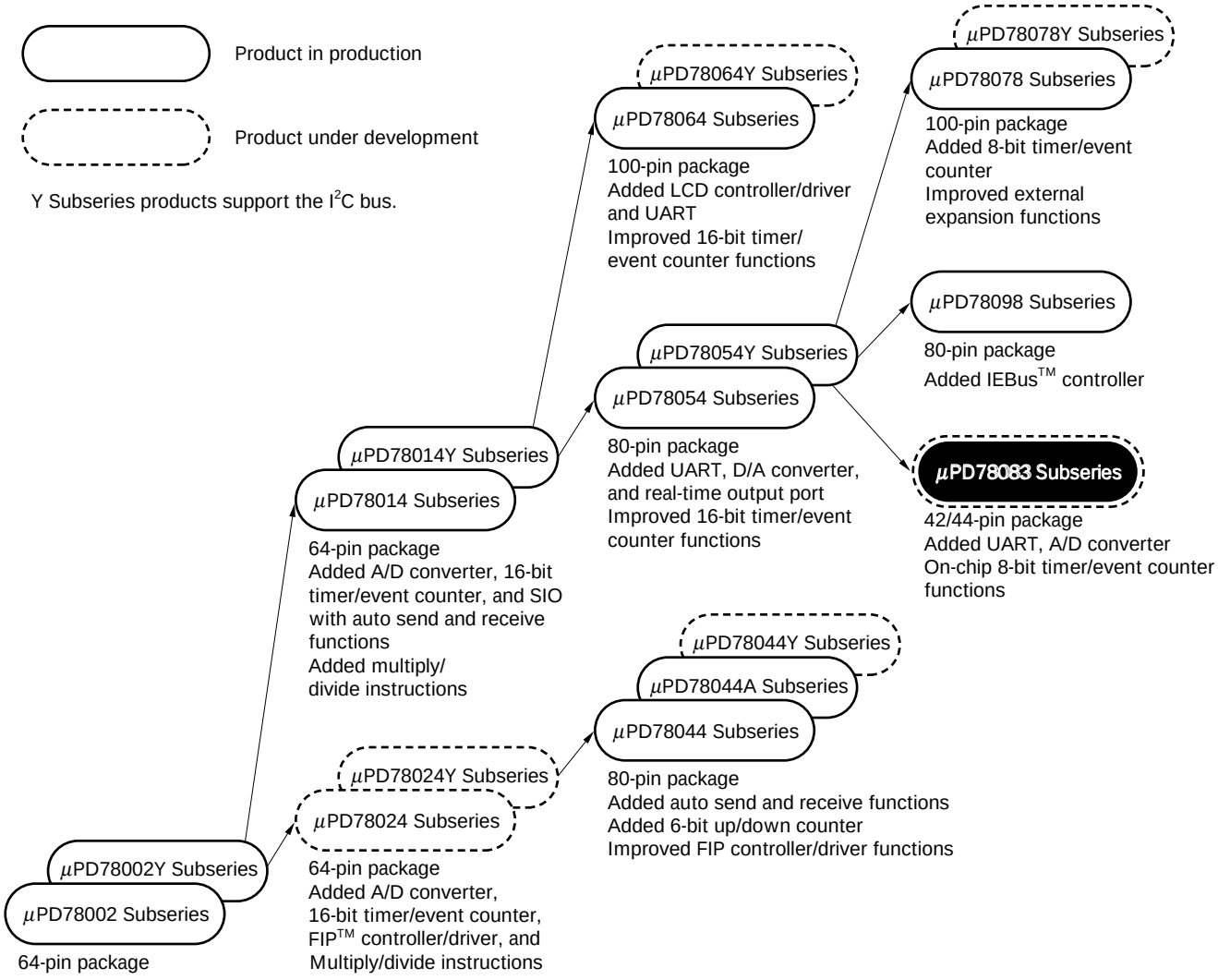
Development of 78K/0 Series



Overview of Functions

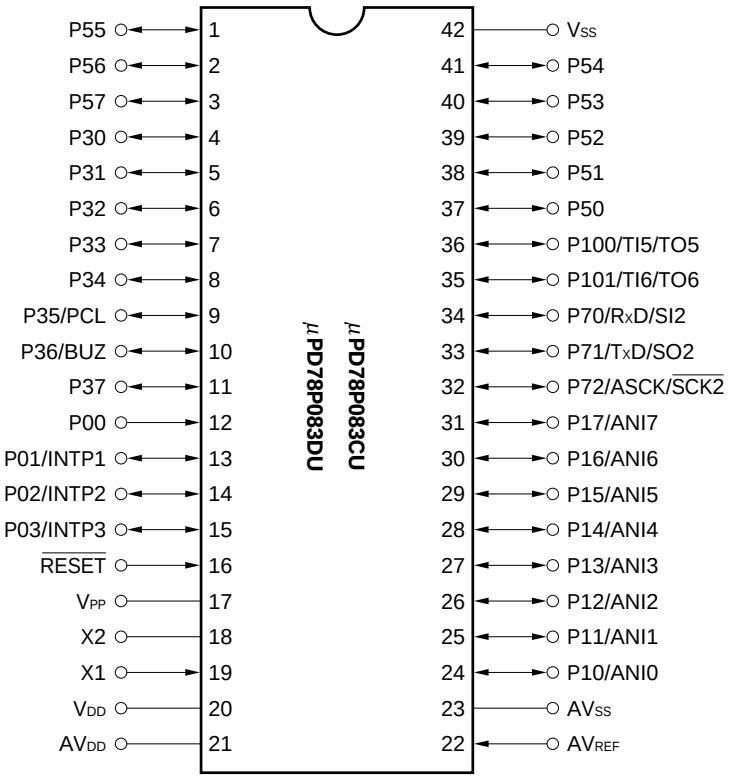
Item		Function
Internal memory		• PROM: 24 K bytes **Note** • RAM Internal high-speed RAM: 512 bytes **Note**
Memory space		64 K bytes
General register		Thirty-two 8-bit registers (8 bits × 8 registers × 4 banks)
Instruction cycle		Variable instruction execution time: 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (during 5.0 MHz operation of main system clock)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operations) • BCD adjust, etc.
I/O ports		Total : 33 lines • CMOS input : 1 line • CMOS I/O : 32 lines
A/D converter		Eight channel 8-bit A/D converter
Serial interface		3-wire/UART mode selectable: one channel
Timers		• 8-bit timer/event counters: two channels • Watchdog timer : one channel
Timer outputs		Two lines (Two 8-bit PWM output lines)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0 MHz with main system clock)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, and 9.8 kHz (@ 5.0 MHz with main system clock)
Vectored interrupts	Maskable interrupt	Internal: 8 causes, external: 3 causes
	Non-maskable interrupt	Internal: 1 cause
	Software interrupt	Internal: 1 cause
Operating power supply voltage range		V_{DD} = 2.0 to 5.5 V
Packages		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm) • 42-pin ceramic shrink DIP (with window)(600 mil)

Note Internal PROM and internal high-speed RAM capacity can be changed with the internal memory switching register.

Pin Configuration (Top View)

(1) Normal operating mode

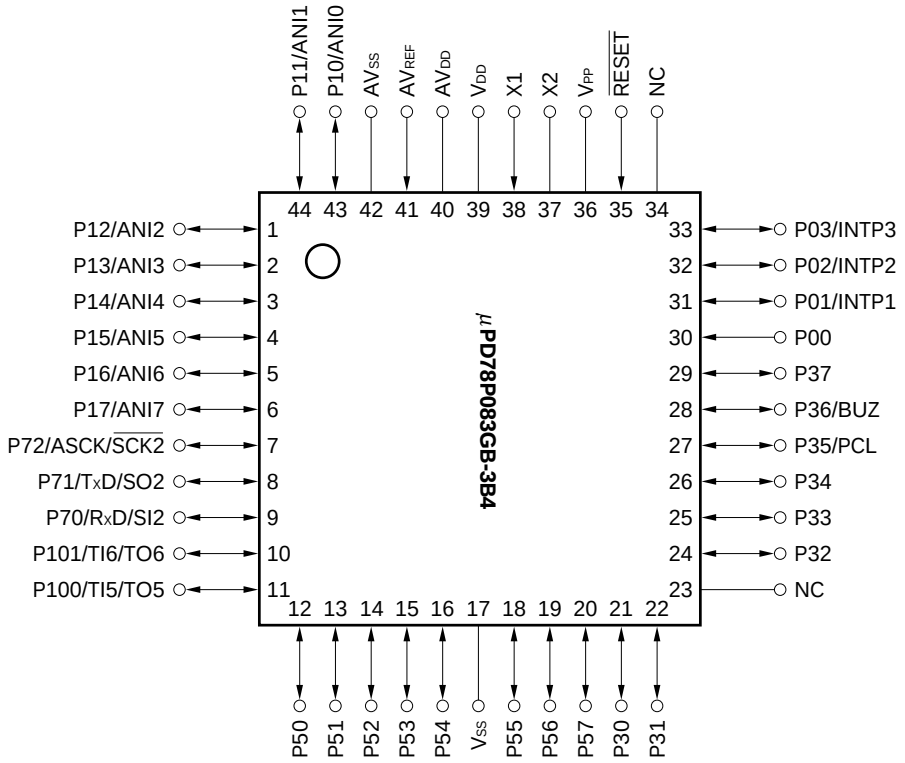
42-pin plastic shrink DIP (600 mil)
42-pin ceramic shrink DIP (with window)(600 mil)



Cautions 1. Connect the V_{PP} pin to V_{SS} directly.
2. Connect the AV_{DD} pin to V_{DD}.
3. Connect the AV_{SS} pin to V_{SS}.

P00 - P03	:	Port 0
P10 - P17	:	Port 1
P30 - P37	:	Port 3
P50 - P57	:	Port 5
P70 - P72	:	Port 7
P100, P101	:	Port 10
INTP1 - INTP3	:	Interrupt from Peripherals
TI5, TI6	:	Timer Input
TO5, TO6	:	Timer Output
SI2	:	Serial Input
SO2	:	Serial Output
SCK2	:	Serial Clock
RxD	:	Receive Data
TxD	:	Transmit Data
ASCK	:	Asynchronous Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
X1, X2	:	Crystal (Main System Clock)
RESET	:	Reset
ANI0 - ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
NC	:	Non-connection

44-pin plastic QFP (10 × 10 mm)



Cautions 1. Connect the V_{PP} pin to V_{SS} directly.

2. Connect the AV_{DD} pin to V_{DD}.

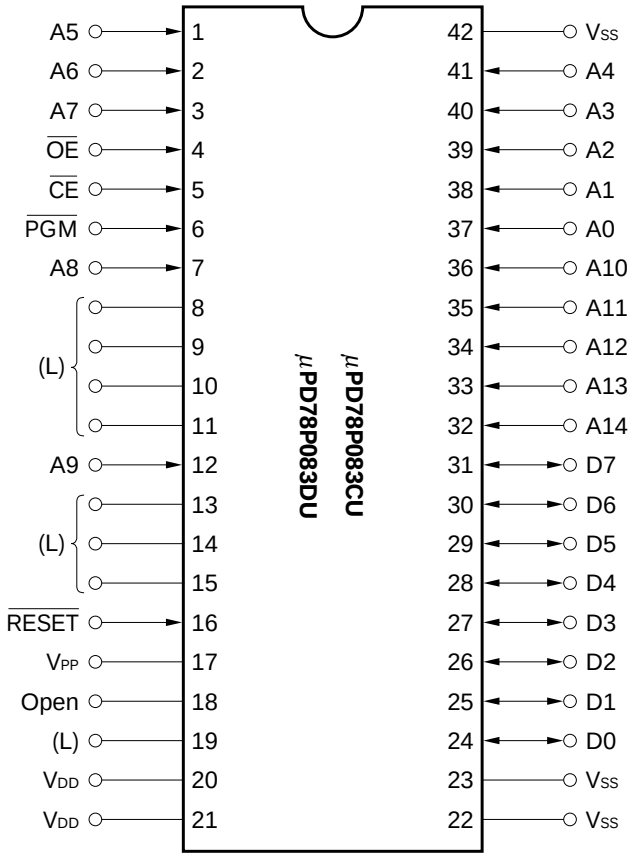
3. Connect the AV_{SS} pin to V_{SS}.

4. Connect the NC pin to V_{SS} as an anti-noise measure (however, it can also be left open).

P00 - P03	:	Port 0
P10 - P17	:	Port 1
P30 - P37	:	Port 3
P50 - P57	:	Port 5
P70 - P72	:	Port 7
P100, P101	:	Port 10
INTP1 - INTP3	:	Interrupt from Peripherals
TI5, TI6	:	Timer Input
TO5, TO6	:	Timer Output
SI2	:	Serial Input
SO2	:	Serial Output
$\overline{SCK2}$	:	Serial Clock
RxD	:	Receive Data
TxD	:	Transmit Data
ASCK	:	Asynchronous Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
X1, X2	:	Crystal (Main System Clock)
$\overline{RESET}$	:	Reset
ANI0 - ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
NC	:	Non-connection

(2) PROM programming mode

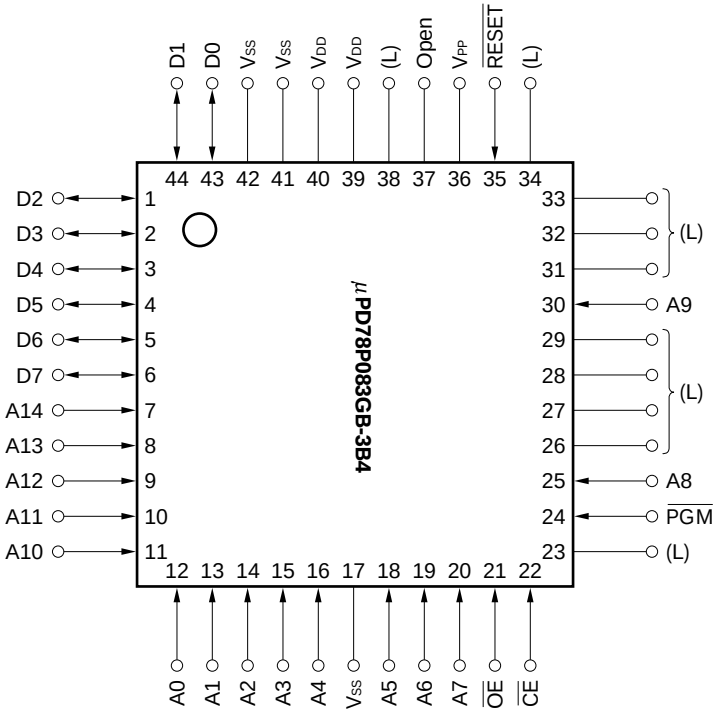
42-pin plastic shrink DIP (600 mil)
42-pin ceramic shrink DIP (with window)(600 mil)



Cautions 1. (L) : Connect to VSS via individual pull-down resistors.
2. VSS : Connect to ground.
3. $\overline{\text{RESET}}$: Set to low level.
4. Open : Do not connect.

A0 - A14 : Address Bus
D0 - D7 : Data Bus
$\overline{\text{CE}}$: Chip Enable
$\overline{\text{OE}}$: Output Enable
$\overline{\text{PGM}}$: Program
$\overline{\text{RESET}}$: Reset
VDD : Power Supply
VPP : Programming Power Supply
VSS : Ground

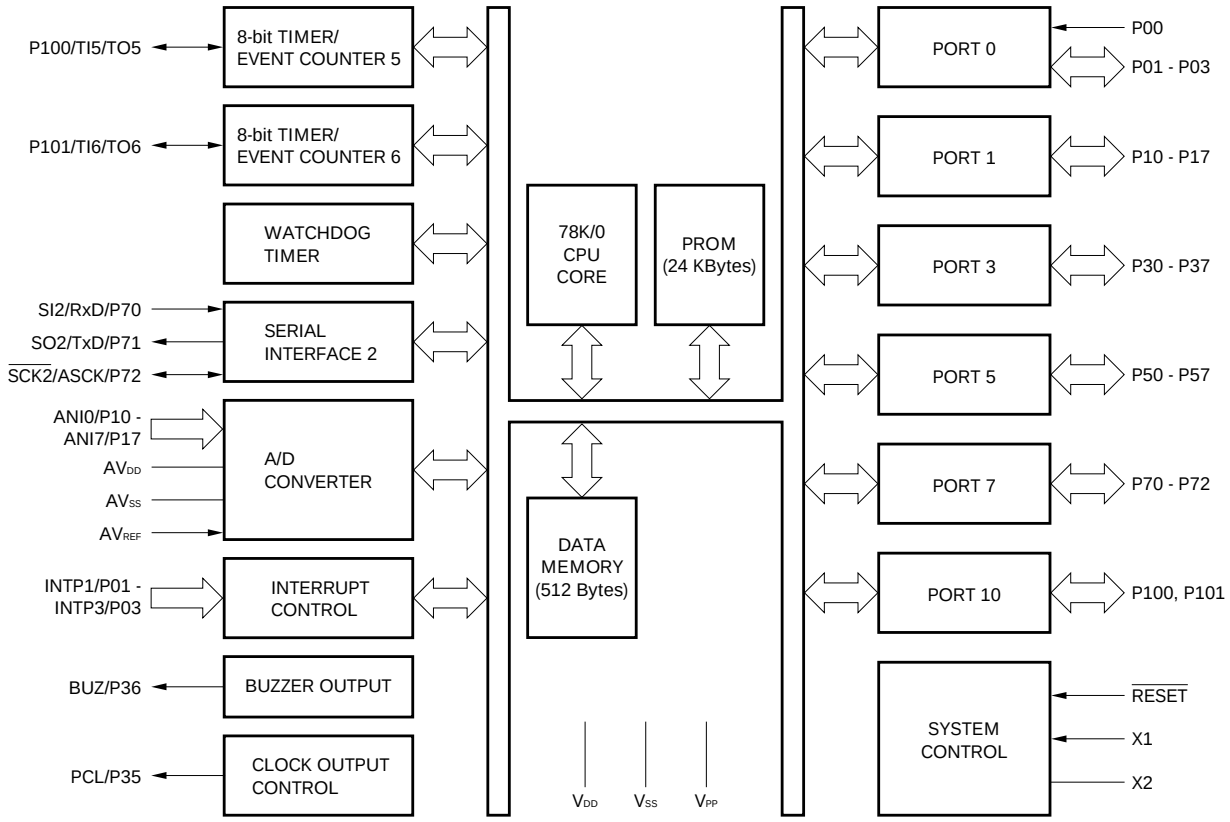
44-pin plastic QFP (10 × 10 mm)



Cautions 1. (L) : Connect to VSS via individual pull-down resistors.
2. VSS : Connect to ground.
3. RESET : Set to low level.
4. Open : Do not connect.

A0 - A14 : Address Bus
D0 - D7 : Data Bus
CE : Chip Enable
OE : Output Enable
PGM : Program
RESET : Reset
VDD : Power Supply
VPP : Programming Power Supply
VSS : Ground

Block Diagram



CONTENTS

1. DIFFERENCES BETWEEN μPD78P083 AND MASK ROM VERSIONS

The μPD78P083 has an on-chip 24-Kbyte one-time PROM or EPROM.

The internal memory switching register settings enable functions other than PROM specifications to be set as equivalent to those of mask ROM versions.

Table 1-1 lists the points of difference between the μPD78P083 and mask ROM versions.

Table 1-1. Differences between μPD78P083 and Mask ROM Versions

Item	μPD78P083	Mask ROM Versions
IC pin	No	Yes
V_{PP} pin	Yes	No

Cautions 1. In the μPD78P083, internal PROM and internal high-speed RAM capacity can be changed by using the internal memory switching register.

2. $\overline{\text{RESET}}$ input sets internal PROM to 24 Kbytes and internal high-speed RAM to 512 bytes.

2. LIST OF PIN FUNCTIONS

2.1 Pins for Normal Operating Mode

(1) Port pins

Pin name	I/O	Function		After reset	Alternate function
P00	Input	Port 0. 4-bit I/O port.	Input only	Input	—
P01	I/O		Can be specified for I/O in 1-bit units. If used as an input port, software pull-up resistor can be connected.	Input	INTP1
P02					INTP2
P03					INTP3
P10 - P17	I/O	Port 1. 8-bit I/O port. Can be specified for I/O in 1-bit units. If used as an input port, software pull-up resistor can be connected.**Note**		Input	ANI0 - ANI7
P30 - P34	I/O	Port 3. 8-bit I/O port. Can be specified for I/O in 1-bit units. If used as an input port, software pull-up resistor can be connected.		Input	—
P35					PCL
P36					BUZ
P37					—
P50 - P57	I/O	Port 5. 8-bit I/O port. Can directly drive up to 7 LEDs. Can be specified for I/O in 1-bit units. If used as an input port, software pull-up resistor can be connected.		Input	—
P70	I/O	Port 7. 3-bit I/O port. Can be specified for I/O in 1-bit units. If used as an input port, software pull-up resistor can be connected.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{\text{SCK2}}$/ASCK
P100	I/O	Port 10. 2-bit I/O port. Can be specified for I/O in 1-bit units. If used as an input port, software pull-up resistor can be connected.		Input	TI5/TO5
P101					TI6/TO6

Note When using P10/ANI0-P17/ANI7 pins as an analog input for an A/D converter, set port 1 to input mode. The pull-up resistors will automatically be disconnected.

(2) Non-port pins

Pin name	I/O	Function	After reset	Alternate function
INTP1	Input	Can be set for effective edge (rising edge, falling edge, or both rising and falling edges). Inputs specifiable external interrupts.	Input	P01
INTP2				P02
INTP3				P03
SI2	Input	Input of serial data for serial interface.	Input	P70/RxD
SO2	Output	Output of serial data for serial interface.	Input	P71/TxD
$\overline{SCK2}$	I/O	Serial clock input/output for serial interface.	Input	P72/ASCK
RxD	Input	Input of serial data for asynchronous serial interface.	Input	P70/SI2
TxD	Output	Output of serial data for asynchronous serial interface.	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface.	Input	P72/$\overline{SCK2}$
TI5	Input	External count clock input to 8-bit timer (TM5).	Input	P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO5	Output	8-bit timer output.	Input	P100/TI5
TO6				P101/TI6
PCL	Output	Clock output (for trimming main system clock or sub system clock)	Input	P35
BUZ	Output	Buzzer output.	Input	P36
ANI0 - ANI7	Input	Analog input for A/D converter	Input	P10 - P17
AV_{REF}	Input	Reference voltage input for A/D converter	—	—
AV_{DD}	—	Analog power supply for A/D converter. Connect to V_{DD}.	—	—
AV_{SS}	—	Ground for A/D converter. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Crystal connection for main system clock oscillation.	—	—
X2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{PP}	—	High-voltage power supply during program write/verify. Connect directly to V_{SS} during normal operation mode.	—	—
V_{SS}	—	Ground.	—	—
NC	—	No internal connection. Connect to V_{SS} (may also be left open).	—	—

2.2 Pins for PROM Programming Mode

Pin name	I/O	Function
$\overline{\text{RESET}}$	Input	PROM programming mode selection. PROM programming mode is selected when +5 V or +12.5 V is applied to the V_{PP} pin or low-level input is applied to the $\overline{\text{RESET}}$ pin.
V_{PP}	Input	PROM programming mode selection and high-voltage input during program write or verification.
A0 - A14	Input	Address bus.
D0 - D7	I/O	Data bus.
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input.
$\overline{\text{OE}}$	Input	Read strobe input to PROM.
$\overline{\text{PGM}}$	Input	Program/program inhibit input during PROM programming mode.
V_{DD}	—	Positive power supply.
V_{SS}	—	Ground.

2.3 Pin I/O Circuits and Unused Pin Connections

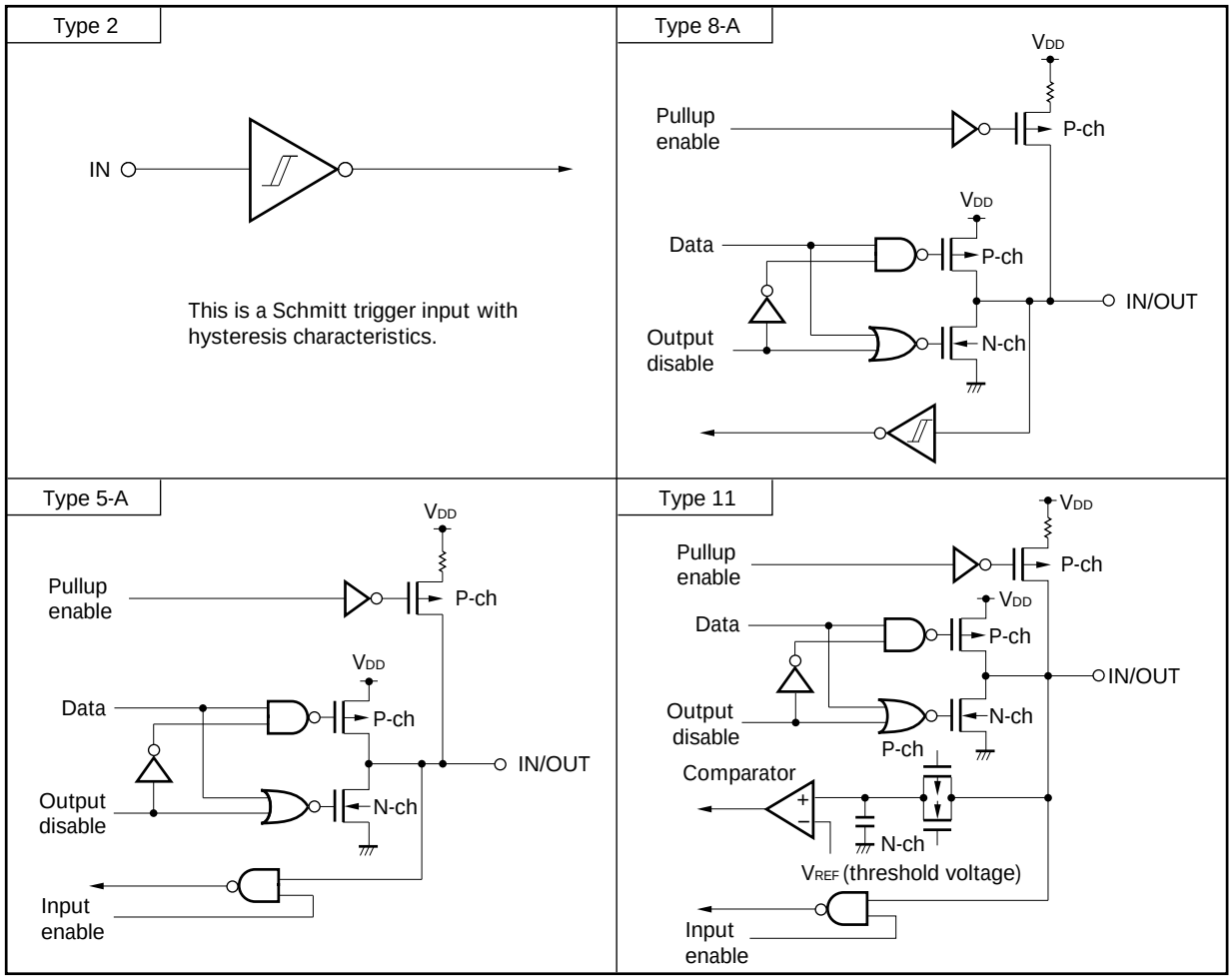
Table 2-1 lists the I/O circuit types for all pins and recommended connections for all unused pins.

Figure 2-1 shows the pin I/O circuits.

Table 2-1. Types of Pin I/O Circuits

Pin name	I/O circuit type	I/O	Recommended connection for unused pins
P00	2	Input	Connect to V_{SS}.
P01/INTP1	8-A	I/O	For input : Connect to V_{SS}.
P02/INTP2			For output: Open
P03/INTP3			
P10/ANI0 - P17/ANI7	11	I/O	For input : Connect to V_{DD} or V_{SS}.
P30 - P32	5-A	I/O	For output: Open
P33, P34	8-A		
P35/PCL	5-A		
P36/BUZ			
P37			
P50 - P57	5-A	I/O	
P70/SI2/RxD	8-A	I/O	
P71/SO2/TxD	5-A		
P72/$\overline{\text{SCK2}}$/ASCK	8-A		
P100/TI5/TO5	8-A	I/O	
P101/TI6/TO6			
$\overline{\text{RESET}}$	2	Input	—
AV_{REF}	—	—	Connect to V_{SS}.
AV_{DD}			Connect to V_{DD}.
AV_{SS}			Connect to V_{SS}.
V_{PP}			Connect to V_{SS}.
NC			Connect to V_{SS}. (can also be left open)

Figure 2-1. Pin I/O Circuits



3. INTERNAL MEMORY SWITCHING (IMS) REGISTER

This register enables the software to avoid using part of the internal memory. The IMS register can be set to establish the same memory mapping as used in ROM versions that have different internal memory (ROM and RAM) configurations.

The IMS register is set using 8-bit memory operation instructions.

$\overline{\text{RESET}}$ input sets a value of 46H.

Figure 3-1. Format of IMS Register

Symbol	7	6	5	4	3	2	1	0	Address	Reset value	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	46H	W

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	0	1	0	8 Kbytes
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Internal high-speed RAM selection
0	1	0	512 bytes
0	1	1	384 bytes
1	0	0	256 bytes
Other than above			Setting prohibited

Table 3-1 lists IMS register settings for memory mapping equivalent to mask ROM versions.

Table 3-1. IMS Register Settings

Target mask ROM version	IMS setting
μPD78081	82H
μPD78082	64H

4. PROM PROGRAMMING

The μPD78P083 has an on-chip 24-Kbyte PROM device for use as program memory. When programming, set the V_{PP} and $\overline{RESET}$ pins for PROM programming mode. See the pin configuration (Top View) under section "(2) PROM programming mode" with regard to recommended connections for unused pins.

Caution Program write operations should take place in the address range 0000H to 5FFFH (i.e., specify 5FFFH as the end address). Write is not possible when using PROM programmers that do not enable write addresses to be set.

4.1 Operation Mode

PROM programming mode is selected when +5 V or +12.5 V is applied to the V_{PP} pin or low-level input is applied to the $\overline{RESET}$ pin. This mode can be set to operation mode by setting the $\overline{CE}$ pin, $\overline{OE}$ pin, and $\overline{PGM}$ pin as shown in Table 4-1 below.

In addition, the PROM contents can be read by setting read mode.

Table 4-1. PROM Programming Operation Mode

Pin / Operation mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0-D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

Remark × = L or H

(1) Read mode

Set $\overline{CE}$ to L and $\overline{OE}$ to L to set read mode.

(2) Output disable mode

Set $\overline{OE}$ to H to set high impedance for data output and output disable mode.

Consequently, if several μPD78P083 devices are connected to a data bus, the $\overline{OE}$ pins can be controlled to read data from any one of the devices.

(3) Standby mode

Set $\overline{CE}$ to H to set standby mode.

In this mode, data output is set to high impedance regardless of the $\overline{OE}$ setting.

(4) Page data latch mode

At the beginning of page write mode, set $\overline{CE}$ to H, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set page data latch mode. In this mode, 1 page (4 bytes) of data are latched to the internal address/data latch circuit.

(5) Page write mode

After latching the address and data for one page (4 bytes) using page latch mode, execute page write by providing a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with both $\overline{CE}$ and $\overline{OE}$ set to H. Next, execute program verification by setting both $\overline{CE}$ and $\overline{OE}$ to L.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where X - 10).

(6) Byte write mode

Provide a 0.1-ms program pulse (active low) to the $\overline{PGM}$ terminal with both $\overline{CE}$ and $\overline{OE}$ set to H to execute page write. Next, execute program verification by setting $\overline{OE}$ to L.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where X - 10).

(7) Program verify mode

Set $\overline{CE}$ to L, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set program verify mode. Use verify mode for verification following each write operation.

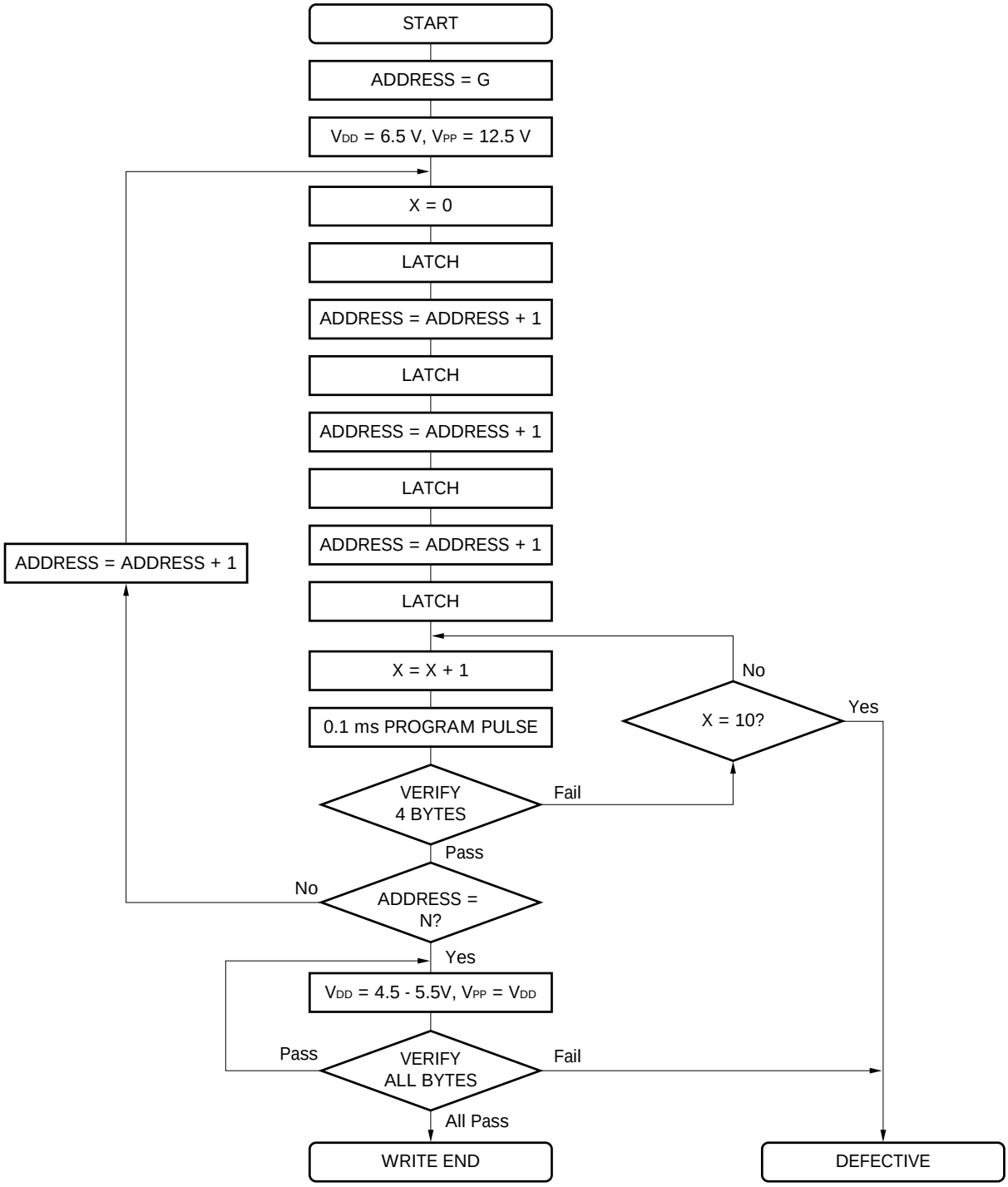
(8) Program inhibit mode

Program inhibit mode is used to write to a single device when $\overline{OE}$, V_{PP}, and D0 to D7 pins of several μPD78P083 devices are connected in parallel.

Use the page write mode or byte write mode described above for each write operation. Write operations cannot be done for devices in which the $\overline{PGM}$ pin has been set to H.

4.2 PROM Write Procedure

Figure 4-1. Page Program Mode Flowchart



Remarks 1. G = Start address

2. N = Program end address

Figure 4-2. Page Program Mode Timing

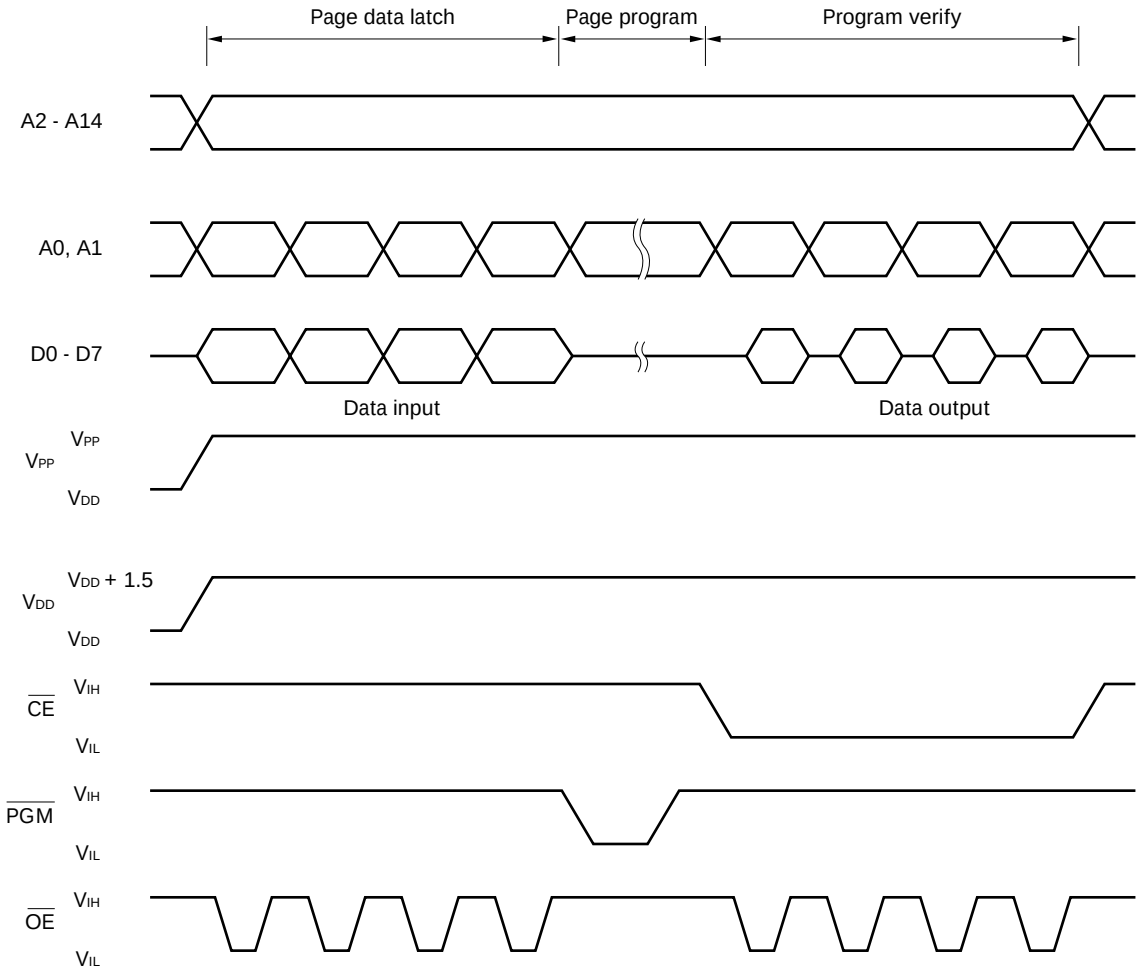
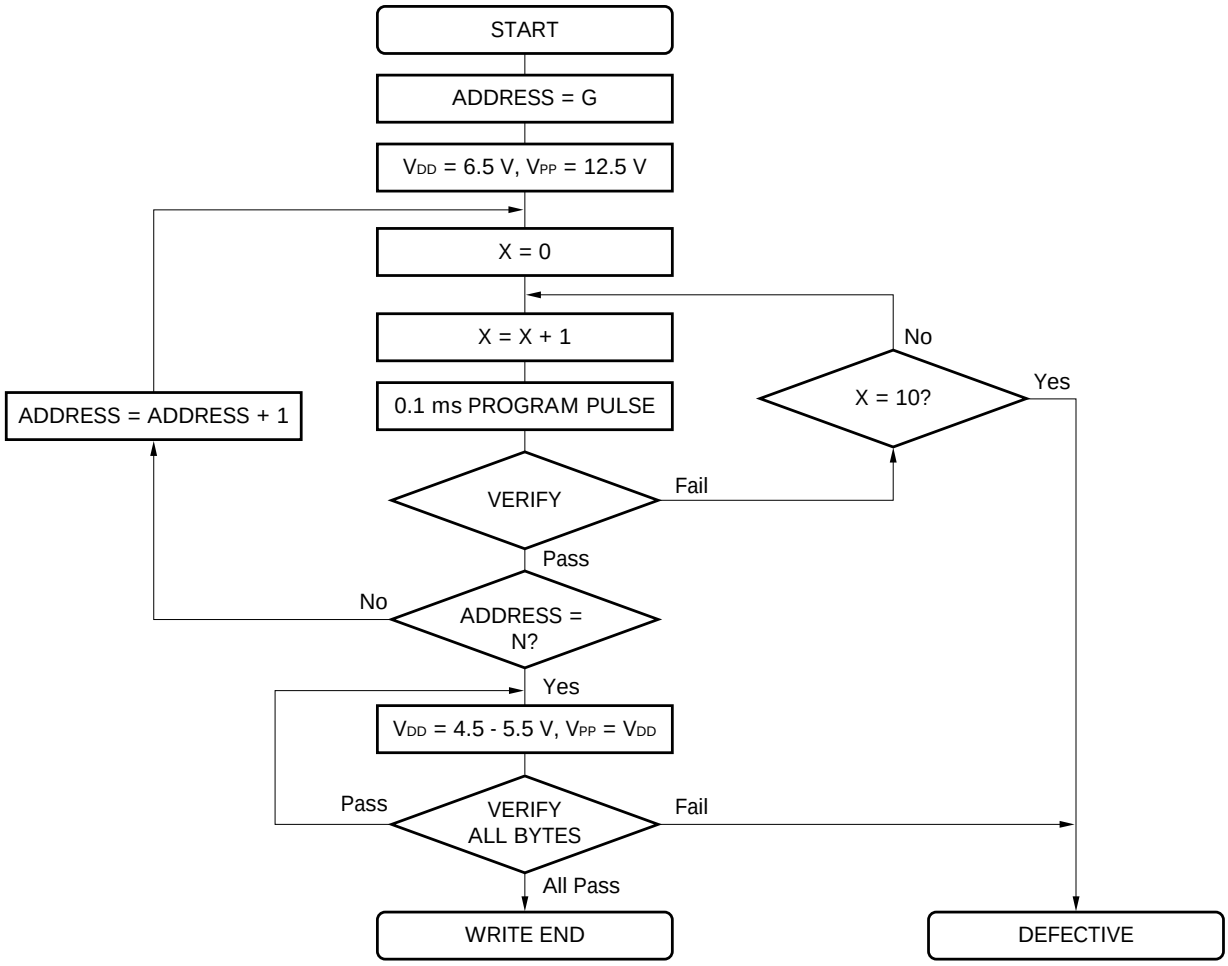


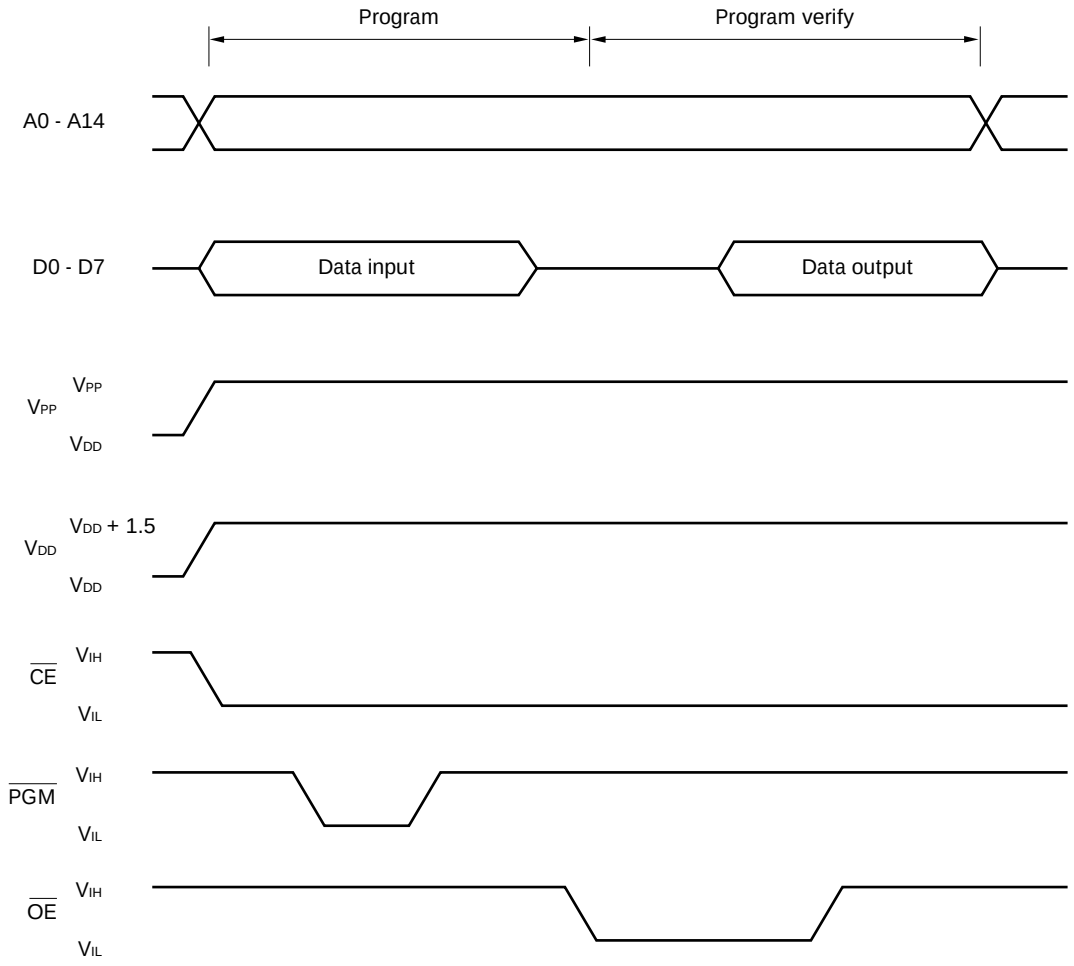
Figure 4-3. Byte Program Mode Flowchart



Remarks 1. G = Start address

2. N = Program end address

Figure 4-4. Byte Program Mode Timing



Cautions 1. V_{DD} must be supplied before applying V_{PP}, it should be removed after removing V_{PP}.

2. V_{PP} must not exceed +13.5V, including overshoot.

3. Reliability problems or other adverse effects may result if V_{PP} is removed while applying +12.5 V.

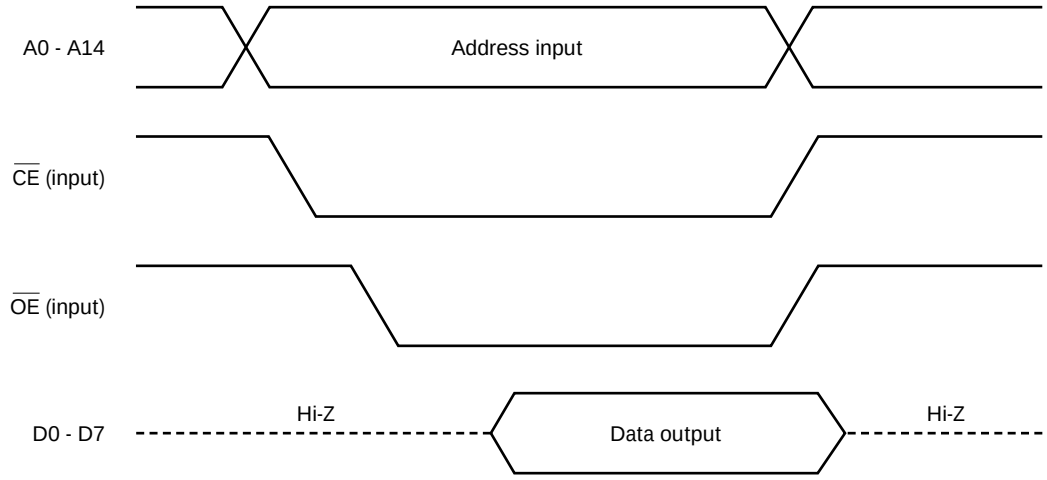
4.3 PROM Read Procedure

Follow this procedure to read the PROM contents to an external data bus (D0 to D7).

(1) Set the $\overline{\text{RESET}}$ pin to low level and supply +5 V to the V_{PP} pin. Refer to the pin configuration (Top View) under section "(2) PROM programming mode" for connections of other unused pins.
(2) Supply +5V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to pins A0 to A14.
(4) Set read mode.
(5) Data is output to pins D0 to D7.

Figure 4-5 shows the timing of steps (2) to (5) above.

Figure 4-5. PROM Read Timing



5. PROGRAM ERASURE (FOR μPD78P083DU ONLY)

In the μPD78P083DU it is possible to erase (FFH) data that has been written to program memory and to write new data.

Erasure is made by exposing the window to light having a very short wavelength of shorter than 400 nm. The program memory contents are usually erased by ultraviolet rays having a wavelength of 254 nm. The amount of exposing needed to completely erase the programmed data is shown below.

- Ultraviolet ray strength × erasure time: 15 W•s/cm^2 or more
- Erasure time: 15 to 20 minutes (when using a 12,000 μW/cm^2 ultraviolet lamp. However, the required erasure time may be longer in some cases, such as when there has been deterioration of ultraviolet lamp performance or when the erasure window is dirty.)

When erasing, place the ultraviolet lamp within 2.5 cm of the erasure window. If a filter has been attached to the ultraviolet lamp, remove the filter before erasing.

6. OPAQUE FILM ON ERASURE WINDOW (FOR μPD78P083DU ONLY)

Except when erasing EPROM contents, be sure to leave the opaque film on the erasure window to prevent unintentional erasure of EPROM contents from light sources other than the ultraviolet lamp and to prevent light sources from inadvertently affecting internal circuits other than the EPROM.

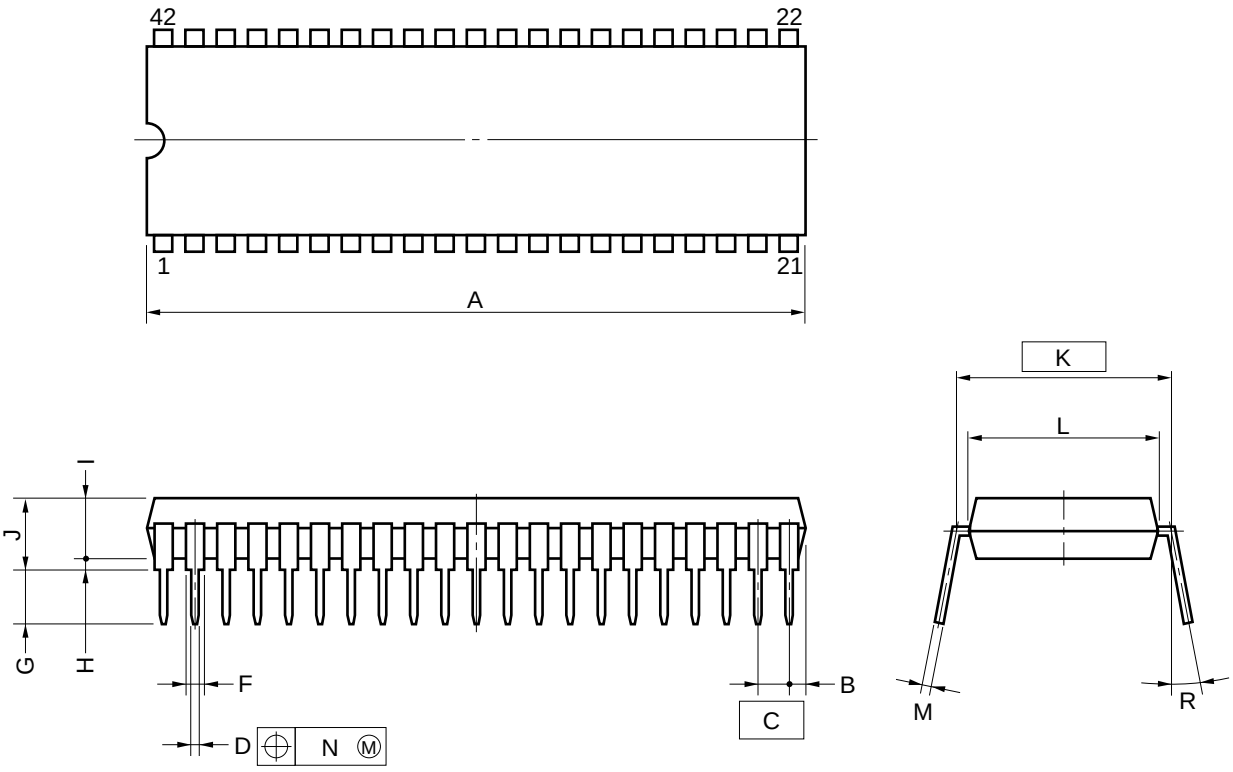
7. SCREENING OF ONE-TIME PROM VERSIONS

Due to the structure of the one-time PROM (μPD78P083CU or 78P083GB-3B4), it is impossible to fully test the device prior to shipment. It is therefore recommended that the device be stored in high temperature conditions shown below, followed by screening to verify the PROM after writing the required data.

Storage temperature	Storage time
125½C	24 hours

8. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

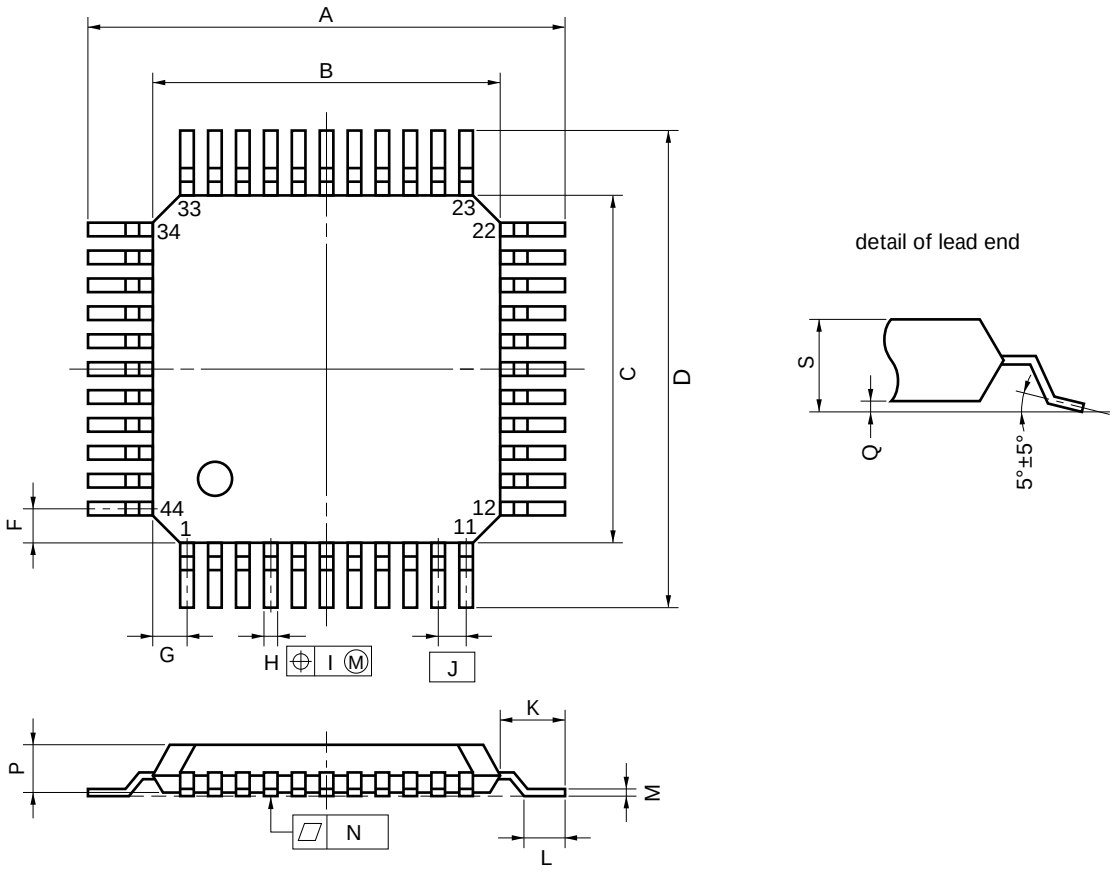
ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

42-pin ceramic shrink DIP (with window) (600 mil)

T.B.D.

44 PIN PLASTIC QFP (□10)



P44GB-80-3B4-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78P083.

Language processing software

RA78K/0 **Notes 1, 2,** and **3**	Assembler package for 78K/0 Series
CC78K/0 **Notes 1, 2,** and **3**	C compiler package for 78K/0 Series
DF78083 **Notes 1, 2, 3** and **6**	Device file for μPD78083 Subseries
CC78K/0-L **Notes 1, 2,** and **3**	C compiler library source file for 78K/0 Series

PROM write tools

PG-1500	PROM programmer
PA-78P083CU **Note 6**	Programmer adapter, connects to PG-1500
PA-78P083GB **Note 6**	
PG-1500 controller **Notes 1** and **2**	Control program for PG-1500

Debugging tools

IE-78000-R	In-circuit emulator for 78K/0 Series
IE-78000-R-BK	Break board for 78K/0 Series
IE-78078-R-EM **Note 6**	Emulation board for μPD78078 Subseries
EP-78083CU-R **Note 6**	Emulation probe for μPD78083 Subseries
EP-78083GB-R **Note 6**	
EV-9200G-44	Socket for mounting on user system board made for 44-pin plastic QFP
SD78K/0 **Notes 1** and **2**	Screen debugger for IE-78000-R
SM78K/0 **Notes 3, 4, 5,** and **6**	System simulator for 78K/0 Series
DF78083 **Notes 1, 2, 3, 4, 5,** and **6**	Device file for μPD78083 Subseries

Fuzzy inference development support systems

FE9000 **Note 1**/FE9200 **Note 5**	Fuzzy knowledge data generation tool
FT9080 **Note 1**/FT9085 **Note 2**	Translator
FI78K0 **Notes 1** and **2**	Fuzzy inference module
FD78K0 **Notes 1** and **2**	Fuzzy inference debugger

Notes 1. Based on PC-9800 Series (running MS-DOS™)
2. Based on IBM PC/AT™ (running PC-DOS™)
3. Based on HP9000 Series 300™ and Series 700™ (running HP-UX™), SPARCstation™ (running Sun OS™), and EWS-4800 Series (running EWS-UX/V).
4. Based on PC-9800 Series (running MS-DOS + Windows™)
5. Based on IBM PC/AT (running PC-DOS + Windows)
6. Currently under development

Remark The RA78K/0, CC78K/0, SD78K/0, or SM78K/0 can be used in combination with the DF78083.

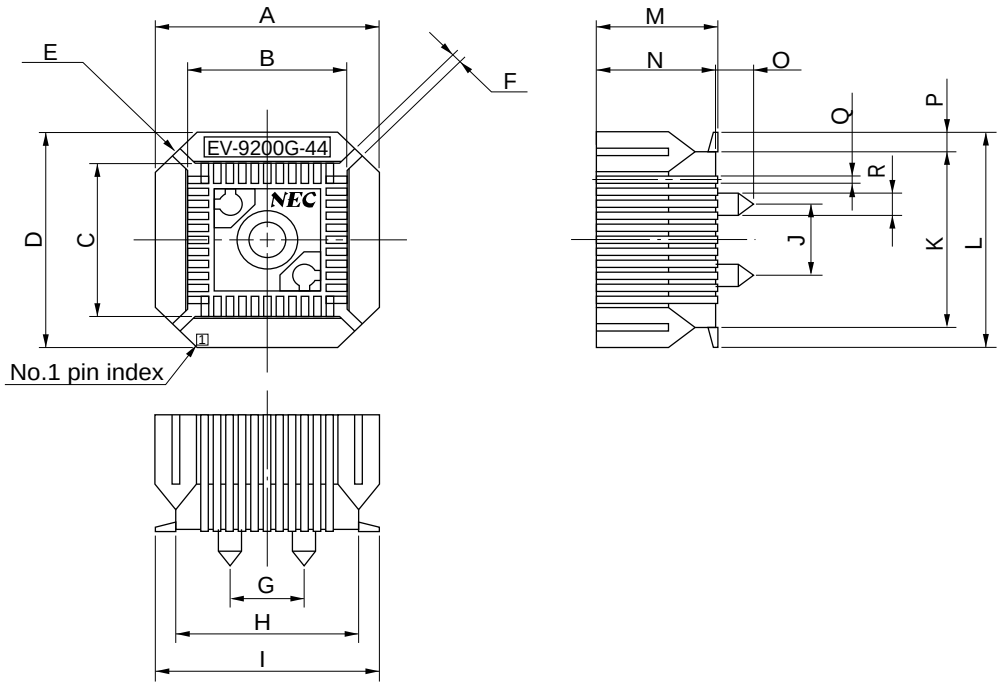
Development Tools by Third-party Manufacturers

Company	Emulator	Assembler	C Compiler	Simulator	Debugger
Advanced Data Controls Co., Ltd. (TEL: 03-3576-5351)	—	—Note	Available (C cross 78K0 compiler)	Available (CXDB/S)	Available (CSDB/E)
Gaio Technology Co., Ltd. (TEL: 03-3662-3041)	—	Available (XASS-V)	—	Available (XDEB-V)	Available (XDDI-V)
Lifeboat, Inc. (TEL: 03-3293-4714)	—	—	—Note (ICC78000)	—	—
Yokogawa Digital Computer Corporation (TEL: 0422-56-9101)	Available (AD200)	—	—	—	Available (μVIEW)

Note Assemblers are bundled with C compiler packages.

Drawing of conversion socket (EV-9200G-44) and footprint

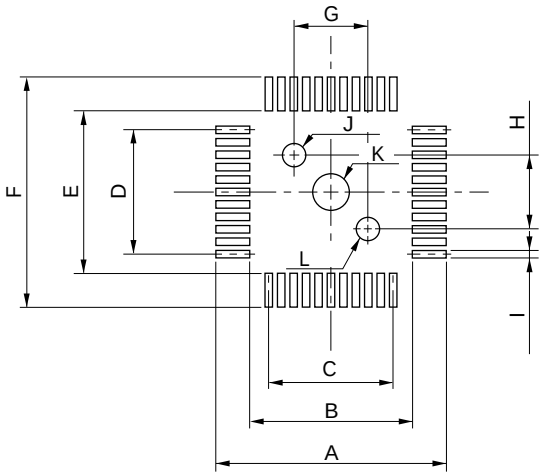
Figure A-1. Socket Drawing of EV-9200G-44 (reference)



EV-9200G-44-G0

ITEM	MILLIMETERS	INCHES
A	15.0	0.591
B	10.3	0.406
C	10.3	0.406
D	15.0	0.591
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	5.0	0.197
H	12.0	0.472
I	14.7	0.579
J	5.0	0.197
K	12.0	0.472
L	14.7	0.579
M	8.0	0.315
O	7.8	0.307
N	2.0	0.079
P	1.35	0.053
Q	0.35±0.1	$0.014^{+0.004}_{-0.005}$
R	ϕ1.5	ϕ0.059

Figure A-2. Footprint for EV-9200G-44 (reference)



EV-9200G-44-P0

ITEM	MILLIMETERS	INCHES
A	15.7	0.618
B	11.0	0.433
C	$0.8\pm0.02\times10=8.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.394=0.315^{+0.002}_{-0.002}$
D	$0.8\pm0.02\times10=8.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.394=0.315^{+0.002}_{-0.002}$
E	11.0	0.433
F	15.7	0.618
G	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
H	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
I	0.5 ± 0.02	$0.02^{+0.001}_{-0.002}$
J	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$
K	$\phi2.2\pm0.1$	$\phi0.087^{+0.004}_{-0.005}$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

APPENDIX B. RELATED DOCUMENTS

Device-related documents

Document name	Document No.	
	Japanese version	English version
μPD78083 Subseries User's Manual	IEU-886	—
78K/0 Series User's Manual: Instructions	IEU-849	IEU-1372
78K/0 Series Instruction Use Manual	IEM-5522	—
78K/0 Series Instruction Set	IEM-5521	—
μPD78083 Subseries Special Function Register Reference Table	IEM-5599	—

Development tool-related documents (user's manuals)

Document name		Document No.	
		Japanese version	English version
RA78K Series Assembler Package	Operation manual	EEU-809	EEU-1399
	Source code manual	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation manual	EEU-656	EEU-1280
	Source code manual	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		EEU-978	—
SD78K/0 Screen Debugger	Introduction	EEU-852	EEU-1414
	Reference manual	EEU-816	EEU-1413

Related documents (user's manuals) for embedded software

Document name	Document No.	
	Japanese version	English version
Fuzzy knowledge data generation tool	EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System: Translator	EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System: Fuzzy Inference Module	EEU-858	—
78K/0 Series Fuzzy Inference Development Support System: Fuzzy Inference Debugger	EEU-921	—

Caution The contents of the above documents are subject to change without prior notice. Be sure to use the latest edition for purposes such as design work.

Other related documents

Document name	Document No.	
	Japanese version	English version
Package manual	IEI-635	IEI-1213
Semiconductor Device Mounting Manual	IEI-616	IEI-1207
NEC Semiconductor Device Quality Grades	IEI-620	IEI-1209
NEC Semiconductor Device Reliability and Quality Control	IEM-5068	—
Electrostatic Discharge (ESD) Tests	MEM-539	—
Semiconductor Device Quality Assurance Guide	MEI-603	MEI-1202
Microcomputer-related Product Guide (Products by other Manufacturers)	MEI-604	—

Caution The contents of the above documents are subject to change without prior notice. Be sure to use the latest edition for purposes such as design work.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related document in this publication may include preliminary versions.
However, preliminary versions are not marked as such.

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