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ApNote AP163703

Reset and System Startup Configuration via PORT0 or Register RSTCON

Presents an overview about the different reset types (power-on reset, long/short hardware reset, software reset, WDT reset) and the system startup configuration via PORT0 or register RSTCON. The calculation for the pull-up/down resistors at PORT0 is also included.

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Note: Some of the products mentioned in this Application Note are not officially announced yet.

AP163703 ApNote - Revision History		
Actual Revision: 12.99 Previous Revision: 6.98		
Page of actual Rev.	Page of prev.Rel.	Subjects (changes since last release)
1	1	RSTCON in title added
3,4	3,4	updated
5	4	Device list updated
7	6	Table updated
11	9	Notes added
12	--	New chapter “System Startup Configuration upon a Single-Chip Mode Reset”
17	12	Note added
18	--	New chapter “Calculation of the Pull-down Resistor at Pin BSL Entry in Single-Chip Mode”
22	15	Appendix “Reset, Clock Options and Steps” updated

1 Overview about the different Reset Sources

During reset, the device executes a special internal sequence in order to set internal signals and the Special Function Registers (SFRs) to their specified default values. The contents of some Special Function Registers are controlled during system startup configuration via PORT0 or default value.

The system startup configuration at PORT0 is sampled upon different reset events. See table 1:

- Hardware Reset: - Power-on Reset
  - Short Hardware Reset (Warm Reset)
  - Long Hardware Reset (Power Down Wakeup Reset)
- Software Reset
- Watchdog Timer Reset

The reset source is also indicated by the reset source indication flags in register WDTCON.

Reset Source	Short-cut	Condition
Power-on Reset	PONR	Power-on, t_{RSTIN} >> 1024 TCL
Short Hardware Reset	SHWR	4 TCL < t_{RSTIN} ≤ 1024 TCL
Long Hardware Reset	LHWR	t_{RSTIN} > 1024 TCL
Watchdog Timer Reset	WDTR	WDT overflow
Software Reset	SWR	SRST command

Table 1:
Reset Sources and Reset Conditions

1.1 Hardware Reset

A hardware reset is triggered when the reset input signal $\overline{\text{RSTIN}}$ is sampled low. To ensure the recognition of the $\overline{\text{RSTIN}}$ signal (latching), it must be held low for at least 2 CPU clock cycles (4 TCL = 100 ns @ 20 MHz CPU Clock). Also shorter $\overline{\text{RSTIN}}$ pulses may trigger a hardware reset, if they coincide with the latch's sample point. However, for microcontrollers with an on-chip PLL it is recommended to keep $\overline{\text{RSTIN}}$ low for ca. 1 ms to guarantee that the PLL is locked. After the reset sequence has been completed, the $\overline{\text{RSTIN}}$ input is sampled again. When the reset input signal is active (low) at that time the internal reset condition is prolonged until $\overline{\text{RSTIN}}$ gets inactive (high).
The input $\overline{\text{RSTIN}}$ provides an internal pull-up device equalling a resistor of 50 KΩ to 250 KΩ (the minimum reset time must be determined by the lowest value). Simply connecting an external capacitor is sufficient for an automatic power-on reset (a proper low level of $\overline{\text{RSTIN}}$ between power off and on has to be reached). $\overline{\text{RSTIN}}$ may also be connected to the output of other logic gates.

Three different kinds of external hardware resets have to be considered:

a) Power-on Reset
A complete power-on reset requires an active RSTIN time of two reset sequences (2 * 1024 TCL = 51.2 µs @ 20 MHz CPU Clock) after a stable clock signal is available. Depending on the oscillation frequency and the type of external oscillator circuit, the on-chip oscillator needs about 0.01...50 ms (quartz crystal: 2...50 ms, ceramic resonator: 0.01...0.5 ms) to stabilize. This means that the power-on reset time is dominant by the oscillator start-up time.

b) Long Hardware Reset
A long hardware reset requires an active RSTIN time longer than the duration of the internal reset sequence. The duration of the internal reset sequence is 1024 TCL (1024 TCL = 25.6 µs @ 20 MHz CPU Clock). The long hardware reset is also named power down wakeup reset.

c) Short Hardware Reset
The active RSTIN time of a short hardware reset is between 4 TCL and 1024 TCL. If the RSTIN signal is active for at least 4 TCL clock cycles (100 ns @ 20 MHz CPU Clock) the internal reset sequence is started (1024 TCL, 25.6 µs @ 20 MHz CPU Clock). After the internal reset sequence has been completed, the RSTIN input is sampled. When the reset input is still active at that time the internal reset condition is prolonged until RSTIN gets inactive. If the RSTIN signal is active for more then 1024 TCL then the behaviour of the PORT0 latch mechanism is equal to a long hardware reset.

1.2 Software Reset

The reset sequence can be triggered at any time via the protected instruction SRST (Software Reset). This instruction can be executed deliberately within a program, e.g. to leave bootstrap loader mode, or upon a hardware trap that reveals a system failure. A software reset takes 1024 TCL (25.6 µs @20 MHz).

1.3 Watchdog Timer Reset

When the watchdog timer is not disabled during the initialization or serviced regularly during program execution it will overflow and trigger the reset sequence. The watchdog timer reset releases automatically a software reset. Other than a hardware reset the watchdog timer reset completes a running external bus cycle if this bus cycle either does not use READY at all, or if READY is sampled active (low) after the programmed waitstates. When READY is sampled inactive (high) after the programmed waitstates the running external bus cycle is aborted. Then the internal reset sequence is started.

Note: The watchdog timer reset cannot occur while the device is in bootstrap loader mode!

1.4 Bidirectional Reset

The bidirectional reset is a new feature and implemented since the devices and steps listed below. The steps in parentheses do only reflect a software- or watchdog timer reset to $\overline{\text{RSTIN}}$ but not a short hardware reset as shown in figure 7.

Device	Step	Device	Step
C161RI	all	C167CR-LM	(CA), CB
C161CI / SI	all	C167CR-4RM	(AB), AC
C161PI	all	C167CR-16RM	FA
C161CS / JC / JI	all	C167S-4RM	(BA), BB
C161OR	all	C167CS	all
C164CI-8EM	all	167SR	FA

Table 2:
Devices with implemented Bidirectional Reset Feature

In bidirectional reset mode the device's line $\overline{\text{RSTIN}}$ (normally an input) may be driven active by the chip logic e.g. in order to support external equipment which is required for startup (e.g. flash memory).

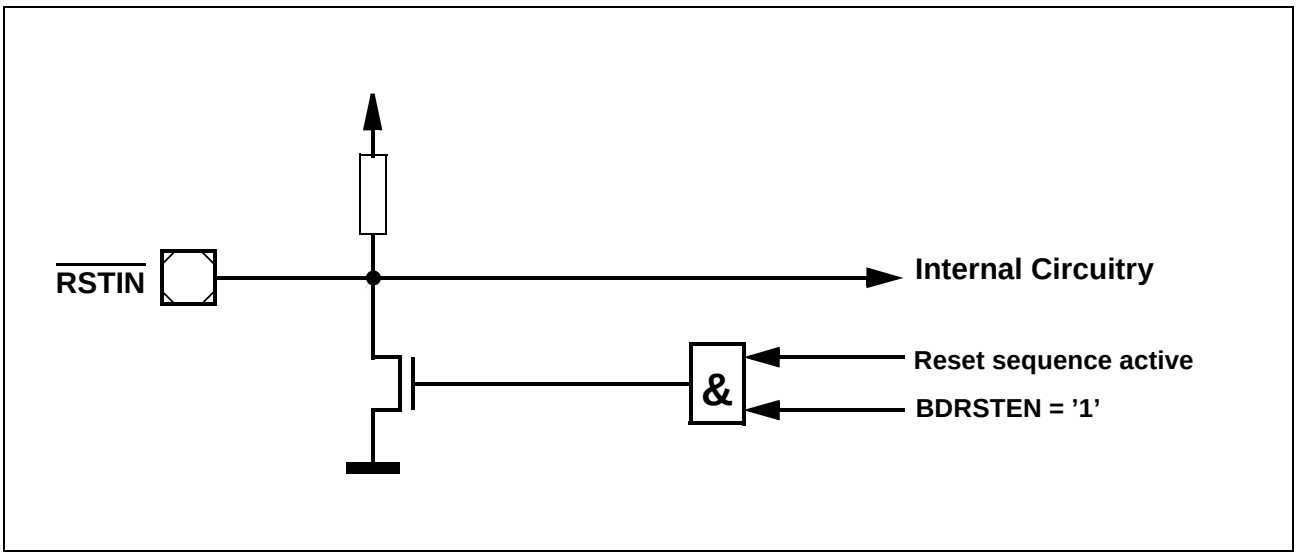


Figure 1 :
Bidirectional Reset Operation

Bidirectional reset reflects internal reset sources (software, watchdog) also to the RSTIN pin and converts short hardware reset pulses to a minimum duration of the internal reset sequence. Bidirectional reset is enabled by setting bit BDRSTEN in register SYSCON (SYSCON.3) and changes RSTIN from a pure input to an open drain IO line with an integrated pull-up resistor. When an internal reset is triggered by the SRST instruction or by a watchdog timer overflow or a low level is applied to the RSTIN line, an internal driver pulls it low for the duration of the internal reset sequence. After that it is released and is then controlled by the external circuitry alone.

The bidirectional reset function is useful in applications where external devices require a defined reset signal but cannot be connected to the device's RSTOUT signal, e.g. an external flash memory which must come out of reset and deliver code well before RSTOUT can be deactivated via EINIT.

The following behaviour differences must be observed when using the bidirectional reset feature in an application:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT.
- After a reset bit BDRSTEN is cleared (bidirectional reset is disabled).
- Bit WDTR will always be '0', even after a watchdog timer reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 (RD) is low.
- Pin RSTIN may only be connected to external reset devices with an open drain output driver.

2 System Startup Configuration

Some system features have to be selected before the first instruction of a program is executed. These selections are made during reset via the pins of PORT0 which are latched at the end of reset, or via a fixed configuration value which is used when $\overline{EA}$ = High (single chip mode reset, see section 2.3 for details).

2.1 PORT0 Configuration during Reset

Table 3 shows PORT0 configuration pins and which kind of reset (sample event) does sample which pin depending whether bidirectional reset is enabled (on) or disabled (off).

X : Pin is sampled **-** : Pin is not transparent and not sampled	BDRST	PORT0																	External Access enable	OWD disable	BSL entry
		Clock options			Segm. Addr. Lines		Chip Selects		WR Config.	Bus Type		Reserved	BSL Reserved	Reserved		Adapt Mode	Emu Mode	Invert P0H.7			
Sample event		P0H.7	P0H.6	P0H.5	P0H.4	P0H.3	P0H.2	P0H.1	P0H.0	P0L.7	P0L.6	P0L.5	P0L.4	P0L.3	P0L.2	P0L.1	P0L.0		$\overline{EA}$	$\overline{RD}$	
PONR	off	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LHWR	off	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SHWR	off	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	-	X	X	X
WDTR/SWR	off	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-	-	X	X	-
LHWR	on	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SHWR	on	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
WDTR/SWR	on	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 3:
System Startup Configuration via PORT0

The PORT0 startup configuration is sampled either with the end of the internal reset sequence or with the end of the external hardware reset. If the external RSTIN signal is deactivated before the end of the internal reset sequence (short hardware reset) then an internal reset signal (IRS) of the device is used to latch the system startup configuration at PORT0, else (power-on reset or long hardware reset) PORT0 is latched after the rising edge of RSTIN with signal IRS. The sampling point of PORT0 is 7 TCL (prescaler enabled) or 10 TCL (direct drive or PLL) after the rising edge of RSTIN as shown in the PORT0 sample timing (see figures below).

The duration of one internal reset sequence is 1024 TCL for initializing the internal Special Function Registers plus 10 TCL for the jump to address $00'0000_H$ after the internal reset sequence.

The bidirectional reset feature converts software reset, WDT reset or short hardware reset to an externally visible hardware reset with a duration of 1024 TCL. This feature is disabled after hardware reset and can be enabled via software.

2.2 PORT0 Sample Timing for the different Reset Types

The different reset sources and timing relations at PORT0 during and at the end of reset are shown below. If a reset event occurs then PORT0 is switched to input mode and the internal pull-ups are active. During that time it is possible that the desired input voltage levels at PORT0 (V_{IH} and V_{IL} forced by the internal/external pull-ups and pull-downs for the startup configuration) are not reached. Therefore PORT0 is **not** transparent for 1024TCL (power-on reset for 2048 TCL) to prevent unexpected behaviour to the system. After that time a part of PORT0 becomes transparent and at the end of reset these pins are sampled with the IRS signal.
Depending on the reset type some PORT0 pins are not transparent, e.g. P0L.1 and P0L.0 which control Adapt Mode and Emulation Mode. Noise on these lines during reset would force the microcontroller to Adapt Mode or Emulation Mode. Therefore both pins are not transparent until the sample point IRS at the end of the reset condition.
The PORT0 sample timings shown below are based on the following conditions:

t_{P0fix}: During t_{P0fix} PORT0 has to be constant so the System Startup Configuration is latched correctly.

t_{SHR}: Duration of a short hardware reset. 4 TCL < t_{SHR} ≤ 1024 TCL

IRS: Internal Reset Signal: Sampling point of PORT0 configuration bits is 7 TCL (prescaler enabled) or 10 TCL (direct drive or PLL) after the rising edge of RSTIN or after the end of the internal reset sequence.

TCL: 1 TCL = 1 / (2 *f_{CPU}), 1 TCL = 25 ns @ 20 MHz CPU Clock

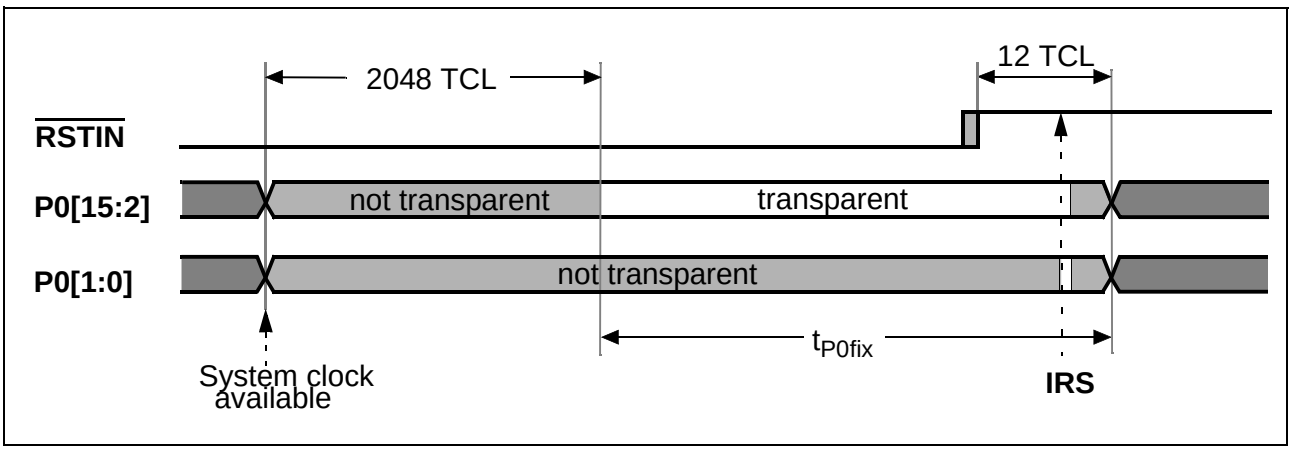


Figure 2 :
PORT0 sample Timing: Power-on Reset

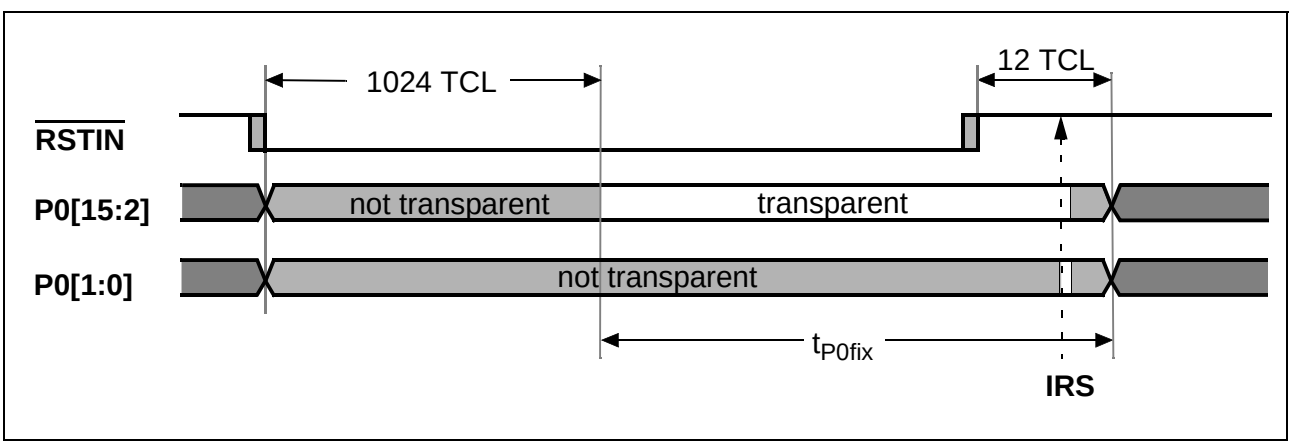


Figure 3 :
PORT0 sample Timing: Long Hardware Reset, Bidirectional Reset enabled or disabled

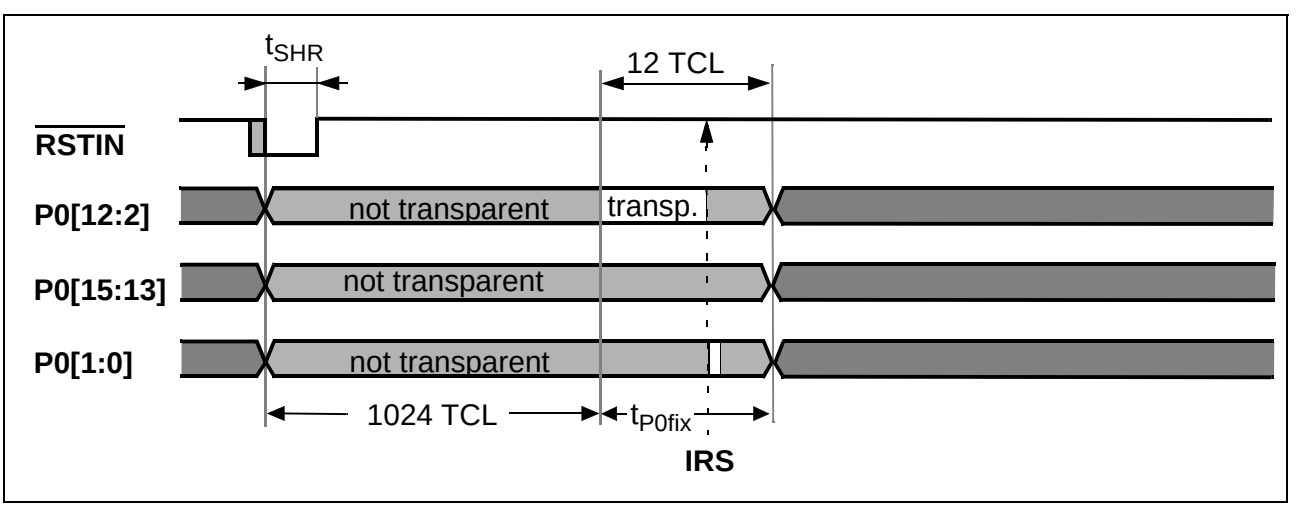


Figure 4 :
PORT0 sample Timing: Short Hardware Reset, Bidirectional Reset disabled

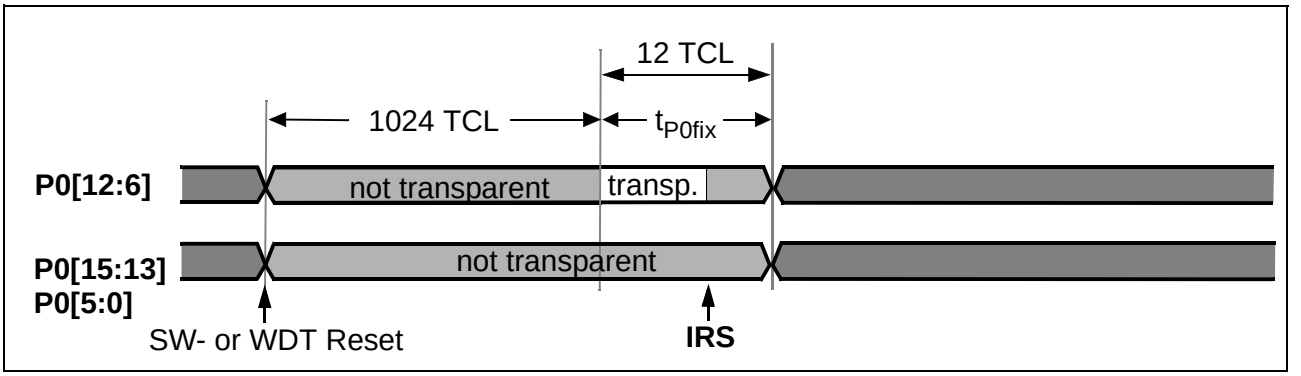


Figure 5 :
PORT0 sample Timing: Software Reset or WDT Reset, Bidirectional Reset disabled

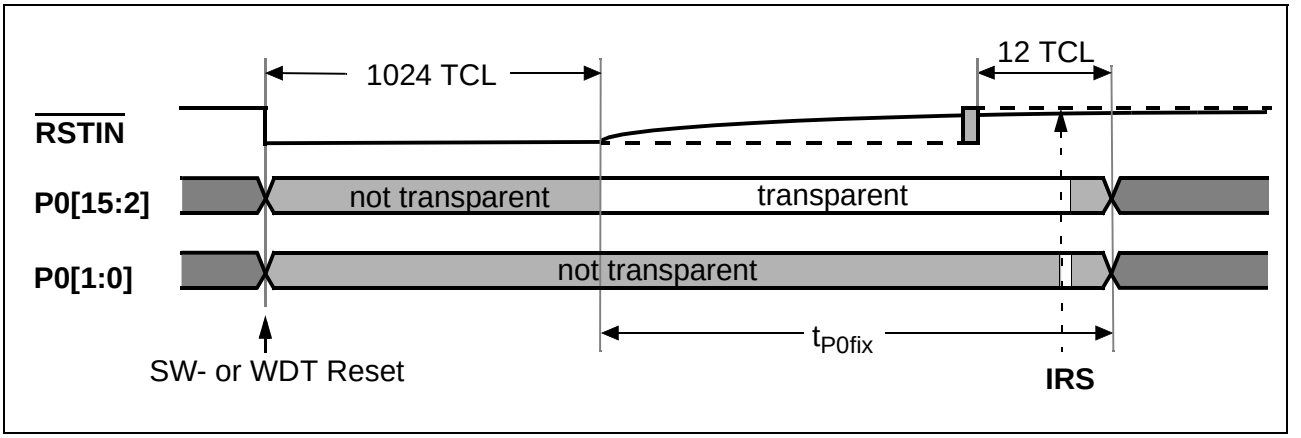


Figure 6 :
PORT0 sample Timing: Software Reset and WDT Reset, Bidirectional Reset enabled

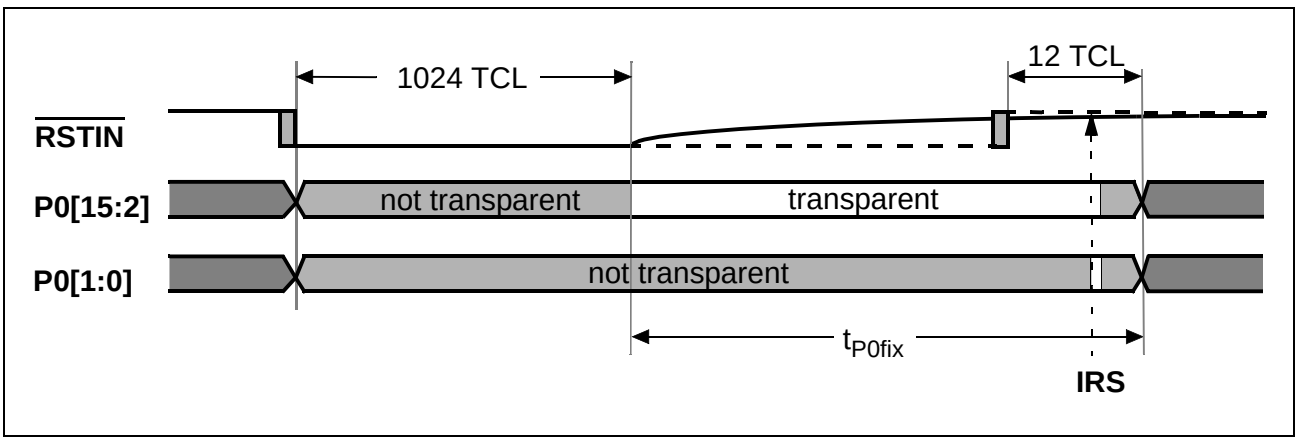


Figure 7 :
PORT0 sample Timing: Short Hardware Reset, Bidirectional Reset enabled

Note: The characteristic that PORT0[1:0] is not transparent before it is latched as shown in figure (2, 3, 4, 6 and 7) is only implemented in the actual devices. The PORT0[1:0] characteristic of the older ones listed below differs in that point. For these devices PORT0[1:0] is transparent for the same duration as PORT0[15:2]. During software reset or WDT reset (bidirectional reset disabled) PORT0[1:0] is not latched and therefore not transparent, see figure 5.

Device	Step	Device	Step
C161V / K / O	AA	C167-LM	BB, BC, BD
C163-L	AB	C167S-4RM	AA, AE
C165	CA, DA	C167SR-LM	BA,BB
C167CR-LM	BA, BB, BE	C167CR-16RM	AA

Table 4:
Devices were PORT0[1:0] are transparent during Reset

Note: Latching of the PORT0 configuration when Pin $\overline{EA}$ = High is different for devices with **flash on chip**. For devices without single chip-mode reset (RSTCON), i.e. the devices not included in Table5, when the level on pin $\overline{EA}$ is high during reset, the configuration on P0H.[4:0] and P0L.[7:0] is not latched with the end of the internal reset condition, but about 120 ± 40 µs later (due to program Flash voltage ramp-up). This behavoiur should not present a problem in systems where the reset configuration is realized by external resistors on PORT0 and where no other device is driving onto PORT0 (the data bus) unless explicitly selected by the microcontroller under software control otherwise, make sure that the reset configuration is maintained on PORT0 until 200 µs after the end of the internal reset condition and that PORT0 is not switched to output or external bus accesses are performed during the first 120 µs of program execution.

2.3 System Startup Configuration upon a Single-Chip Mode Reset

For a single-chip mode reset (indicated by $\overline{EA}$ = High) the configuration via PORT0 is replaced by the fixed configuration value $XX2B_H$, (see User's Manual chapter "System Startup Configuration upon a Single-Chip Mode Reset"). In this case PORT0 needs no external circuitry (pull-ups/pull-downs) and also the internal configuration pull-ups are not activated.

This fixed default configuration is activated after each long hardware reset (LHWR) or power-on reset (PONR). The fixed default configuration selects a safe worst-case configuration. The initialization software can then modify these parameters via register RSTCON and select the intended configuration for a given application.

Table 6 includes the principle differences for the system startup configuration related to $\overline{EA}$ = Low and $\overline{EA}$ = High. The column "Configuration Source" shows a comparison for devices with and without register RSTCON.

The single-chip mode reset via register RSTCON is a new feature and implemented since the devices listed below.

Device	Step	Device	Step
C164CI-xRM	AA*)	C161CS-32RM	AA
C164xy-8FM	AA	C167CS-4RM	AA

Table 5:
Devices with Single-Chip Mode Reset (RSTCON)

*) In the first step of the C164CI-4RM or -8RM (32/64 Kbyte ROM version), as an intermediate solution, when pin $\overline{EA}$ = High during reset, the configuration is read from internal ROM address 00.003Eh instead of P0H.[7:0], and is copied into register RP0H. In this case, the status of PORT0 during reset is not evaluated. Register RSTCON is not implemented and during startup the content of ROM address 00.003Eh is used instead of the default configuration for single-chip mode reset.

Mode	Type of Reset BDRST (on/off)	Configuration / { Behaviour }	Configuration Source	
			Device with RSTCON	Device without RSTCON
$\overline{EA}$ = High Single Chip Mode	PONR, LHWR, (SHWR, WDTR, SWR) and BDRST on	P0H[7:5] clock options	default/RSTCON	P0H[7:5]
		P0H[4:3] segm. addr. lines	default/RSTCON	don't care/P0H[4:3] 4)
		P0H[2:1] chip select lines	default/RSTCON	don't care/P0H[2:1] 4)
		P0H[0] WR configuration	default/RSTCON	P0H[0] 4)
		P0L[7:6] bus type	default/RSTCON	don't care
		P0L[5:2] BSL entry	not possible	P0L[5:2]
		P0L[1] adapt mode	not possible 1)	P0L[1]
		P0L[0] emulation mode	not possible 2)	P0L[0]
		$\overline{RD}$ BSL entry	$\overline{RD}$	not possible 3)
	(SHWR, WDTR, SWR) and BDRST off	P0H[7:5] clock options	RSTCON	don't care
		P0H[4:3] segm. addr. lines	RSTCON	don't care/P0H[4:3] 4)
		P0H[2:1] chip select lines	RSTCON 5)	P0H[2:1] 4)
		P0H[0] WR configuration	RSTCON	don't care/P0H[0] 4)
		P0L[7:6] bus type	RSTCON	don't care
		P0L[5:2] BSL entry	not possible	P0L[5:2] 6)
		P0L[1] adapt mode	not possible 1)	P0L[1] 6)
		P0L[0] emulation mode	not possible 2)	P0L[0] 6)
		$\overline{RD}$ BSL entry	$\overline{RD}$ 6)	not possible 3)
	Any Reset BDRST on/off	Startup configuration source	default/RSTCON	PORT0
		{ PORT0 pull-ups during reset }	off	on
		{ $\overline{CS}$ pull-ups after reset }	off 7)	
		{ $\overline{RD}$, $\overline{WR}$ pull-ups after reset }	on 8)	
		{ ALE pull-down after reset }	on 9)	
$\overline{EA}$ = Low Ext. Bus	Any Reset BDRST on/off	Startup configuration source	PORT0	
		{ PORT0 pull-ups during reset }	on	
		{ $\overline{CS}$ pull-ups after reset }	off (if selected, active high level is driven)	
		{ $\overline{RD}$, $\overline{WR}$ pull-ups after reset }	off (active high level is driven)	
		{ ALE pull-down after reset }	off (active low level is driven)	
		Oscillator watchdog disable	$\overline{RD}$ 3)	
$\overline{EA}$=Low $\overline{EA}$=High	Any Reset BDRST on/off	{ PORT0 pull-ups after reset }	off	
		{ $\overline{CS}$ pull-ups during reset }	on	
		{ $\overline{RD}$, $\overline{WR}$ pull-ups during reset }	on	
		{ ALE pull-down during reset }	on	

Table 6:
$\overline{EA}$ Pin and System Startup Configuration

[1] Adapt mode entry only via pin $\overline{EA}$ = Low.
In single-chip mode it is not possible to activate adapt mode.

[2] Emulation mode entry only via pin $\overline{EA}$ = Low.
In single-chip mode it is not possible to activate emulation mode.

[3] Oscillator watchdog can be disabled for test purposes via pull-down at pin $\overline{RD}$.

4) If system starts in single-chip mode and external bus is enabled via software later, then PORT0 startup configuration is used for the external bus but it can be changed via software.
P0H[2:1]: $\overline{CS}$ signals selected via PORT0 will be driven active high after reset.

[5] Internal $\overline{CS}$x pull-ups are active during reset.

[6] Only for SHWR. For WDTR and SWR not possible.
P0L[5:2]: If the BSL entry is done via pin RD then the CPU clock is, XTAL1 clock divided by two ($f_{CPU} = f_{OSC/2}$). This has to be considered for the appropriate communication baudrate with the external host.

[7] $\overline{CS}$ signals are driven active high after RSTCON is copied to RP0H.
If the system starts in single-chip mode and $\overline{CS}$ will be used for external access then depending on the system demands, external pull-up resistors are necessary at the $\overline{CS}$ signals because after reset and before RSTCON is copied to RP0H, the $\overline{CS}$ signals are in tristate and without defined level (internal pull-ups are disabled).

[8] Pull-ups are active until bit BUSACTx in register BUSCONx is set; then $\overline{RD}$ and $\overline{WR}$ are driven active high.

[9] Pull-down is active until bit BUSACTx in register BUSCONx is set; then ALE is driven active low.

Table 6:
$\overline{EA}$ Pin and System Startup Configuration (cont'd)

3 Calculation of the Pull-up/down Resistors at PORT0 for Startup Configuration

The specification in the Data Sheet includes the values of the PORT0 configuration currents I_{P0L} and I_{P0H}.

3.1 Pull-down Calculation

I_{P0L} is the base for the calculation of the pull-down resistors for PORT0 startup configuration. I_{P0Lmin} = -100 µA @ $V_{IN} = V_{ILmax}$. That means that the port configuration current has to be greater or equal than 100 µA to get an input voltage V_{IN} lower or equal to V_{ILmax}. The system current I_{SYSL} has a direct influence on the value of the needed pull-down resistor. The relation between the different parameters and the calculation with an example are shown below.

Note: All currents flowing into the microcontroller are defined as positive and all currents flowing out of it are defined as negative. Because of the internal pull-up transistor the direction of I_{P0L} and I_{P0H} is out of the device and therefore the sign in the current specification is negative.

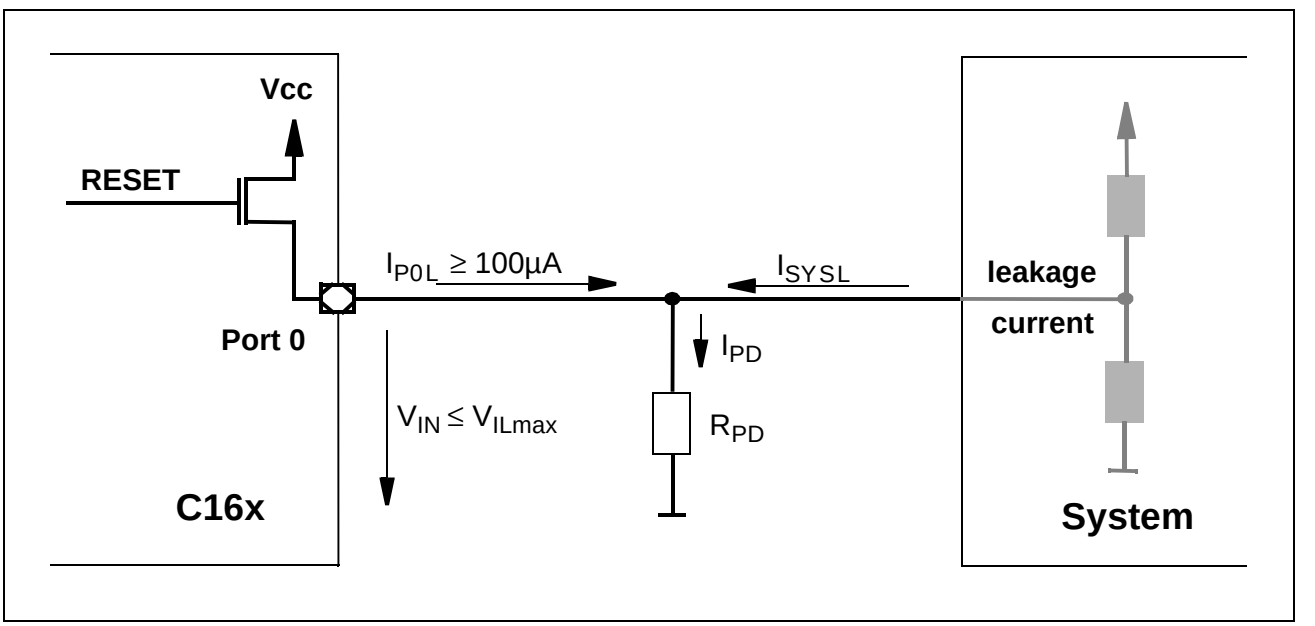


Figure 8 :
System Environment and Pull-down Resistor for Startup

Current Specification in the Data Sheet:

Vcc	= 5V ± 10%	⇒	4.5V ≤ Vcc ≤ 5.5V
V_{ILmax}	= 0.2Vcc - 0.1V	⇒	0.8V ≤ V_{ILmax} ≤ 1.0V
I_{P0Lmin}	= -100µA	⇒	I_{P0L} ≥ |-100µA|

Pull-down resistor calculation:

$$R_{PD} < \frac{V_{ILmax}}{I_{PD}} = \frac{V_{ILmax}}{I_{P0L} + I_{SYSL}}$$

Example **without** system current:
(I_{SYSL} = 0 A)

$$R_{PD} < \frac{V_{ILmax}}{I_{PD}} = \frac{0.8\ V}{100\mu A}$$

The recommended maximum value: R_{PD} = 8000 Ω

3.2 Pull-up Calculation

I_{P0H} is the base for the calculation of the pull-up resistors for PORT0 startup configuration. I_{P0Hmax} = -10 µA @ $V_{IN} = V_{IHmin}$. As already mentioned PORT0 supplies internal pull-up resistors which are only active during Reset, or during Hold-or Adapt-mode. For normal systems this internal pull-up resistors are sufficient to reach the input high voltages at the PORT0 pins. This situation changes when the system current I_{SYSH} exceeds 10 µA. Then additional external pull-up resistors are mandatory. For example system flash memory with a high leakage current can cause an increased I_{SYSH}. The calculation and an example are shown below.

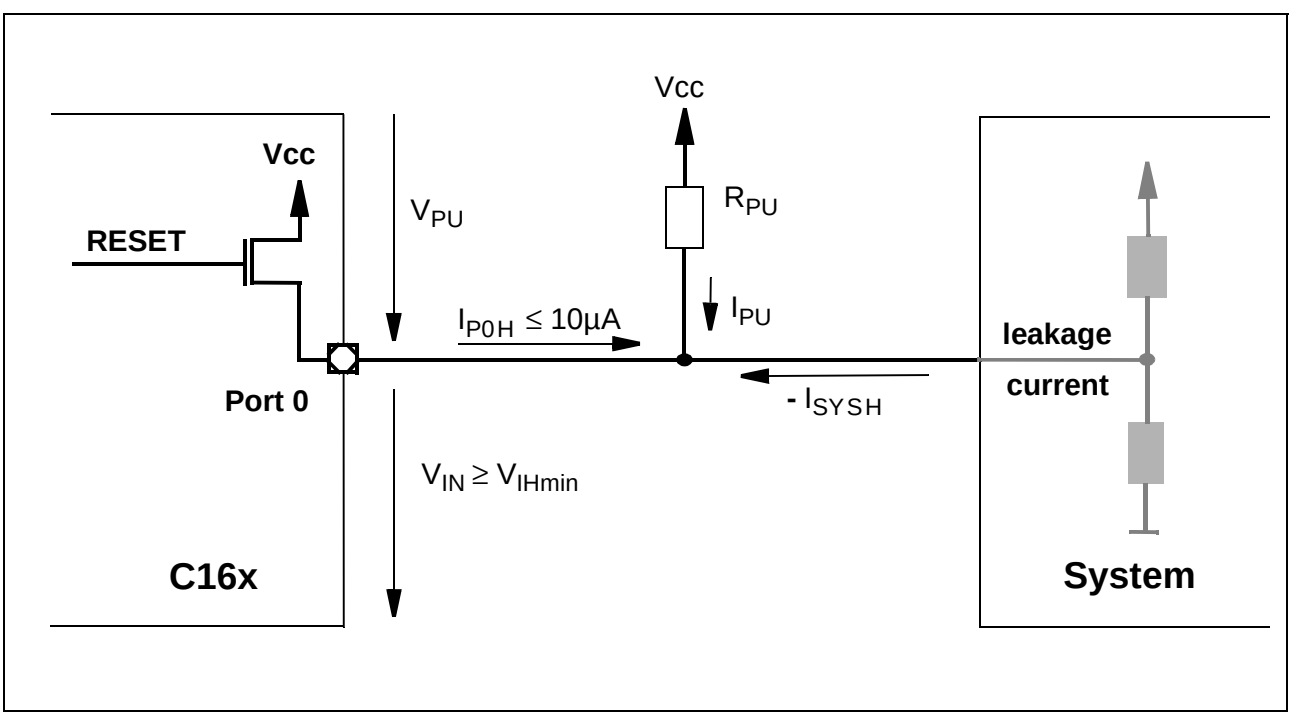


Figure 9 :
System Environment and Pull-up Resistor for Startup

Current Specification in the Data Sheet:

Vcc	= 5 V ± 10 %	⇒	4.5 V	≤	Vcc	≤ 5.5 V
V_{IHmin}	= 0.2 Vcc + 0.9 V	⇒	1.8 V	≤	V_{IHmin}	≤ 2.0 V
I_{P0Hmax}	= -10 µA	⇒	I_{P0H}	≤	|-10 µA|	

Pull-up resistor calculation:

$$R_{PU} < \frac{V_{PU}}{I_{PU}} = \frac{V_{CCmin} - V_{IHmin}}{I_{SYSH} - I_{P0H}}$$

Example: I_{SYSH} = 50µA:

$$R_{PU} < \frac{4.5\ V - 1.8\ V}{50\mu A - 10\mu A} = 67.5\ k\Omega$$

The recommended maximum value: R_{PU} = 67.5 kΩ

Note: The leakage current of some bus hold devices exceeds the specified value of I_{P0Hmax} = |10 µA|. In that case all PORT0 pins not configured to low level need a pull-up resistor. For calculation of the pull-up value please refer to the specified leakage current of the bus hold device.

4 Calculation of the Pull-down Resistor at Pin $\overline{RD}$ for BSL Entry in Single-Chip Mode

I_{RWL} is the base for the calculation of the pull-down resistor at pin $\overline{RD}$ for BSL entry when single-chip mode is selected.

The specification of Read/Write active current I_{RWLmin} = -500µA for pin $\overline{RD}$ (V_{OUT} = V_{OLmax}) is also valid for V_{IN} = V_{ILmax}. That means that the read active current has to be greater or equal than 500 µA to get an input voltage V_{IN} lower or equal to V_{ILmax}. The system current I_{SYSL} has a direct influence on the value of the needed pull-down resistor. The relation between the different parameters and the calculation with an example are shown below.

Note: All currents flowing into the microcontroller are defined as positive and all currents flowing out of it are defined as negative. Because of the internal pull-up transistor the direction of I_{RWL} is out of the device and therefore the sign in the current specification is negative.

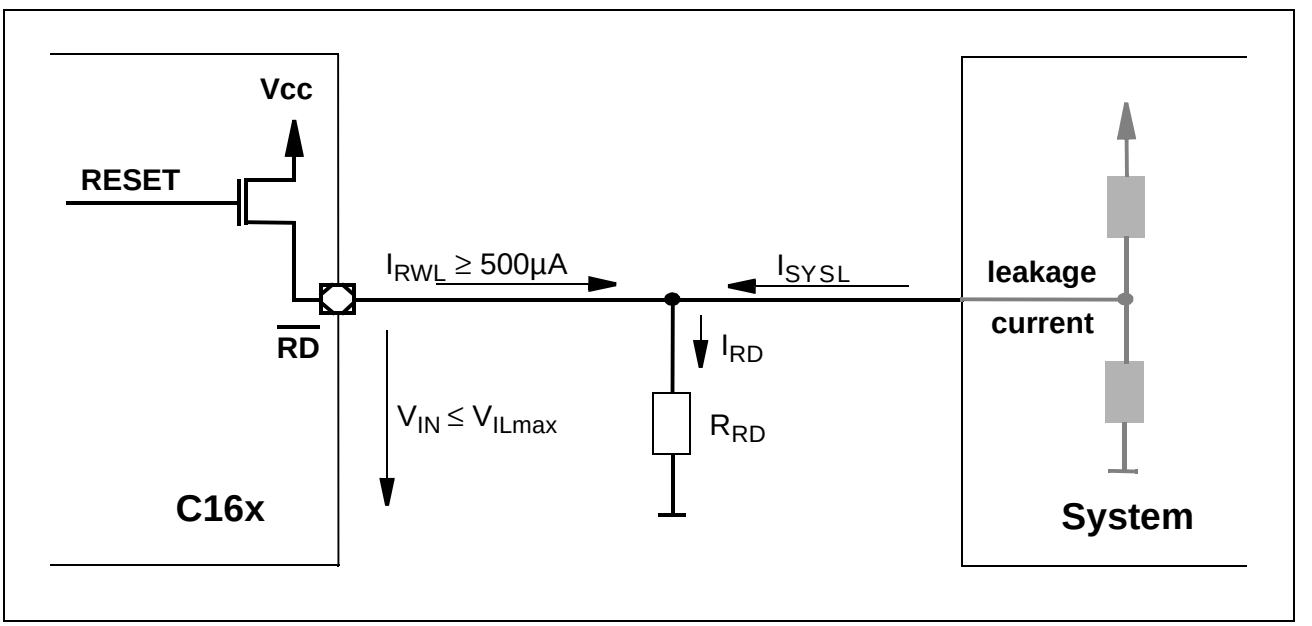


Figure 10 :
System Environment and Pull-down Resistor at Pin $\overline{RD}$ for BSL Entry

Current Specification in the Data Sheet:

Vcc	= 5V ± 10%	⇒	4.5V ≤ Vcc ≤ 5.5V
V_{ILmax}	= 0.2Vcc - 0.1V	⇒	0.8V ≤ V_{ILmax} ≤ 1.0V
I_{RWLmin}	= -500µA	⇒	I_{RWL} ≥ |-500µA|

Note: Worst case for calculation is in that case V_{ILmax} @ V_{DD} = 5.5V

Pull-down resistor calculation:

$$R_{RD} < \frac{V_{ILmax}}{I_{RD}} = \frac{V_{ILmax}}{I_{RWL} + I_{SYSL}}$$

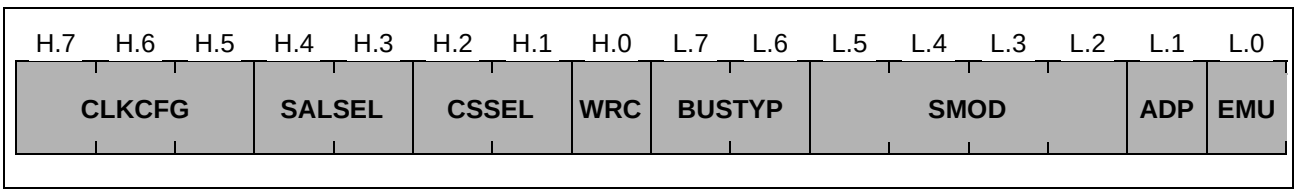
Example **without** system current:
(I_{SYSL} = 0 A)

$$R_{RD} < \frac{V_{ILmax}}{I_{RD}} = \frac{1.0V}{500\mu A}$$

The recommended maximum value: R_{RD} = 2000 Ω

5 Appendix

5.1 PORT0 Configuration during Reset



Pin	Mode	Comment
EMU	**Emulation Mode**	**Condition for EHM and Quality of P0H.7 is inverted**
ADP	**Adapt Mode**	
SMOD (P0L.5:2)	**Special Modes**	
0 0 0 0	reserved	do not use this combination
0 0 0 1	reserved	do not use this combination
0 0 1 0	reserved	do not use this combination
0 0 1 1	reserved	do not use this combination
0 1 0 0	reserved	do not use this combination
0 1 0 1	reserved	do not use this combination
0 1 1 0	reserved	do not use this combination
0 1 1 1	**External Host Mode (EHM)[1)]**	**requires Emulation Mode**
1 0 0 0	reserved	do not use this combination
1 0 0 1	reserved	do not use this combination
1 0 1 0	**Bootstrap Loader + CPU Host Mode[1)]**	**Serial OTP programming via BSL**
1 0 1 1	**Bootstrap Loader**	**Start from internal boot ROM**
1 1 0 0	reserved	do not use this combination
1 1 0 1	reserved	do not use this combination
1 1 1 0	**CPU Host Mode (CHM)[1)]**	**CPU programming mode for OTP**
1 1 1 1	**normal Start**	**normal start as defined by $\overline{EA}$ pin**

BUSTYP (P0L.7:6)	External Data Bus Width	External Address Bus Mode
0 0	8-bit Data	Demultiplexed Addresses
0 1	8-bit Data	Multiplexed Addresses
1 0	16-bit Data	Demultiplexed Addresses
1 1	16-bit Data	Multiplexed Addresses
WRC	**Write Configuration**	
CSSEL (P0H.2:1)	**Chip Select Lines**	
1 1	Max: $\overline{CSx}$...$\overline{CS0}$	Default without pull-downs
1 0	None	Port 6 pins free for IO
0 1	Two: $\overline{CS1}$...$\overline{CS0}$	
0 0	Three: $\overline{CS2}$...$\overline{CS0}$	
SALSEL (P0H.4:3)	**Segment Address Lines**	**Directly accessible Address Space**
1 1	Two: A17...A16	256 KByte (Default, without pull-downs)
1 0	Axx...A16	(Maximum)
0 1	None	64 KByte (Minimum)
0 0	Four: A19...A16	1 MByte
CLKCFG (P0H.7-5)	**CPU Frequency $f_{CPU} = f_{XTAL} * F$**	**Notes[2)]**
1 1 1	$f_{XTAL} * 4$	Default configuration
1 1 0	$f_{XTAL} * 3$	
1 0 1	$f_{XTAL} * 2$	
1 0 0	$f_{XTAL} * 5$	
0 1 1	$f_{XTAL} * 1$	Direct drive
0 1 0	$f_{XTAL} * 1.5$	
0 0 1	$f_{XTAL} / 2$	Prescaler
0 0 0	$f_{XTAL} * 2.5$	

[1)] This modes are not implemented in all devices. Please refer to the User's Manuals.

[2)] The clock configuration bits are not fully decoded in all devices and steps. Please use Appendix and the User's Manuals for detailed information.

5.2 Reset, Clock Options and Steps

Device	Step [1]	OWD [2]	PM [3]	BDRST	RSTCON	Clock Options [4]	PLL Factors (F)
C161RI	AA, BA, BB	==	yes	yes	no	0.5 / 1	no
C161V / K / O	AA, FA	==	no	no	no	0.5 / 1	no
C161OR	FA	$\overline{RD}$	yes	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C161PI	AA	$\overline{RD}$	yes	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C161CS/JC/JI-32F	AC, BC, CB	$\overline{RD}$	yes	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C161SI/CI-32F	AA,BA	$\overline{RD}$	yes	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C161CS-32R	AA	$\overline{RD}$	yes	yes	yes	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C163-L	AA, AB, AC	V_{PP}/OWE	no	no	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C163-16F	AA, AB, BA	V_{PP}/OWE	no	no	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C163-16F x	BB x, BC x	==	no	no	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C164CI-8E	BC, CA	$\overline{RD}$	yes	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C164CI-8R	AB	$\overline{RD}$	yes	yes	no[5]	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C164CH-8F	AA	$\overline{RD}$	yes	yes	yes	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C165	BB	==	no	no	no	0.5	no
	CA, FA	==	no	no	no	0.5 / 1	no
C167 -LM	AD, BA, BB, BC	==	no	no	no	0.5	no
C167CR-LM	AB	==	no	no	no	1 / PLL	4
	BA, BB, BE,	==	no	no	no	1 / PLL	2/3/4/5
	CB, DA, DB, FA	OWE	no	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C167CR-4RM	AA	V_{PP}/OWE	no	no	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
	AC, DA, DB, FA	V_{PP}/OWE	no	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C167CR-16FM	AC	==	no	no	no	1 / PLL	4
C167CR-16RM	AA	==	no	no	no	1 / PLL	2/3/4/5
	FA	OWE	no	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5

Device	Step [1]	OWD [2]	PM [3]	BDRST	RSTCON	Clock Options [4]	PLL Factors (F)
C167CS-32FM	AA,AB,AD,AE,CA,CB	$\overline{RD}$	yes	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C167CS-4RM	AA	$\overline{RD}$	yes	yes	yes	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C167S-4RM	AA	V_{PP}	no	no	no	1 / PLL	2/3/4/5
	BA, BB, FA	V_{PP}	no	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
C167SR-LM	AB	==	no	no	no	1 / PLL	4
	BA	==	no	no	no	1 / PLL	2/3/4/5
	FA	V_{PP}	no	yes	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5

1) The described options are implemented since the steps listed below.

2) The Oscillator Watchdog (OWD) can be disabled in different kinds.

== : No OWD implemented.

V_{PP}/OWE : A low level on pin V_{PP}/OWE disables the OWD.

OWE : A low level on pin OWE disables the OWD.

$\overline{RD}$: A low level on pin $\overline{RD}$ at the end of any type of reset disables the OWD. The level of $\overline{RD}$ is latched with the IRS. See figure (2 ... 7).

V_{PP} : A low level on pin V_{PP} disables the OWD.

3) Besides other features the Power Management (PM) includes the Slow Down Divider (SDD). A separate clock path can be selected for Slow Down operation bypassing the basic clock path used for standard operation. The programmable Slow Down Divider divides the oscillator frequency by a factor of 1 ... 32. In SDD mode the OWD has no effect.

4) Prescaler option : 0.5
Direct drive option : 1
The PLL clock is not used for prescaler option and direct drive option ($f_{CPU} = f_{OSC} * 0.5$) ($f_{CPU} = f_{OSC} * 1.0$).

5) In the first step of the C164CI-4RM or -8RM (32/64 Kbyte ROM version), as an intermediate solution, when pin $\overline{EA}$ = High during reset, the configuration is read from internal ROM address 00.003Eh instead of P0H.[7:0], and is copied into register RP0H. In this case, the status of PORT0 during reset is not evaluated. Register RSTCON is not implemented and during startup the content of ROM address 00.003Eh is used instead of the default configuration for single-chip mode reset.