Hardware User Manual

TCM-BF537 V1.4

BGA and Border Pad Versions

Tinyboards from Bluetechnix
www.bluetechnix.com

Contact

Bluetechnix Mechatronische Systeme GmbH

Waidhausenstr. 3/19
A-1140 Vienna
AUSTRIA/EUROPE
office@bluetechnix.at
http://www.bluetechnix.com

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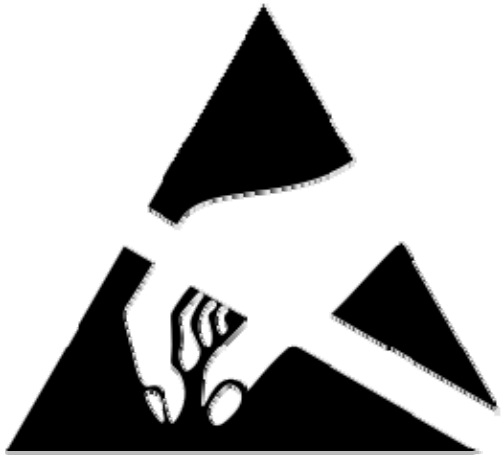
Warnings
Due to technical requirements components may contain dangerous substances.

The Core Modules and development systems contain ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused Core Modules and Development Boards should be stored in the protective shipping package.



BLACKFIN Products

Core Modules:

CM-BF533:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF533 processor; up to 600MHz, 32MB RAM, 2MB Flash, 120 pin expansion connector and a size of 36.5x31.5mm
CM-BF537E:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 600MHz, 32MB RAM, 4MB Flash, integrated TP10/100 Ethernet physical transceiver, 120 pin expansion connector and a size of 36.5x31.5mm
CM-BF537U:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 600MHz, 32MB RAM, 4MB Flash, integrated USB 2.0 Device, 120 pin expansion connector and a size of 36.5x31.5mm (will be replaced by CM-BF527).
TCM-BF537:	Blackfin Processor Module powered by Analog Devices single core ADSP-BF537 processor; up to 500MHz, 32MB RAM, 8MB Flash, 28x28mm, 120 pin expansion connector, Ball Grid Array or Border Pads for reflow soldering, industrial temperature range -40°C to +85°C.
CM-BF561:	Blackfin Processor Module powered by Analog Devices dual core ADSP-BF561 processor; up to 2x 600MHz, 64MB RAM, 8MB Flash, 120 pin expansion connector and a size of 36.5x31.5mm.
CM-BF527:	The new Blackfin Processor Module is powered by Analog Devices single core ADSP-BF527 processor; key features are USB OTG 2.0 and Ethernet. The 2x60 pin expansion connectors are backwards compatible with other Core Modules.
CM-BF548:	The new Blackfin Processor Module is powered by Analog Devices single core ADSP-BF548 processor; key features are 64MB DDR SD-RAM 2x100 pin expansion connectors.

Development Boards:

EVAL-BF5xx:	Low cost Blackfin processor Evaluation Board with one socket for any Bluetechnix Blackfin Core Module. Additional peripherals are available, such as an SD-Card.
DEV-BF5xxDA-Lite:	Get ready to program and debug Bluetechnix Core Modules with this tiny development platform including a USB Based Debug Agent. The DEV-BF5xxDA-Lite is a low cost starter development system including VDSP++ Evaluation Software License.

DEV-BF5xx-FPGA: Blackfin Development Board with two sockets for any combination of Blackfin Core Modules. Additional peripherals are available, such as SD-Card, Ethernet, USB host, multi-port JTAG including a USB based Debug Agent, connector for an LCD-TFT Display and connector for a digital camera system. A large on-board SPARTAN-3 FPGA and Soft IPs make this board the most flexible Blackfin development platforms ever developed.

DEV-BF548DA-Lite: Get ready to program and debug Bluetechnix CM-BF548 Core Module with this tiny development platform including a USB Based Debug Agent. The DEV-BF548DA-Lite is a low cost starter development system including VDSP++ Evaluation Software License.

EXT-Boards: The following Extender Boards are available: EXT-BF5xx-Audio, EXT-BF5xx-Video, EXT-BF5xx-Camera, EXT-BF5xx-Exp, EXT-BF5xx-ETH-USB, EXT-BF5xx-AD/DA. Additional boards based on customer request are also available.

Software Support:

BLACKSheep: The BLACKSheep VDK is a multithreaded framework for the Blackfin processor family from Analog Devices that includes driver support for a variety of hardware extensions. It is based on the real-time VDK kernel included within the VDSP++ development environment.

LabVIEW: LabVIEW embedded support for the CM-BF537E, CM-BF537U and TCM-BF537 Core Modules is based upon the BLACKSheep VDK driver Framework.

uClinux: All the Core Modules are fully supported by uClinux. The required boot loader and uClinux can be downloaded from: http://blackfin.uClinux.org.

Upcoming Products and Software Releases:

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BLACKFIN Design Service

Based on more than five years of experience with Blackfin, Bluetechnix offers development assistance as well as custom design services and software development.

1 Introduction

The TCM-BF537 is a chip size Core Module designed for industrial temperature range and volume production. It combines power supply, RAM and FLASH into a module as small as a chip package. Different connector options (Ball Grid Array (BGA), Border Pads (BP) and Connectors) provides solutions for all possible requirements.

1.1 Overview

The Core Module TCM-BF537 consists of the following components shown in Figure 1-1.

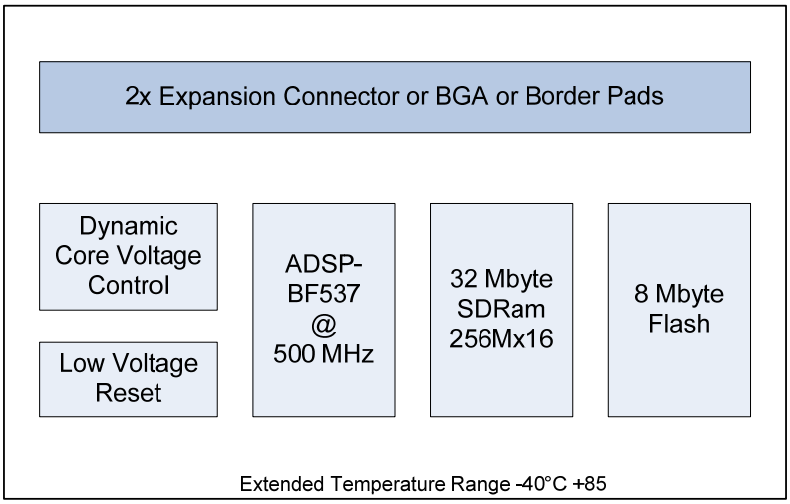

Figure 1-1: Main Components of the TCM-BF537 Core Module

- **Analog Devices Blackfin Processor BF537**
  - ADSP-BF537BBCZ-5A, 500MHz (-40°-85°C)
- **32 MB SDRAM**
  - SDRAM Clock up to 133MHz
  - MT48LC16M16A2BG-7 (16Mx16, 256Mbit at 3.3 V)
- **8 MB of Byte Addressable Flash**
  - PF48F2000P0ZBQ0S (32Mx16, at 3.3V; all 8MByte addressable, bottom boot)
  - Additional flash memory upon request: It can be connected through the expansion board as parallel flash using asynchronous chip select lines or as SPI flash.
- **Low Voltage Reset Circuit**
  - Resets module if power supply goes below 2.93V.

- **Dynamic Core Voltage Control**
    - Core voltage adjustable by setting software registers on the Blackfin processor
    - Core voltage range: 0.8 – 1.32V
- **Peripherals available on all Core Module versions**
    - Power Supply
    - SPORT 0
    - JTAG
    - UART0/Uart1
    - CAN
    - TWI (I2C compatible)
    - SPI (Serial Port Interface)
    - PPI (Parallel Port Interface)
    - Boot Mode Pins
    - GPIO's
- **Peripherals available on the Connector and BGA version only.**
    - Data Bus
    - Address Bus
    - Further GPIO's
    - Memory Control Signals

1.2 Versions

TCM-BF537: Connector Version 2x60 connector pins

TCM-BF537BGA: 169 BGAs 1.5 mm pitch for volume production

TCM-BF537BP: 76 Border Pads, no Data- and Address bus on border pads

1.3 Key Features

- The TCM-BF537, measuring only 28x28mm is the smallest core module available.
- An extended temperature range, suitable for industrial production.
- Allows integration on a two layer baseboard.
- Reduces development costs, fast time to market.
- Very cost effective for small and medium volumes

1.4 Target Applications

- Generic high performance signal processor module
- Industrial Automation

1.5 Further Information

Further information, and document updates are available on the product homepage: http://www.bluetechnix.com/goto/tcm-bf537

2 Specification

2.1 Functional Specification

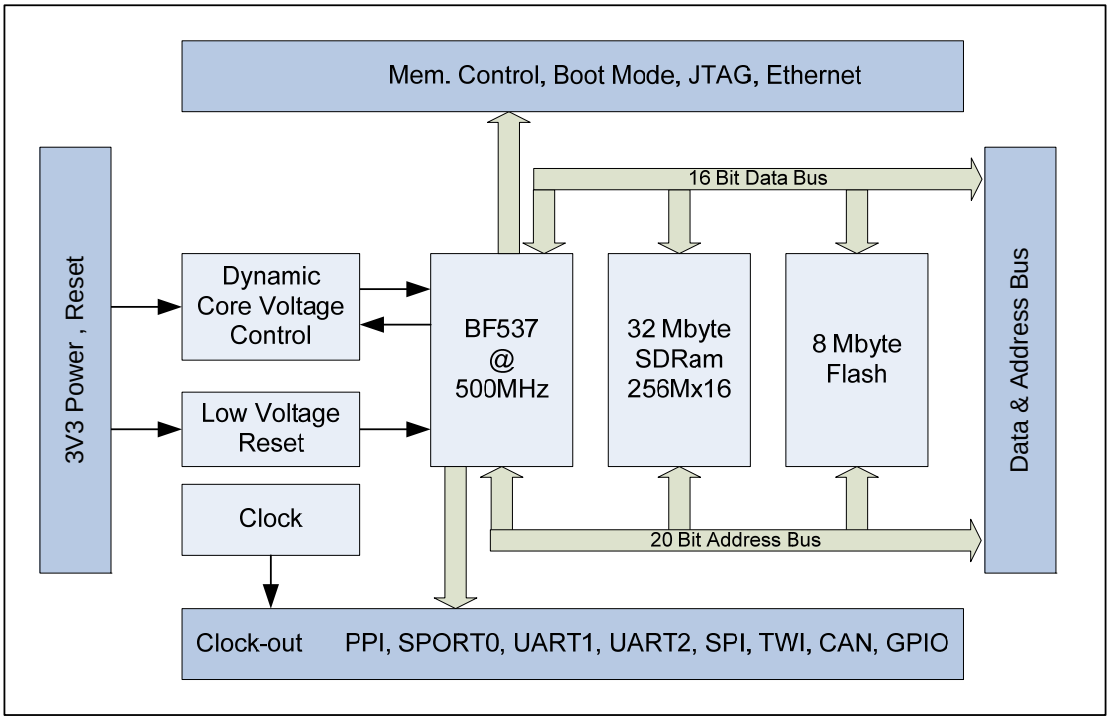

Figure 2-1: Detailed Block Diagram

Figure 2-1 shows a detailed block diagram of the TCM-BF537 module. Beside the SDRAM and a few other control pins, the TCM-BF537 has most pins of the Blackfin processor on its two 60 pin connectors, or its BGA, or its Border Pads.

Dynamic voltage control allows reducing power consumption to a minimum adjusting the core voltage and the clock frequency dynamically in accordance to the required processing power.
A low voltage reset circuit guarantees a power on reset and resets the system when the input voltage drops below 2.93V for at least 140ms.

2.2 Boot Mode

By default the boot mode = 000 (BMODE2 = Low, BMODE1 = Low, BMODE0=Low). All BMODE pins have on board pull down resistors.

Switch Settings BM3,BM2,BM1,BM0	Boot Mode	Description
0000	0	Execute from16Bit ext. mem. Bypass ROM
0001	1	Boot from 8Bit or 16Bit EEPROM/Flash
0010	2	Reserved
0011	3	Boot from serial SPI Memory
0100	4	Boot from SPI Host (slave mode)
0101	5	Boot from serial TWI memory
0110	6	Boot from TWI host
0111	7	Boot from UART host (slave mode)
1000	8	Execute from16Bit ext. mem. Bypass ROM
1001	9	Boot from 8Bit or 16Bit EEPROM/Flash
1010	10	Reserved
1011	11	Boot from serial SPI Memory
1100	12	Boot from SPI Host (slave mode)
1101	13	Boot from serial TWI memory
1110	14	Boot from TWI host
1111	15	Boot from UART host (slave mode)

Table 2-1: Boot Mode TCM-BF537

Connect BMODE0 to Vcc and leave BMODE1, BMODE2 pins open for Boot Mode 001 equals to 8 or 16 bit PROM/FLASH boot mode. This is the default boot mode for the Blacksheep software.

BMODE3 is tied to low, so all bootmodes 1XXX are not possible without hardware modification to the core module.

2.3 Core Module Memory MAP

Type	Start Address	End Address	Size	Comment	PF4	PF5
FLASH *)	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S	0	0
FLASH *)	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S	1	0
FLASH *)	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S	0	1
FLASH *)	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S	1	1
SD-RAM	0x00000000	0x01FFFFFF	32MB	16 Bit Bus Micron,MT48LC16M16A2FG		

Table 2-2: Memory Map

*) Be aware that you have to unlock the flash before starting an erase process!

2.3.1 Asynchronous Memory Banks

The maximum amount of memory addressable by a single asynchronous memory bank, of the Blackfin processor is 1MB. On this module, each 2MB segment of Flash is addressed over 2 asynchronous memory banks. In order to be able to use more than 2MB without using more than 2 banks, 2 GPIOs (PF4, PF5) are used to select which 2MB section of the FLASH is visible in the memory window of the Blackfin processor. This frees up the remaining banks for the user.

Aside from the first 2 async memory banks, which are used for FLASH addressing, the core module has 2 banks of the Asynchronous Memory interface available, these can be addressed through the following addresses:

Bank	Start Address	End Address	Size	Comment
0	0x20000000	0x200FFFFF	1MB	(Addresses FLASH)
1	0x20100000	0x201FFFFF	1MB	(Addresses FLASH)
2	0x20200000	0x202FFFFF	1MB	Use nAMS 1
3	0x20300000	0x203FFFFF	1MB	Use nAMS 2

These memory banks can be used to access various memory mapped devices or peripherals.

*There are 19 address lines (A1 to A19) (The A0 signal is produced through addressing logic on ABE0 and ABE1), this allows the entire 1MB to be addressable.

See section 5.6, Flash Memory Extension PINS.

2.4 Electrical Specification

2.4.1 Supply Voltage

- 3.3V DC +/-10%

2.4.2 Supply Voltage Ripple

- 100mV peak to peak 0-20 MHz

2.4.3 Input Clock Frequency

- 25MHz

  The Blackfin Processor Input Clock frequency is 25 MHz, this frequency is derived from the on-board crystal/oscillator and drives the Blackfin Processor's Clock generator. This frequency is also provided on the connector as pin 78 (CLKBUF).

2.4.4 Real Time Clock Crystal

- 32.768kHz

2.4.5 Supply Current

- Maximum current: 200mA at 3.3V
- Typical operating conditions at 25°C environment temperature:
  - Processor running at 500MHz, Core Voltage 1.2V, SDRAM 50% bandwidth utilization at 125MHz; 150mA at 3.3V
  - Processor running at 250MHz, Core Voltage 0.85V SDRAM 50% bandwidth utilization at 83,3MHz; ; Ethernet Idle: 85mA at 3.3V
  - Processor running at 600MHz, Core Voltage 1.2V, SDRAM 50% bandwidth utilization at 120MHz, 160mA at 3.3V

2.5 Environmental Specification

2.5.1 Temperature

- Operating at full 500MHz:: -40 to + 85° C

2.5.2 Humidity

Operating: 10% to 90% (non condensing)

3 TCM-BF537C (Connector Version)

3.1 Mechanical Outline

Figure 3-1 shows the top view of the Core Module. All dimensions are given in millimeters!

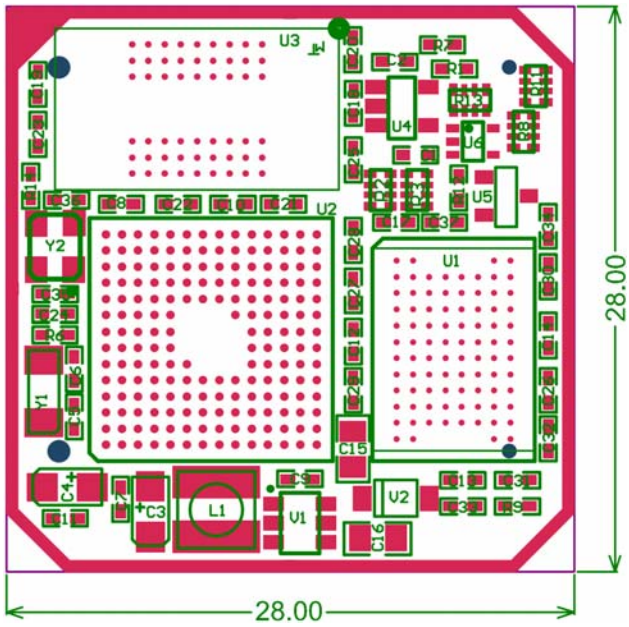

Figure 3-1: Mechanical Outline (**top view**)

Figure 3-2 shows the bottom view of the Core Module (connector version).

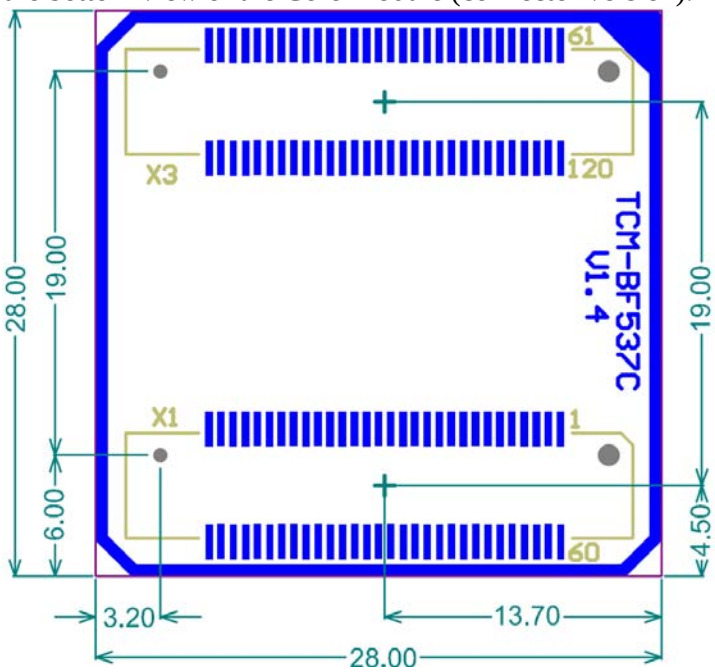

Figure 3-2: Mechanical Outline (**bottom view**)

Figure 3-3 shows a side view of the Core Module with mounted connectors.

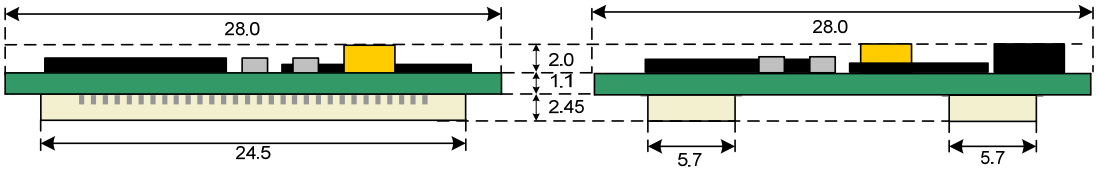

Figure 3-3: Side View with Connectors mounted

The total minimum mounting height including receptacle at the motherboard is 5.8mm.

3.2 Footprint

For the Connector version (2x Hirose 0.6mm pitch) the footprint for the base board looks like that as shown in Figure 3-4.

For the baseboard the following connectors have to be used.

Baseboard Part	Manufacturer	Manufacturer Part No.
X1, X2	Hirose	FX8-60S-SV

Table 3-1: Baseboard connector types

The Connectors on the TCM-BF537 are of the following type:

Part	Manufacturer	Manufacturer Part No.
X1, X2	Hirose 3mm height	FX8-60P-SV

Table 3-2: Core Module connector types

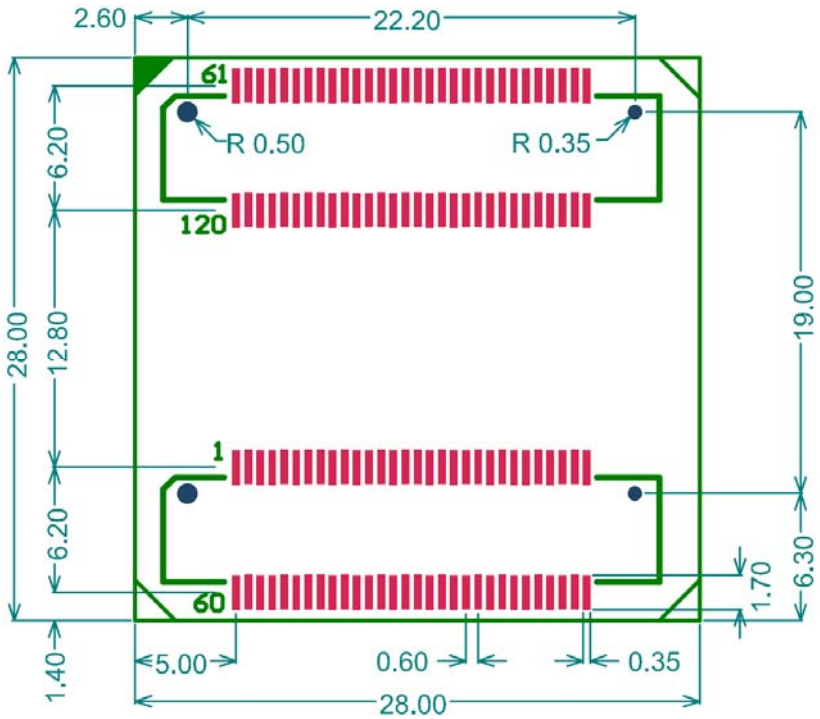

Figure 3-4: Recommended Footprint for Base Board (**top view**)

3.3 Schematic Symbol of Connector Version

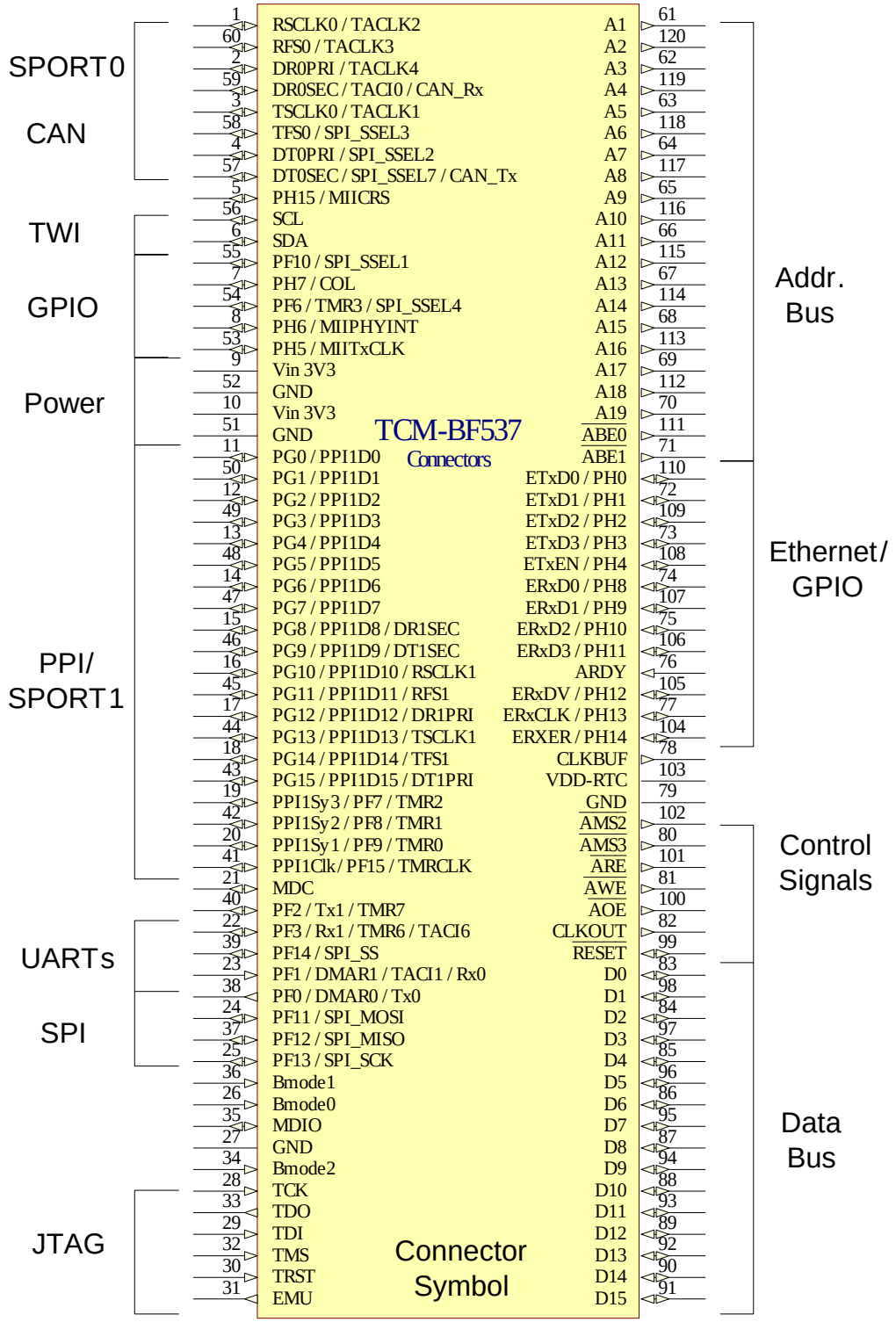

Figure 3-5: Schematics Symbol of Connector Version of the TCM-BF537

3.4 Connectors PIN Assignment

3.4.1 Connector X1 – (1-60)

Pin No.	Signal	Signal Type.
1	RSCLK0 / TACLK2	I/O
2	DR0PRI / SPI_SSEL2	O
3	TSCLK0 / TACLK1	I/O
4	DT0PRI / TACLK4	I
5	PH15 / MIICRS	I/O
6	SDA	I/O
7	PH7 / COL	I/O
8	PH6 / MIIPHYINT	I/O
9	Vin 3.3 V	PWR
10	Vin 3.3V	PWR
11	PG0 / PPI1D0	I/O
12	PG2 / PPI1D2	I/O
13	PG4 / PPI1D4	I/O
14	PG6 / PPI1D6	I/O
15	PG8 / PPID8 / DR1SEC	I/O
16	PG10 / PPI1D10 / RSCLK1	I/O
17	PG12 / PPI1D12 / RE1PRI	I/O
18	PG14 / PPI1D14 / TFS1	I/O
19	PPI1SY3/PF7/TMR2	I/O
20	PPI1SY1/PF8/TMR0	I/O
21	MDC	I/O
22	PF3 / Rx1 / TMR6 / TACI6	I/O
23	PF1 / DMAR1 / TACI1 / Rx0	I/O
24	PF11 / SPI_MOSI	I/O
25	PF13 / SPI_SCK	I/O
26	BMODE0	I – 10k pull down
27	GND	PWR
28	TCK	I – 10k pull up
29	TDI	I – 10k pull up
30	$\overline{\text{TRST}}$	I – 4k7 pull down
31	$\overline{\text{EMU}}$	O
32	TMS	I – 10k pull up
33	TDO	O
34	BMODE2	I – 10k pull down
35	MDIO	I/O – 10k pull up
36	BMODE1	I – 10k pull down
37	PF12 / SPI_MISO	I/O
38	PF0 / DMAR0 / Tx0	I/O
39	PF14 / SPI_SS	I/O
40	PF2 / Tx1 / TMR7	I/O
41	PPI1Clk / PF15 / TMRCLK	I/O
42	PPI1Sy2 / PF8 / TMR1	I/O
43	PG15 / PPI1D15 / DT1PRI	I/O

44	PG13 / PPI1D13 / TSCLK1	I/O
45	PG11 / PPI1D11 / RFS1	I/O
46	PG9 / PPI1D9 / TD1SEC	I/O
47	PG7 / PPI1D7	I/O
48	PG5 / PPI1D5	I/O
49	PG3 / PPI1D3	I/O
50	PG1 / PPI1D1	I/O
51	GND	PWR
52	GND	PWR
53	PH5 / MIITxCLK	I/O
54	PF6 / TMR3 / SPI_SSEL4	I/O
55	PF10 / SPI_SSEL1	I
56	SCL	I/O
57	DT0SEC / CANTX / SPI_SSEL7	O
58	TFS0	I/O
59	DR0SEC / TACI0 / CANRX	I
60	RFS0 / TACLK3	I/O

Table 3-3: Connector X1 pin assignment

Signal names correspond to those of the Blackfin processor unless otherwise stated.

NOTE: The processor pins PF4 and PF5 are used for flash addressing on the Core Module. They are not available on the connectors.

3.4.2 Connector X2 – (61-120)

Pin No.	Signal	Signal Type.
61	A1	O
62	A3	O
63	A5	O
64	A7	O
65	A9	O
66	A11	O
67	A13	O
68	A15	O
69	A17	O
70	A19	O
71	$\overline{ABE1}$ / SDQM1	O
72	PH1/ETxD1	I/O
73	PH3/ETxD3	I/O
74	PH8/ERxD0	I/O
75	PH10/ERxD2	I/O
76	ADRY	I – 10k pull up
77	PH13/ERxCLK	I/O
78	CLKBUF	O
79	GND	PWR
80	$\overline{AMS3}$	O
81	$\overline{AWE}$	O

82	CLKOUT (SCLK)	I
83	D0	I/O
84	D2	I/O
85	D4	I/O
86	D6	I/O
87	D8	I/O
88	D10	I/O
89	D12	I/O
90	D14	I/O
91	D15	I/O
92	D13	I/O
93	D11	I/O
94	D9	I/O
95	D7	I/O
96	D5	I/O
97	D3	I/O
98	D1	I/O
99	$\overline{\text{Reset}}$	I - see chapter 4.9
100	$\overline{\text{AOE}}$	O
101	$\overline{\text{ARE}}$	O
102	$\overline{\text{AMS2}}$	O
103	VDD-RTC	PWR
104	PH14/ERXER	I/O
105	PH12/ERxDV	I/O
106	PH11/ERxD3	PWR
107	PH9/ERxD1	I/O
108	PH4/ETxEN	I/O
109	PH2/ETxD2	I/O
110	PH0/ETxD0	I/O
111	$\overline{\text{ABE0}}$/ SDQM0	O
112	A18	O
113	A16	O
114	A14	O
115	A12	O
116	A10	O
117	A8	O
118	A6	O
119	A4	O
120	A2	O

Table 3-4: Connector X2 pin assignment

Signal names correspond to those of the Blackfin processor unless otherwise stated.

4 TCM-BF537B (Border Pad and BGA Versions)

4.1 Mechanical Outline

The two figures below shows the top and bottom view of the Core Module. All dimensions are given in millimeters!

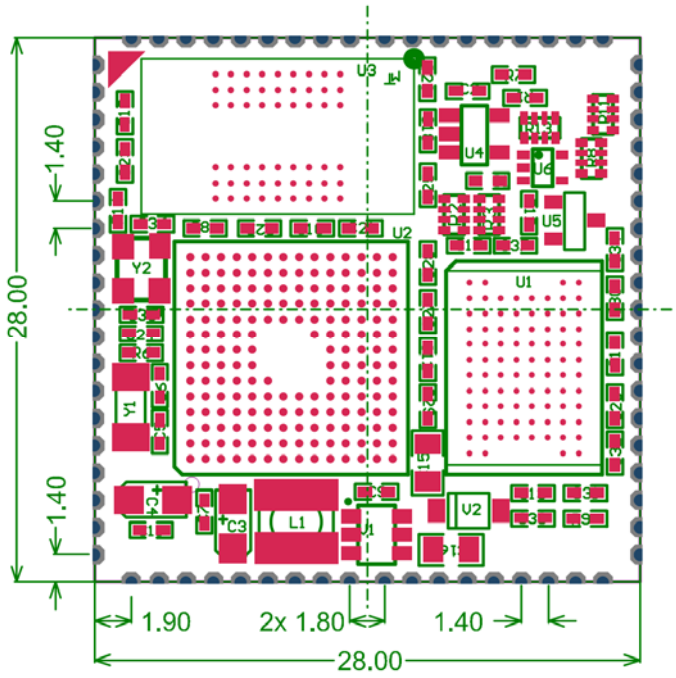

Figure 4-1: Mechanical Outline (**top view**)

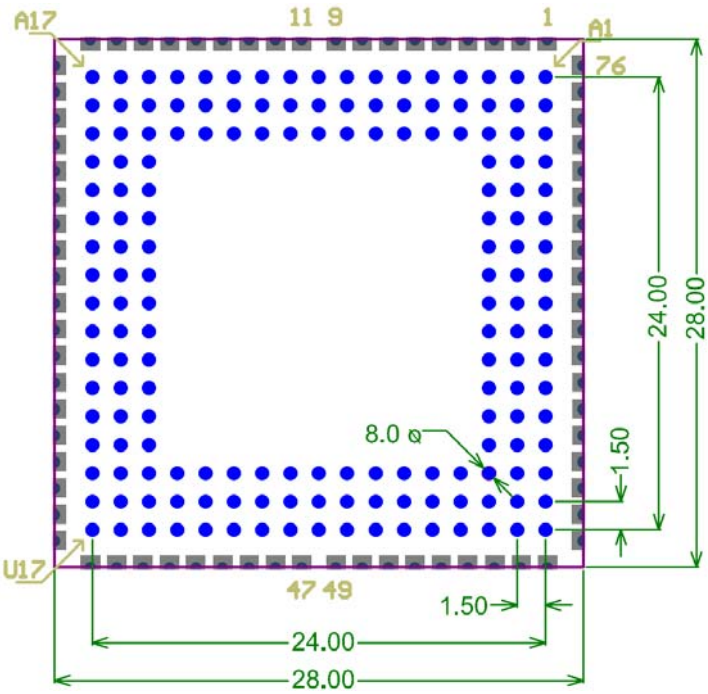

Figure 4-2: Mechanical Outline (**bottom view**)

Figure 4-3 shows a side view of the Core Module with border pads.

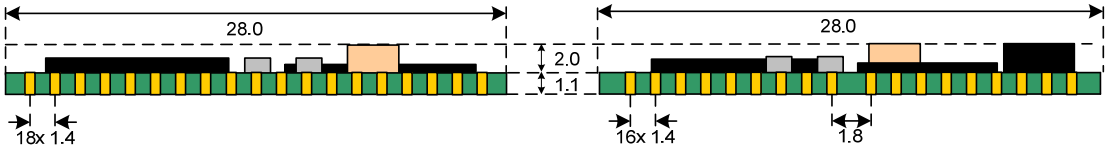

Figure 4-3: Side View of the Border Pads

The total minimum mounting height of the Border Pad version is only 3.1mm!

4.2 Footprint of Border Pad Baseboard

Figure 4-4 shows the pin assignment of the Border Pad Version. The pin Numbering is clockwise ascending. The Pins No. 10 and 48 are not present.

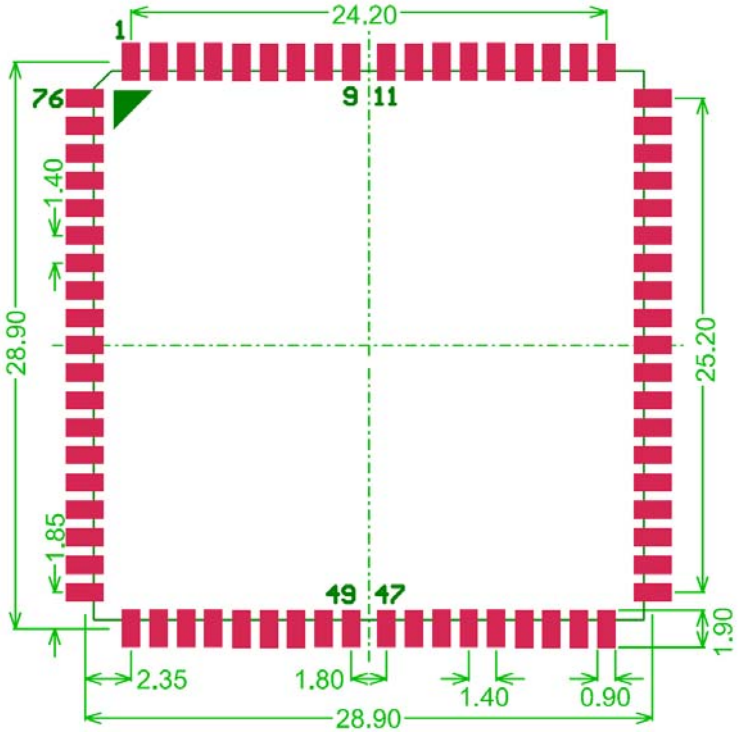

Figure 4-4: Border Pad Footprint for the Base Board (**top view**)

Note: Conducting paths and vias within the footprint must be **solder resistant**. Do not place any component within the footprint either.

4.3 Schematic Symbol of Border Pad Version

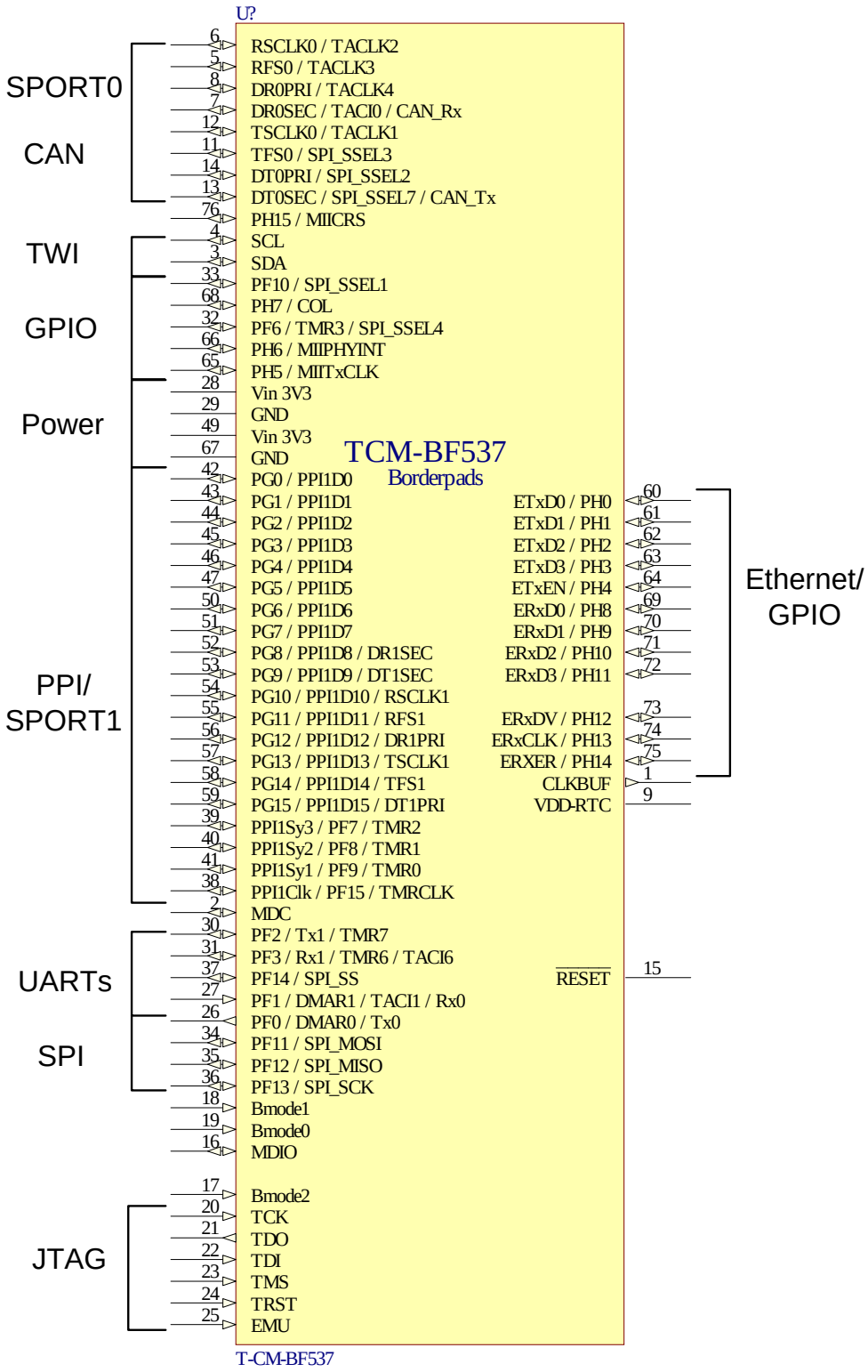

Figure 4-5: Schematics of the Border Pad Version of the TCM-BF537BP

4.4 Border Pad Pin Assignment

Pin No.	Signal	Type
1	CLKBUF	O
2	MDC	O
3	SDA	I/O
4	SCL	I/O
5	RFS0 / TACLK3	I/O
6	RSCLK0 / TACLK2	I/O
7	DR0SEC / TACI0 / CAN_Rx	I
8	DR0PRI / TACLK4	I
9	VDD-RTC	PWR
10	not available	
11	TFS0 / SPI_SSEL3	I/O
12	TSCLK0 / TACLK1	I/O
13	DT0SEC / SPI_SSEL7 / CAN_Tx	O
14	DT0PRI / SPI_SSEL2	O
15	$\overline{\text{RESET}}$	I – see chapter 4.9
16	MDIO	I/O – 10k pull up
17	BMODE2	I – 10k pull down
18	BMODE1	I – 10k pull down
19	BMODE0	I – 10k pull down
20	TCK	I – 10k pull up
21	TDO	O
22	TDI	I – 10k pull up
23	TMS	I – 10k pull up
24	$\overline{\text{TRST}}$	I – 4k7 pull down
25	EMU	O
26	PF0 / DMAR0 / Tx0	I/O
27	PF1 / DMAR1 / TACI1 / Rx0	I/O
28	Vin 3.3V	PWR
29	GND	PWR
30	PF2 / Tx1 / TMR7	I/O
31	PF3 / Rx1 / TMR6 / TACI6	I/O
32	PF6 / TMR3 / SPI_SSEL4	I/O
33	PF10 / SPI_SSEL1	I/O
34	PF11 / SPI_MOSI	I/O
35	PF12 / SPI_MISO	I/O
36	PF13 / SPI_SCK	I/O
37	PF14 / SPI_SS	I/O
38	PPI1Clk / PF15 / TMRCLK	I/O
39	PPI1Sy3 / PF7 / TMR2	I/O
40	PPI1Sy2 / PF8 / TMR1	I/O
41	PPI1Sy1 / PF9 / TMR0	I/O
42	PG0 / PPI1D0	I/O
43	PG1 / PPI1D1	I/O
44	PG2 / PPI1D2	I/O
45	PG3 / PPI1D3	I/O

46	PG4 / PPI1D4	I/O
47	PG5 / PPI1D5	I/O
48	not present	-
49	Vin 3.3V	PWR
50	PG6 / PPI1D6	I/O
51	PG7 / PPI1D7	I/O
52	PG8 / PPI1D8 / DR1SEC	I/O
53	PG9 / PPI1D9 / DT1SEC	I/O
54	PG10 / PPI1D10 / RSCLK1	I/O
55	PG11 / PPI1D11 / RFS1	I/O
56	PG12 / PPI1D12 / DR1PRI	I/O
57	PG13 / PPI1D13 / TSCLK1	I/O
58	PG14 / PPI1D14 / TFS1	I/O
59	PG15 / PPI1D15 / DT1PRI	I/O
60	PH0 / ETxD0	I/O
61	PH1 / ETxD1	I/O
62	PH2 / ETxD2	I/O
63	PH3 / ETxD3	I/O
64	PH4 / ETxEN	I/O
65	PH5 / MIITxCLK	I/O
66	PH6 / MIIPHYINT	I/O
67	GND	PWR
68	PH7 / COL	I/O
69	PH8 / ERxD0	I/O
70	PH9 / ERxD1	I/O
71	PH10 / ERxD2	I/O
72	PH11 / ERxD3	I/O
73	PH12 / ERxDV	I/O
74	PH13 / ERxCLK	I/O
75	PH14 / ERXER	I/O
76	PH15 / MIICRS	I/O

Table 4-1: Border pin assignment

Signal names correspond to those of the Blackfin processor unless otherwise stated.

4.5 BGA PAD Numbering

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17
D1	D2	D3												D15	D16	D17
E1	E2	E3												E15	E16	E17
F1	F2	F3												F15	F16	F17
G1	G2	G3												G15	G16	G17
H1	H2	H3												H15	H16	H17
J1	J2	J3												J15	J16	J17
K1	K2	K3												K15	K16	K17
L1	L2	L3												L15	L16	L17
M1	M2	M3												M15	M16	M17
N1	N2	N3												N15	N16	N17
P1	P2	P3												P15	P16	P17
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17
U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17

Figure 4-6: BGA Pad Numbering (**top view**)

4.6 Footprint of BGA Baseboard

Figure 4-7 shows the top view of the BGA footprint for your base board.

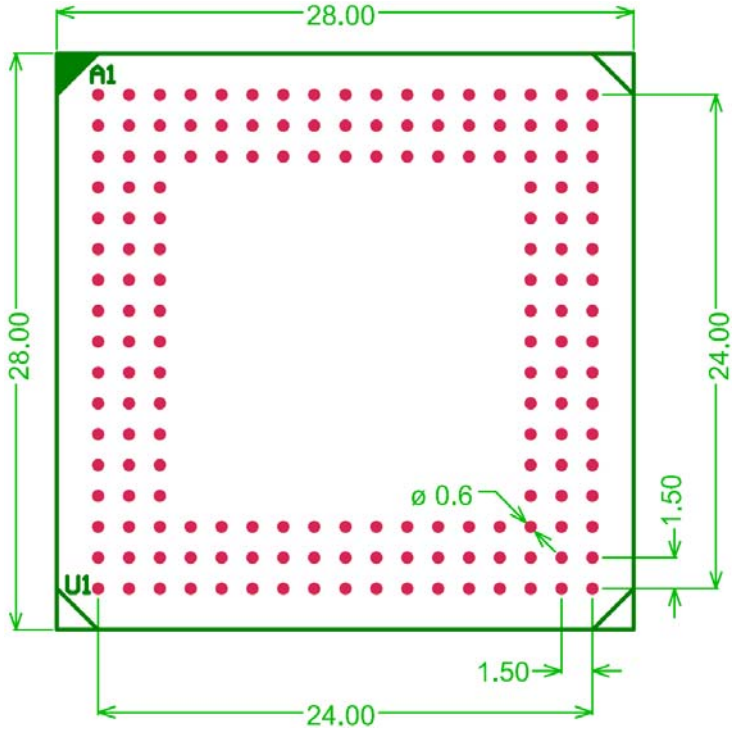

Figure 4-7: Recommended BGA Footprint for the Base Board (**top view**)

4.7 Schematic Symbol of BGA Version

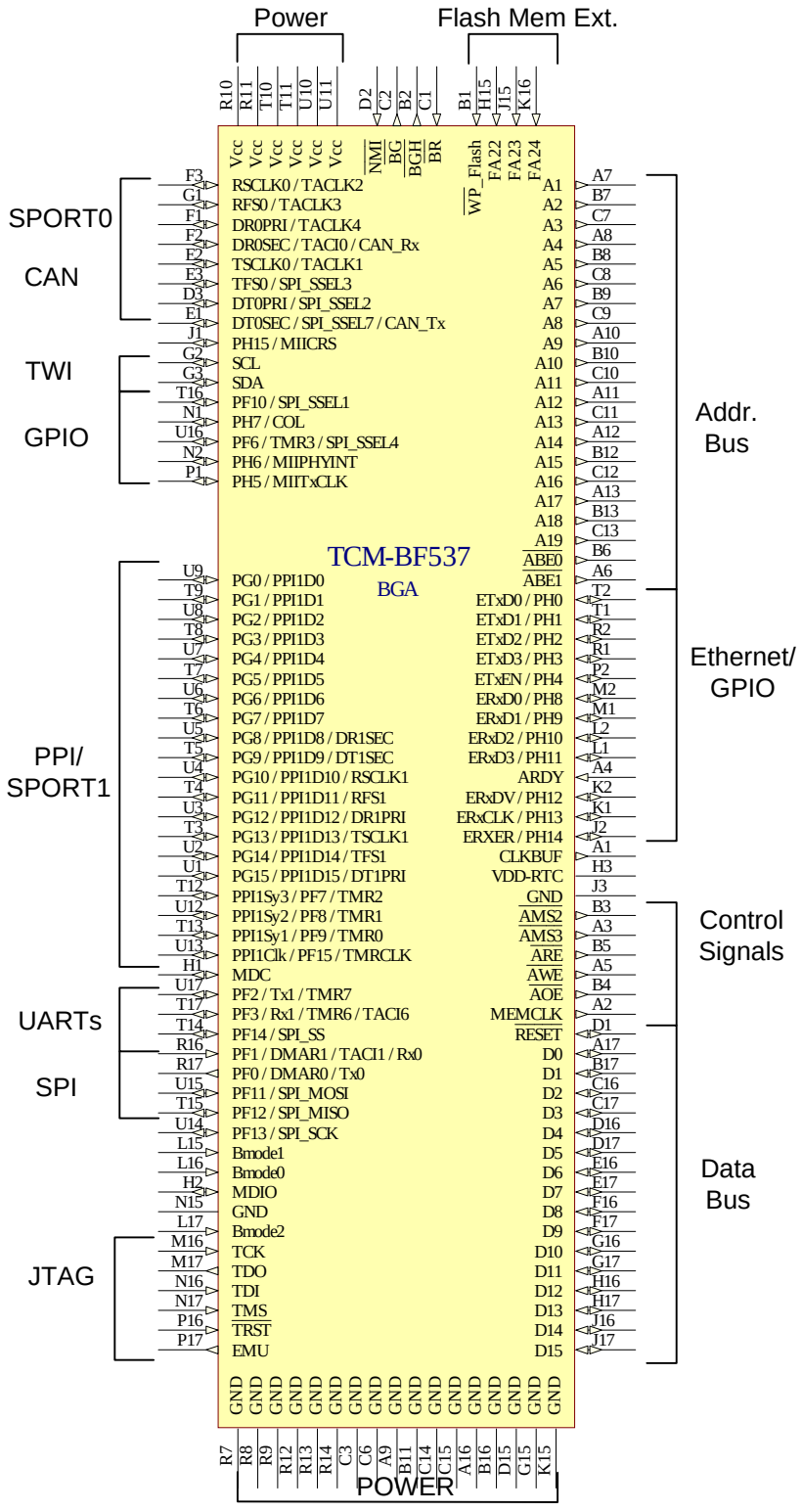

Figure 4-8: Schematics Symbol of the BGA Version of the TCM-BF537BGA

4.8 BGA Pin Assignment

Pin No.	Signal	Signal Type.
A1	CLKBUF	O
A2	MEMCLK	O
A3	$\overline{\text{AMS3}}$	O
A4	ARDY	I – 10k pull up
A5	$\overline{\text{AWE}}$	O
A6	$\overline{\text{ABE1}}$	O
A7	A1	O
A8	A4	O
A9	GND	PWR
A10	A9	O
A11	A12	O
A12	A14	O
A13	A17	O
A14	n.c.	-
A15	n.c.	-
A16	GND	PWR
A17	D0	I/O
B1	$\overline{\text{WP\_Flash}}$	I – 10k pull up
B2	$\overline{\text{BGH}}$	O
B3	$\overline{\text{AMS2}}$	O
B4	$\overline{\text{AOE}}$	O
B5	$\overline{\text{ARE}}$	O
B6	$\overline{\text{ABE0}}$	O
B7	A2	O
B8	A5	O
B9	A7	O
B10	A10	O
B11	GND	PWR
B12	A15	O
B13	A18	O
B14	n.c.	-
B15	n.c.	-
B16	GND	PWR
B17	D1	I/O
C1	$\overline{\text{BR}}$	I – 10k pull up
C2	$\overline{\text{BG}}$	O
C3	GND	PWR
C4	n.c.	-
C5	n.c.	-
C6	GND	PWR
C7	A3	O
C8	A6	O
C9	A8	O
C10	A11	O
C11	A13	O

C12	A16	O
C13	A19	O
C14	GND	PWR
C15	GND	PWR
C16	D2	I/O
C17	D3	I/O
D1	$\overline{\text{Reset}}$	I – see chapter 4.9
D2	$\overline{\text{NMI}}$	I – 10k pull up
D3	DT0PRI / SPI_SSEL2	O
D15	GND	PWR
D16	D4	I/O
D17	D5	I/O
E1	DT0SEC / CANTX / SPI_SSEL7	O
E2	TSCLK0 / TACLK1	I/O
E3	TFS0 / SPI_SSEL3	I/O
E15	n.c.	-
E16	D6	I/O
E17	D7	I/O
F1	DR0PRI / TACLK4	I
F2	DR0SEC / TACI0 / CANRX	I
F3	RSCLK0 / TACLK2	I/O
F15	n.c.	-
F16	D8	I/O
F17	D9	I/O
G1	RFS0 / TACLK3	I/O
G2	SCL	I/O
G3	SDA	I/O
G15	GND	PWR
G16	D10	I/O
G17	D11	I/O
H1	MDC	I/O
H2	MDIO	I/O – 10k pull up
H3	VDD-RTC	PWR
H15	FA22	I – 10k pull down
H16	D12	I/O
H17	D13	I/O
J1	PH15 / MIICRS	I/O
J2	PH14 / ERXER	I/O
J3	GND	PWR
J15	FA23	I – 10k pull down
J16	D14	I/O
J17	D15	I/O
K1	PH13 / ERxCLK	I/O
K2	PH12 / ERxDV	I/O
K3	n.c.	-
K15	GND	PWR
K16	FA24	I – 10k pull down
K17	n.c.	-
L1	PH11 / ERxD3	PWR

L2	PH10 / ERxD2	I/O
L3	n.c.	-
L15	BMODE1	I – 10k pull down
L16	BMODE0	I – 10k pull down
L17	BMODE2	I – 10k pull down
M1	PH9 / ERxD1	I/O
M2	PH8 / ERxD0	I/O
M3	n.c.	-
M15	n.c.	-
M16	TCK	I – 10k pull up
M17	TDO	O
N1	PH7 / COL	I/O
N2	PH6 / MIIPHYINT	I/O
N3	n.c.	-
N15	GND	PWR
N16	TDI	I – 10k pull up
N17	TMS	I – 10k pull up
P1	PH5 / MIITxCLK	I/O
P2	PH4 / ETxEN	I/O
P3	n.c.	-
P15	n.c.	-
P16	$\overline{\text{TRST}}$	I – 4k7 pull down
P17	EMU	O
R1	PH3 / ETxD3	I/O
R2	PH2 / ETxD2	I/O
R3	n.c.	-
R4	n.c.	-
R5	n.c.	-
R6	n.c.	-
R7	GND	PWR
R8	GND	PWR
R9	GND	PWR
R10	Vcc	PWR
R11	Vcc	PWR
R12	GND	PWR
R13	GND	PWR
R14	GND	PWR
R15	n.c.	-
R16	PF1 / DMAR1 / TACI1 / Rx0	I/O
R17	PF0 / DMAR0 / Tx0	I/O
T1	PH1 / ETxD1	I/O
T2	PH0 / ETxD0	I/O
T3	PG13 / PPI1D13 / TSCLK1	I/O
T4	PG11 / PPI1D11 / RFS1	I/O
T5	PG9 / PPI1D9 / DT1SEC	I/O
T6	PG7 / PPI1D7	I/O
T7	PG5 / PPI1D5	I/O
T8	PG3 / PPI1D3	I/O
T9	PG1 / PPI1D1	I/O

T10	Vcc	PWR
T11	Vcc	PWR
T12	PF7 / PPI1SY3 / TMR2	I/O
T13	PF9 / PPI1SY1 / TMR0	I/O
T14	PF14 / SPI_SS	I/O
T15	PF12 / SPI_MISO	I/O
T16	PF10 / SPI_SSEL1	I/O
T17	PF3 / Rx1 / TMR6 / TACI6	I/O
U1	PG15 / PPI1D15 / DT1PRI	I/O
U2	PG14 / PPI1D14 / TFS1	I/O
U3	PG12 / PPI1D12 / DR1PRI	I/O
U4	PG10 / PPI1D10 / RSCLK1	I/O
U5	PG8 / PPI1D8 / DR1SEC	I/O
U6	PG6 / PPI1D6	I/O
U7	PG4 / PPI1D4	I/O
U8	PG2 / PPI1D2	I/O
U9	PG0 / PPI1D0	I/O
U10	Vcc	I/O
U11	Vcc	I/O
U12	PF8 / PPI1_SY2 / TMR1	I/O
U13	PF15 / PPI1CLK / TMRCLK	I/O
U14	PF13 / SPI_SCLK	I/O
U15	PF11 / SPI_MOSI	I/O
U16	PF6 / TMR3 / SPI_SSEL4	I/O
U17	PF2 / Tx1 / TMR7	I/O

Table 4-2: BGA Version Pin Assignment

Signal names correspond to those of the Blackfin processor unless otherwise stated.

4.9 Reset circuit

The reset of the flash and the processor are connected to a power monitoring IC. The output can be used as power on reset for external devices, see Figure 4-9.

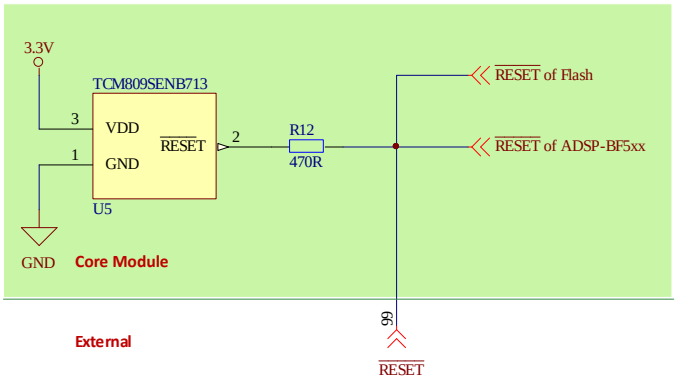

Figure 4-9: Schematic of reset circuit on the Core Module

4.10 Flash Memory Extension PINS

4.10.1 PINS FA20 and FA21

These pins are the Address lines A20 (PF4) and A21 (PF5) of the Intel P30 Flash and are pulled down by default.

4.10.2 WP_FLASH

Is pulled high by default so flash is unprotected. To write protect the flash connect this pin to GND.

5 Application Example Schematics

In the following two examples connection of a Physical Ethernet chip and a USB 2.0 chip to the Core Module are provided.

5.1 Schematic Example for Connecting a Physical Ethernet Chip

Since the ADSP-BF537 Blackfin Chip from Analog Devices already has Ethernet functionality only a physical Ethernet chip needs to be connected to the TCM-BF537 Core Module in order to make use of this feature.

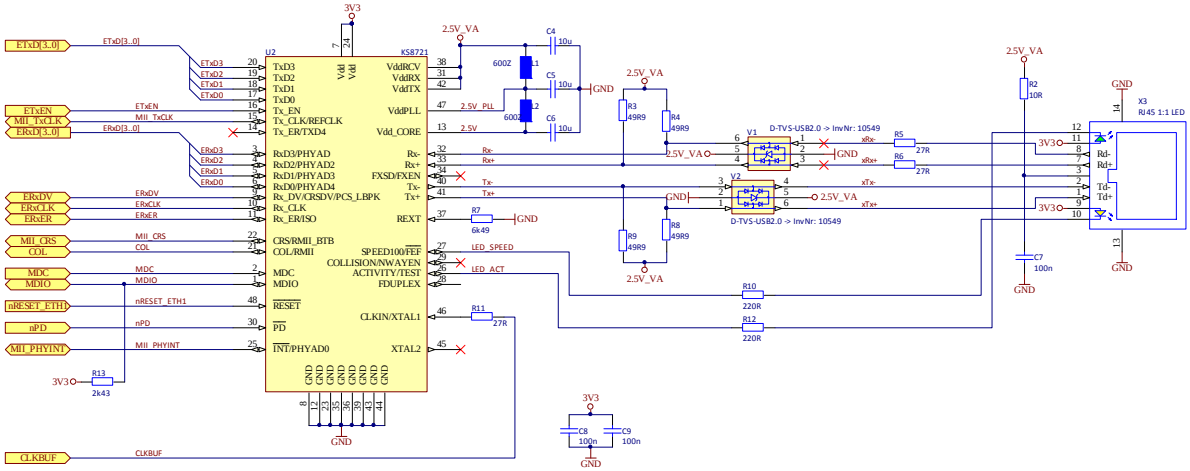

Figure 5-1: Configuration with Physical Chip

Designator	Value	Part Number	Description	Quantity
C4, C5, C6	10u	C0805C106K9PAC	Capacitor non-polarized	3
C7, C8, C9	100n	2238 246 19876	Capacitor non-polarized	3
L1, L2	600Z	74279265	Ferrite	2
R2	10R	MC 0.063W 0603 1% 10R	Resistor	1
R3, R4, R8, R9	49R9	MC 0.063W 0603 1% 49R9	Resistor	4
R5, R6, R11	27R	MC 0.063W 0603 1% 27R	Resistor	3
R7	6k49	MC 0.063W 0603 1% 6K49	Resistor	1
R10, R12	220R	MC 0.063W 0603 1% 220R	Resistor	2
R13	2k43	MULTICOMP	Resistor	1
U2		KSZ8721BLI-LQFP48L	10/100BASE Physical Layer Transceiver	1
V1, V2		USBLC6-2P6	TSV-Diode for USB 2.0	2
X3		RJLBC-060TC1	RJ45-Connector with LEDs	1

Table 5-1: Bill of Material of Sample Schematic

5.2 Schematic Example for Connecting a USB 2.0 Chip

The following example shows how to connect a USB 2.0 chip to the TCM-BF537 core Module.

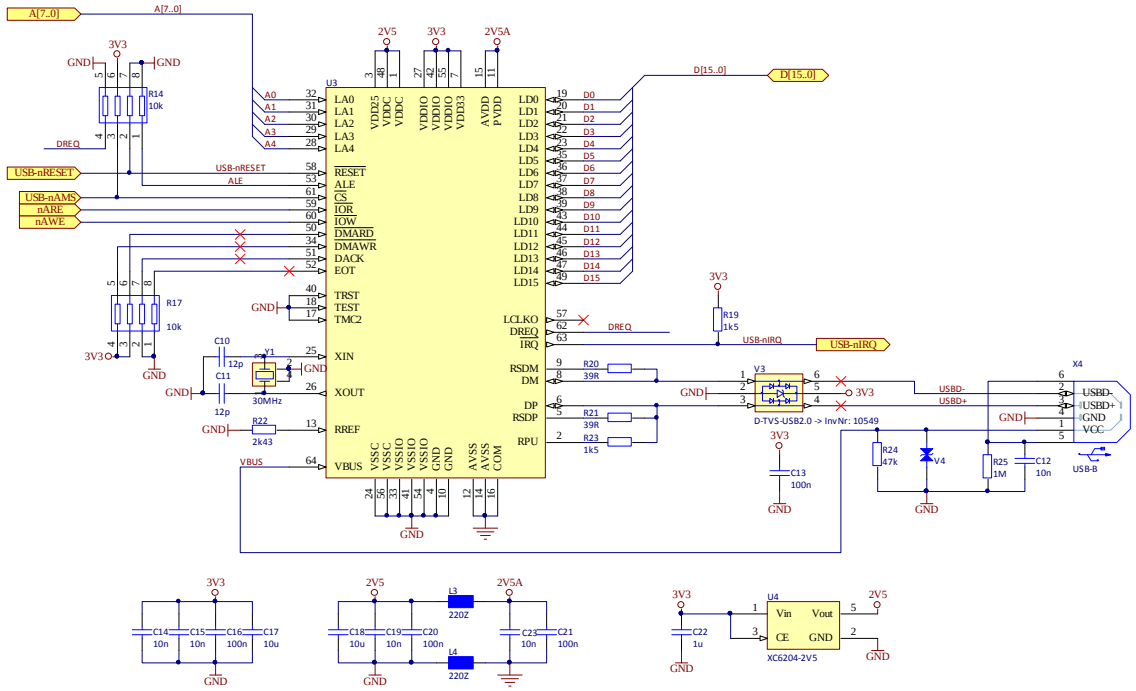

Figure 5-2: Configuration with USB 2.0 Chip

Designator	Value	Part Number	Description	Quantity
C1u, C2u	12p	2238 867 15129	Capacitor non-polarized	2
C3u, C4u, C5u, C9u, C11u	10n	2238 916 15636	Capacitor non-polarized	5
C6u, C10u, C12u	100n	2238 246 19876	Capacitor non-polarized	3
C7u, C8u	10u	C0805C106K9PAC	Capacitor non-polarized	2
L1u, L2u	220R	74279263	Ferrite	2
R1u, R3u, R11u, R12u	10k	MC 0.063W 0603 1% 10K	Resistor	4
R2u	10k	2350 025 11003	4-Resistor Array	1
R4u	1k	MC 0.063W 0603 1% 1k	Resistor	1
R5u, R6u	39R	MC 0.0654W 0603 1% 39R	Resistor	2
R7u	2k43	MULTICOMP	Resistor	1
R8u	1k5	MC 0.063W 0603 1% 1K5	Resistor	1
R9u	47k	MC 0.063W 0603 1% 47k	Resistor	1
R10u	1M	MC 0.063W 0603 1% 1M	Resistor	1
U1u		NET2272REV1A-LF	USB 2.0 Peripheral Controller TQPF	1
V1u		CDS3C05GTA		1
X1u		2411 01	USB-Device Normal	1
Y1u		Q 30.0-JXS32-12-10/20	Crystal Oscillator	1

Table 5-2: Bill of Material of Sample Schematic

6 Software Support

6.1 BLACKSheep

The Core Module is delivered with a pre-flashed basic version of the BLACKSheep VDK multithreaded framework. It contains a boot-loader for flashing the Core Module via the serial port.

Please consult the software development documents.

6.2 uClinux

The Core Module is fully supported by the open source platform at http://blackfin.uclinux.org. Since the Core Modules are pre-flashed with BLACKSheep you have to flash uBoot first. To flash uBoot you can use the BLACKSheep boot-loader.

To use the Ethernet functionality of the TCM-BF537 Core Modules you need the EXT-BF5xx-ETH-USB Blackfin Extension Board.

7 Anomalies

For the latest information regarding anomalies for this product, please consult the product home page:

http://www.bluetechnix.com/goto/tcm-bf537

Date	Revisions	Description
24.10.2007	V1.1 V1.2 V1.3	RTC-Problem: The Clock accuracy of the RTC is much less than specified by the crystal (20ppm). Due to layout issues the measured inaccuracy is about 7-9 sec. / Hour. The RTC Bug affects both the BGA and Border Pad Versions. For accurate time measurements please use the main crystal or an external RTC.

Table 8-1: Anomalies

8 Production Report

8.1 TCM-BF537 (100-1225)

Version	Component	Type
V1.4.1	Processor	ADSP-BF537 BBCZ-5A 1.0.2
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F2000P0XBQ0
V1.3.5	Processor	ADSP-BF537 BBCZ-5A 1.0.2
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F2000P0XBQ0
V1.3	Processor	ADSP-BF537 BBCZ-5A 1.0.2
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F2000P0ZBQ0

Table 9-1: Production Report TCM-BF537

8.2 TCM-BF537B (100-1226)

Version	Component	Type
V1.4.1	Processor	ADSP-BF537 BBCZ-5A 1.0.2
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F2000P0XBQ0
V1.1.5	Processor	ADSP-BF537 BBCZ-5A 1.0.2
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F2000P0XBQ0
V1.1	Processor	ADSP-BF537 BBCZ-5A 1.0.2
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F2000P0ZBQ0

Table 9-2: Production Report TCM-BF537B

8.3 TCM-BF537B-64 (100-1228)

Version	Component	Type
V1.1.2	Processor	ADSP-BF537 BBCZ-5A 1.0.2
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F4400P0VBQ

Table 9-3: Production Report TCM-BF537B-64 with 64MB-Flash

9 Product Changes

For the latest product change information please consult the product web-page at:

http://www.bluetechnix.com/goto/tcm-bf537

Version	Changes
V1.1	Border Pad and BGA Versions added with 64MB flash addressing option, 28mmx28mm outline
V1.2	Component placement changed (connector version)
V1.3	Mount option for 64MB flash addressing (connector version)
V1.4	Correction of RTC inaccurateness

10 Document Revision History

Version	Date	Document Revision
17	2009-05-25	Table 4.2 L14 -> J16 Symbol BGA updated
16	2009-03-19	Table 8.2 new version added
15	2009-01-19	Chapter 5-1 new schematic, new part list
14	2008-12-02	Chapter 4.9 added Pull up/down information added Correction of the BGA-Pin assignment table
13	2008-10-21	Pin 48 not available instead of 49
12	2008-09-05	Footprints and mechanical drawings updated
11	2008-08-11	English checked for spelling, grammar and clarity
10	2008-08-06	Fixed memory map
9	2008 03 27	Production Report Added
8	2007 24 10	RTC Problem in the Anomaly List added
7	2007 06 04	Unlock flash hint, Document Revision History Table
6	2007 04 17	BP and BGA symbols corrected; Rx1 and Tx1 were mixed up
5	2007 04 04	Corrections of the description of the BP and BGA versions.
4	2007 01 08	Corrected Typo in page 7 Table 2-2: PF5 one time instead of two times PF4
3	2006 10 02	Release V1.1 of TCM Boards Main updates: Separate Connector, Border and BGA pad version Border Pads: 76 Border pads without Data and Address bus pins Connector Version: As in version V1.0 BGA Version: Additional Processor pins, added Flash addressing flexibility Removed limited address range, all 8MB addressable
2	2006 04 26	Updated anomaly list: only 4MB addressable.
2	2006 04 26	Updated document: Connector symbol, fixed Bug naming of pin 22 and pin 40 (connector version) Rx and Tx was flipped.
1	2006 03 07	First release V1.0 of the Document

Table 10-1: Revision History

A List of Figures and Tables

Figures

Tables