XC6SLX150 X1 Coprocessor Module User Manual

Issue – 1.0

Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR XC6SLX150 X1 Coprocessor MODULE. PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

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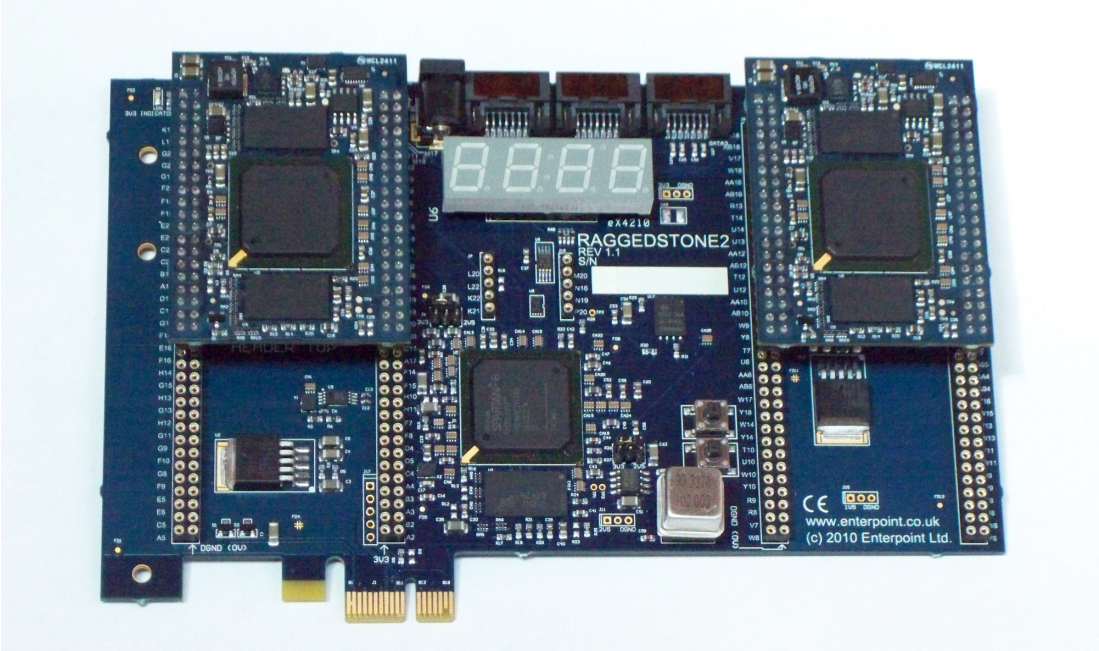
Introduction

The Enterpoint XC6SLX150 X1 Coprocessor Module is a Spartan-6 FPGA based module offering a highly powerful, flexible and low cost approach to extending the performance and processing power of our range of development boards. It can be plugged into our Raggedstone1, Raggedstone2, Drigmorn 3 or 4 or Broaddown series boards. It can also be used as a stand-alone module using its 0.1inch pitch header pins to interface to a user's power and JTAG circuit.



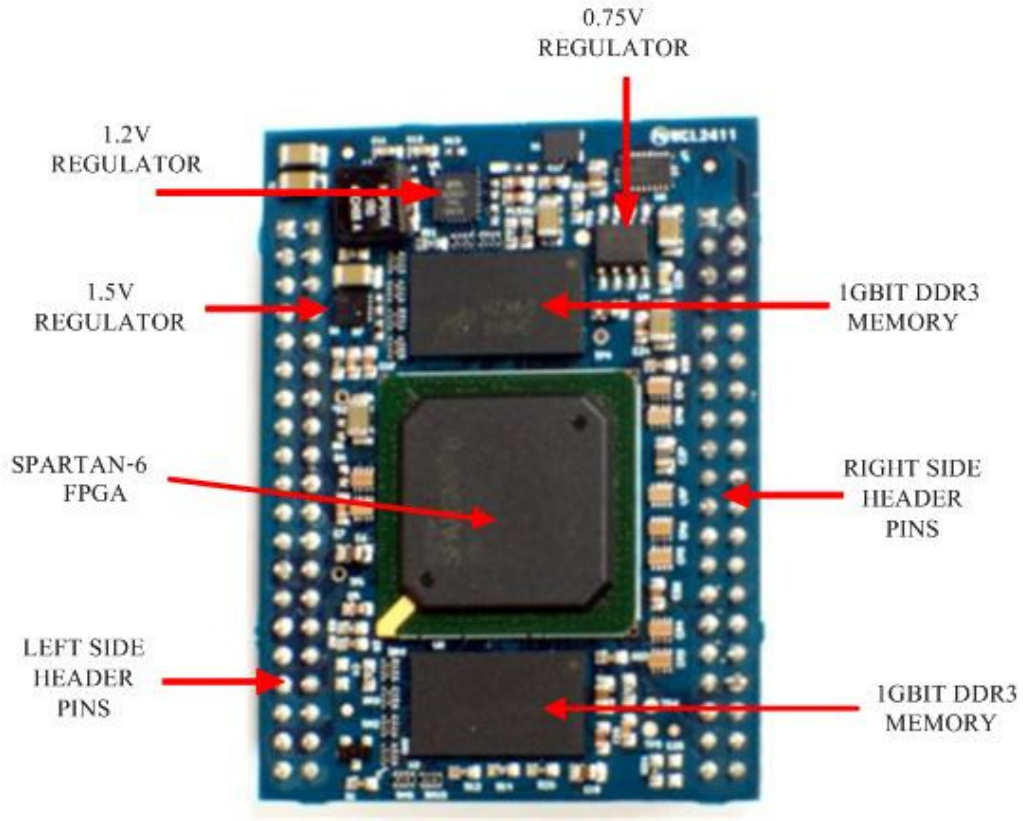
Enterpoint's Raggedstone2 development board with 2 XC6SLX150 X1 Coprocessor Modules

The aim of this manual is to assist in using the main features of the XC6SLX150 X1 Coprocessor Module. There are features that are beyond the scope of the manual. Should you need to use these features then please email support@enterpoint.co.uk for detailed instructions.

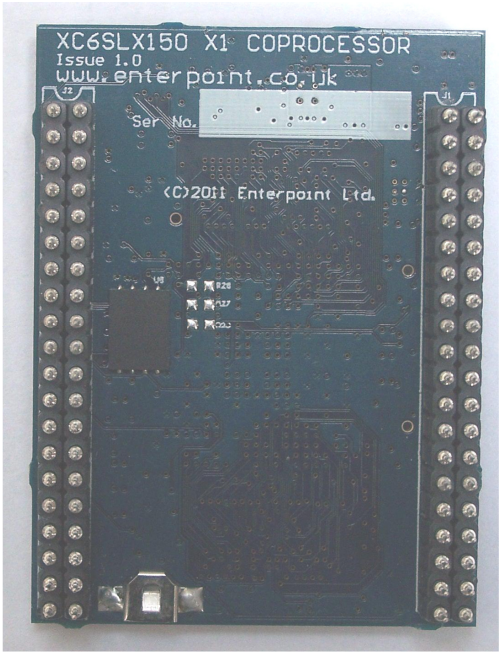
The XC6SLX150 X1 Coprocessor Module currently comes with an XC6SLX150-2FGG484C Spartan-6. Other variants may be offered at a later date or as an OEM product. Please contact out us on boardsales@enterpoint.co.uk should you need further information.

We can offer a PCB design service to interface with this product should you require a function not covered by our current range of development boards. Typical turn around for this service is 6-8 weeks depending upon complexity, quantity ordered and availability of components.

XC6SLX150 X1 Coprocessor Module



XC6SLX150 X1 Coprocessor Module Front View



XC6SLX150 X1 Coprocessor Module Back View

The XC6SLX150 X1 Coprocessor Module will be supplied un-programmed. You will need a programming cable to program the XC6SLX150 X1 Coprocessor Module – for example the Enterpoint Prog2 parallel port programming cable or the Enterpoint Prog3 USB port programming cable.

The Xilinx toolset required to program the XC6SLX150 X1 Coprocessor Module depends upon the Spartan6 device fitted to the board.

If your XC6SLX150 X1 Coprocessor Module is fitted with an LX150 device (standard version) it will require the full Xilinx toolset to build a design. If you have a custom version fitted with an LX75 device or smaller it is supported by the free ISE Webpack . ISE Version11.1 SP4 or later is required, available from Xilinx. This provides all the tools to enter and build a design. Using this tool in conjunction with your programming cable you will also be able to program the Spartan-6, and the supporting SPI Flash, that are on the XC6SLX150 X1 Coprocessor Module.

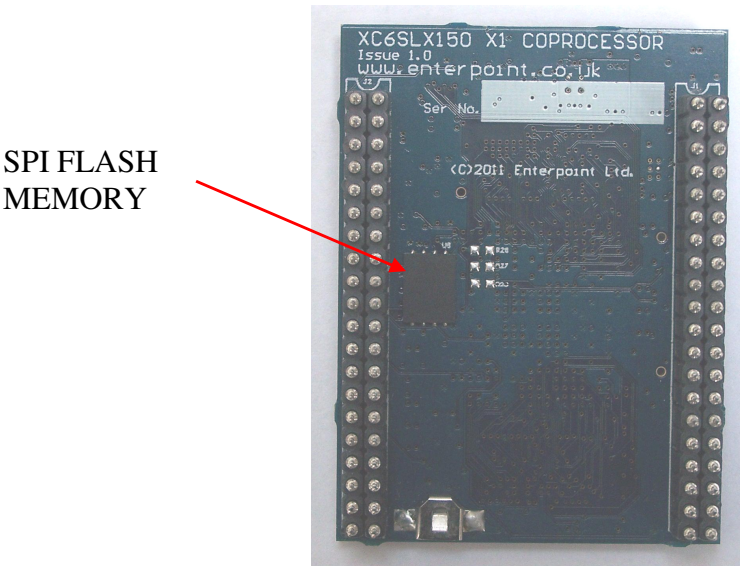
ISE Webpack can be obtained directly from the Xilinx website at http://www.xilinx.com/ise. Registration will be necessary to complete the download. The full ISE toolset can also be purchased from the Xilinx website.

FPGA

The XC6SLX150 X1 Coprocessor Module supports Spartan-6 devices in the FGG484 package. This module is normally available with commercial grade -2 speed devices fitted in the XC6SLX150 size. Should you have an application that needs a different size of FPGA, industrial specification parts or faster speed grades please contact sales for a quote at boardsales@enterpoint.co.uk.

The FPGA PROG_B signal is routed to the Right Side DIL header and is available on pin 10 (outer row) should the user wish to initiate reconfiguration of the Spartan6.

SPI FLASH MEMORY



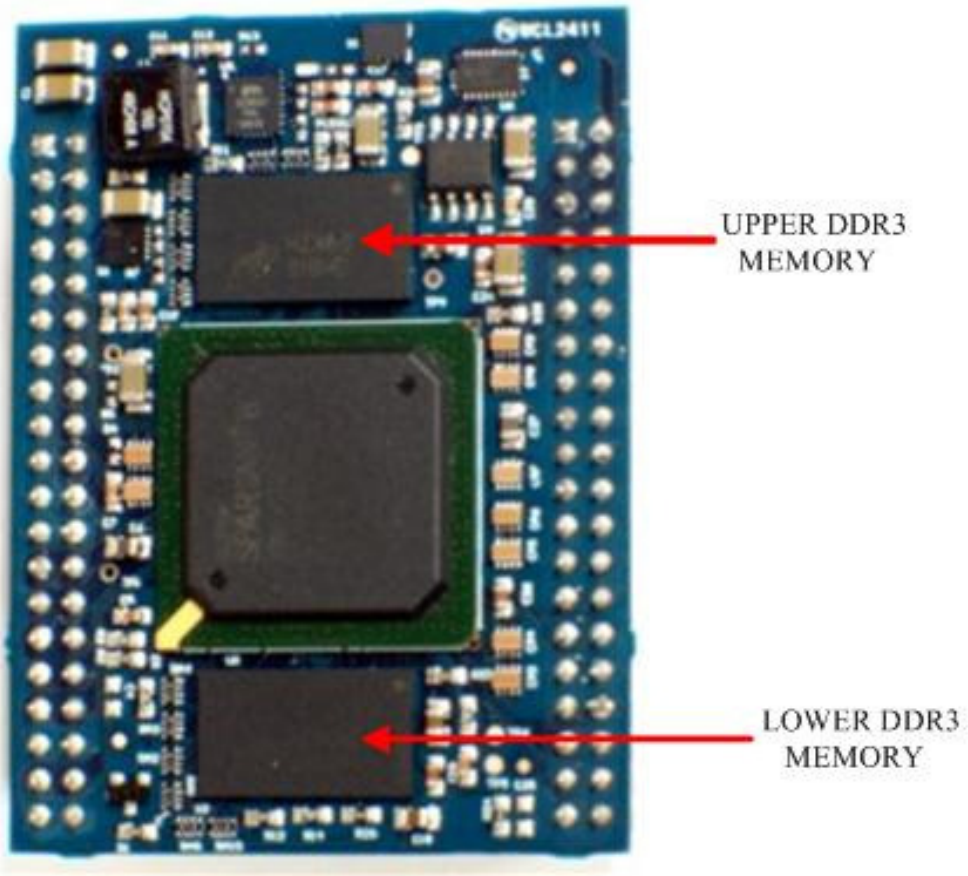
The M25P128 SPI flash memory device configures the FPGA when it is powered provided a suitable bitstream is programmed into the device. The M25P128 has a capacity of 128Mbits with a single configuration bitstream for the XC6SLX150 X1 Coprocessor Module taking 4.1Mbits. Any remaining space can be used for alternative configurations or code and data storage.

The SPI flash memory signals are routed to the Right side outer DIL header on the pins shown in the table below. After configuration the SPI Flash can be accessed via the following pins of the FPGA:

M25P128 FUNCTION	FPGA PIN	RIGHT HEADER PIN
CCLK	Y21	8
MOSI	AB20	9
WRITE	U9	11
DIN	AA20	10
CSO_B	T5	12
HOLD	U13	7

The flash memory can be programmed via the JTAG interface.

DDR3 MEMORY



XC6SLX150 X1 Coprocessor DDR3

The XC6SLX150 X1 Coprocessor Module has two 1GBIT DDR3 Micron MT41J64M16LA devices as standard. These devices are organised as 8 Meg x 16 x 8 banks and are supported by the hard core memory controller that is in the Spartan-6 FPGA. To add this core to your design the COREGEN tool, part of the ISE suite, will generate implementation templates in VHDL or Verilog for the configuration that you want to use. More details on the memory controller can be found in the user guide http://www.xilinx.com/support/documentation/user_guides/ug388.pdf.

The DDR3 has 12 address lines and 16 data lines to address all the available memory, which can be accessed at speeds of 1.87ns. More details of the DDR3 can be found in http://download.micron.com/pdf/datasheets/dram/ddr3/1Gb_DDR3_SDRAM.pdf.

For OEM applications we can fit bigger DDR3 parts subject to limitations of the memory controller.

The upper DDR3 device has the following connections to the FPGA:

DDR3 FUNCTION	FPGA PIN	DDR3 FUNCTION	FPGA PIN
DDR_A0	F21	DDR_DQ3	M22
DDR_A1	F22	DDR_DQ4	J20
DDR_A2	E22	DDR_DQ5	J22
DDR_A3	G20	DDR_DQ6	K21
DDR_A4	F20	DDR_DQ7	K22
DDR_A5	K20	DDR_DQ8	P21
DDR_A6	K19	DDR_DQ9	P22
DDR_A7	E20	DDR_DQ10	R20
DDR_A8	C20	DDR_DQ11	R22
DDR_A9	C22	DDR_DQ12	U20
DDR_A10	G19	DDR_DQ13	U22
DDR_A11	F19	DDR_DQ14	V21
DDR_A12	D22	DDR_DQ15	V22
DDR_A13	D19	DDR_LDM	L19
DDR_A14	D20	DDR_LDQS	L20
DDR_A15	B21	DDR_LDQS_N	L22
DDR_BA0	J17	DDR_UDM	M20
DDR_BA1	K17	DDR_UDQS	T21
DDR_BA2	H18	DDR_UDQS_N	T22
DDR_CS_N	P20	DDR_ODT	G22
DDR_RAS_N	H2	DDR_CAS_N	H22
DDR_WE_N	H19	DDR_RESET_N	F18
DDR_DQ0	N20	DDR_CKE	D21
DDR_DQ1	N22	DDR_CLK_N	J19
DDR_DQ2	M21	DDR_CLK	H20

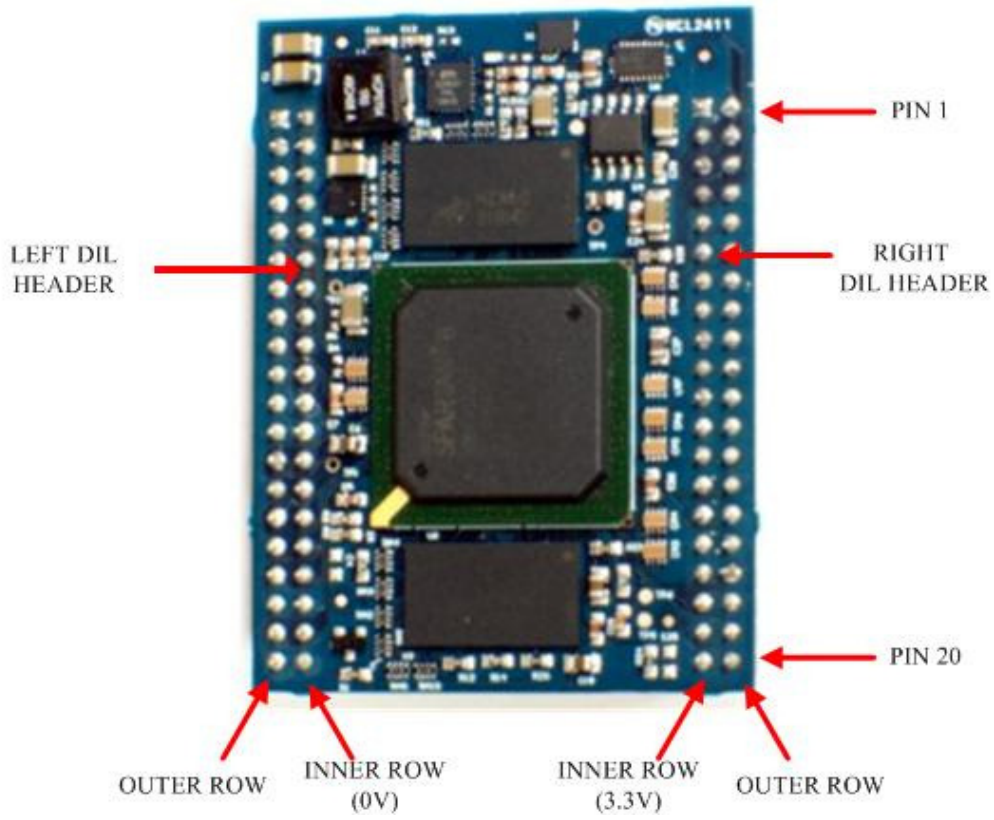
The lower DDR3 device has the following connections to the FPGA:

DDR3 FUNCTION	FPGA PIN	DDR3 FUNCTION	FPGA PIN
DDR_A0	H2	DDR_DQ3	M1
DDR_A1	H1	DDR_DQ4	J3
DDR_A2	H5	DDR_DQ5	J1
DDR_A3	K6	DDR_DQ6	K2
DDR_A4	F3	DDR_DQ7	K1
DDR_A5	K3	DDR_DQ8	P2
DDR_A6	J4	DDR_DQ9	P1
DDR_A7	H6	DDR_DQ10	R3
DDR_A8	E3	DDR_DQ11	R1
DDR_A9	E1	DDR_DQ12	U3

DDR_A10	G4	DDR_DQ13	U1
DDR_A11	C1	DDR_DQ14	V2
DDR_A12	D1	DDR_DQ15	V1
DDR_A13	G6	DDR_LDM	L4
DDR_A14	F5	DDR_LDQS_P	L3
DDR_A15	H8	DDR_LDQS_N	L1
DDR_BA0	G3	DDR_UDM	M3
DDR_BA1	G1	DDR_UDQS_P	T2
DDR_BA2	F1	DDR_UDQS_N	T1
DDR_CS_N	J7	DDR_ODT	J6
DDR_RAS_N	K5	DDR_CAS_N	K4
DDR_WE_N	F2	DDR_RESET_N	C3
DDR_DQ0	N3	DDR_CKE	D2
DDR_DQ1	N1	DDR_CLK_N	H3
DDR_DQ2	M2	DDR_CLK_P	H4

The signals shown shaded in yellow are terminated using suitable arrangements of resistors.

DIL HEADERS



The DIL Headers provide a simple mechanical and electrical interface for connection to the module. There are twenty I/O on the left side of the module and up to 12 IO on the right hand side of the module giving a total of 32 possible I/O available.

4 of the IO on the right hand side of the module (Right Header outer pins 1 to 4) are shared with the JTAG signals and pass through bus switches. Bus switch technology has a minimal effect on I/O timing with propagation times of less than 250ps through these devices.

The DIL Headers can support up 16 pairs of LVDS signalling. The Spartan-6 FPGA can terminate any of these pairs. LVDS termination on individual signal pairs is a programmable option that can be set in build constraints for the FPGA when using the ISE toolset. The LVDS pairs are shown in the table above along with Spartan-6 pin numbers.

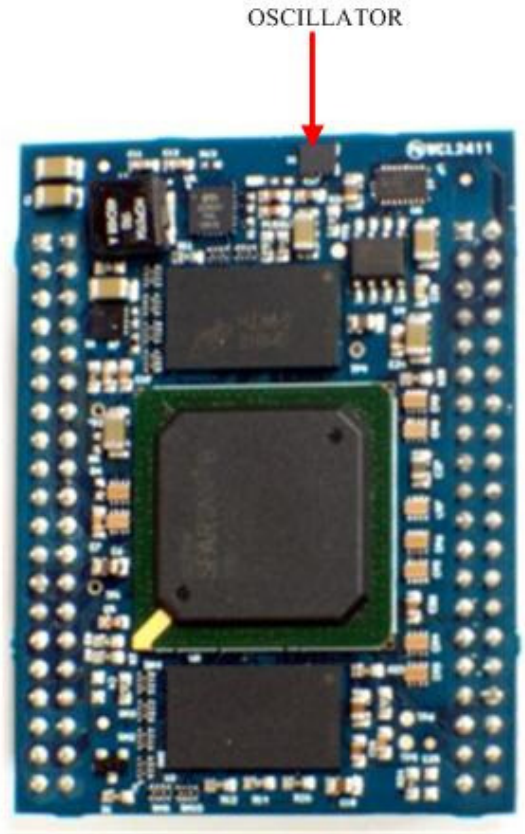
The DIL Headers will also support the use of crude prototype circuits using stripboard or other prototype materials. The DIL Header connectors are arranged on a standard 0.1inch (2.54mm) pitch. The horizontal pitch of the DIL Headers is 1.6 inches between the outer rows of the headers. The inner pins of the header form continuous power strips. The right hand side header has an inner column of 3.3V pins. The LHS header has an inner column of DGND (0V).

	LEFT COLUMNS				RIGHT COLUMNS		
	OUTER PINS		INNER PINS	INNER PINS	OUTER PINS		
ROW	FUNCTION	S6 PIN			FUNCTION	S6 PIN	
1	IO_L63P_0	B16	0V		3.3V	IO_L2P_2/TMS	AA21
2	IO_L63N_0	A16	0V		3.3V	IO_L2N_2/TDO	AB21
3	IO_L51P_0	C15	0V		3.3V	IO_L5P_2/TDI	Y19
4	IO_L51N_0	A15	0V		3.3V	IO_L5N_2/TCK	AB19
5	IO_L38P_0	C13	0V		3.3V	IO_L14P_2	AA18
6	IO_L38N_0	A13	0V		3.3V	IO_L14N_2	AB18
7	IO_L37P_0	B12	0V		3.3V	HOLD	U13
8	IO_L37N_0	A12	0V		3.3V	CCLK	Y21
9	IO_L35P_0	C11	0V		3.3V	MOSI	AB20
10	IO_L35N_0	A11	0V		3.3V	DIN	AA20
11	IO_L34P_0	B10	0V		3.3V	WRITE	U14
12	IO_L34N_0	A10	0V		3.3V	CSO_B	T5
13	IO_L8P_0	C9	0V		3.3V	PROG_B	AA1
14	IO_L8N_0	A9	0V		3.3V	JTAG_ENABLE	
15	IO_L6P_0	B8	0V		3.3V	IO_L49P_2	AB6
16	IO_L6N_0	A8	0V		3.3V	IO_L49N_2	AA6
17	IO_L4P_0	B6	0V		3.3V	IO_L57P_2	AA4
18	IO_L4N_0	A6	0V		3.3V	IO_L57N_2	AB4
19	IO_L2P_0	C5	0V		3.3V	IO_L64P_2	AA2
20	IO_L2N_0	A5	0V		3.3V	IO_L64N_2	AB2

It should be noted that the pins on the XC6SLX150 X1 Coprocessor Module should be treated with respect. The XC6SLX150 X1 Coprocessor Module is usually supplied with an extra row of pin-socket headers to protect the row of pins which are soldered into the board. This means that if a pin is broken this extra row of headers can be replaced easily and cheaply. Enterpoint can supply extra pins-socket headers if required. Contact boardsales@enterpoint.co.uk. Enterpoint does not accept responsibility if the header pins on the module have been damaged due to poor handling.

OSCILLATOR

The oscillator on the XC6SLX150 X1 Coprocessor Module is an ASEM 25MHz oscillator. The oscillator is situated as shown below and is connected to the FPGA on **PIN AB13**.



The Spartan-6 has PLLs and DCMs to produce multiples, divisions and phases of the clock for specific application requirements. Please consult the Spartan-6 datasheet available from the Xilinx website at http://www.xilinx.com if multiple clock signals are required.

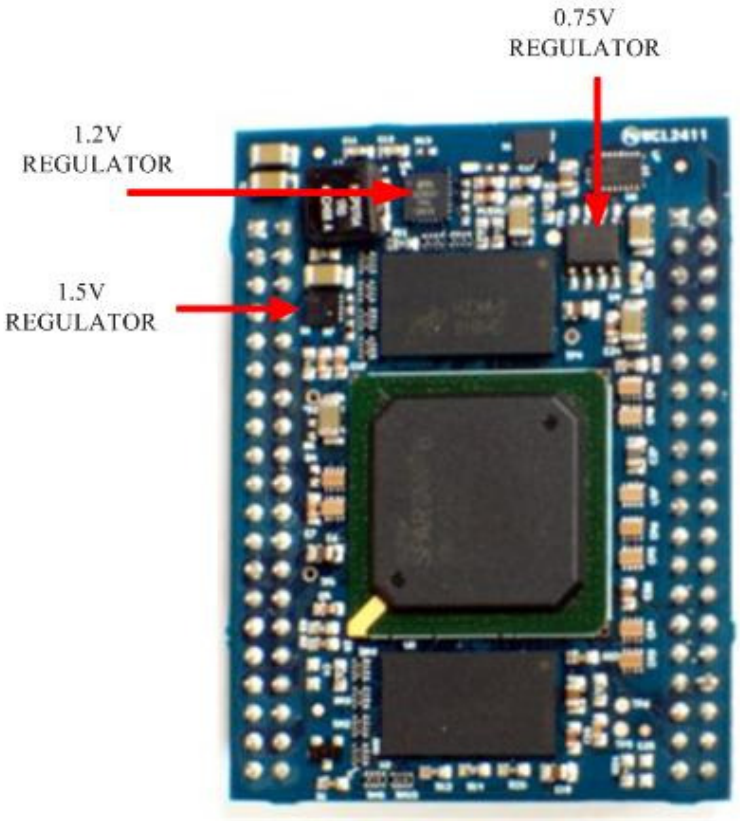
POWER CONNECTIONS

The user must supply 3.3v to the module on any or all of the right hand side inner header pins and 0V on any or all of the left hand side inner header pins. This can be achieved by plugging the module into one of the Enterpoint Raggedstone, Drigmorn or Broaddown series development boards, which all have sockets with appropriate power connections for this module and resettable fuses to limit the current. Alternatively the user may wish to plug the module into his/her own circuitry. **Whatever power supply is used care should be taken not to exceed 3.3v input as this can cause damage to the XC6SLX150 X1 Coprocessor Module**.

BATTERY

A battery holder is supplied on the underside of the XC6SLX150 X1 Coprocessor Module that can take a nominal 4.8mm diameter, 1.5mm thick rechargeable coin cell battery providing 1V to 3.6V e.g Panasonic ML414S/ZT. We do not normally supply the battery to avoid shipping issues with batteries. It is connected to pin R17 of the FPGA and recharges from the 3.3V supply. V_{BATT} is required to maintain the battery backed RAM AES key when VCC_{AUX} is not applied to the FPGA.

POWER REGULATORS



The XC6SLX150 X1 Coprocessor Module has three regulators supplying 1.5V, 1.2V and 0.75V power rails.

WARNING – REGULATORS CAN BECOME HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE XC6SLX150 X1 COPROCESSOR MODULE IS IN OPERATION.

A Micrel MIC22600 regulator supplies 1.2V with a maximum current available of 6A. This is used for the core voltage of the FPGA .

A Diodes Inc. AP7167 linear regulator supplies 1.5V with a maximum current of 1.2A for the DDR3.

A National Semiconductor LP2996 push-pull regulator produces up to 1.5A at 0.75V. This supply is used as reference and termination voltage for the DDR3 memory and related FPGA I/O.

Programming XC6SLX150 X1 Coprocessor Module

The programming of the FPGA and SPI Flash parts on the XC6SLX150 X1 Coprocessor Module is achieved using the JTAG interface. There is no JTAG connector on the XC6SLX150 X1 Coprocessor Module.

The JTAG signals are routed to the following pins on the Right side DIL header (outer column). These signals should be routed through a host board to a JTAG connector if you wish to program the Coprocessor module directly.

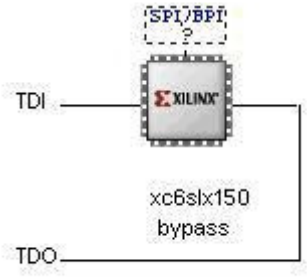
JTAG SIGNAL	HEADER PIN
TDI	3
TDO	2
TCK	4
TMS	1
JTAG ENABLE	14

These pins are also routed to GPIO on the Spartan-6 FPGA which can be used after the FPGA programming is complete. When the JTAG ENABLE signal is LOW the header pins are routed to the GPIO as shown previously in the section DIL HEADERS. When the JTAG ENABLE signal is asserted HIGH the JTAG signals are connected to the Header pins and those GPIO are not available.

Principally it is anticipated that a JTAG connection will be used in conjunction with Xilinx ISE software although other alternatives do exist including self re-programming. The Spartan-6 series needs to be programmed using ISE 11 or higher. Versions of ISE prior to 11 do not support Spartan-6. The full version of the Xilinx tools is required to program the XC6SLX150-2FGG484C. The free Webpack version of ISE is sufficient to support the smaller versions of the FPGA.

There is a single JTAG chain on the XC6SLX150 X1 Coprocessor Module. The JTAG chain allows the programming of the Spartan-6 and SPI Flash device.

Using iMPACT Boundary Scan the JTAG chain appears like this:



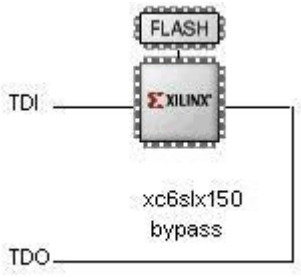
1. Programming the FPGA directly.

Direct JTAG programming of the Spartan-6 FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 and 3 below).

Direct JTAG programming using .bit files is useful for fast, temporary programming during development of FPGA programs. Right click the icon representing the Spartan-6 FPGA and choose 'Assign New Configuration File'. Navigate to your .bit file and choose 'OPEN'. The next dialogue box will offer to add a flash memory and you should decline. Right click the icon representing the Spartan-6 FPGA and choose 'Program'. On the next dialogue box ensure that the 'Verify' box is not checked. (If it is you should uncheck it, failure to do this will result in error messages being displayed). Click OK. The Spartan-6 will program. This process is very quick (typically a few seconds)

2. Programming the SPI flash memory using Boundary Scan.

Once the SPI Flash memory has been programmed, the Spartan-6 device will automatically load from the Flash memory at power up. Generation of suitable Flash memory files (.mcs) can be achieved using ISE iMPACT's Prom File Formatter. Right click on the icon representing the Spartan-6 and choose 'Add SPI/BPI Flash' Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and M25P128 . Data width should be set to 1. The flash memory should appear as shown below.



Right click on the icon representing the flash memory and choose 'Program' to load your program into the device. It is recommended that options to 'Verify' and 'Erase

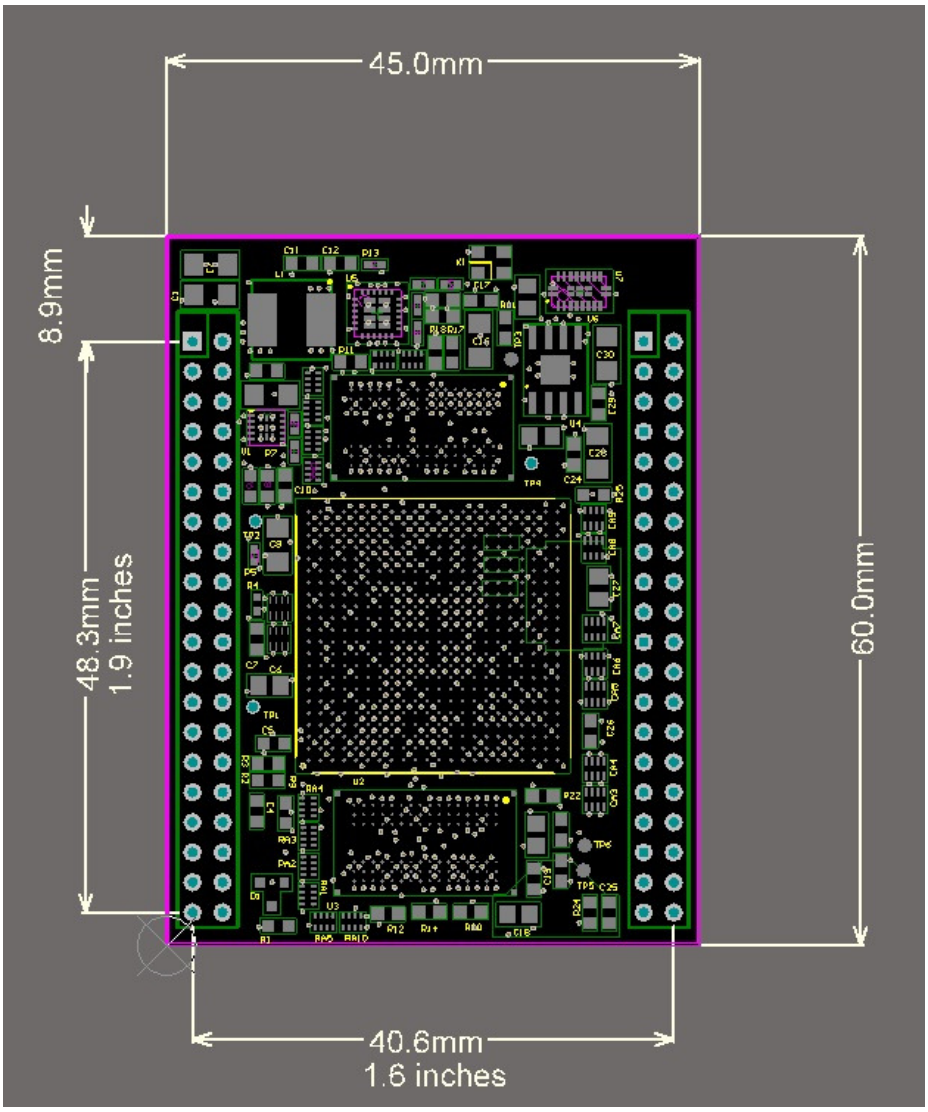
before programming' are chosen. Otherwise all defaults can be accepted. The programming operation will take some time (at least 3 or 4 minutes).

Depending upon the settings used when generating the bitfile using ISE, it will take up to 20 seconds for the XC6LX150 to configure upon power-up. In order to decrease this time the following process can be followed:

1. In the main ISE menu, right-click 'Generate Programming file'. Choose Properties.
2. On the left hand side of the Process Properties Dialogue box, choose Configuration Options.
3. The first item on the menu which appears on the right hand side of the dialogue box is 'Configuration Rate'. The default setting is 2. Increase this number. The maximum value we suggest is 22. Choose 'Apply' and 'OK'.
4. Generate the program file as normal.

MECHANICAL ARRANGEMENT

The Dimensions on the drawings below are millimetres (mm). All sizes quoted are subject to manufacturing tolerances and should only be used as a general guide.



The socket pins on the DIL headers are arranged on a 2.45mm (0.1inch) pitch

The maximum height of the components, measured from the lower surface of the board is 5mm.

When the XC6SLX150 X1 Coprocessor Module is plugged into a Raggedstone2 development board using doubled header pins the total height from the underside of the Raggedstone2 to the top of the XC6SLX150 X1 Coprocessor Module components is approximately 22mm.

Medical and Safety Critical Use

XC6SLX150 X1 Coprocessor Modules are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd accepts no liability for any failure or defect of the XC6SLX150 X1 Coprocessor Module, or its design, when it is used in any medical or safety critical application.

Warranty

The XC6SLX150 X1 Coprocessor Module comes with a 90 day return to base warranty. Do not attempt to solder connections to the XC6SLX150 X1 Coprocessor Module. Enterpoint reserves the right not honour a warranty if the failure is due to soldering or other maltreatment of the XC6SLX150 X1 Coprocessor Module.

Outside warranty Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a XC6SLX150 X1 Coprocessor Module has been maltreated or otherwise deliberately damaged. Please contact support if you need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Please check our online FAQ page for this product first before contacting support. Telephone and email support is offered during normal United Kingdom working hours (GMT or GMT + 1) 9.00am to 5.00pm.

Telephone - +44 (0) 121 288 3945
Email - support@enterpoint.co.uk