ML67Q5270

DFT Based Fingerprint Authentication LSI

GENERAL DESCRIPTION

The ML67Q5270 is a single chip LSI that executes fingerprint authentication without external memory by using the embedded fingerprint authentication accelerator. This fingerprint authentication accelerator uses DFT(Discrete Fourier Transform) based algorithm licensed from Precise Biometrics, and supports AuthenTec's slide sensors and certain touch sensors from several sensor manufacturers. Besides the ML67Q5270 has the secure circuit to protect enrolled fingerprint data from unauthorized access. Thus this LSI helps customers quickly design new products that offer convenient security as far as high performance fingerprint authentication, low cost, small size and high level of security.

FEATURES

• Fingerprint authentication
- DFT (Discrete Fourier Transform) based algorithm licensed from Precise Biometrics
  This DFT based algorithm achieves a lower FTE (False To Enrollment rate) and a higher authentication accuracy especially when a slide sensor is used, as compared to the minutiae algorithm.
- Easy-to-use
  The fingerprint authentication is performed by the fingerprint authentication accelerator, which does not ask customers for so complicated control.
- No external memory

Customer's application program and up to 45 fingerprint data can be stored in the embedded Flash memory on the ML67Q5270. No external memory is required, when a slide sensor is used.
- High-speed authentication, besides low power consumption
  The highly optimized fingerprint authentication accelerator achieves high-speed authentication using a low speed clock.
  Authentication : < 0.8 seconds (1:1 authentication)
  < 1.8 seconds (1:45 authentication)
  Enrollment : < 2 seconds/finger
- Applicable fingerprint sensor
  Slide sensor : AuthenTec AES1751 (128 × 8 pixels)

• CPU
- 32-bit RISC CPU (ARM7TDMI-S)
- Little endian format
- Instruction system: A high-density 32-bit instruction and a 16-bit instruction of high-object efficiency, which is the subset of the 32-bit instruction, can be executed in mixed mode.
- General-purpose register: 32 bits x 31 registers
- Built-in barrel shifter (ALU and barrel shift operation can be executed by one instruction)
- Built-in debugging function (JTAG interface)
  The JTAG interface pin is shared with GPIO.

• Built-in Memories
- 16 Kbyte working RAM for CPU
- 128 Kbyte Flash ROM for application program and fingerprint template data, whose erase/rewrite times are maximum 10,000
- 8 Kbyte Mask ROM for update of program in the Built-in Flash ROM

• External memory controller
- ROM/Flash
  • 1 bank x 4 Mbytes
  • Supports 16-bit devices
  • Bootable from external ROM/Flash
  This function can not be used during security function being activated.
- SRAM
  • 1 bank × 4 Mbytes
  • Supports 16-bit devices
- External I/O
  • 1-bank × 4 Mbytes
  • Supports 8-bit/16-bit devices
  • Enable to setting address setup, RW/WE pulse, and data off timing in system clock cycle unit.
  • Supports an access wait function by wait signal

• Interrupt control
- 1 FIQ resource
  External : 1
- 20 IRQ resources
  External : 3, Internal : 17
  7 priority levels for each source

• DMA controller (DMAC)
- 2 channels
- Enable to allocate multiple DMA transfer request sources for each channel.
- Channel priority: fixed mode/round robin mode
- DMA transfer mode: cycle steal mode/burst mode
- DMA request type: software requests/hardware requests
- Maximum transfer count : 65,536
- Data transfer size: 8 bits/16 bits/32 bits
- Transfer request source: CPU, SPI, Synchronous SIO, Smartcard IF

• GPIO
- 13 bits × 1 channel, 12 bits × 2 channel
- Enable to setting input mode or output mode for each bit
- Enable to setting as interruption source for each bit
- Interruption mode: level/edge and positive logic/negative logic

• Timer
- 16-bit auto reload timer × 1 channel for system operation
- 16-bit auto reload timer × 1 channel for applications
- 16-bit flexible timer × 2 channel for applications
  Auto reload timer (ART) mode / Compare out (CMO) mode / Pulse width modulation (PWM) mode / Capture (CAP) mode

• Watch dog timer (WDT)
- 16-bit timer
- 8.389 seconds max. (when CPU operating frequency is 32 MHz)
- Enables generation of interrupt or reset by setting

• SIO (UART)
- Full-duplex asynchronous mode
- Built-in baud rate generator

• SPI
- 2 channels of full-duplex serial peripheral interfaces
- Operating mode: master mode/slave mode
- Data transfer size: 8 bits (byte) / 16 bits (word)
- Built-in 16-byte/16-word FIFO on the transmission side and the reception side
- Supports DMA transfer (master/slave mode)

• Synchronous SIO (SSIO)
- clock synchronous serial port × 1 channel
- Data transfer size : 8 bits (byte)
- Selectable clock polarity
- Selectable LSB first or MSB first
- Operation mode: master mode/slave mode
- Supports DMAC transfer (in master mode only)

• Smart Card interface (Smartcard IF)
- ISO UART × 1 channel
- Built-in 16-byte FIFO
- Built-in parity error counter in receive mode and transmit mode at automatic retransmission
- Supports asynchronous protocol of T = 0 and T = 1 according to ISO7816 and EMV
- Built-in error detection code generation and error detection functions by hardware
- Supports DMA transfer

• USB2.0 full-speed device
- Compliant with Universal Serial Bus (USB) 2.0
- Full speed (12 Mbps) × 1 port.
- End points: 5 or 6
- Supports all data transfer types (control transfer, bulk transfer, interrupt transfer, isochronous transfer).
- Built-in SOP generation and CRC5/16 generation functions
- Access size to data transfer FIFOs: 8 bits/16 bits/32 bits

• Random number generator (RANDOM)
- Generates 8-bit random numbers

• 8bit Parallel I/F
- 8-bit (byte) parallel port × 1 channel
- Receive clock: 13.5 MHz max.
- Enable level for clock edge and synchronous signal can be selected

• Clock
- Input clock: 12 MHz (oscillator connected)
- System clock (CPU operating clock): 32 MHz
  System clock is generated by PLL using 12MHz clock.
- Output clock: 6/12 MHz for fingerprint sensor

• Power management
- Power saving mode
  •Individual module clock stop mode:
    Clock operation/stop can be set for each functional block.
  •HALT mode:
    Only CPU clock is stopped.
  •STOP mode:
    All clocks are stopped, and start /stop of internal PLL and oscillator circuit are selectable.

• Package
- 144-pin LFBGA (P-LFBGA144-1111-0.80)

BLOCK DIAGRAM

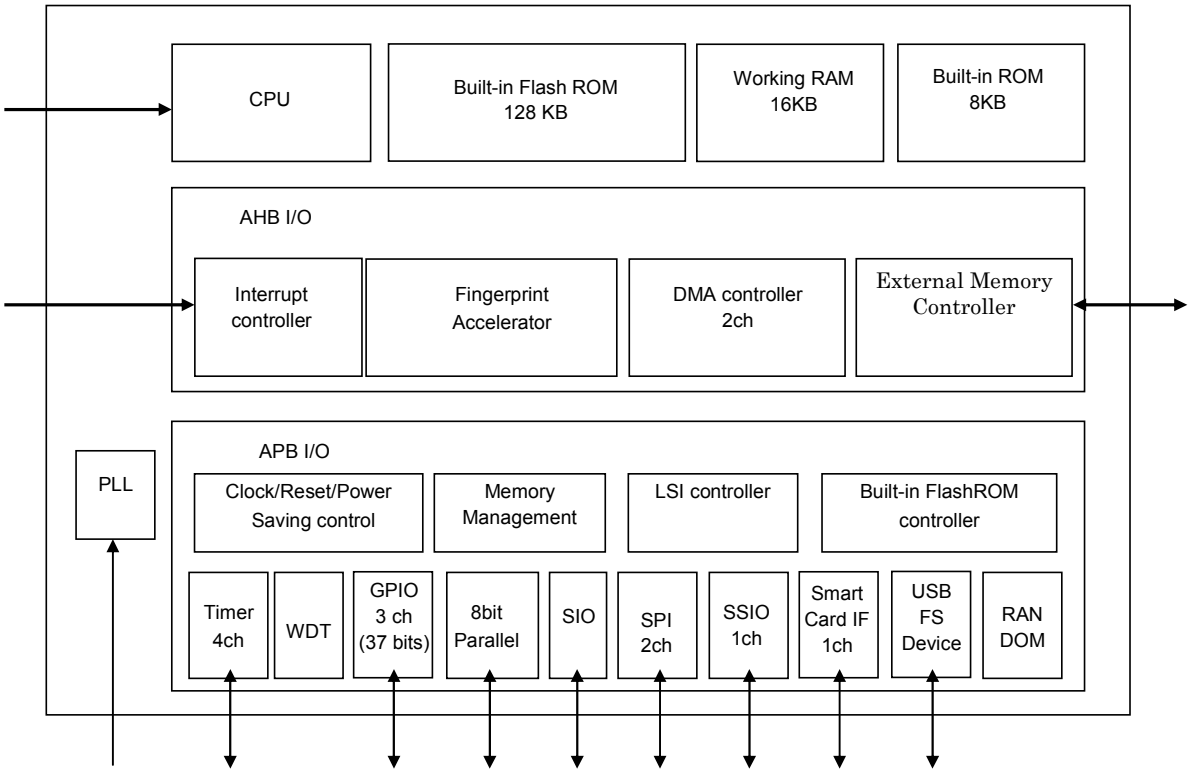


Figure 1 Block Diagram

PIN LAYOUT

BSEL1	GNDIO	TCK	TDI	NTRST	VDDIO	PB04 (SIMDATA)	VDD CORE	XD08	XD07	BSEL0	XD06	TESTF	13
XBSN0	XBSN1	TMS	GND CORE	XD15	XD14	GNDIO	XD10	XD09	GND CORE	PB01 (SIMVCTL0)	PB00 (SIMDET)	PA10 (SSIOCLK)	12
VDDIO	N.C.	RTCK	VDD CORE	TDO	PB06 (SIMCLK)	XD13	XD12	VDDIO	PB02 (SIMVCTL1)	PA09 (SSIORX)	PC09 (BPIFD7)	XD05	11
PC10 (FTM0)	PC11 (FTM1)	PA12 (SIORX)	XWAIT0N	N.C.	PR0	PB05 (SIMRST)	XD11	PB03 (SIMVCMD)	GNDIO	PA08 (SSIOTX)	XD03	XD04	10
XREN	XROMCSN	XWEN	GNDIO						XD01	VDDIO	XD00	XD02	9
XRAMCSN	PA11 (SIOTX)	GND CORE	XIO0CSN						AFSEL	PC07 (BPIFD5)	PC08 (BPIFD6)	GNDIO	8
VDDIO	XA01	VDD CORE	XA00			**P-LFBGA-144-1111-0.80 (Bottom View)**			PC05 (BPIFD3)	VDDIO	PC06 (BPIFD4)	PB11 (CLKO)	7
XA04	GNDIO	XA02	XA03						PC03 (BPIFD1)	N.C.	PC02 (BPIFD0)	PC01 (BPIFSYNC)	6
VDDIO	XA05	XA08	XA06						PC00 (BPIFVCLK)	GND CORE	GNDIO	PUCTL	5
XA09	XA07	XA11	XA16	PA01 (SPI0MISO)	XA21	PA05 (SPI1MISO)	PA06 (SPI1SSN)	XI	DP	VDDUSB	VDD CORE	VDDIO	4
XA12	XA10	GNDIO	XA18	XA19	TESTE	PA04 (SPI1MOSI)	PA00 (SPI0MOSI)	VDDPLL	PB07 (FIQ)	VDD CORE	DM	GNDIO	3
XA13	XA14	VDD CORE	PR1	VDDIO	XA20	N.C.	PA07 (SPI1SCK)	XO	GNDPLL	GND CORE	GNDUSB	PC04 (BPIFD2)	2
VDDIO	GND CORE	XA15	XA17	GNDIO	PA02 (SPI0SSN)	PA03 (SPI0SCK)	VDDIO	GNDIO	RESETN	PB08 (EXINT0)	PB09 (EXINT1)	PB10 (VBUS)	1
N	M	L	K	J	H	G	F	E	D	C	B	A	

PIN LIST

Pin No.	Pin name	Description						Schmitt	PU/PD(*1)	Drive capacity	5V Tolerant	Initial direction	Initial value
		Primary function			Secondary function								
		I/O	Polarity	Description	I/O	Polarity	Description						
E4	XI	I	-	Oscillation Pin	-	-	-	-	-	-	-	I	-
E2	XO	O	-	Oscillation Pin	-	-	-	-	-	-	-	O	-
D1	RESETN	I	N	System Reset	-	-	-	S	PU	-	-	I	-
L11	RTCK	O	-	JTAG Return Clock	-	-	-	-	-	4mA	-	O	L
L13	TCK	I	-	JTAG Test Clock	-	-	-	-	PU	-	-	I	-
L12	TMS	I	P	JTAG Test Mode State	-	-	-	-	PU	-	-	I	-
K13	TDI	I	-	JTAG Test Data In	-	-	-	-	PU	-	-	I	-
J11	TDO	O	-	JTAG Test Data Out	-	-	-	-	-	4mA	-	O	H
J13	NTRST	I	N	JTAG Test Reset	-	-	-	-	PU	-	-	I	-
L10	PA12	I/O	-	General Purpose Port A12	I	-	SIO Receive Data	-	-	4mA	-	I	-
M8	PA11	I/O	-	General Purpose Port A11	O	-	SIO Transmit Data	-	-	4mA	-	I	-
A12	PA10	I/O	-	General Purpose Port A10	I/O	-	SSIO Communication Clock	-	-	4mA	-	I	-
C11	PA09	I/O	-	General Purpose Port A9	I	-	SSIO Receive Data	-	-	4mA	-	I	-
C10	PA08	I/O	-	General Purpose Port A8	O	-	SSIO Transmit Data	-	-	4mA	-	I	-
F2	PA07	I/O	-	General Purpose Port A7	I/O	-	SPI Clock for CH1	-	-	4mA	-	I	-
F4	PA06	I/O	-	General Purpose Port A6	I	N	SPI Slave Select for CH1	-	-	4mA	-	I	-
G4	PA05	I/O	-	General Purpose Port A5	I/O	-	SPI Data for CH1 (Master Receive / Slave Transmit)	-	-	4mA	-	I	-
G3	PA04	I/O	-	General Purpose Port A4	I/O	-	SPI Data for CH1 (Master Transmit / Slave Receive)	-	-	4mA	-	I	-
G1	PA03	I/O	-	General Purpose Port A3	I/O	-	SPI Clock for CH0	-	-	4mA	-	I	-
H1	PA02	I/O	-	General Purpose Port A2	I	N	SPI Slave Select for CH0	-	-	4mA	-	I	-
J4	PA01	I/O	-	General Purpose Port A1	I/O	-	SPI Data for CH0 (Master Receive / Slave Transmit)	-	-	4mA	-	I	-
F3	PA00	I/O	-	General Purpose Port A0	I/O	-	SPI Data for CH0 (Master Transmit / Slave Receive)	-	-	4mA	-	I	-
A7	PB11	I/O	-	General Purpose Port B11	O	-	Clock Output (for sensor)	-	-	4mA	-	I	-
A1	PB10	I/O	-	General Purpose Port B10	I	-	External Interrupt Input (for USB VBUS)	S	-	4mA	T	I	-
B1	PB09	I/O	-	General Purpose Port B09	I	-	External Interrupt Input (for IRQ 28)	S	-	4mA	-	I	-
C1	PB08	I/O	-	General Purpose Port B08	I	-	External Interrupt Input (for IRQ 30)	S	-	4mA	-	I	-
D3	PB07	I/O	-	General Purpose Port B07	I	-	External Interrupt Input (for FIQ)	S	-	4mA	-	I	-
H11	PB06	I/O	-	General Purpose Port B06	O	-	Smartcard IF Clock	-	-	4mA	-	I	-
G10	PB05	I/O	-	General Purpose Port B05	O	N	Smartcard IF Reset	-	-	4mA	-	I	-
G13	PB04	I/O	-	General Purpose Port B04	I/O	-	Smartcard IF Serial Data	-	-	4mA	-	I	-
E10	PB03	I/O	-	General Purpose Port B03	O	-	Smartcard IF Power Control	-	-	4mA	-	I	-
D11	PB02	I/O	-	General Purpose Port B02	O	-	Smartcard IF Voltage Control 1	-	-	4mA	-	I	-
C12	PB01	I/O	-	General Purpose Port B01	O	-	Smartcard IF Voltage Control 0	-	-	4mA	-	I	-
B12	PB00	I/O	-	General Purpose Port B00	O	-	Smartcard IF Card Detection	-	-	4mA	-	I	-
M10	PC11	I/O	-	General Purpose Port C11	I/O	-	Flexible Timer for CH1	-	PD	4mA	-	I	-
N10	PC10	I/O	-	General Purpose Port C10	I/O	-	Flexible Timer for CH0	-	PD	4mA	-	I	-
B11	PC09	I/O	-	General Purpose Port C09	I	-	Parallel IF Data7	-	PD	4mA	-	I	-
B8	PC08	I/O	-	General Purpose Port C08	I	-	Parallel IF Data6	-	PD	4mA	-	I	-
C8	PC07	I/O	-	General Purpose Port C07	I	-	Parallel IF Data5	-	PD	4mA	-	I	-
B7	PC06	I/O	-	General Purpose Port C06	I	-	Parallel IF Data4	-	PD	4mA	-	I	-
D7	PC05	I/O	-	General Purpose Port C05	I	-	Parallel IF Data3	-	PD	4mA	-	I	-
A2	PC04	I/O	-	General Purpose Port C04	I	-	Parallel IF Data2	-	PD	4mA	-	I	-
D6	PC03	I/O	-	General Purpose Port C03	I	-	Parallel IF Data1	-	PD	4mA	-	I	-
B6	PC02	I/O	-	General Purpose Port C02	I	-	Parallel IF Data0	-	PD	4mA	-	I	-

Pin No.	Pin name	Description						Schmitt	PU/PD(*1)	Drive capacity	5V Tolerant	Initial direction	Initial value
		Primary function			Secondary function								
		I/O	Polarity	Description	I/O	Polarity	Description						
A6	PC01	I/O	-	General Purpose Port C01	I	-	Parallel IF Synchronous Signal	-	PD	4mA	-	I	-
D5	PC00	I/O	-	General Purpose Port C00	I	-	Parallel IF Clock	-	PD	4mA	-	I	-
B3	DM	A	-	USB dev D-	-	-	-	-	-	-	-	I	-
D4	DP	A	-	USB dev D+	-	-	-	-	-	-	-	I	-
A5	PUCTL	O	P	USB dev Pull-up Control	-	-	-	-	-	4mA	-	O	L
H4	XA21	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
H2	XA20	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
J3	XA19	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
K3	XA18	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
K1	XA17	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
K4	XA16	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
L1	XA15	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
M2	XA14	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
N2	XA13	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
N3	XA12	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
L4	XA11	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
M3	XA10	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
N4	XA09	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
L5	XA08	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
M4	XA07	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
K5	XA06	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
M5	XA05	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
N6	XA04	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
K6	XA03	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
L6	XA02	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
M7	XA01	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
K7	XA00	O	-	External bus address signal	-	-	-	-	-	4mA	-	O	L
J12	XD15	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
H12	XD14	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
G11	XD13	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
F11	XD12	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
F10	XD11	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
F12	XD10	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
E12	XD09	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
E13	XD08	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
D13	XD07	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
B13	XD06	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
A11	XD05	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
A10	XD04	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
B10	XD03	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
A9	XD02	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
D9	XD01	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
B9	XD00	I/O	-	External bus data signal	-	-	-	-	PU	4mA	-	I	-
M9	XROMCSN	O	N	External ROM chip select	-	-	-	-	-	4mA	-	O	H
N8	XRAMCSN	O	N	External RAM chip select	-	-	-	-	-	4mA	-	O	H
K8	XIO0CSN	O	N	External IO chip select	-	-	-	-	-	4mA	-	O	H
N9	XREN	O	N	External bus read enable	-	-	-	-	-	4mA	-	O	H
L9	XWEN	O	N	External bus write enable	-	-	-	-	-	4mA	-	O	H
M12	XBSN1	O	N	External bus byte select	-	-	-	-	-	4mA	-	O	H

Pin No.	Pin name	Description						Schmitt	PU/PD(*1)	Drive capacity	5V Tolerant	Initial direction	Initial value
		Primary function			Secondary function								
		I/O	Polarity	Description	I/O	Polarity	Description						
N12	XBSN0	O	N	External bus byte select	-	-	-	-	-	4mA	-	O	H
K10	XWAIT0N	I	N	External IO access wait	-	-	-	-	PU	-	-	I	-
N13	BSEL1	I	P	Boot Device Select 1	-	-	-	-	PD	-	-	I	-
C13	BSEL0	I	P	Boot Device Select 0	-	-	-	-	PD	-	-	I	-
K2	PR1	I	P	Input Port	-	-	-	-	PD	-	-	I	-
H10	PR0	I	P	Built-in ROM Port0 (*2)	-	-	-	-	PU	-	-	I	-
D8	AFSEL	I	P	JTAG Select (ARM/FLASH)	-	-	-	-	PD	-	-	I	-
H3	TESTE	I	P	Test Mode Select	-	-	-	-	PD	-	-	I	-
A13	TESTF	A	-	FLASH Test Pin	-	-	-	-	-	-	-	A	-
F13 K11 B4 C3 L2 L7	VDDCORE	-	-	1.8V Power Supply for CORE	-	-	-	-	-	-	-	-	-
K12 D12 L8 C5 C2 M1	GNDCORE	-	-	Ground for CORE	-	-	-	-	-	-	-	-	-
H13 N11 E11 C9 N7 C7 N5 A4 J2 N1 F1	VDDIO	-	-	3.3V Power Supply for IO	-	-	-	-	-	-	-	-	-
M13 G12 D10 K9 A8 M6 B5 L3 A3 J1 E1	GNDIO	-	-	Ground for IO	-	-	-	-	-	-	-	-	-
E3	VDDPLL	-	-	1.8V Power Supply for PLL	-	-	-	-	-	-	-	-	-
D2	GNDPLL	-	-	Ground for PLL	-	-	-	-	-	-	-	-	-
C4	VDDUSB	-	-	3.3V Power Supply for USB	-	-	-	-	-	-	-	-	-
B2	GNDUSB	-	-	Ground for PLL	-	-	-	-	-	-	-	-	-

*1: PU/PD column:
PU: Pulled up with a built-in resistor
PD: Pulled down with a built-in resistor
*2: This pin is used in the Built-in ROM for an update function of the Built-in FlashROM.

For details, see the User's manual for USB firmware update function.

Termination of Pins Not Used

Pin name	Pin termination
DM, DP, PUCTL	Open
PA00-12 PB00-11, PC00-11	Pulled down
TDO, RTCK	Open
TCK, TMS, TDI, NTRST	Pulled up
XA00-21, XROMCSN, XRAMCSN, IO0CSN, XREN, XWRN, XBSN1, XBSN0	Open
XD00-15, XWAIT0N	pulled up
TESTF	Must be used as open

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage CORE (1.8 V)	V_{DD_CORE}	—	−0.3 to +2.5	V
PLL power supply voltage (1.8 V)	V_{DD_PLL}			
Digital power supply voltage I/O (3.3 V)	V_{DD_IO}	—	−0.3 to +4.6	
USB power supply voltage I/O (3.3 V)	V_{DD_USB}			
Input voltage (normal buffer)	V_I	—	−0.3 to V_{DD_IO}+0.3	
Input voltage (5 V tolerant)		V_{DD_IO} = 3.0 V to 3.6 V	−0.3 to +6.0	
		V_{DD_IO} < 3.0 V	−0.3 to V_{DD_IO}+0.3	
Output voltage	V_O	—	−0.3 to V_{DD_IO}+0.3	
Input allowable current	I_I	—	−10 to +10	mA
“H” output allowable current	I_{OH}	—	+10	
“L” output allowable current	I_{OL}	—	−10	
Power dissipation	P_D	T_a = 85°C	601	mW
Storage temperature	T_{STG}	—	−50 to 150	°C

GUARANTEED OPERATING RANGES

(GND = 0 V)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply voltage (CORE) (*1)		V_{DD_CORE}	—	1.62	1.8	1.98	V
PLL power supply voltage (*1)		V_{DD_PLL}		1.62	1.8	1.98	
Digital power supply voltage (I/O)		V_{DD_IO}		3.0	3.3	3.6	
USB power supply voltage		V_{DD_USB}		3.0	3.3	3.6	
CPU operating frequency		f_{BUSCLK}		-	32	-	MHz
Ambient temperature		T_a		–40	25	85	°C
	Flash read	T_{a_fread}		–40	25	85	
	Flash write	T_{a_fwrite}		–40	25	85	
Flash write count		C_{WR}		-	-	10,000	cycle

* 1: Please supply from same power source to both V_{DD_CORE} pins and V_{DD_PLL} pin.

ELECTRICAL CHARACTERISTICS

DC Characteristics

DC characteristics (Core/IO)

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	2.0	—	V_{DD_IO} +0.3	V
"L" input voltage	V_{IL}	—	−0.3	—	0.8	
Schmitt trigger input threshold voltage(3.3V)	V_{T+}	—	—	—	2.0	
	V_{T-}		0.6	—	—	
Schmitt trigger input threshold voltage (5 V tolerant)	V_{T+}	—	—	—	2.0	
	V_{T-}		0.6	—	—	
"H" output voltage	V_{OH}	I_{OH} = −4 mA	2.4	—	—	
"L" output voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	
High level input current (*1)	I_{IH}	V_{IH} = V_{DD_IO}	—	—	10	μA
		pull-down	30	—	140	
High level input current (*2)		V_{IH} = V_{DD_IO}	—	—	10	
		V_{IH} = 5.5 V	—	—	30	
Low level input current (*1)	I_{IL}	V_{IL} = 0 V	−10	—	—	
		pull-up	−140	—	−30	
Low level input current (*2)		V_{IL} = 0 V	−10	—	—	
3-state output leakage current	I_{OZH}	V_{OH} = V_{DD_IO}	—	—	10	μA
		pull-down	30	—	140	
	I_{OZL}	V_{OL} = 0 V	−10	—	—	
		pull-up	−140	—	−30	
Supply current (during STOP) (*4)	I_{DDS_CORE}	—	—	80	1500	μA
	I_{DDS_IO}	(*3)	—	4	20	
	I_{DDS_PLL}	—	—	2	10	
Supply current (during operation) (*5)	I_{DDO_CORE}	f_{BUSCLK} = 32.0 MHz	—	50	70	mA
	I_{DDO_IO}	(*3) (*6)	—	5	10	
	I_{DDO_PLL}	—	—	1	3	

*1: Pins other than 5 V tolerant pins
*2: 5 V tolerant pins
*3: Input ports: VDD_IO or 0 V
Other ports: No load excluding the current flowing in pull-up/pull-down resistors
*4: LSI supply current when going into LSI stop mode by stopping clock oscillation, PLL operation, and random number generator operation and setting USB power-down mode.
*5: The current supplied to the LSI when fingerprint authentication is executed without USB operation under the conditions that the programs are stored in the built-in Flash ROM and no external memory are connected.
*6: Clock pulse is driven to XI clock input pin.

DC characteristics (USB)

(V_{DD_CORE} = 1.62 to 1.98V, V_{DD_USB} = 3.0 to 3.6V, Ta = –40 to +85°C)

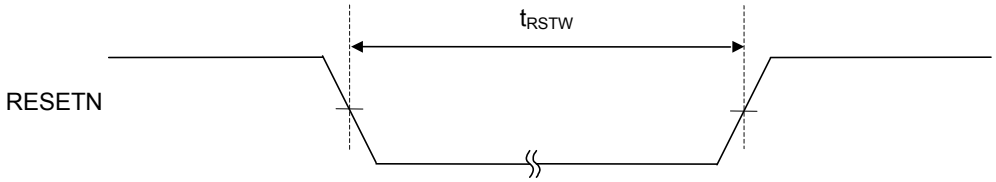
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential input sensitivity	V_{DI}	Absolute value of the difference between the DP and DM pins	0.2	—	—	V
Differential common mode range	V_{CM}	Includes VDI range	0.8	—	2.5	V
Single end input threshold voltage	V_{SE}		0.8	—	2.0	V
High level output voltage	V_{OH}	15K W RL is connected to GND	2.8	—	—	V
Low level output voltage	V_{OL}	1.5K W RL to 3.6 V	—	—	0.3	V
Hi-Z state input/output leakage current	I_{LO}	0 V < VIN < 3.3 V	–10	—	10	μA
Driver output resistance	Z_{DRV}	Steady state	28	—	44	Ω

AC Characteristics

Reset Timing

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset pulse width	t_{RSTW}	—	6.0	—	—	ms



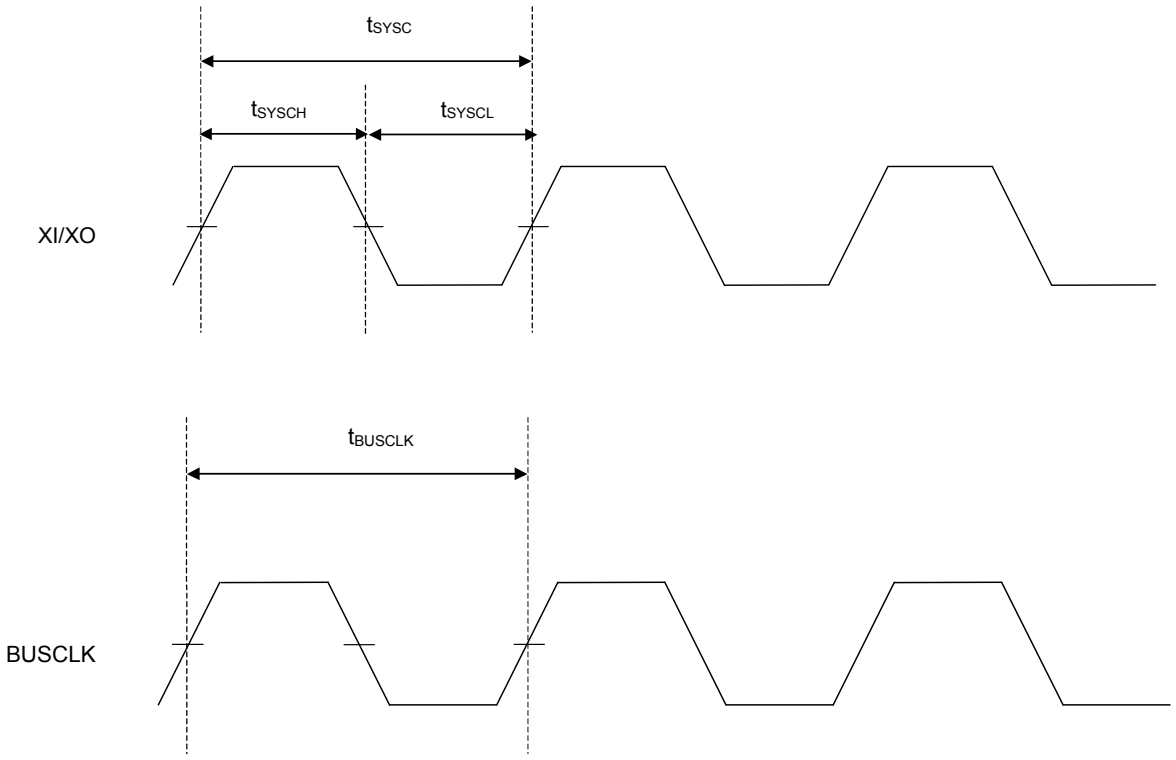
*When power on, release the reset after the clock oscillation stabilization.

Main Clock Timing

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Main clock (XI/XO) frequency	f_{SYSC}	—	12 × 0.9975	12	12 × 1.0025	MHz
Main clock (XI/XO) cycle	t_{SYSC}	—	83.33 × 0.9975	83.33	83.33 × 1.0025	ns
Main clock (XI/XO) H pulse width	t_{SYSCH}	—	0.45 × t_{SYSC}	—	0.55 × t_{SYSC}	ns
Main clock (XI/XO) L pulse width	t_{SYSCL}	—	0.45 × t_{SYSC}	—	0.55 × t_{SYSC}	ns
Bus clock frequency (*1)	f_{BUSCLK}	—	—	32	—	MHz
Bus clock cycle (*1)	t_{BUSCLK}	—	—	31.25	—	ns

* 1: Main system bus clock within the LSI and operating clocks of CPU, DMA, etc.



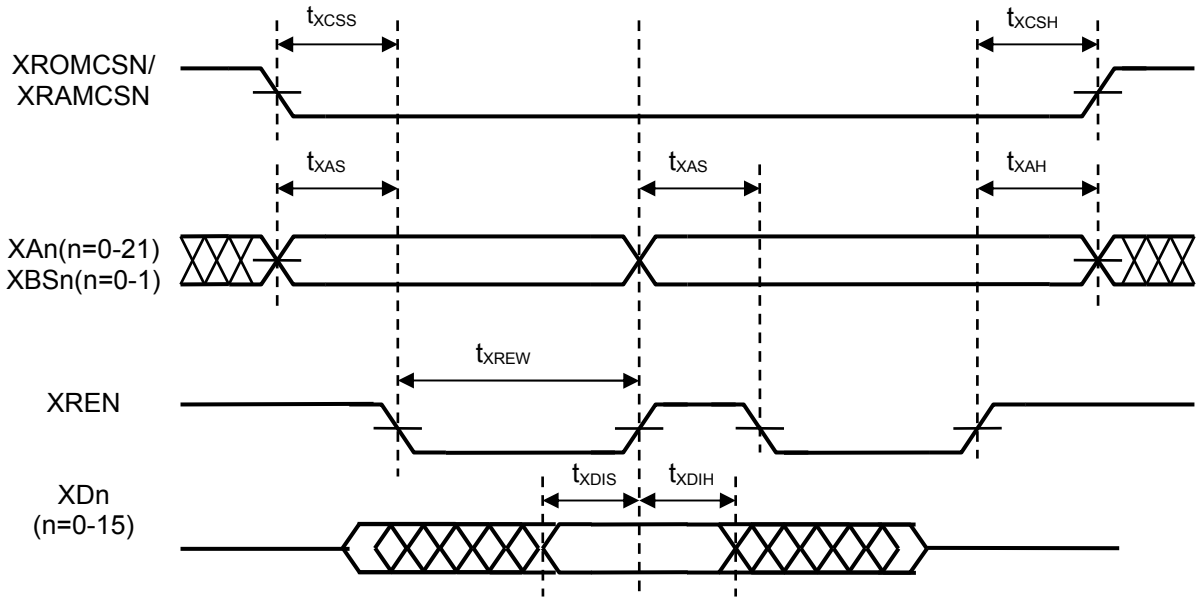
External ROM/ External RAM Timing

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

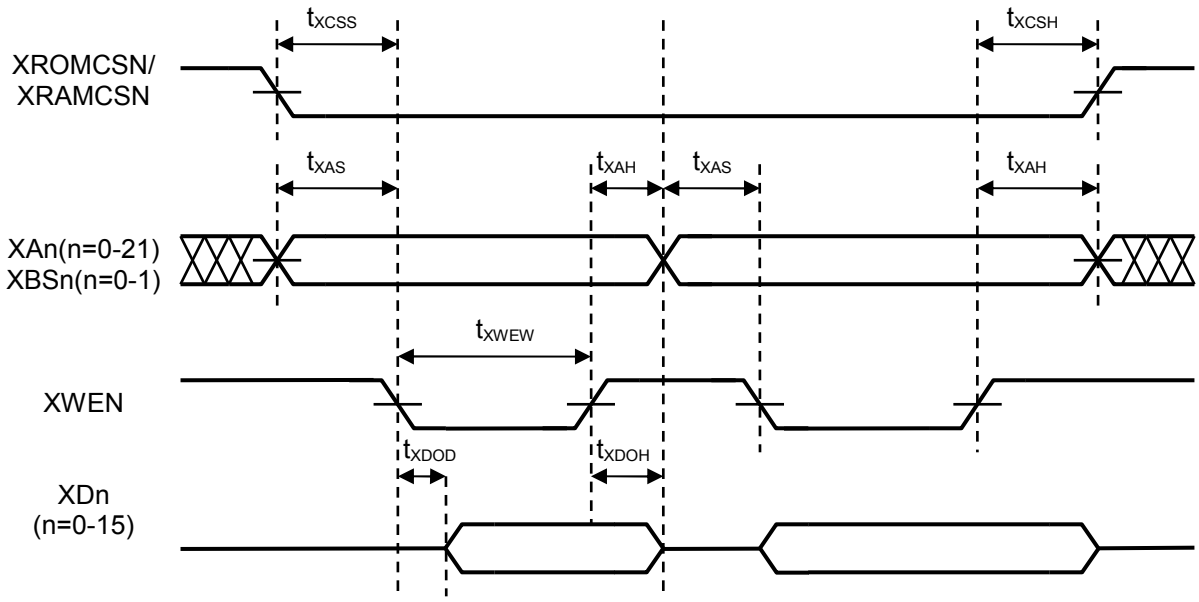
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XROMCSN, XRAMCSN output setup time	t_{XCSS}	C_L = 15pF	t_{ASETUP} - 6	-	t_{ASETUP} + 6	ns
XROMCSN, XRAMCSN output hold time	t_{XCSH}		t_{BUSCLK} - 6	-	t_{BUSCLK} + 6	
XA, XBSN output setup time	t_{XAS}		t_{ASETUP} - 6	-	t_{ASETUP} + 6	
XA, XBSN output hold time	t_{XAH}		t_{BUSCLK} - 6	-	t_{BUSCLK} + 6	
XREN pulse width	t_{XREW}		t_{RWIDTH} - 15	-	t_{RWIDTH} + 15	
XWEN pulse width	t_{XWEW}		t_{WWIDTH} - 15	-	t_{WWIDTH} + 15	
XD input setup time	t_{XDIS}		22.5	-	-	
XD input hold time	t_{XDIH}		0	-	-	
XD output setup time	t_{XDOD}		-6	-	+6	
XD output hold time	t_{XDOH}		t_{BUSCLK} - 6	-	t_{BUSCLK} + 6	

t_{ASETUP}: Address setup time (set by register)
t_{RWIDTH}: RE pulse width (set by register)
t_{WWIDTH}: WE pulse width (set by register)
t_{DOFF}: Data-off wait time (set by register)

External ROM/ External RAM read timing



External ROM/ External RAM write timing



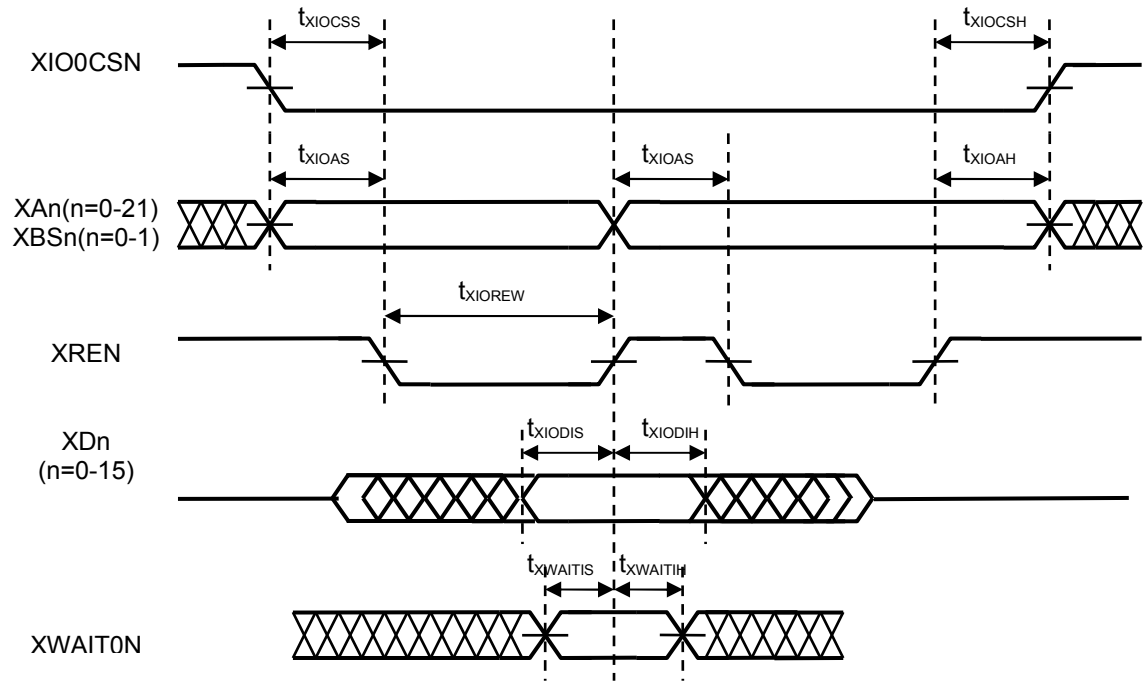
External IO Timing

(V_{DD_CORE} = 1.62 to 1.98V, V_{DD_IO} = 3.0 to 3.6V, T_a = -40 to +85°C)

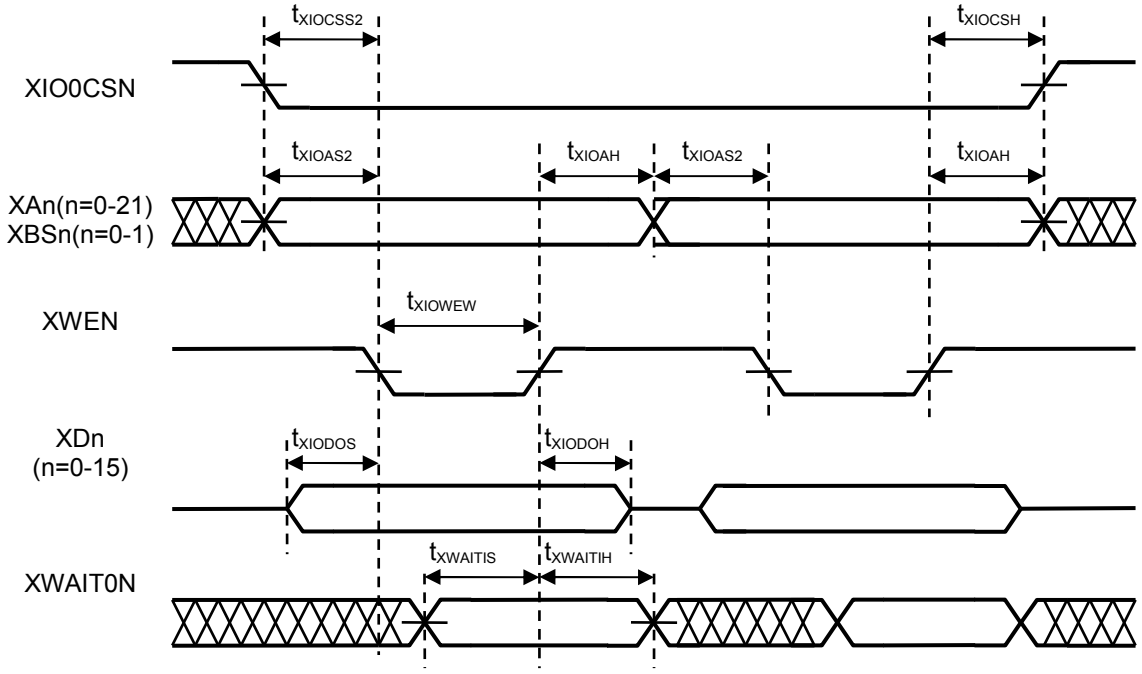
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XIO0CSN output setup time	$t_{XIOCSS1}$	C_L = 15pF	t_{IOAS} - 8	-	t_{IOAS} + 8	ns
XIO0CSN output setup time 2	$t_{XIOCSS2}$		t_{BUSCLK} +t_{IOAS} - 8	-	t_{BUSCLK} +t_{IOAS} + 8	
XIO0CSN output hold time	t_{XIOCSH}		t_{BUSCLK} - 6	-	t_{BUSCLK} + 6	
XA, XBSN output setup time	t_{XIOAS}		t_{IOAS} - 8	-	t_{IOAS} + 8	
XA, XBSN output setup time 2	t_{XIOAS2}		t_{BUSCLK} +t_{IOAS} - 8	-	t_{BUSCLK} +t_{IOAS} + 8	
XA, XBSN output hold time	t_{XIOAH}		t_{BUSCLK} - 6	-	t_{BUSCLK} + 6	
XREN pulse width	t_{XIOREW}		$t_{IORWIDTH}$ - 10	-	$t_{IORWIDTH}$ + 10	
XWEN pulse width	t_{XIOWEW}		$t_{IOWWIDTH}$ - 10	-	$t_{IOWWIDTH}$ + 10	
XD input setup time	t_{XIODIS}		20	-	-	
XD input hold time	t_{XIODIH}		0	-	-	
XD output setup time	t_{XIODOD}		t_{IOAS} - 13	-	t_{IOAS} + 13	
XD output hold time	t_{XIODOH}		t_{BUSCLK} - 15	-	t_{BUSCLK} + 15	
XWAIT0N input setup time	$t_{XWAITIS}$		t_{BUSCLK} + 20	-	-	
XWAIT0N input hold time	$t_{XWAITIH}$		0	-	-	

t_{IOAS}: Address setup time (set by register)
$t_{IORWIDTH}$: RE pulse width (set by register)
$t_{IOWWIDTH}$: WE pulse width (set by register)
t_{IODOFF}: Data-off wait time (set by register)

External IO read timing



External IO write timing



USB Access Timing (Full-Speed)

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_USB}= 3.0 to 3.6 V, T_a = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied pin
Rise time (*1)	T_R	CL = 50 pF	4	—	20	ns	DP, DM
Fall time (*1)	T_F	CL = 50 pF	4	—	20	ns	
Output signal crossover voltage	V_{CRS}	CL = 50 pF	0.8	—	2.5	V	
Data rate	T_{DRATE}	Average bit rate (12Mbps ±0.25%)	11.97	—	12.03	Mbps	

*1 TR and TF are transition time from 10% to 90% of V_{DD_USB}.

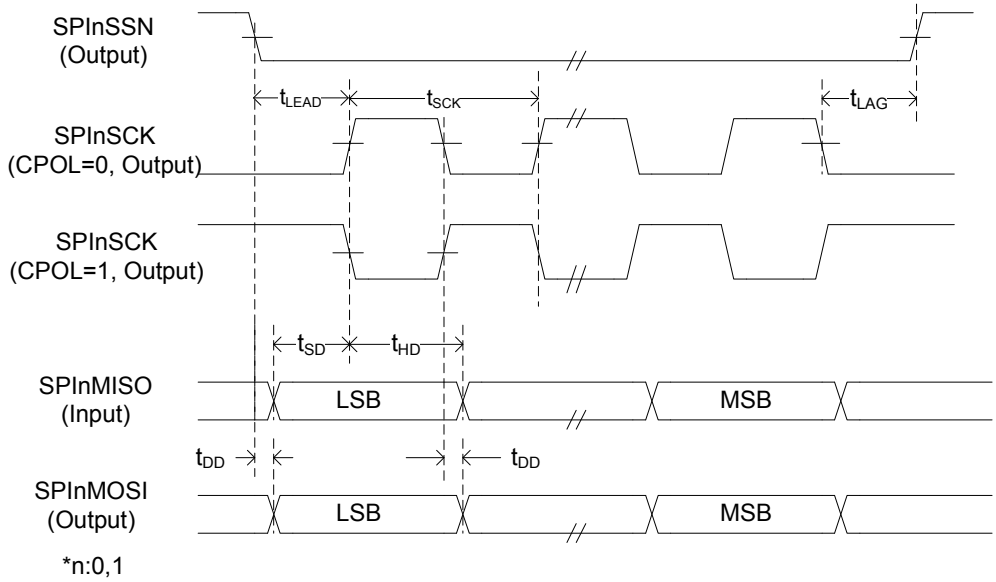
SPI Access Timing
- Characteristics of master mode timing

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

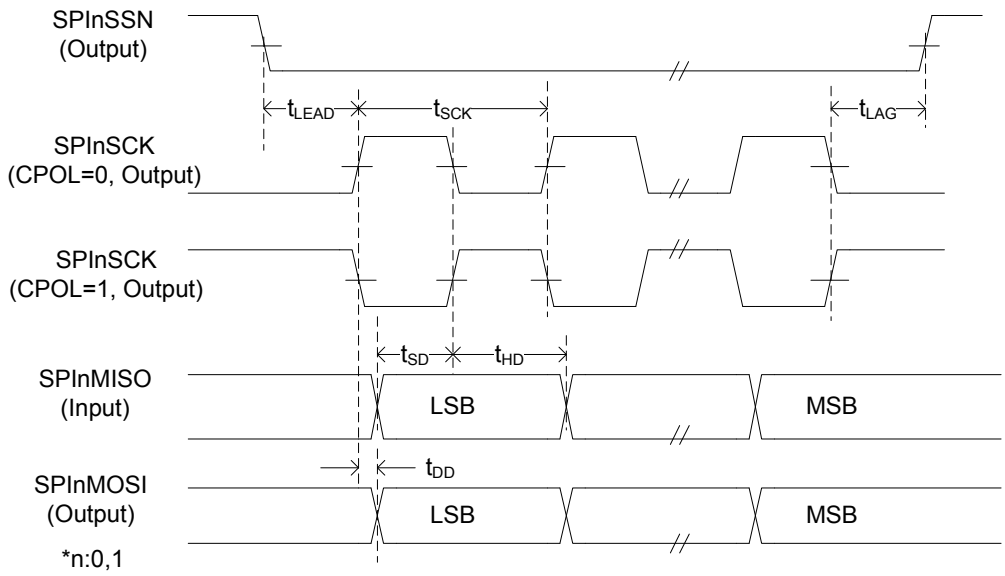
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data delay time (output)	t_{DD}	CL = 30 pF	—	—	25	ns
Data setup time (input)	t_{SD}		25	—	—	ns
Data hold time (input)	t_{HD}		0 (*1)	—	—	ns
SPInSSN-SPInSCK lead time	t_{LEAD}		0.5*t_{SCK} –15	—	0.5*t_{SCK} +15	ns(*2)
SPInSCK-SPInSSN lag time	t_{LAG}		0.5*t_{SCK} –15	—	0.5*t_{SCK} +15	ns(*2)

* 1: Although actual values may become negative depending on the external load, input the serial data so that the data hold time can be guaranteed.
* 2: tSCK is the cycle time of the serial clock for SPI transferring which is obtained by dividing the frequency of the bus clock, whose cycle time is tBUSCLK.

SPI master mode timing (CPHA = 0)



SPI master mode timing (CPHA = 1)

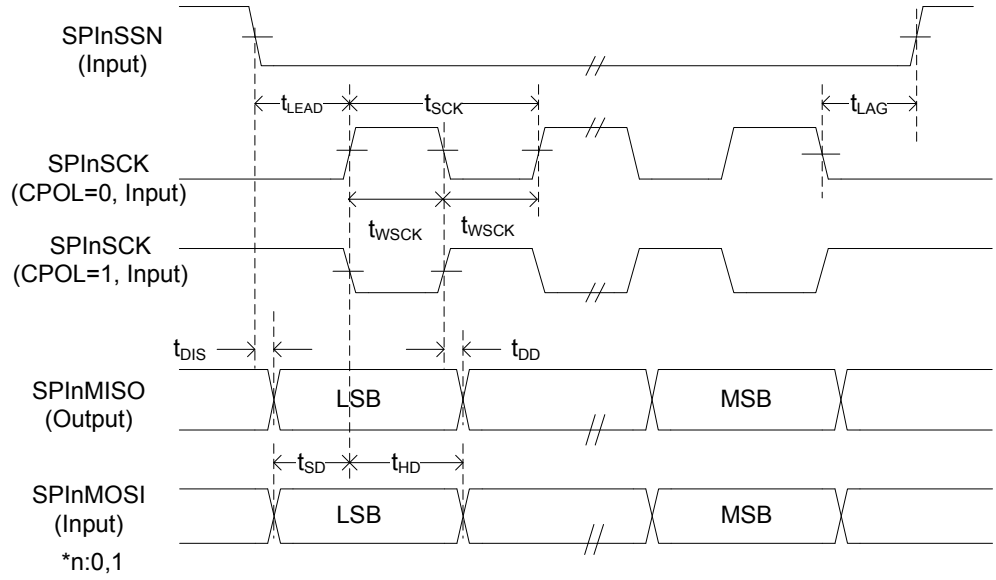


- Characteristics of slave mode timing

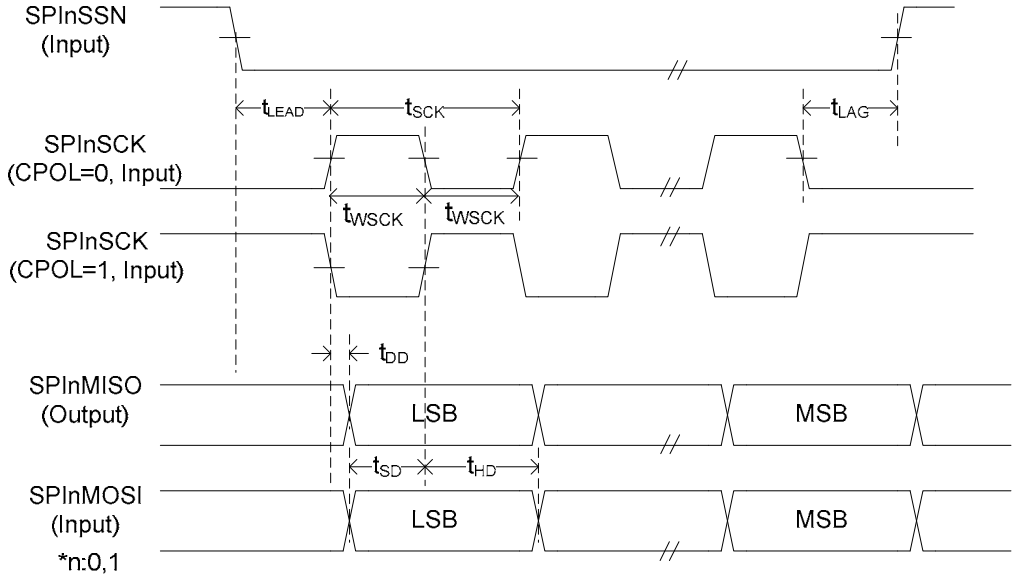
(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial clock cycle time	t_{SCK}	CL = 30 pF	2	—	—	t_{BUSCLK}
Serial clock High/Low time	t_{WSCK}		1	—	—	t_{BUSCLK}
Data delay time (output)	t_{DD}		—	—	25	ns
Data setup time (input)	t_{SD}		25	—	—	ns
Data hold time (input)	t_{HD}		25	—	—	ns
SPInSSN-SPInSCK lead time	t_{LEAD}		25	—	—	ns
SPInSCK-SPInSSN lag time	t_{LAG}		t_{BUSCLK} + 15	—	—	ns
Slave data invalid time	t_{DIS}		—	—	25	ns

SPI slave mode timing (CPHA = 0)



SPI slave mode timing (CPHA = 1)



Synchronous SIO Access Timing

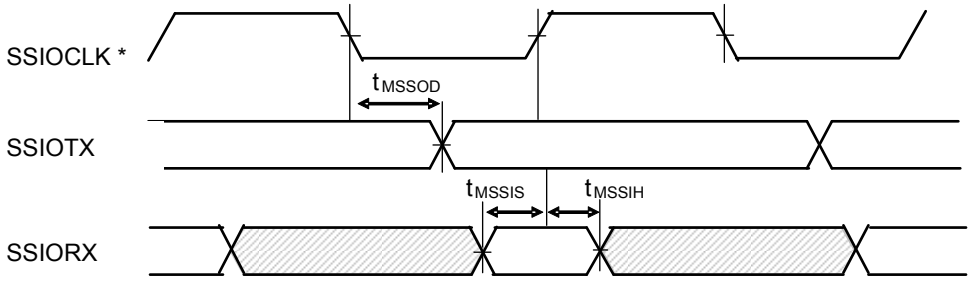
Switching between master mode and slave mode can be set for this synchronous SIO by the software register setting. Serial clock polarity can be switched.
When clock polarity is set to positive, data is transmitted (shifted out) on the falling edge of the clock and is received (shifted in) on the rising edge of the clock. At completion of 8-bit data transmission/reception, the clock stops at a high level and the last data is retained for data output.
When clock polarity is set to negative, data is transmitted (shifted out) on the rising edge of the clock and is received (shifted in) on the falling edge of the clock. At completion of 8-bit data transmission/reception, the clock stops at a low level and the last data is retained for data output.
The following waveforms show the cases where the clock polarity is positive.

– Master mode

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output data delay time	t_{MSSOD}	CL = 30 pF	—	—	20	ns
Input data setting time	t_{MSSIS}		30	—	—	
Input data retained time	t_{MSSIH}		10	—	—	

Note:
11 clock outputs for transferring is selectable from 2 synchronous SIO clock sources and the frequency divide ratios.

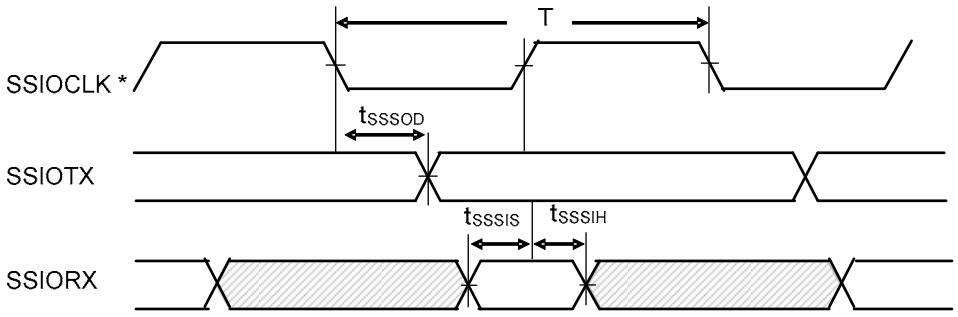


* Serial clock: Positive polarity

– Slave mode

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial clock cycle	T	CL = 30 pF	62.5	—	—	ns
Output data delay time	t_{SSSOD}		—	—	40	
Input data setting time	t_{SSSIS}		20	—	—	
Input data retained time	t_{SSSIH}		20	—	—	



* Serial clock: Positive polarity

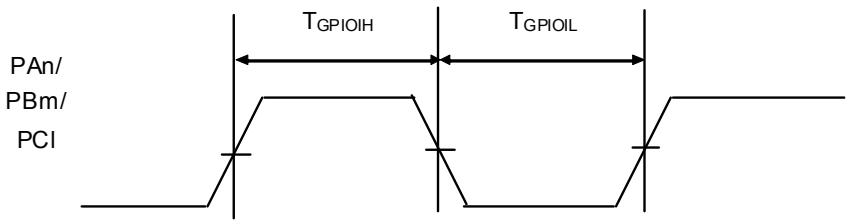
GPIO (PA, PB, PC) Access Timing

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PAn, PBm, PCl input H duration	T_{GPIOIH}	—	t_{BUSCLK} ×2	—	—	ns
PAn, PBm , PCl input L duration	T_{GPIOIL}	—	t_{BUSCLK} ×2	—	—	ns

Note 1: n = 12 to 0, m=11 to 0, l = 11 to 0

PAn, PBm and PCl input timing (n = 12 to 0, m = 11 to 0, l = 11 to 0)



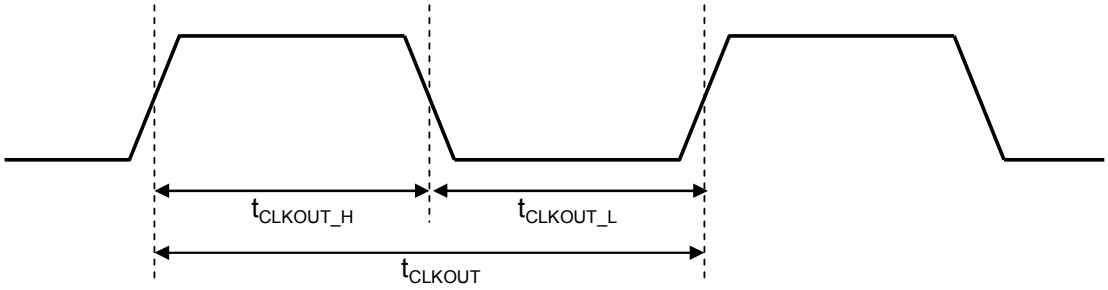
Clock Output (Secondary Function of PB11 Pin) Timing

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, T_a = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock output High duration	t_{CLKOUT_H}	—	45% × t_{CLKOUT}	50% × t_{CLKOUT}	55% × t_{CLKOUT}	ns(*1)
Clock output Low duration	t_{CLKOUT_L}	—	45% × t_{CLKOUT}	50% × t_{CLKOUT}	55% × t_{CLKOUT}	ns(*1)

*t_{CLKOUT} is the cycle time of the 6 MHz or 12 MHz clock generated by 2 clock sources and the frequency divide ratio.

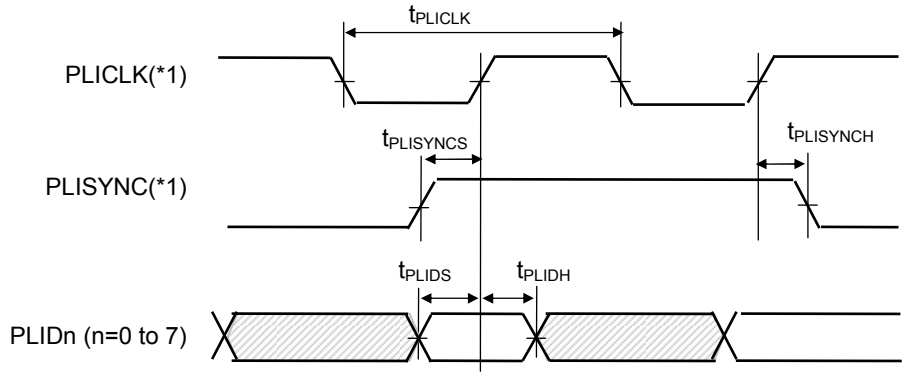
Clock output (secondary function of PB11 pin) timing



8-bit Parallel IO Access Timing

(V_{DD_CORE} = 1.62 to 1.98 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PLICLK cycle time	t_{PLICLK}	CL=30pF	74	-	-	ns
PLICLK to PLISYNC setup time (input)	$t_{PLISYNCS}$		10	-	-	ns
PLICLK to PLISYNC hold time(input)	$t_{PLISYNCH}$		5	-	-	ns
PLID data setup time (input)	t_{PLIS}		10	-	-	ns
PLID data hold time(input)	t_{PLIDH}		5	-	-	ns



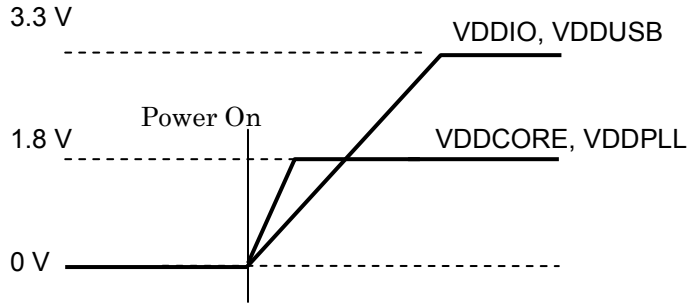
*1 PLI clock : Positive polarity

*2 PLISYNC : Positive polarity

POWER ON / OFF SEQUENCE

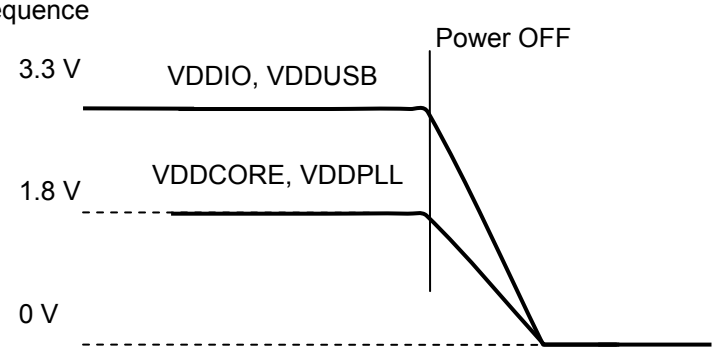
Power ON sequence
- Core(VDDCORE,VDDPLL) and IO(VDDIO, VDDUSB) power should be on at the same time, or IO(VDDIO, VDDUSB) power should be on after Core(VDDCORE,VDDPLL) on.

Power ON Sequence

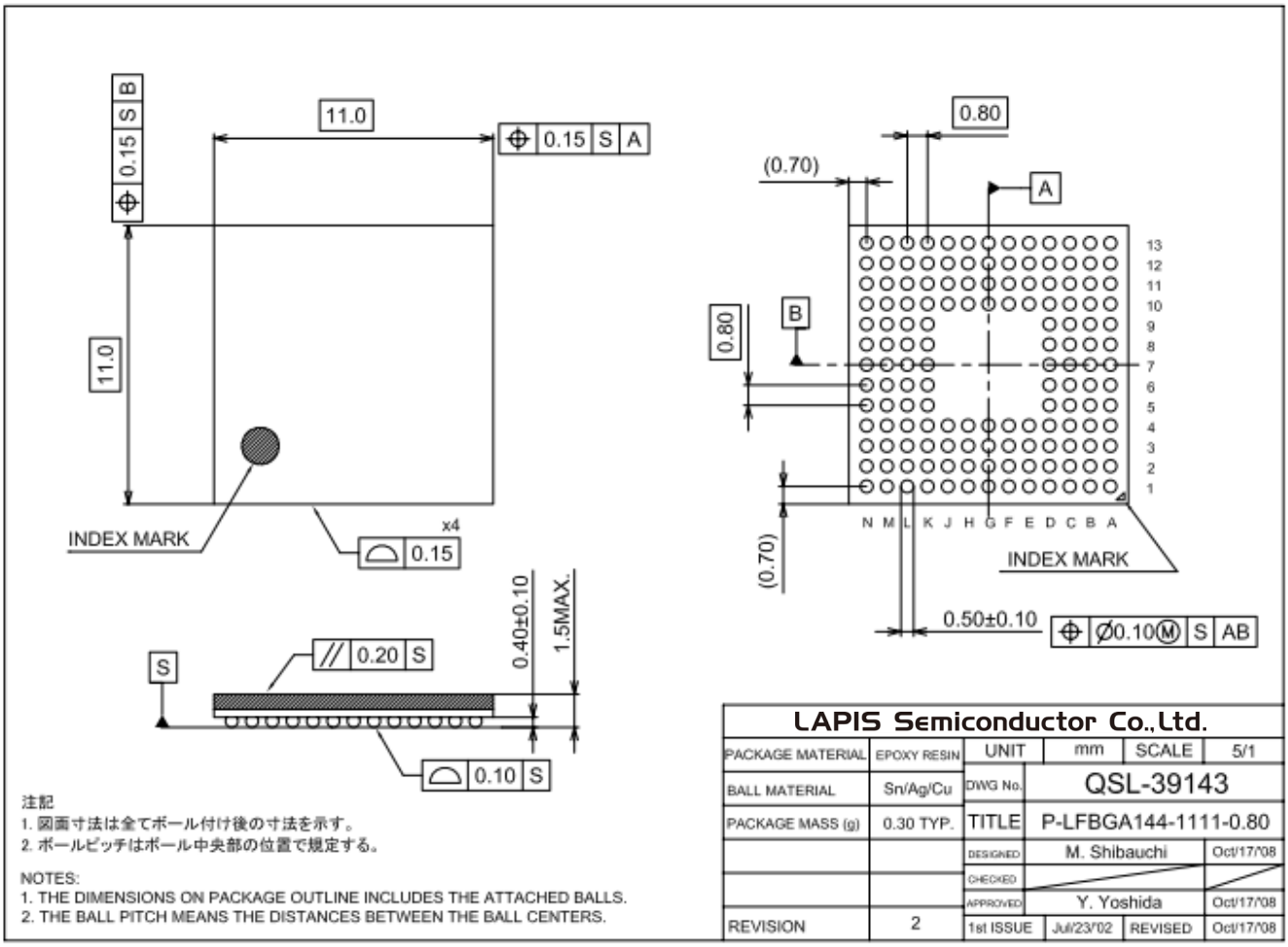


Power OFF sequence
- Core(VDDCORE,VDDPLL) and IO(VDDIO, VDDUSB) power should be off at the same time, or Core(VDDCORE,VDDPLL) power should be off after IO(VDDIO, VDDUSB) off.

Power OFF Sequence



PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contactROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL67Q5270-01	Sep.15, 2010	29	29	Final edition 1
FEDL67Q5270-02	Jul.1, 2011	1	1	Applicable fingerprint sensor AES1711 is deleted.

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