Laboratory Experiment 7
EE348L

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Table of Contents

Table of Figures

7 Experiment #7: MOSFETs Continued

7.1 Introduction

Laboratory experiment 6 introduced the MOSFET canonic cells used in MOSFET amplifier design. The ac small-signal model was presented for each canonic cell, and was used to discuss its performance. What the previous lab didn't clearly present are the limitations of the canonic cells. These limitations are one reason why circuits don't comprise of just a single stage that incorporates a single canonic cell. An integrated circuit amplifier doesn't consist on just one common-source amplifier. To be sure, a common-source canonic cell(s) may be used in the amplifier topology, but other elements and canonic cells are also used to address the performance limitations of the amplifier. Another example is the voltage buffer. A voltage buffer in an integrated circuit design doesn't consist of a single common-drain (source follower) canonic cell. As you probably discovered in the previous lab, the gain of a common-drain (source follower) amplifier is less than unity, and depending on the MOS technology used, it can be considerably less than one. This lab will present ways to combine the canonic cells in order to overcome certain inherent limitations of a single cell. The design strategies and topologies presented here are not comprehensive of all the possible solutions known to overcome the limitations of MOSFET amplifiers. However, they should give you insight into how to approach practical problems in MOSFET analog integrated circuit design.

7.2 A systematic procedure for biasing a common-source amplifier

In laboratory experiment 6 we simply calculated the gain of the common-source amplifier without doing any design procedure. However, we familiarized ourselves with the gain equation and how it is impacted by circuit components. In this section, we will look at the systematic procedure for biasing a common-source amplifier for a given set of design criteria. The common-source amplifier can be seen in **Figure 7-1.** The following are the design criteria:

Voltage gain = A = 20dB = 10
Vdd: 10V
Rl: As low as 10kΩ
No clipping is allowed.

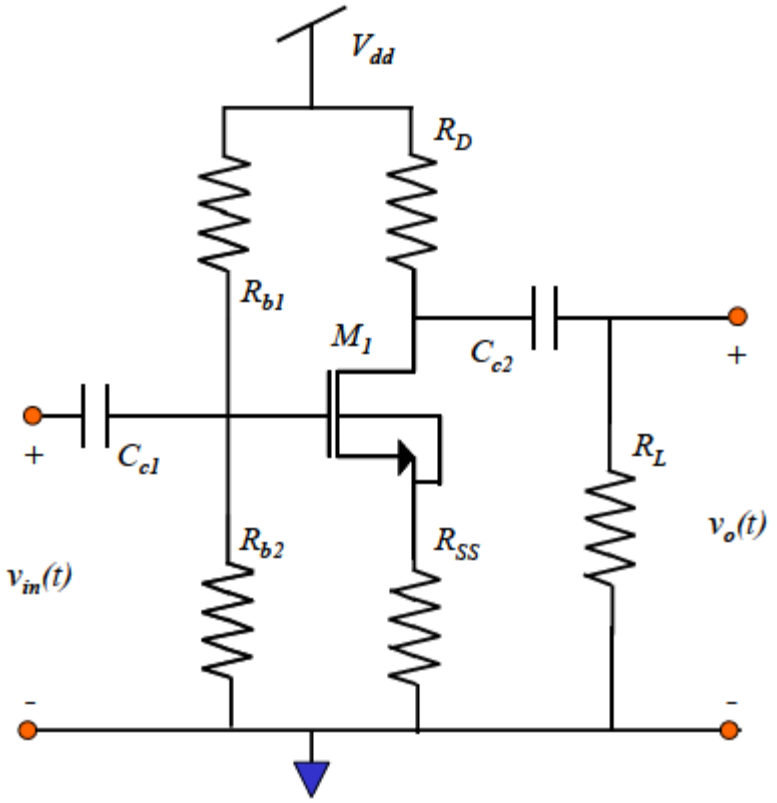

Figure 7-1: Common-source amplifier with variable load impedance RL.

The first thing we do is to set V_D to Vdd/2 so as to minimize the chance of any clipping.

$$V_D = \frac{Vdd}{2} = Vdd - I_D R_D \tag{7.1}$$

We then solve for R_D from the gain equation.

$$A = \frac{gm(R_D \,//\, Rl)}{1 + gmRss} = \frac{gm(R_D Rl)}{(1 + gmRss)(R_D + Rl)} \tag{7.2}$$

This leads to

$$R_D = \frac{ARl(1 + gmRss)}{gmRl - A(1 + gmRss)} \tag{7.3}$$

We then plug this back in to equation 7.1 to get

$$\frac{Vdd}{2} = Vdd - \frac{AI_D Rl(1 + gmRss)}{gmRl - A(1 + gmRss)} \tag{7.4}$$

Which leads to

$$\frac{Vdd}{2} = \frac{AI_D Rl(1 + gmRss)}{gmRl - A(1 + gmRss)} \tag{7.5}$$

Now, we use the following relationship between I_D and gm:

$$gm = \sqrt{2Kn\frac{W}{L}I_D} \qquad \text{or} \qquad I_D = \frac{gm^2}{2Kn\frac{W}{L}} \tag{7.6}$$

Plugging this into equation 7.5 leads to the following second order equation in terms of gm:

$$\frac{Vdd}{2} = \frac{Agm^2 Rl(1 + gmRss)}{2Kn\frac{W}{L}[gmRl - A(1 + gmRss)]} \tag{7.7}$$

Using equation 7.7 we can solve for gm in terms of A, Rl, Vdd, and Rss. The first three values are given to us while Rss can be chosen.

NOTE: If A, Rl, Vdd, and Rss are not chosen properly, we will get only negative or imaginary solutions to the second order equation. This means the circuit topology will not work. In other words, this circuit will only work if: A is not too big, Rl is not too small, Vdd is not too small, Rss is not too big.

We can use the value for Kn that we found in pre-lab exercise 1 which should be roughly 250 uA/V^2. The gate aspect ratio is 3,200 for these transistors. By letting Rss be 500Ω, we get the following result:

$$gm = 6.5\frac{mA}{V} \qquad gm = 2.3\frac{mA}{V}$$

These solutions lead to

$$I_D = .264mA \qquad I_D = 33uA$$

NOTE: The second solution, I_D = 33uA is not a valid solution because it implies that the transistor is in the subthreshold operation region. This can be found by plotting log(I_D) VS Vgs (while keeping the transistor saturated) and finding where the plot leaves the linear region. This happens at about I_D=100uA.

We can then find R_D by

$$V_D = \frac{Vdd}{2} = Vdd - I_D R_D$$

Which yields

$$R_D = 18.94k\Omega$$

The next step is to find what Vgs is necessary to produce 264uA of current through the transistor. This can be done by choosing a value for Rb1 and varying Rb2 until we get $Vss=I_DRss=264uA*500\Omega=.132V$. You will use a potentiometer to do this in the lab, and a DC sweep in HSpice for the pre-lab. **Figure 7-2** shows the dc sweep for Rb2 with Rb1=10k that produces a Vss=.132V.

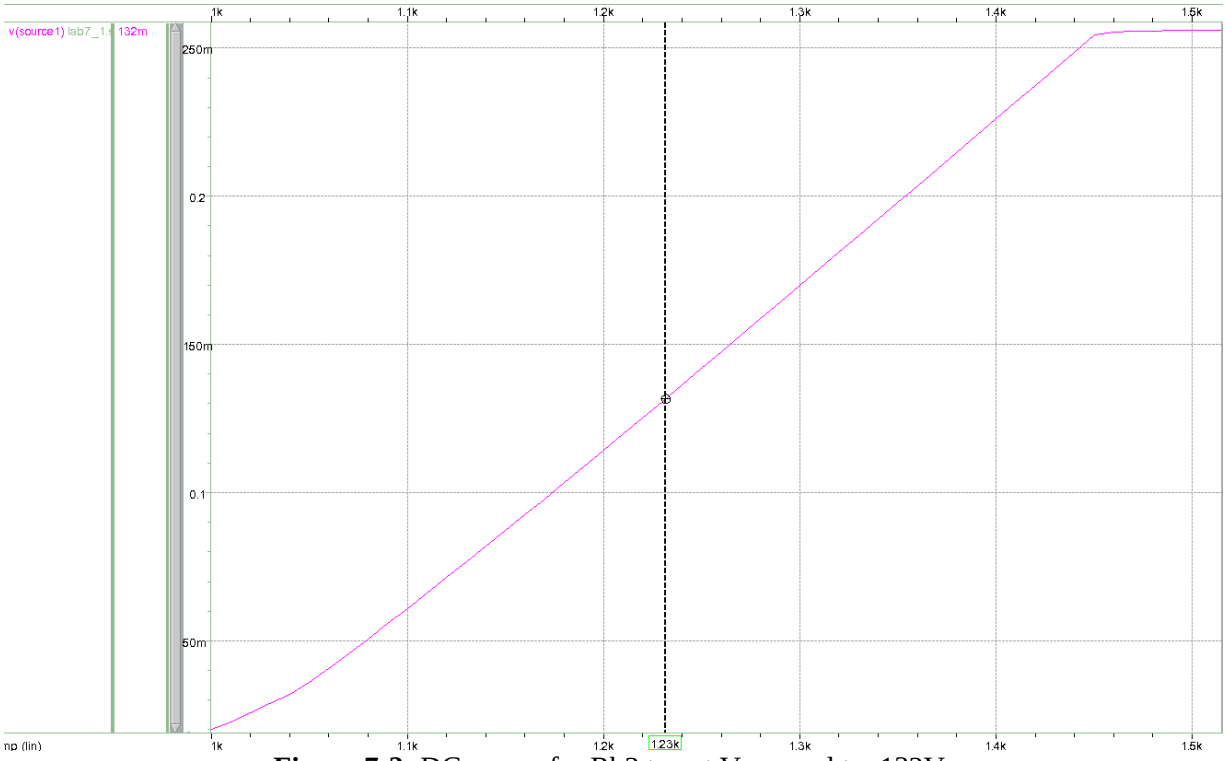

Figure 7-2: DC sweep for Rb2 to get Vss equal to .132V

From the plot we see that for Rb2=1.23kΩ, we get a Vss of .132 or a drain current of 264uA. Now we have our finalized design:

Rb1=10k
Rb2=1.23k
Rss=500
R_D=18.94k
I_D=.264mA
Vg=1.095V
Vss=.132V

The next step is to perform ac and transient analyses with a sin wave with amplitude of 50mV and a frequency of 10 kHz. These are plotted for this design example in **Figure 7-3** and **Figure 7-4**. The ac sweep is to verify the gain over frequency we desire. The transient sweep is to verify the amplifier does not go out of saturation or clip.

NOTE: Be sure to pay attention to the relationship between R_D and Rl. If you get a solution such as R_D=30k and Rl=10k, then R_D is a lot larger than Rl. R_l is affecting your gain more than R_D. In this case, if you need to increase your gain, you would be better off reducing R_D while increasing I_D than vice versa.

NOTE: It is good practice to design your circuit to BEAT the design criteria as opposed to MEET design criteria. That way, you have 'wiggle room' incase your circuit does not operate exactly as expected.

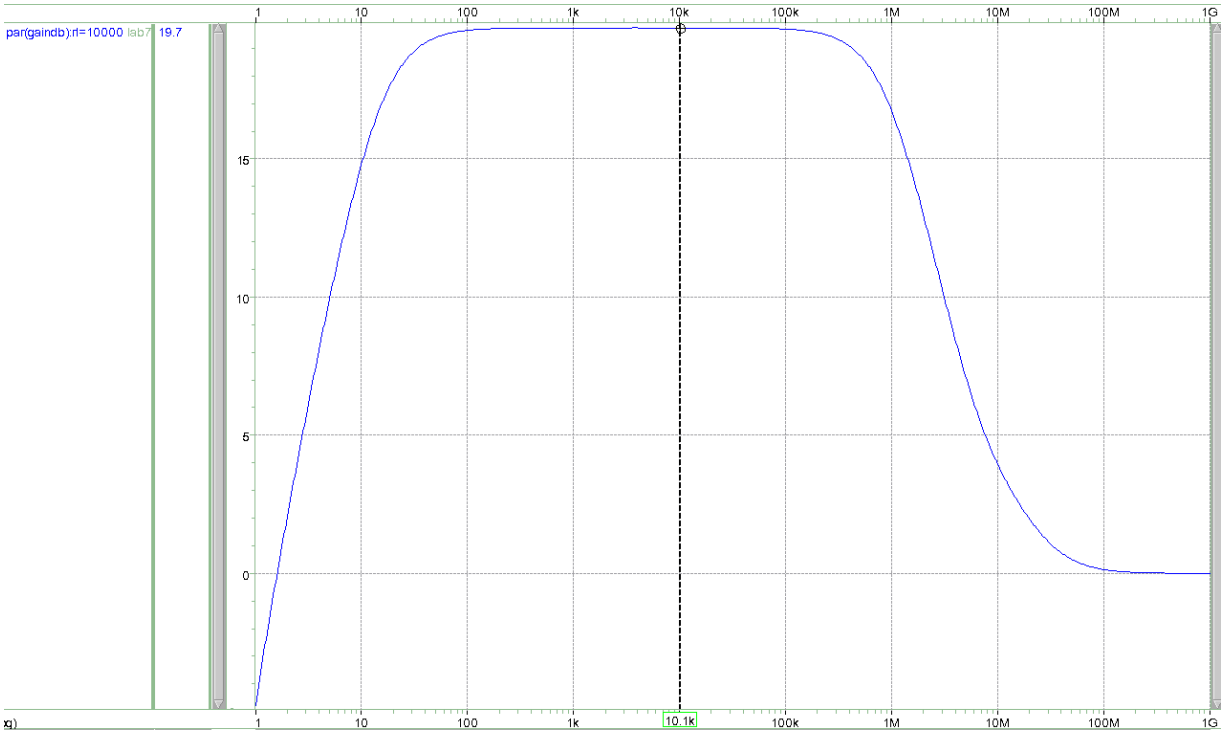

Figure 7-3: AC simulation for the design example of the common-source amplifier. The mid-band gain is approximately 19.7dB.

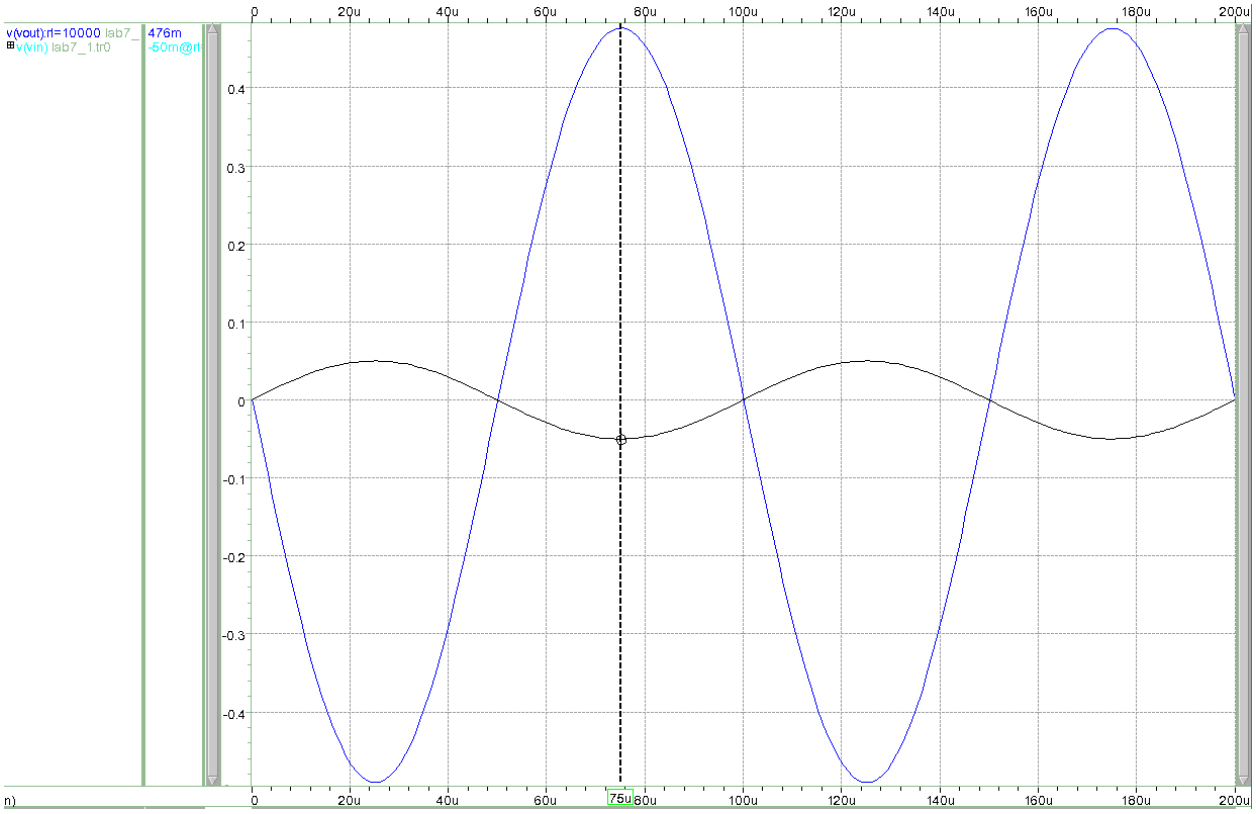

Figure 7-4: Transient simulation for the design example of the common-source amplifier. The gain is approximately 9.52. No clipping can be seen.

7.3 A systematic procedure for biasing a source-follower amplifier

In laboratory experiment 6, we saw that a common source amplifier does a poor job at voltage amplification due to its large output impedance; however, a source-follower does a good job at sourcing voltage since it has a relatively small output impedance.

The effective load impedance seen by MOSFET M_1 in **Figure7-1** the frequency range of interest when ac-coupling capacitor C_{C2} is a short is given by $R_D \parallel R_L$. As we saw in the previous lab, R_L does not affect the gain of the amplifier in **Figure 7-1** as long as it is much larger than R_D. However, as R_L becomes comparable or smaller than R_D, the ac small-signal gain of the amplifier in **Figure 7-1** begins to decrease. The ac small-signal gain in **Figure 7-1** is given approximately by

$$A_v \approx -\left(\frac{g_m\left(R_D \parallel R_L\right)}{1+g_m R_{ss}}\right) \tag{7.8}$$

In order to reduce the impact of varying load resistance on the small-signal gain of the common-source amplifier in **Figure 7-1**, we need to insert a buffer stage between the drain of MOSFET M_1 and the load resistance R_L. The output impedance of the buffer needs to be low, so that the variation in R_L does not affect the output impedance of the buffer. Since the output of the common-source

amplifier in **Figure 7-1** is a voltage signal, the buffer stage is a voltage-in, voltage-out stage, with high input impedance and low output impedance. The canonic cell that has these characteristics is the source-follower amplifier, whose output impedance is approximately $1/g_m$, but suffers from a gain that is at best close to 1, but always less than 1.

A schematic of a source-follower (common-drain) amplifier is shown in **Figure 7-5**. M_2 is a discrete n-channel MOSFET device such as the 2N7000 used in this lab experiment. The function of resistor R_{D2} is to limit the voltage at the drain of MOSFET M_2 so that it does not enter into breakdown. For low values of V_{dd}, R_{D2} can be eliminated from the circuit schematic.

The ac small-signal gain of the source-follower amplifier in **Figure 7-5** is given approximately by

$$A_v \approx \left(\frac{g_{m2}\left(R_{ss2} \,//\, R_L\right)}{1 + g_{m2}\left(R_{ss2} \,//\, R_L\right)} \right) \tag{7.9}$$

where g_{m2} is the transconductance of MOSFET M_2, which is biased in saturation. Now, since Rl appears in both numerator and denominator, its affect on the gain is reduced.

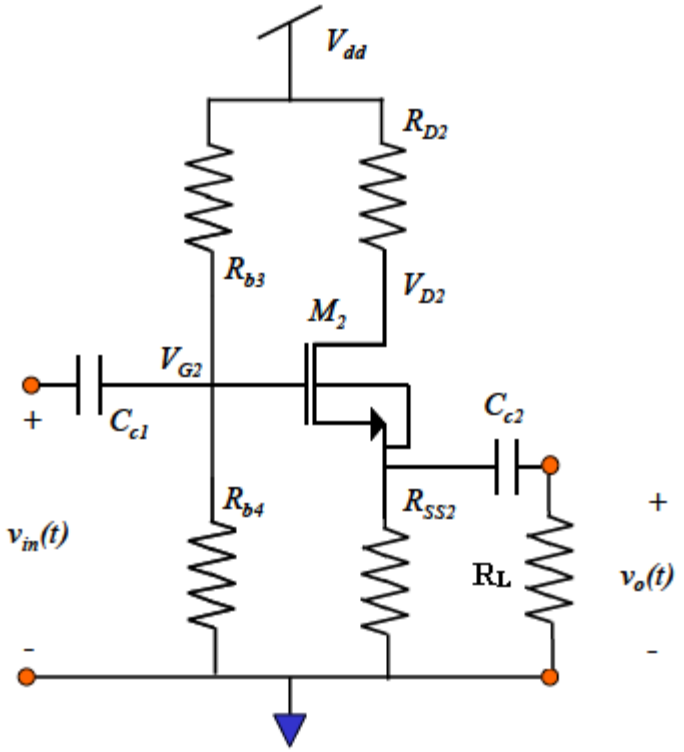

Figure 7-5: Source-follower amplifier schematic with dc-blocking capacitors C_{c1} and C_{c2} isolating the dc-potentials at the gate and drain terminals of M_2 from that of the signal source and that of the load.

Now we want to design the source follower to achieve the following design criteria:

Voltage gain = A2 = -1.94dB = .8
Vdd: 10V

Rl: As low as 100Ω
No clipping is allowed.

The first thing we do is to set V_{ss2} to Vdd/2 so as to minimize the chance of any clipping.

$$Vss2 = \frac{Vdd}{2} = I_{D2} R_{ss2} \tag{7.1}$$

We then solve for R_{ss} from the gain equation.

$$A2 = \frac{g_{m2}\left(R_{ss2} \,//\, R_L\right)}{1 + g_{m2}\left(R_{ss2} \,//\, R_L\right)} = \frac{gm(R_{ss2} Rl)}{\left(R_{ss2} + Rl + gmR_{ss2} Rl\right)} \tag{7.2}$$

This leads to

$$R_{ss2} = \frac{-A2Rl}{A2 + gmRl\left(A2 - 1\right)} \tag{7.3}$$

We then plug this back in to equation 7.1 to get

$$\frac{Vdd}{2} = \frac{-A2I_{D2}Rl}{A2 + gmRl\left(A2 - 1\right)} \tag{7.4}$$

Now, we use the following relationship between I_D and gm:

$$gm = \sqrt{2Kn\frac{W}{L}I_D} \qquad \text{or} \qquad I_D = \frac{gm^2}{2Kn\frac{W}{L}} \tag{7.6}$$

Plugging this into equation 7.5 leads to the following second order equation in terms of gm:

$$\frac{Vdd}{2} = \frac{-A2gm^2 Rl}{2Kn\frac{W}{L}\left[A2 + gmRl\left(A2 - 1\right)\right]} \tag{7.7}$$

Using equation 7.7 we can solve for gm in terms of A2, Rl, and Vdd. All of these values have been given to us.

NOTE: If A2, Rl, Vdd, are not chosen properly, we will get only negative or imaginary solutions to the second order equation. This means the circuit topology will not work. In other words, this circuit will only work if: A2 is not too big, Rl is not too small, and Vdd is not too small.

We can use the value for Kn that we found in pre-lab exercise 1 which should be roughly 250 uA/V^2. The gate aspect ratio of these transistors is 3,200. This yields the result:

$$gm = 55.3\frac{mA}{V} \qquad gm = 144.7\frac{mA}{V}$$

These solutions lead to

$$I_{D2} = 19.2mA \qquad I_{D2} = 129.6mA$$

NOTE: We will choose the first solution since it provides us with less bias drain current. This means we will consume less power to achieve our performance specs.

We can then find Rss2 by

$$V_{ss2} = \frac{Vdd}{2} = I_{D2}R_{ss2}$$

Which yields

$$R_{ss2} = 260.4$$

As can be seen, R_{D2} does not affect this circuit performance. It can be removed unless Vds of M2 becomes too large.

The next step is to find what Vgs is necessary to produce 19.2mA of current through the transistor. This can be done by choosing a value for Rb3 and varying Rb4 until we get Vss2=5V. You will use a potentiometer to do this in the lab, and a DC sweep in HSpice for the pre-lab. **Figure 7-6** shows the dc sweep for Rb4 with Rb3=10k that produces a Vss2=5V.

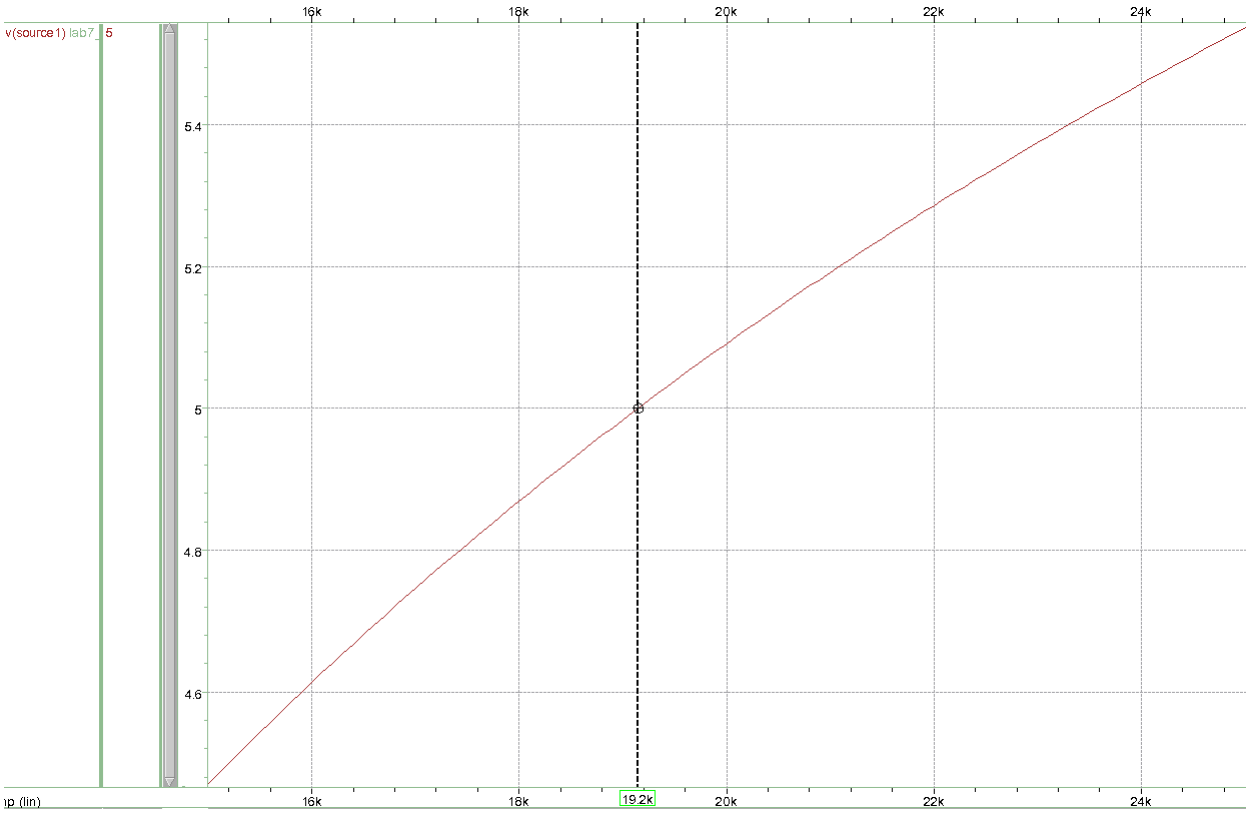

Figure 7-6: DC sweep for Rb4 to get Vss2 equal to 5V

From the plot we see that for Rb4=19.2kΩ, we get a Vss2 of 5 or a drain current of 19.2mA. Now we have our finalized design:

Rb3=10k
Rb4=19.2k
Rss2=260.4
R_{D2}=0
I_{D2}=19.2mA
Vg2=6.56V (found using HSpice)
Vss2=5V

The next step is to perform ac and transient analyses with a sin wave with amplitude of 50mV and a frequency of 10 kHz. These are plotted for this design example in **Figure 7-7** and **Figure 7-8**. The ac sweep is to verify the gain over frequency we desire. The transient sweep is to verify the amplifier does not go out of saturation or clip.

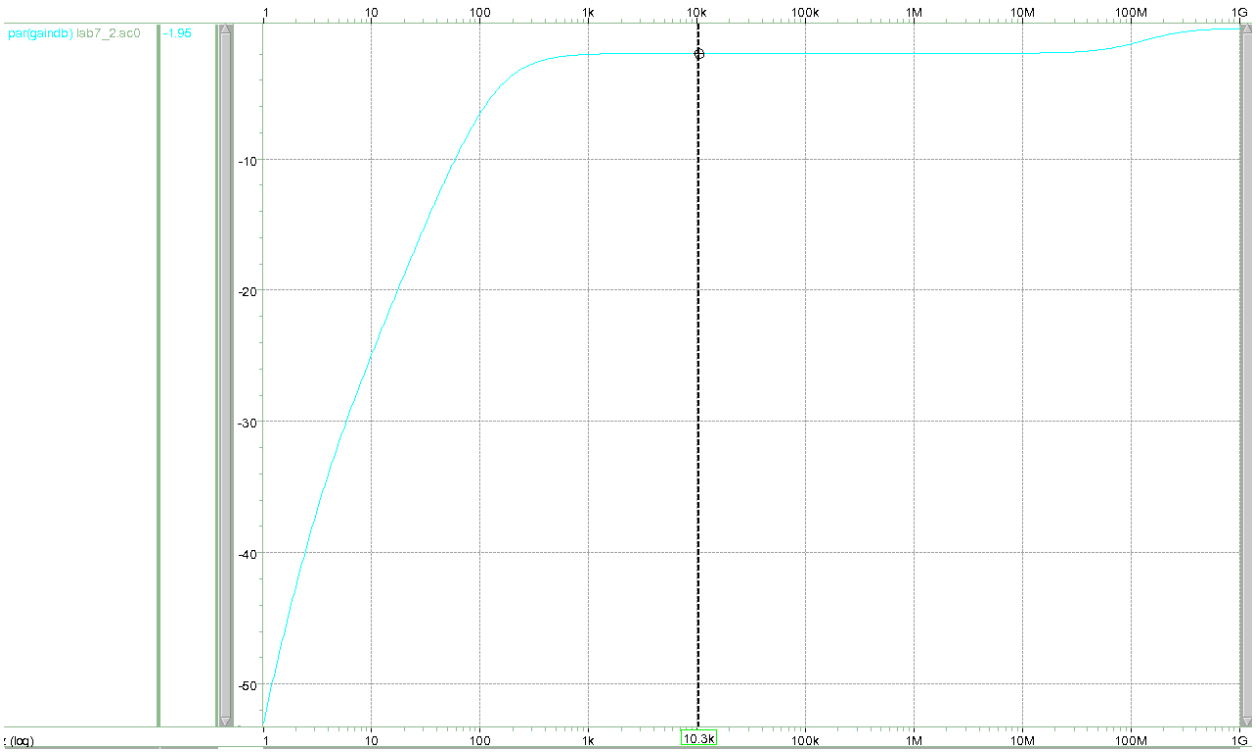

Figure 7-7: AC simulation for the design example of the source-follower amplifier. The mid-band gain is approximately -1.95dB.

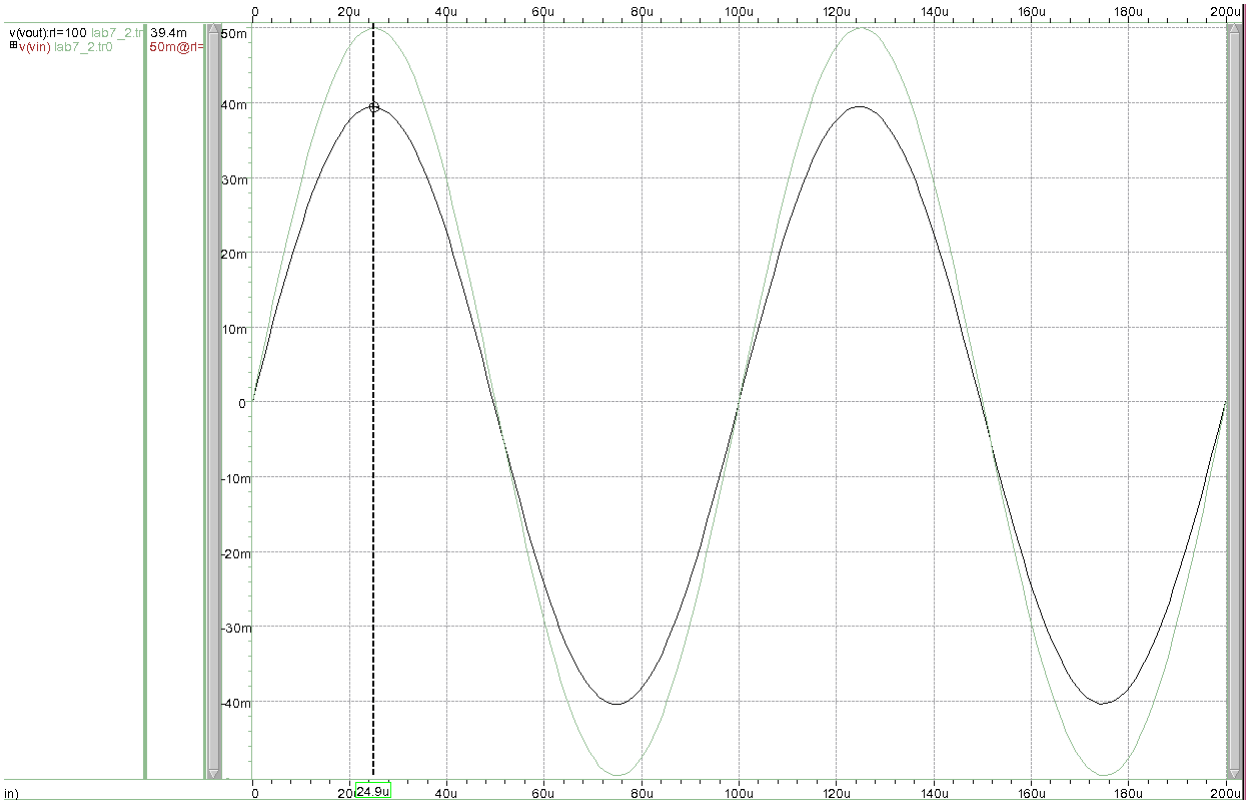

Figure 7-8: Transient simulation for the design example of the source-follower amplifier. The gain is approximately .79. No clipping can be seen.

7.4 A systematic procedure for biasing a common-source source-follower cascade amplifier

We now want to cascade the two amplifiers so that we can get gain from the common-source amplifier, and then buffer the output voltage with a source-follower amplifier. The schematic can be seen in **Figure 7-9.**

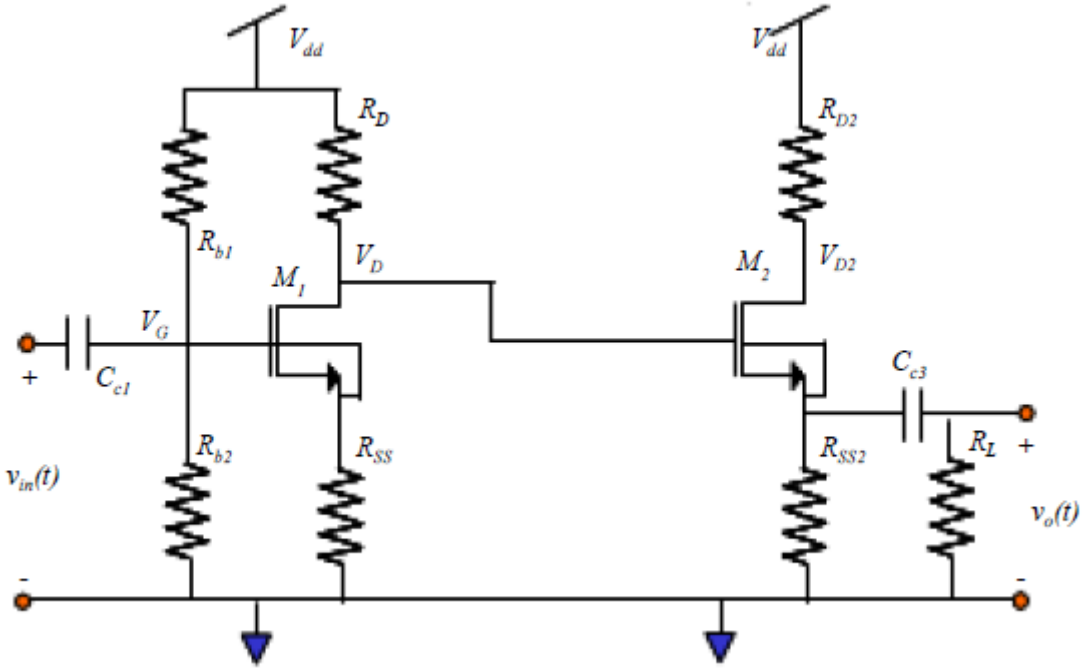

Figure 7-9: Cascade of common-source amplifier with source-follower amplifier.

The first thing that we see is that the load resistance of the common-source amplifier is infinity since the load is the gate of transistor M2. Therefore, we can redesign our common-source amplifier with less-stringent design criteria.

The second thing that we see is that we designed the common-source amplifier for a V_D of 5V and we designed the source-follower for a Vss2 of 5V. This will not work since it would put Vgs of M2 at 0V. We need to either increase the drain voltage of M1, decrease the source voltage of M2, or both. Our HSpice simulation from our source-follower design gave us a Vgs of M2 of 1.57V. Thus, lets split the voltage across both transistors and let V_D of M1 be 5.8V and Vss of M2 be 4.2V.

Our overall design criteria are listed below:
Voltage gain = A = 20dB = 10
Vdd: 10V
Rl: As low as 100Ω
No clipping is allowed.

Our common-source amplifier has the following design criteria:
Voltage gain = A1 = A/A2 = 10/.8 = 12.5
Vdd: 10V
Rl: infinity
V_{D1}: 5.8V

No clipping is allowed.

Our source-follower has the following design criteria:
Voltage gain = A2 = .8
Vdd: 10V
Rl: as low as 100Ω
Vss2: 4.2V
No clipping is allowed.

Repeating the systematic procedure from sections 7.2 and 7.3 we get the following values:

Rb1=10k
Rb2=1.46k
Rss1=500
R_{D1}=7.61k
Rss2=156
R_{D2}=1
I_{D1}=.55mA
I_{D2}=27mA
Vg1=1.27V
Vss1=.275V

7.5 Verification of the systematic procedure for biasing a common-source source-follower cascade amplifier

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```
AC-coupled Common-Source Source-Follower cascade amplifier
*Written 4/29/13 by Aaron Curry
**********************************************************
**** options section
**********************************************************
.opt post
**********************************************************
**** circuit description
**********************************************************
rb1 vdd gate1 10K
rb2 gate1 source1 'rb2'
m1 drain1 gate1 source1 source1 2N7000 W=0.8E-2 L=2.5E-6
rss1 source1 0 500
rd1 vdd drain1 7.61k
cc1 vin gate1 10uF

*source-follower amplifier, dc-coupled
rd2 vdd drain2 1
m2 drain2 drain1 source2 source2 nmos2N7000 W=0.8E-2 L=2.5E-6
rss2 source2 0 156
cc2 source2 out 10uF
rl out 0 'Rl'

**********************************************************
```

```
**** parameters section
*********************************************************
.param Rl=100k
.param rb2=1.46k

*********************************************************
**** sources section
*********************************************************
vdd vdd  0 10V
vs vin 0  ac 1 sin(0V 50mV 10k)
*********************************************************
**** specify nominal temperature of circuit in degrees C
*********************************************************
.TEMP=27
*********************************************************
**** probe section
*********************************************************
.probe ac gaindB=par('20*log10(v(out))')
*********************************************************
**** analysis section
*********************************************************
.op
.dc rb2 .1k 2k .01k
.ac dec 100 1 1G sweep Rl poi 4 100k 10k 1k 100
.tran 1u 200u 0 1u sweep Rl poi 4 100k 10k 1k 100
*********************************************************
**** models section
*********************************************************
*(this Model is from supertex.com)
.MODEL nmos2N7000   NMOS (LEVEL=3   RS=0.205          NSUB=1.0E15
+DELTA=0.1      KAPPA=0.0506    TPG=1             CGDO=3.1716E-9
+RD=0.239       VTO=1.000       VMAX=1.0E7        ETA=0.0223089
+NFS=6.6E10     TOX=1.0E-7      LD=1.698E-9       UO=862.425
+XJ=6.4666E-7   THETA=1.0E-5    CGSO=9.09E-9
*
*2N7002 MODEL

.end
```

Figure 7-10: Spice netlist of the cascade of common-source and source-follower amplifier in **Figure 7-9.**

The simulation results of the ac and transient responses of the cascade of common-source and source-follower amplifiers in **Figure 7-9** using the netlist in **Figure 7-10** are shown in **Figure 7-11** and **Figure 7-12** for values of RL varying from 100kΩ to 100Ω. As can be seen, the cascade amplifier is able to provide gain to small loads.

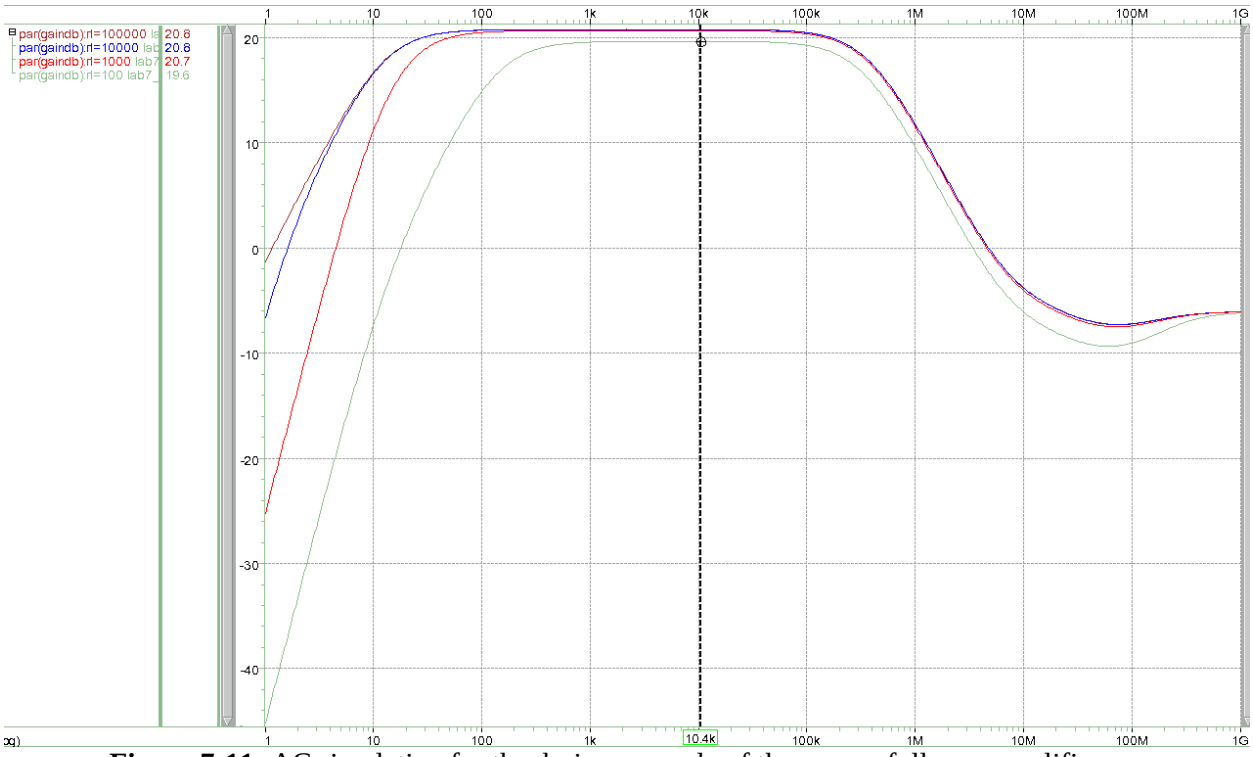

Figure 7-11: AC simulation for the design example of the source-follower amplifier. The mid-band gain ranges from 20.8dB to 19.6dB for 100kΩ to 100Ω loads.

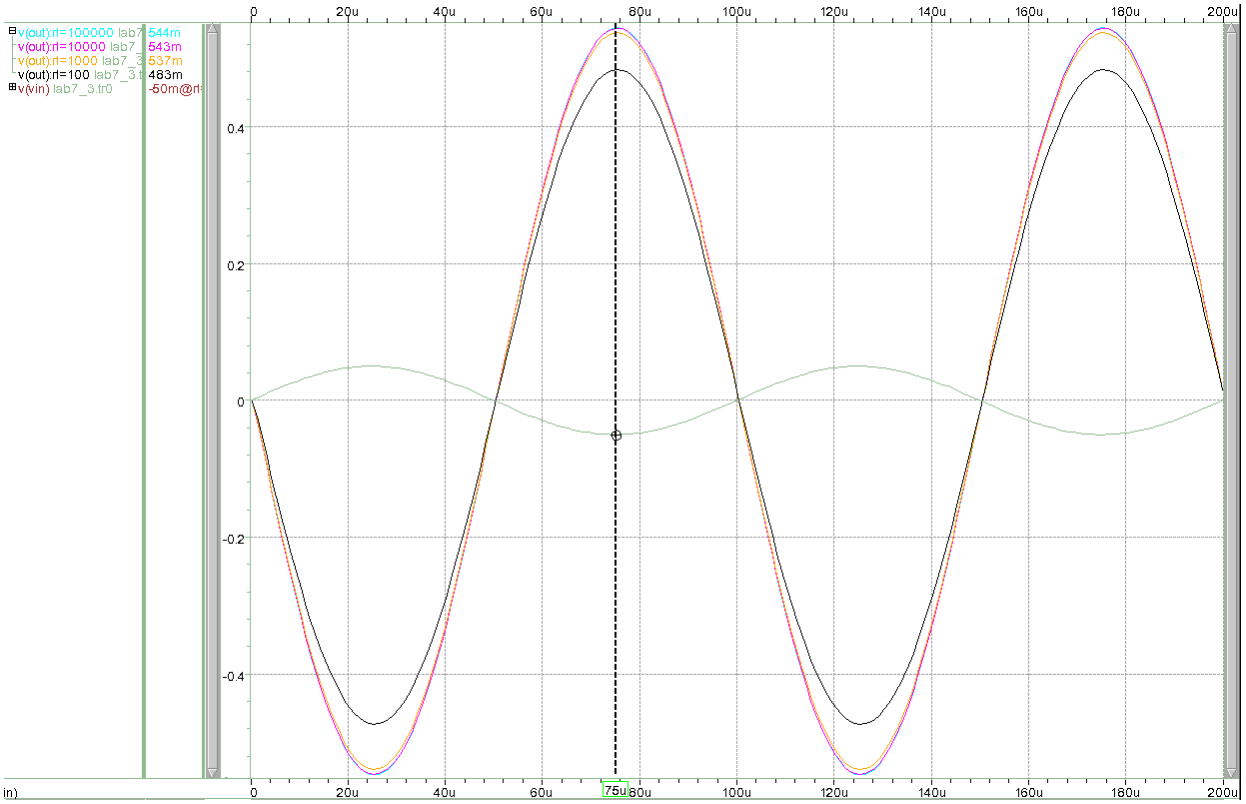

Figure 7-12: Transient simulation for the design example of the source-follower amplifier. The gain ranges from 10.9 to 9.7 for 100kΩ to 100Ω loads. No clipping can be seen.

7.6 High gain amplifiers

7.6.1 Active load

A common desire a circuit designer faces is to get more gain out of a common-source amplifier. One reason is the relatively low transconductance associated with a MOSFET, as compared to a bipolar transistor. A common-source amplifier is shown below in **Figure 7-13.**

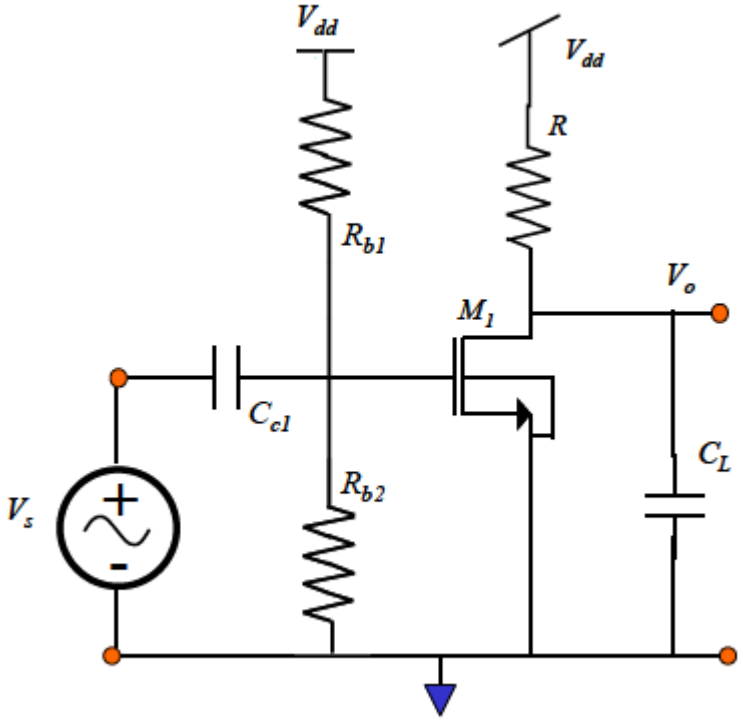

Figure 7-13: Schematic diagram of a common-source amplifier.

From the previous lab, it was shown that a common-source amplifier has gain:

$$A_V = \frac{V_o}{V_s} = -g_m R \tag{7.1}$$

This is assuming that the drain to source resistance, r_{ds}, of the MOSFET is much greater than R. If it isn't, than the net effective resistance is the parallel combination of the resistor R and the drain-source resistance of the device. The transconductance, g_m, of a MOSFET is defined as:

$$g_m = \sqrt{2k_n\left(\frac{W}{L}\right)I_{DQ}} \tag{7.2}$$

From these equations it can be seen that the only gain variables that a circuit designer has control over are the load resistance, R, the drain bias current, I_{DQ}, and the gate aspect ratio (or size) of the transistor, W/L.

In integrated circuit design, a resistor is not usually a passive element as depicted in **Figure 7-13**. Active devices usually realize resistances. Large on-chip passive resistance takes up much more area than a resistance realized by using an active device.

We can attempt to maximize the amount of gain that can be realistically obtained from the circuit topology in **Figure 7-13** by making the small-signal resistance as large as possible. This can be done replacing the drain resistance, R, in **Figure 7-13** with a PMOS version of the current mirror that was presented in laboratory experiment 5, as shown below in **Figure 7-14**.

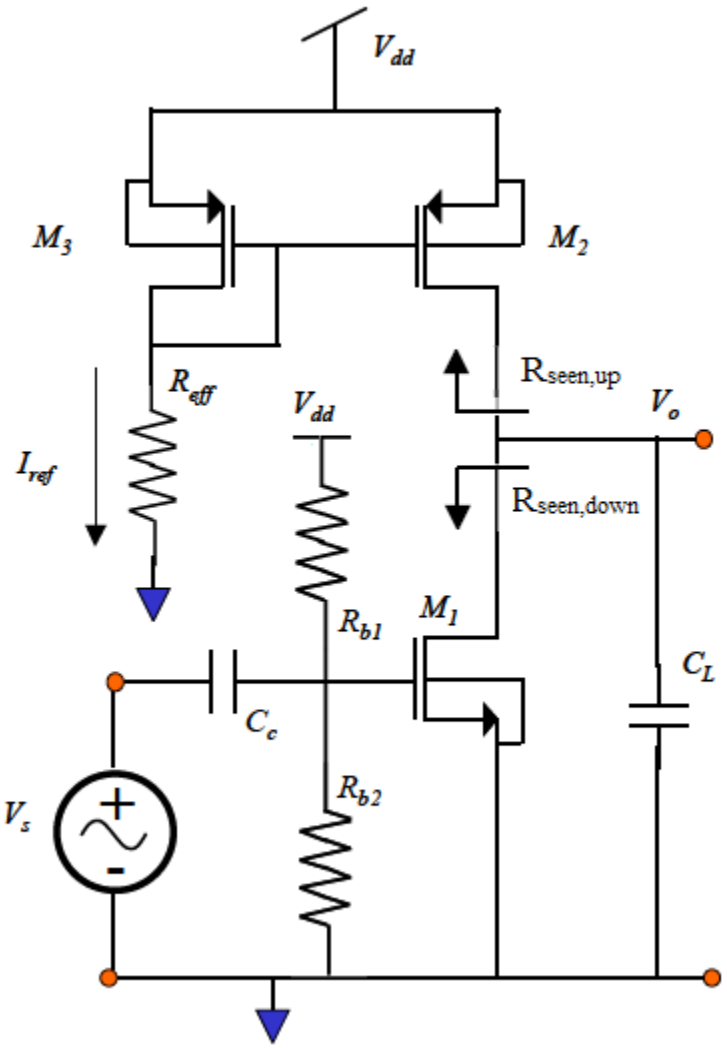

Figure 7-14: A common-source amplifier with an active load.

Note: It can be seen in **Figure 7-14** that the PMOS current mirror uses a passive resistor Reff to establish the reference current, I_{ref}, needed to bias the common- source amplifier. Normally, another NMOS transistor that is either diode-connected or biased with a dc voltage is used to present the required amount of resistance. For the purposes of this explanation, it will be left as an effective resistance, R_{eff}. The current mirror formed by PMOS transistors M_2 and M_3 are correctly biased by appropriate choice of current I_{ref}, resistor R_{eff} and device sizes (if applicable) of M_2 and M_3.

One may recognize that the small-signal output resistance of the topology feature in **Figure 7-14**, R_{out}, is nothing more than the parallel combination of the output resistance of MOSFET M_2 and that of MOSFET M_1. This derivation is left as a pre-lab exercise.

As stated before, a passive on-chip resistor consumes a great deal of area and its resistance is proportional to that area. Thus, high-value on-chip passive resistors are extremely inefficient from a layout area standpoint. The gain of the common-source canonic cell **Figure 7-11** was increased by using the low frequency, small-signal resistance of a MOSFET current mirror as shown in **Figure 7-14**, which is much higher than the resistance that can be realized with a typical on-chip passive resistor. However, this assumes that the drain-to-source (or output) resistance, r_{ds}, of a MOSFET is very large. As device geometries become smaller, this assumption begins to fail. This next section will deal with what is known as a cascode configuration, which is a cascade of the common-source and common-gate canonic cells that increases the drain-to- source resistance of a MOSFET.

7.6.2 Active load cascode configuration

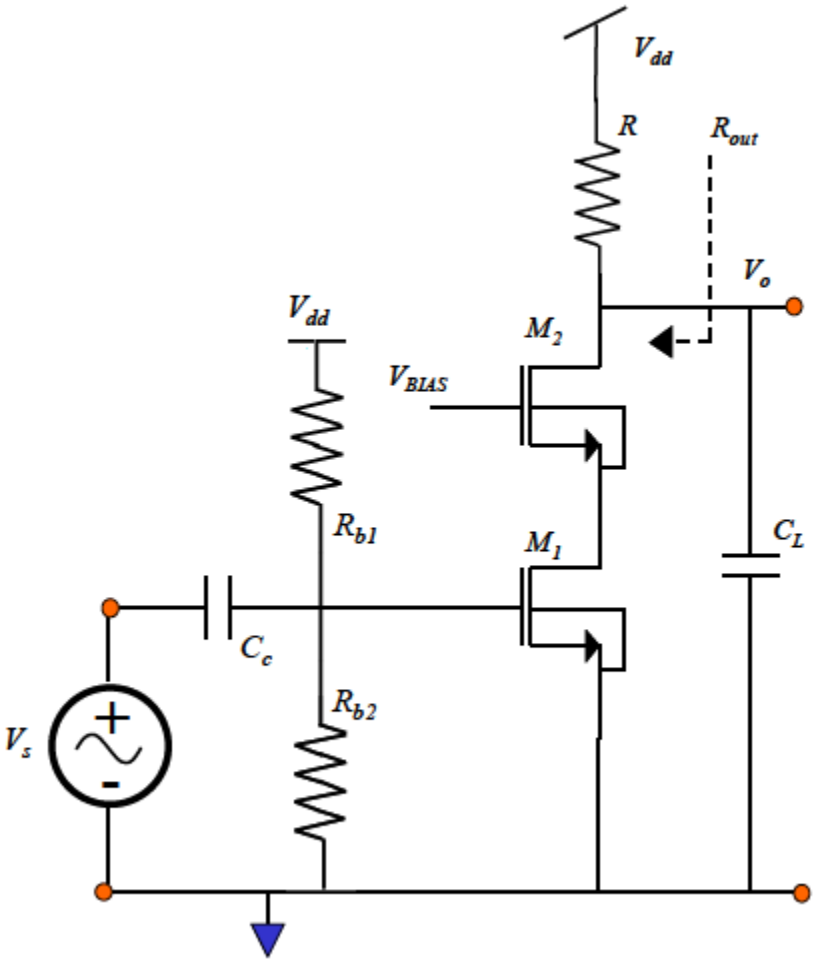

Figure 7-15: Common-source cascode.

The cascode configuration is shown in **Figure 7-15**. Going back to laboratory experiment 6, one can see that this cascode configuration is nothing more than a common gate that has been stacked on top of the common-source amplifier. Since we have derived the small-signal transfer- function of each canonic cell, we should be able to calculate the small-signal transfer function of the overall amplifier by inspection. The new output resistance should be calculated by replacing each transistor with its ac small-signal model. Both of the above are left as pre-lab exercises.

The cascode configuration has a couple of advantages over the traditional common-source amplifier. As you should find out in the pre-lab, the output resistance, R_{out}, in **Figure 7-15** is increased (especially for short-channel devices with gate length < 1μm). Consequently, the gain of the overall circuit is increased. Another benefit is achieved from a speed perspective. The common-gate stage reduces the Miller multiplication of the gate-to-drain capacitance, C_{gd}, of transistor M_1, seen by the source Vs.

The Miller Effect occurs when a capacitor is connected between two nodes, one of which experiences inverting gain with respect to the other. This increases the effective capacitance seen at the input by a factor of one plus the gain. In a traditional common-source configuration such **as Figure 7-13**, there isn't an explicit capacitor between the gate and drain terminals of the MOSFET M_1. However, the MOSFET small-signal model has a parasitic gate-drain capacitance, C_{gd}, associated with it. Also from laboratory experiment 6, it is known that a common-source amplifier has a gain of ($-g_mR$) between the gate and drain. Therefore, the effective capacitance seen by the input to the common-source amplifier **Figure 7-13** is:

$$C_{eff} = C_{gd}(1 + g_m R) \tag{7.3}$$

where R is the effective load resistance at the drain. Hence, one can now see that the time constant associated with this node has increased, and will effectively slow the circuit down. In a cascade configuration, R=1/gm2 since the load at the drain of M1 is looking into the source of M2. Therefore, the Miller Multiplication is reduced.

In short channel devices, the output resistance associated with a transistor is much smaller than in long channel devices. Therefore, using cascode topologies is necessary in order to achieve a large output resistance. In order to have a balanced cascode circuit in **Figure 7-15**, we would append the cascode current mirror where resistance R is located which is shown in **Figure 7-16.**

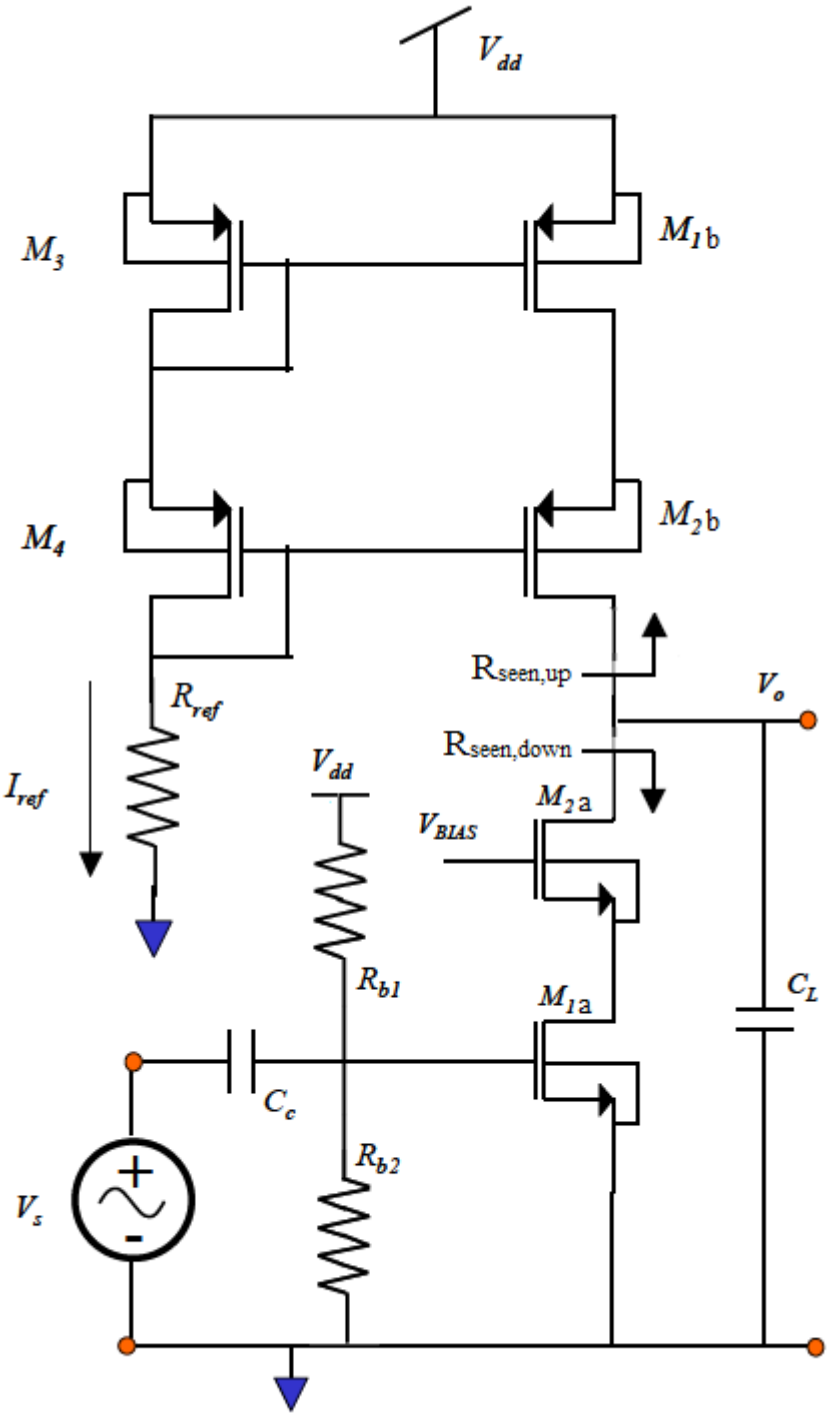

Figure 7-16: Common-source cascode with cascode current mirror.

7.7 HSpice simulation of discrete p-channel MOSFET, BS250P

Figure 7-17 is an example of a netlist that can be used to plot the i_D-v_{DS} characteristics of the MOSFET BS250P, specified by the subcircuit named BS250P in section 7.9. We use a subcircuit

definition because we do not have a properly characterized model deck for the BS250P from the manufacturer that accounts for all aspects of its behavior. The drain to source voltage, $V_{DS,}$ is swept from 0V through 10V in steps of 0.01V at gate to source voltages, V_{GS} of 2 V-10 V = -8V, 4V-10V = -6V, and 6V-10V = -4V. The Spice simulation results are shown in **Figure 7-18**.

```
PMOSFET I-V characteristic for BS250P
*Written May 1, 2013 for EE348L by Aaron Curry
**********************************************************
**** options section
**********************************************************
.opt post
**********************************************************
**** subcircuit definition
**********************************************************
 .SUBCKT BS250P drain gate source
M1 drain gate1 source source MBS250
RG gate gate1 160
RL drain source 1.2E8
C1 gate1 source 47E-12
C2 gate1 drain   10E-12
D1 drain source DBS250
.MODEL MBS250 PMOS
+VTO=-3.193   RS=2.041 RD=0.697 IS=1E-15 KP=0.277
+CBD=105E-12 PB=1 LAMBDA=1.2E-2
.MODEL DBS250 D IS=2E-13 RS=0.309
.ENDS BS250P
**********************************************************
**** circuit description
**********************************************************
x1 drain gate source BS250P
**********************************************************
**** sources section
**********************************************************
Vdrain drain 0 5
Vdd vdd 0 5
Vgate gate 0 5
**********************************************************
**** probe section
**********************************************************
.probe dc id=par('id(x1.m1)')
**********************************************************
**** specify nominal temperature of circuit in degrees C
**********************************************************
.TEMP=27
**********************************************************
**** analysis section
**********************************************************
.dc vdrain 0 5 .01 sweep vgate poi 3 0 1 2

.END
```

Figure 7-17: HSpice netlist for obtaining I-V characteristic of a p-channel MOSFET, MBS250.

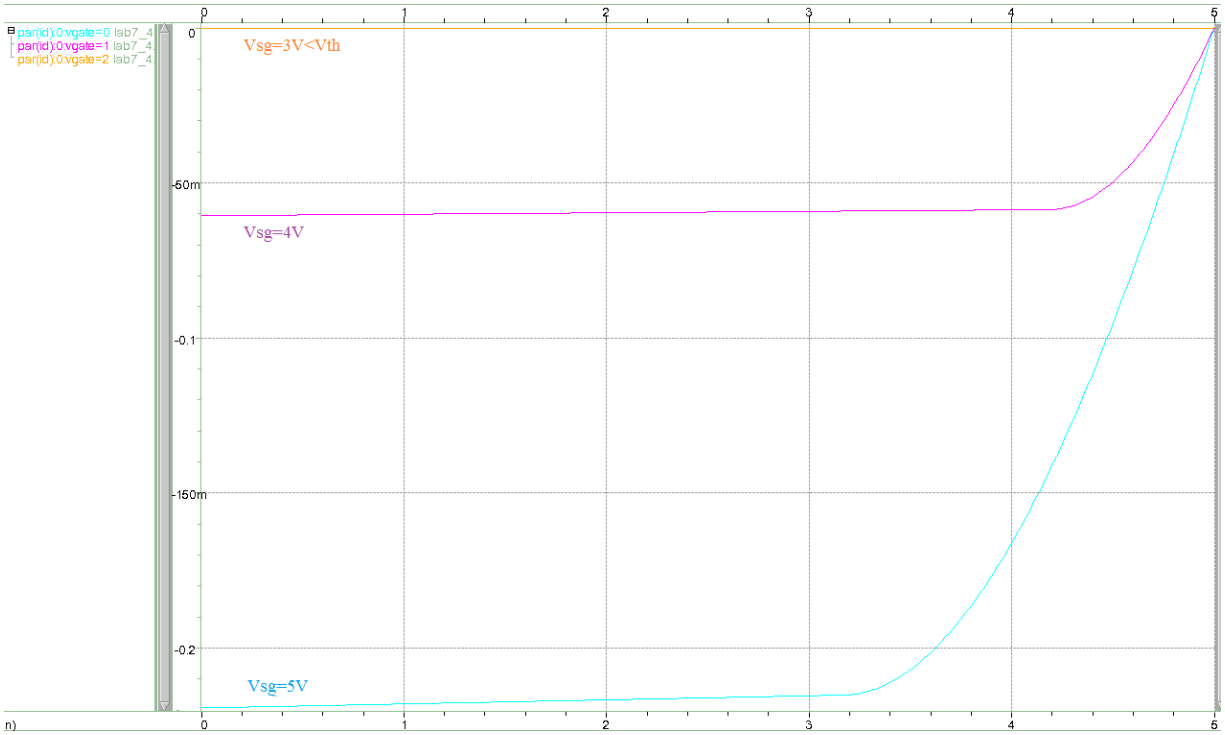

Figure 7-18: iD-vDS characteristics of MOSFET x1 in **Figure 7-11** for source to gate voltages of 3V, 4V, and 5V.

7.8 Conclusion

The MOS canonic cells were presented in laboratory experiment 6. These cells are the fundamental building blocks of analog integrated circuit design. This lab focused on using the canonic cells in combination to overcome their inherent limitations when used as a single cell. Thus when doing circuit analysis, one may always break down a circuit topology into the canonic cells in order to obtain insight into the design of a circuit. An advanced understanding of these basic building blocks will allow a circuit designer to effectively use canonic cells to overcome their individual limitations, and satisfy the largest possible subset of circuit design specifications.

7.9 MOSFET Spice model for PMOS transistor BS250P

Note that the spice model for the discrete p-channel MOSFET used in this laboratory experiment, BS250P, utilizes a subcircuit definition, which includes a first-order PMOS model deck.

```
.SUBCKT BS250P drain gate source
M1 drain gate1 source source MBS250
RG gate          gate1    160
RL drain source 1.2E8
C1 gate1 source 47E-12
C2 gate1 drain  10E-12
D1 drain source DBS250
.MODEL MBS250 PMOS
+VTO=-3.193 RS=2.041 RD=0.697 IS=1E-15 KP=0.277
+CBD=105E-12 PB=1 LAMBDA=1.2E-2
```

.MODEL DBS250 D IS=2E-13 RS=0.309
.ENDS BS250P

In order to use this device in an Spice netlist, the above subcircuit is defined before the start of the circuit description. Then, a subcircuit call is used to instantiate the BS250P in the SPice netlist, as shown below.

X1 drain gate source BS250P

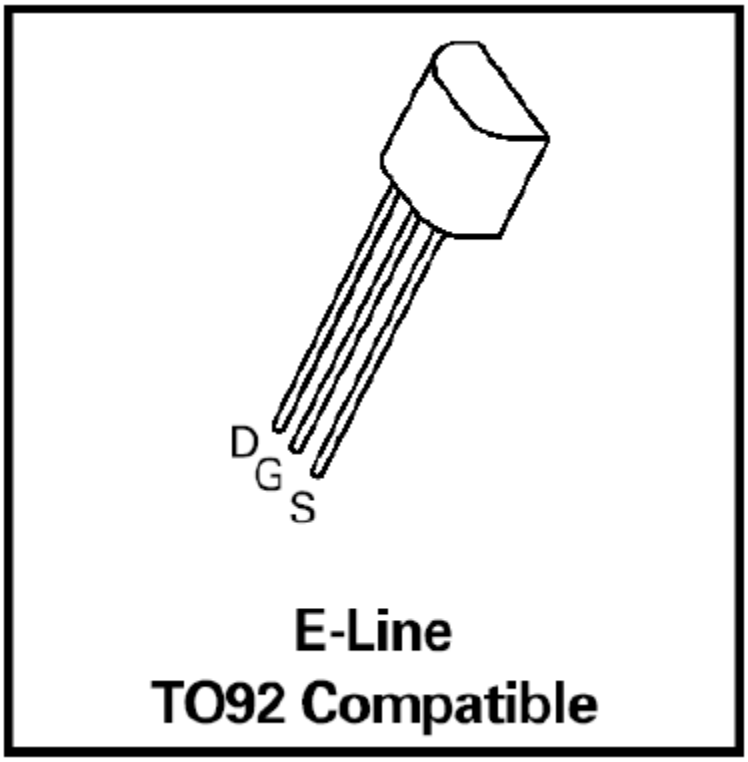

Figure 7-19: Pin diagram of the BS250P (Courtesy of Zetex).

7.10 Revision History

This laboratory experiment is a modified version of the laboratory experiment 7 (MOSFETs Continued) by B. Madhaven which was a revision of experiment 7 (MOSFET Dynamic circuitsII) created by Jonathan Roderick.

7.11 References

[2] HSpice user manual posted on EE348L class web site.

[5] Adel Sedra and K. C. Smith, *Microelectronic Circuits*, fifth edition, Oxford University Press.

[6] Ben G. Streetman. *Solid State Electronic Devices*. Prentice-Hall Inc., Englewood Cliffs, New Jersey, 1990.

[7] Richard C. Jaeger. *Introduction to Microelectronic Fabrication*. Addison-Wesley Publishing Company, Reading, Massachusetts, 1993.

[8] S. M. Sze. *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., New York, 1981.

[9] Paul R. Gray & Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Inc., New York, 1993.

7.12 Pre-lab Exercises

Note:

- For Spice simulations, use the model deck for 2N7000 in Figure 7-9 and the model deck for BS250P in Figure 7-11.
- Submit plots relevant to each question in your lab report.
- Note: The 2N7000 and BS250P are not small geometry devices, so the approximation of large small-signal, drain-to-source resistance in the saturation region, r_{ds}, is normally valid.
- Device Specifications:

Caution: Never exceed the device maximum limitations during design.

2N7000	Idmax=200mA	Vdsmax=60V	Vth≈0.8V
BS250P	Idmax=-250mA	Vdsmax=-45V	Vth≈-1V

1) Confirm in Spice (See the note at the bottom of page 6.) that for I_D of the 2n7000 less than 100uA, the transistor is in the subthreshold operating region as discussed in the common-source design example in section 7.2.

2) Simulate the design example for the common-source amplifier with Rl=1e6, 100k, 10k. Use an ac sweep.
   A) What happens when Rl is larger than the designed value of 10k? Why?
   B) If we were to repeat this design for the load resistance being the gate of another transistor, what should we set Rl to?

3) Design a common-source amplifier (**Figure 7-1**) in HSpice (See section 7.2 for design example), with source degeneration resistance which has the following specifications:
   A) Supply voltage of 10 V (bonus points if you achieve specification with lower supply voltage between 5V and 8V)
   B) small-signal gain > 25 dB between 1kHz and 100kHz that can support a an ac-coupled load resistance as low as R_L=10 KΩ.

   Your answer should indicate

   i) How you arrived at the dc-operating point of the common-source amplifier
   ii) How the component values were chosen.
   iii) Show that the calculated small-signal gain is in good agreement with that obtained from your Spice simulations.
   iv) Submit the results of both ac and transient simulations for 100kΩ, 10kΩ, 1kΩ, and 100Ω. For the transient simulation, use a 50mV peak-to-peak sinusoidal input at 10 KHz. Does the gain inferred from the transient simulation agree with the gain obtained from the frequency response (small- signal) simulation in Spice? Why or Why not?

   NOTE: Make sure your transistor is operating at above-threshold!

4) Design a common-source common-drain cascade as shown in **Figure 7-9** in HSpice (See sections 7.3 and 7.4 for design examples), which has the following specifications:
   A) Supply voltage of 10 V (bonus points if you achieve specification with lower supply voltage between 5V and 8V)
   B) small-signal gain > 25 dB between 1kHz and 100kHz that can support a an ac-coupled load resistance as low as R_L=100Ω.
   C) Variation in mid-band small-signal gain due to variation in road resistance from 100Ω-100kΩ is no more than 5dB.

   Your answer should indicate

i) How you arrived at the dc-operating point of the common-source amplifier
ii) How the component values were chosen.
iii) Show that the calculated small-signal gain is in good agreement with that obtained from your Spice simulations.
iv) Submit the results of both ac and transient simulations for 100kΩ, 10kΩ, 1kΩ, and 100Ω. For the transient simulation, use a 50mV peak-to-peak sinusoidal input at 10 KHz. Does the gain inferred from the transient simulation agree with the gain obtained from the frequency response (small- signal) simulation in Spice? Why or Why not?

NOTE: Make sure your transistors are operating at above-threshold!

5) Derive $R_{seen,down}$ of the common-source cascode with active load in **Figure 7-16**, taking into account the small-signal MOSFET drain-to-source resistance, r_{ds}. How much greater is it as compared to Rsee,down of the traditional common-source amplifier in **Figure 7-14**? Assume gm*rds>>1.

6) Derive $R_{seen,up}$ of the cascode current mirror in **Figure 7-16**, taking into account the small-signal MOSFET drain-to-source resistance, r_{ds}. How much greater is it as compared to Rsee,up of the traditional current mirror in **Figure 7-14**? Assume gm*rds>>1.

7) Derive the Rout of the common-source cascade with active load in **Figure 7-16**, taking int o account the small-signal MOSFET drain-to-source resistance, rds. How much greater is it as compared to Rout of the traditional common-source amplifier in **Figure 7-14**? Assume gm*rds>>1.
Hint: Rout=Rsee,up//Rseen,down.

8) Simulate the high gain amplifier in **Figure 7-14** with HSpice. Let Reff=1k and Cl=1pF. Perform a .dc sweep on Rb2 to find what value is needed to put vout at vdd/2. Use this value to perform both ac and transient simulations. For the transient simulation, use an input sine wave with amplitude 50mV and frequency 10 KHz.

7.13 Lab Exercises

- Submit plots relevant to reach question in your lab report.
- Use the supply voltage that you used in your pre-lab Spice simulations for this lab.
- Remember that an amplitude of 50mV corresponds to a Vpp of 100mV.

1) Build the common-source amplifier you designed in pre-lab question 3. Verify and record your results for load resistances of 100kΩ, 10kΩ, 1kΩ, and 100Ω for a 10 kHz sine wave with amplitude 50mV. Do your results agree with you Spice results? Why or why not? For a 10kΩ load, record any changes in gain when you increase the sine wave amplitude to the 100mV, 200mV, and 400mV. Does your output clip? Now, record the gain for an open load. Is it different? Why?
   Hint: use a potentiometer for Rb2 and adjust it until your drain current is the desired value. To measure the drain current, do NOT use an ammeter. Instead, use a dc voltage probe and measure the voltage across Rss. When this voltage hits Vss=Id*Rss, you have the proper drain current.

2) Build the cascade amplifier you designed in pre-lab question 4. Verify and record your results for load resistances of 100kΩ, 10kΩ, 1kΩ, and 100Ω for a 10 kHz sine wave with amplitude 50mV. Do your results agree with you Spice results? Why or why not? For a 100Ω load, record any changes in gain when you increase the sine wave amplitude to the 100mV, 200mV, and 400mV. Does your output clip?
   Hint: You can use a potentiometer for Rb2 to ensure Id1 is at the desired value; however, there is no way to adjust the gate of M2 to ensure Id2 is at the desired value! Instead, Rss2 can be adjusted if needed.

3) Build the circuit from **Figure 7-14**. Let Reff be 1k, Vdd be 5V and do not use a load capacitance. Use a potentiometer for the bias circuitry (Rb2) of transistor M1 and adjust it until the output sits at Vdd/2. How sensitive is the output voltage to the bias scheme of M1? After you get the output as close to Vdd/2 as you can, simulate with an input sinusoid with frequency of 10kHz and amplitude of 50mV. What is the gain of this amplifier? What happens as you increase the input amplitude?