ASIC Design Center

User Manual

TDC502

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MSC Vertriebs GmbH
ASIC Design Center
Industriestraße 16
76297 Stutensee

Author: AP
Phone: +497249/910-288
Fax: +497249/910-268
Email: ap@msc-ge.com

... competence in electronics ...

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1 Introduction

MSC Vertriebs GmbH has many years of experience in the development of high precision Time to Digital Converters (TDCs). Our first TDC was developed in 1990 and implemented in a cost-effective Gate Array technology.

This manual describes the TDC502 - the latest member of our TDC family. The TDC502 is implemented in a 0,6µm-CMOS-process technology featuring 2.7V – 5.5V operation and is delivered in a LQFP44 0,8 mm fine pitch package [*)].

Supplied with 5V the TDC502 achieves a typical resolution of up to 45ps. This resolution cannot be achieved using conventional time measuring components. In combination with its multi-hit capability the multi-channel function of the TDC502 allows simultaneous and/or successive measurement of time differences. The Burst Measurement Mode and the integrated ALU complete the TDC502's performance.

The integrated measurement principle - together with the technology used - allows high-precision time difference measurement at low power consumption. The integration of the TDC502 in battery-powered applications is a common procedure.

The TDC502 is perfectly suited for measurement of time differences. Applications like distance measurement using laser, phase measurement, ultrasonic positioning, temperature measurement, etc. have been implemented successfully with our TDCs many times.

Go ahead and discover the world of our TDCs.

[*)] *LQFP = Low Profile Quad Flat Package*

2 Features

Channels:	2 channels with identical resolution, consisting of a common Start- and two Stop-inputs, programmable edge-sensitivity of the inputs, retriggerable Start-input, separated power supply for the Measuring Core
Resolution (5V, typ):	Half-Resolution: 360 ps Normal-Resolution: 180 ps High-Resolution: 90 ps Smart-Resolution: 45 ps
Measurement ranges: (5V, typ)	range I: short time measurement: 0ps – 10µs *) range II: long time measurement: 180ns – 210ms *) **)
Measurement modes:	8 measurement modes with up to 10-fold multi-hit capability and up to 10 measurements within a burst
Calibration clock:	external calibration clock required: 500 kHz - 20 MHz, internal programmable clock divider
Calibration measurement:	automatically after time measurement or stand-alone
ALU:	calculation of every hit to start and every hit to each other hit, calibration and multiplication using a 24 bit unsigned integer number
Voltage range:	2.7 V - 5.5 V
Temperature range:	-40°C - 85°C
Processor interface:	8 bit data bus / 4 bit address bus, programmable interrupt-pin, 4 individually programmable I/O-pins
Internal memory:	up to 10 uncalibrated measurement values up to 2 calibrated/ multiplied measurement values
Configuration:	programmable via processor interface
Measurement improvement:	Auto Noise Unit
Package:	LQFP44 with 0.8 mm pitch

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**)* *- High-Resolution: Maximum measurement period is shortened by half*
- Smart-Resolution: Maximum measurement period is shortened to the fourth part

***)* *Measurement range depends on period of calibration clock*

3 Block Diagram

Figure 3.1 shows the block diagram of the TDC502.

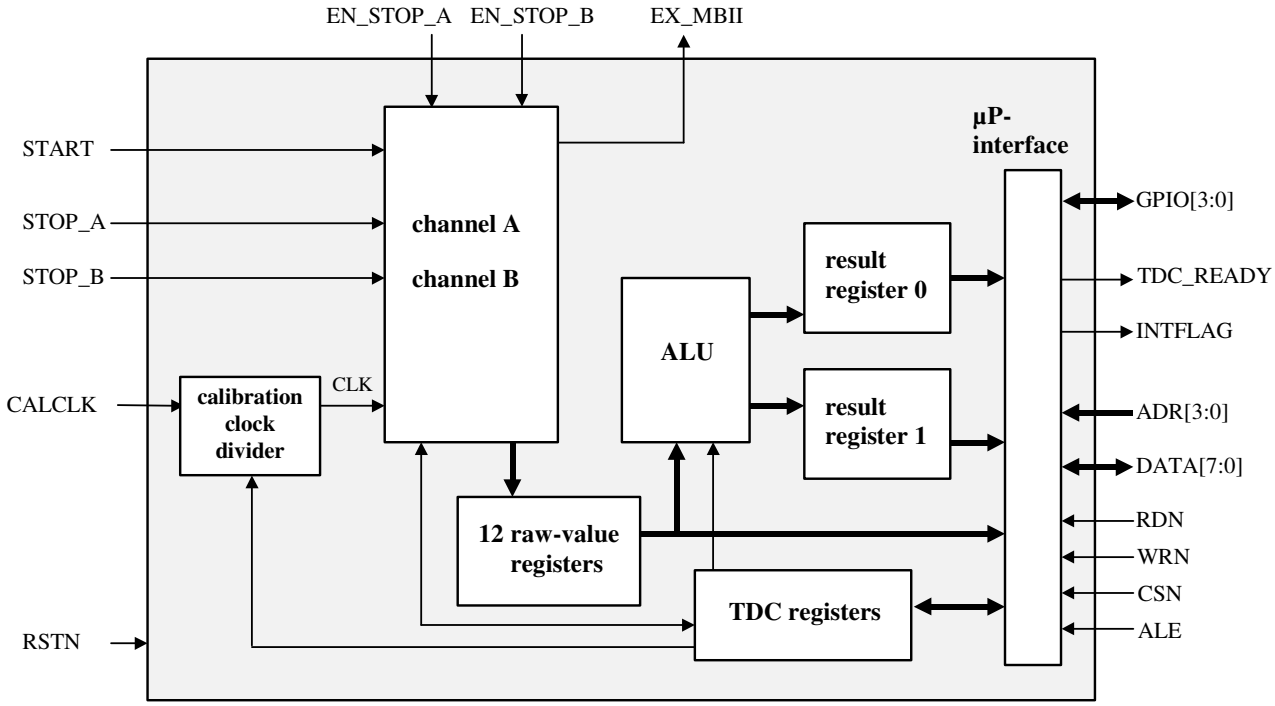


Figure 3.1: TDC502 Block Diagram

The TDC offers two **channels A** and **B** for time measurement between one start at the start-input START and up to 10 hits at the stop-inputs STOP_A and STOP_B. The uncalibrated measurement values are stored in the **raw-value registers** and can either be read out via the **processor interface** or processed within the **ALU** (Calculation of every hit to start and every hit to each other hit, calibration and multiplication using a 24 bit unsigned integer number). The ALU's measurement results are stored in the **result registers** and can be read out via the processor interface.

The configuration of the TDC as well as the selection of the measurement mode and range is done by writing the **TDC registers** via the processor interface. Status information can be accessed by reading the TDC registers.

The calibration clock, necessary for the calibration of the uncalibrated measurement values, has to be supplied by an externally generated quartz oscillator clock at the input CALCLK. The calibration clock is divided by the internal **calibration clock divider** circuit.

4 Package and Pin Configuration

4.1 Package

Figure 4.1 shows the TDC's Plastic Quad Flat Package with 44 pins (LQFP44) and 0,8 mm pitch. The package dimensions are specified in Table 4.1.

The TDC's marking is ´MSC TDC502 V2´.

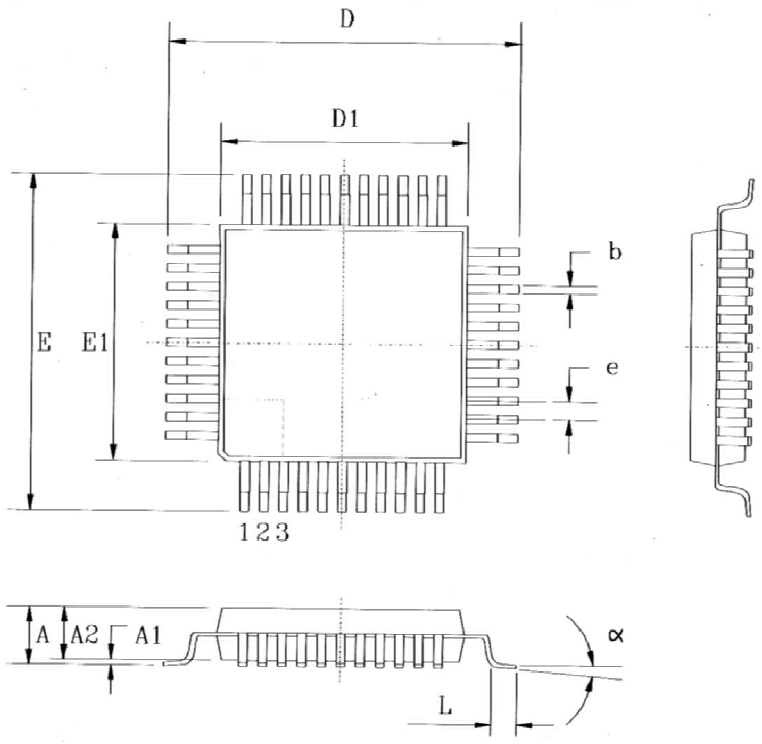


Figure 4.1: Package

	E1 / D1	A	A1	A2	e	b	L	α	D / E	Copl.
min			0,05	1,35		0,30	0,45	0°		
typ	10				0,80				12,00	
max		1,60	0,15	1,45		0,45	0,75	7°		0,10

Table 4.1: Package Dimensions [mm]

4.2 Pin Configuration

Table 4.2 shows the TDC's pin configuration. Pin names of low active signals end with 'N'.

Pin No.	Pin name	I/O	Function
5, 7, 17, 28, 35, 39	VDD	-	Power supply for internal logic and I/O's
2, 6, 12, 18, 27, 40	GND	-	Ground for internal logic and I/O's
44	VDD_C	-	Power supply for measuring core
43	GND_C	-	Ground for measuring core
1	RSTN	In	Power-on reset (low active)
3	CALCLK	In	Input for calibration clock: 500 kHz - 20 MHz
4	EX_MBII	Tri-state Out, 4mA	- Expansion of measurement range II enabled: EX_MBII toggles at every overflow of the pre-counter: 0-1-0-... - Expansion of measurement range II disabled: high impedance
8	GPIO0	Bidi, 4mA	Bit0 general purpose I/O, default: high impedance
9	GPIO1	Bidi, 4mA	Bit1 general purpose I/O, default: high impedance
10	GPIO2	Bidi, 4mA	Bit2 general purpose I/O, default: high impedance
11	GPIO3	Bidi, 4mA	Bit3 general purpose I/O, default: high impedance
13	DATA0	Bidi, 4mA	Bit0 data bus
14	DATA1	Bidi, 4mA	Bit1 data bus
15	DATA2	Bidi, 4mA	Bit2 data bus
16	DATA3	Bidi, 4mA	Bit3 data bus
19	DATA4	Bidi, 4mA	Bit4 data bus
20	DATA5	Bidi, 4mA	Bit5 data bus
21	DATA6	Bidi, 4mA	Bit6 data bus
22	DATA7	Bidi, 4mA	Bit7 data bus
23	ADR0	In	Bit0 address bus
24	ADR1	In	Bit1 address bus
25	ADR2	In	Bit2 address bus
26	ADR3	In	Bit3 address bus
29	ALE	In	Address latch enable (high active)
30	RDN	In	Read strobe (low active)
31	WRN	In	Write strobe (low active)
32	CSN	In	Chip select (low active)
33	TDC_READY	Out, 4mA	0 : TDC not ready, measurement channels disabled 1 : TDC ready for measurement, TDC waits for start
34	INTFLAG	Out, 4mA	0 : no interrupt request 1 : interrupt request
36	START	In	Common start-input

Pin No.	Pin name	I/O	Function
37	EN_STOP_B	In	Enable stop-input channel B *): 0 : Stop-input STOP_B disabled, cannot be enabled via software. 1 : Stop-input STOP_B enabled, if not disabled via software.
38	STOP_B	In	Stop-input channel B
41	STOP_A	In	Stop-input channel A
42	EN_STOP_A	In	Enable stop-input channel A *): 0 : Stop-input STOP_A disabled, cannot be enabled via software. 1 : Stop-input STOP_A enabled, if not disabled via software.

*) In measurement range II the stop-input of the selected channel has to be enabled during the whole time measurement.

Remarks:

- *All inputs are CMOS.*
- *Connect all unused inputs to GND.*
- *Data bus DATA[7:0] is not allowed to float: please pull up or down (with e.g. 10kΩ).*
- *Do not connect unused outputs.*

Table 4.2: Pin Function List

5 Measuring Procedure

The TDC502 provides two identical measurement channels A and B with a common start-input and two independent stop-inputs. The resolution of both channels is identical. Via the processor interface a resolution of 45ps (**Smart Resolution**), 90ps (**High Resolution**), 180ps (**Normal Resolution**) or 360ps (**Half Resolution**) is selectable (5V, typ.).

5.1 Time Difference Measurement

As shown in Figure 5.1, one edge-sensitive start-input and two edge-sensitive stop-inputs are available for measuring the time differences $\mathbf{t_{RESi}}$. The stop-inputs represent the measurement channels A and B. A start on the start-input starts the time measurement in the measuring core. Depending on the selected measurement mode every stop on the stop-inputs is detected as a so called **hit** and the time "hit – start" is measured and stored as measurement value **VAL** in one of the raw-value registers. The time measurement ends, when the last hit – up to 10 hits are configurable – is detected.

With the measurement values of the raw-value registers all possible time differences $\mathbf{t_{RESi}}$ (hit to start, hit to another hit) can be calculated, either externally or using the internal ALU. The ALU's measurement results (positive and negative time differences are possible!) are stored in the result registers.

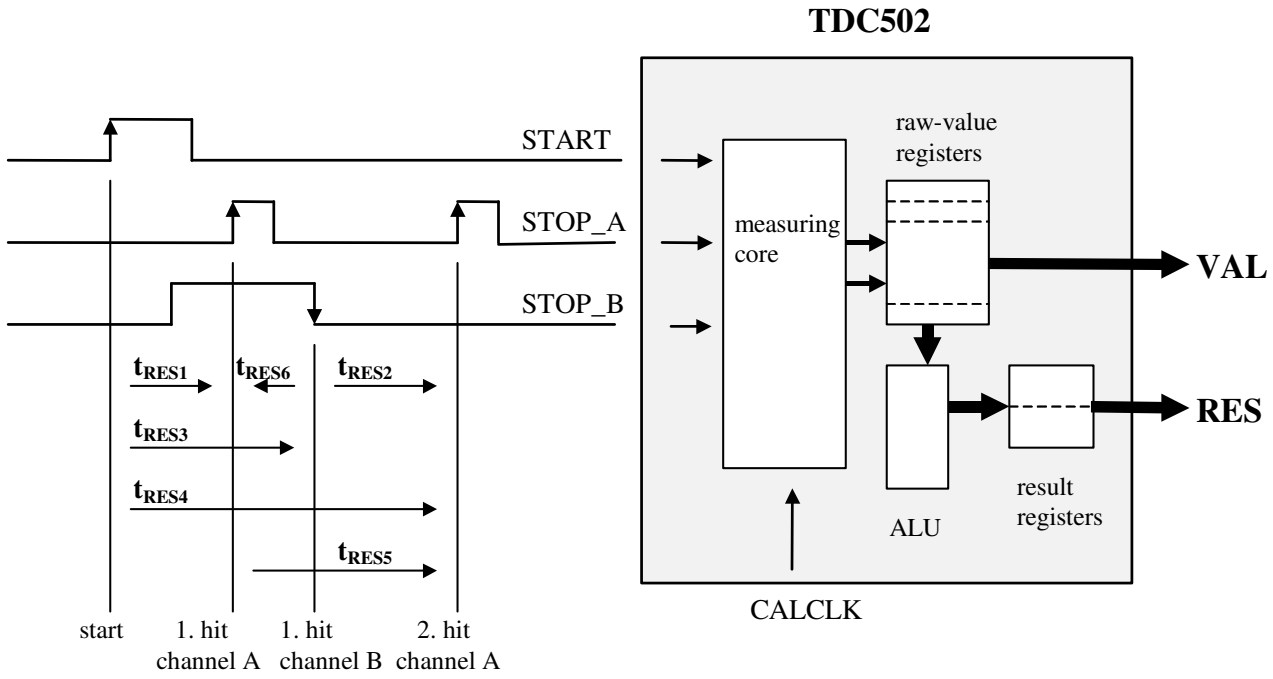


Figure 5.1: Time Difference Measurement Example

The measurement value VAL is dependant on the temperature and the supply voltage. Therefore it has to be weighted according to the TDC characteristic (see Figure 5.2). Offset and gradient of the characteristic have to be determined by a so-called *calibration measurement*.

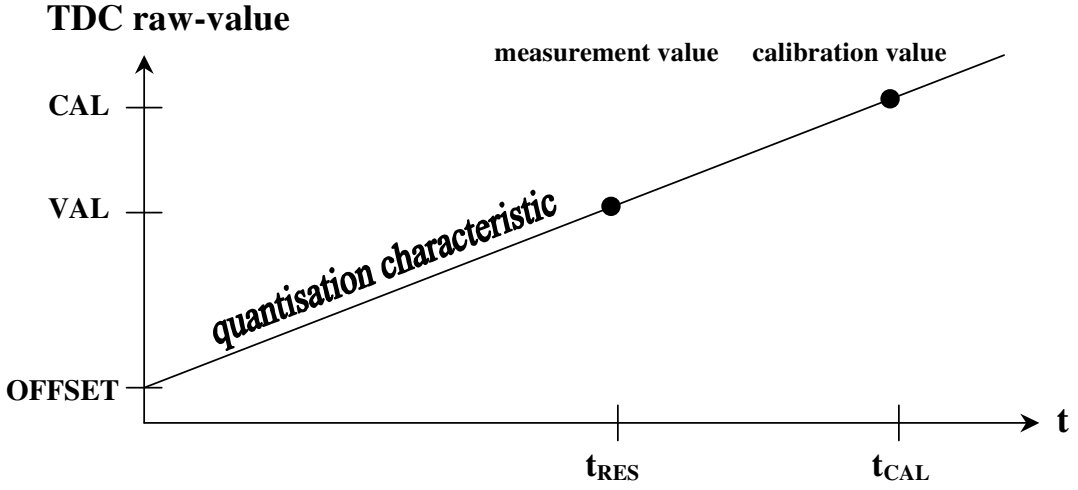


Figure 5.2: Characteristic of the TDC Measuring Core

5.2 Generating Calibration Values

To generate the calibration values OFFSET and CAL, shown in Figure 5.2, a calibration clock has to be provided at the TDC's pin CALCLK. This clock is the absolute time reference and therefore it must have the precision of a quartz crystal. The calibration clock is divided by the internal calibration clock divider. The resulting clock CLK is the internal reference clock. Its period length is measured during a calibration measurement using the measuring core.

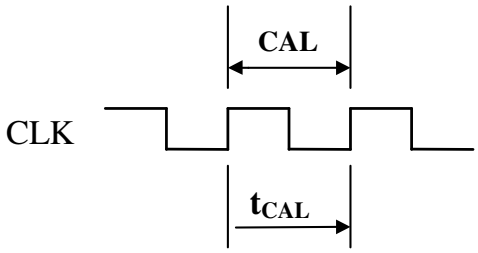


Figure 5.3: Calibration Measurement

Depending on the measurement mode the calibration measurement is performed for only one channel or both. Just like a measurement value **VAL** the resulting calibration values **CAL A / CAL B** and **OFFSET A / OFFSET B** are stored in the raw-value registers. The time $\mathbf{t_{CAL}}$ is well known: It is the divided calibration clock period.

A calibration measurement is performed either automatically after a timing measurement or has to be started separately from time to time depending on the measurement mode.

Unlike the measurement and calibration values VAL and CAL, the offset is very constant within a wide range of temperature and supply voltage. So it's not necessary to generate OFFSET all the times a calibration measurement is performed. Via software it's possible to disable the offset-generation during calibration measurement, resulting in a higher precision accuracy, when adapted to the measurement application properly.

5.3 Measurement Ranges and Measurement Modes

The TDC502 offers two measurement ranges:

- Range I: use of TDC-core for short time measurement: 0ps - 10µs *)
- Range II: use of TDC-core and precounter for long time measurement: 180ns – 210ms *) **)

The TDC502 provides eight measurement modes, programmable via the processor interface. In Table 5.1 all measurement modes are listed.

Measurement mode	Auto-calibration	Short description
0	yes	• Measurement range I • 1 channel (A or B programmable) with 10-fold multi-hit capability • Double pulse resolution: 25ns (5V, 25°C) • ALU: Calculation of every hit to start and every hit to each other hit, negative results possible
1	no	
2	yes	• Measurement range I • 2 channels with common start and 4-fold multi-hit capability each • Double pulse resolution: 0ps (different channels) resp. 25ns (same channel; 5V, 25°C) • ALU: Calculation of every hit to start and every hit to each other hit, negative results possible
3	no	
4	yes	• Measurement range I • 1 channel (A or B programmable) with 10-fold burst capability 'start-stop' • Dead time between burst mode measurements 'start-stop': 100ns (5V, 25°C) • ALU: calculation of each 'start-stop'
5	no	
6	yes	• Measurement range II • 1 channel (A or B programmable) with 4-fold multi-hit capability • Double pulse resolution: 1,5 * (divided) period of calibration clock + 105ns (5V, 25°C) • ALU: Calculation of every hit to start and every hit to each other hit, negative results not possible
7	no	

Note:

- *In measurement modes 1, 3, 5 and 7* ***separate calibration measurements*** *have to be performed on occasion by activating the action-bit 'separate calibration measurement' within the Init Register (see Chapter 6.5.1.1).*

Table 5.1: Measurement Modes

_____

*) *- typical at 5V, 25°C*
- High-Resolution: Maximum measurement period is shortened by half
- Smart-Resolution: Maximum measurement period is shortened to the fourth part

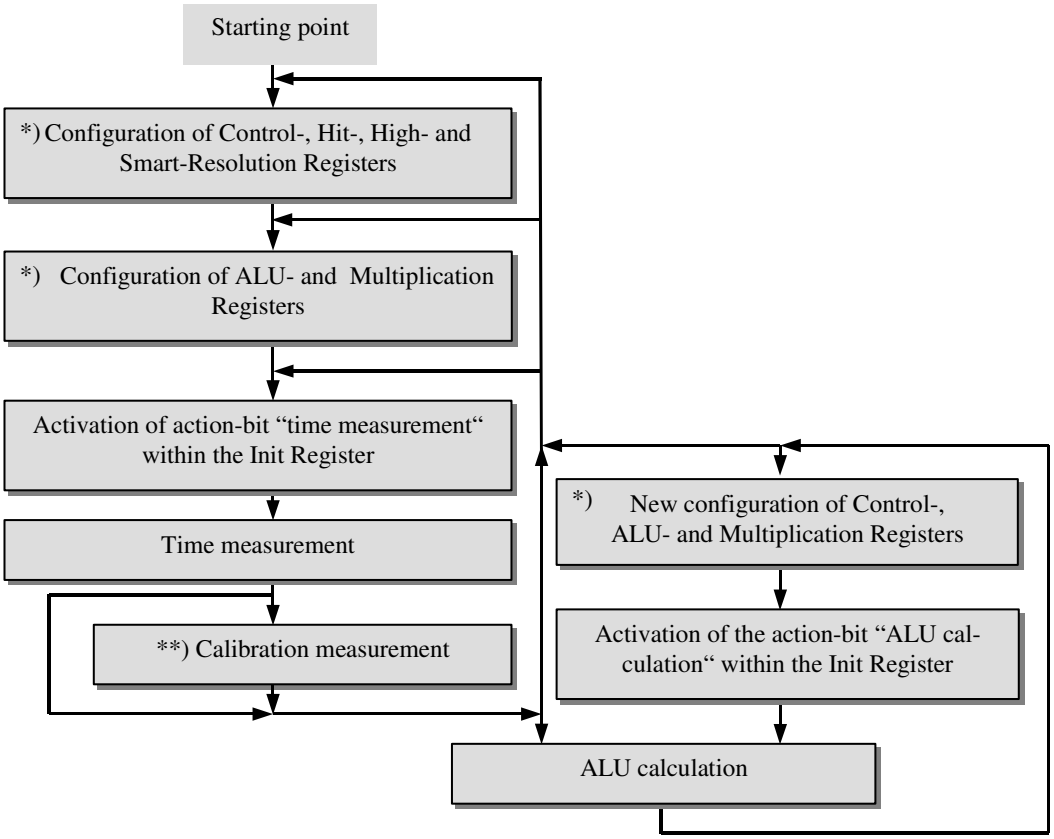
**) *Measurement range depends on period of calibration clock*

5.3.1 General Measurement Cycle

Figure 5.4 shows the flowchart of a general measurement cycle. At the very beginning of a measurement cycle the measurement mode, the usage of the ALU and so on has to be specified within the TDC's *Control Registers*. In the *Hit Register* the number of hits or burst mode measurements has to be defined a measurement cycle consists of. For optimization the TDC's differential non-linearity the *Smart-* and *High-Resolution Registers* have to be configured. If the ALU is used for calculation the measurement results, the *ALU Register* and maybe the *Multiplication Registers* have to be configured as well. For detailed information on the TDC registers refer to Chapter 6.5.

The actual measurement cycle is initiated by activating the action-bit 'time measurement' within the *Init-Register*: Now the TDC is ready for measurement and waits for a start-signal on the start-input START. After start has taken place the time measurement continues until the number of hits on the Stop-inputs STOP_A and STOP_B or the number of burst mode measurements specified in the Hit Register (cp. Chapter 6.5.1.3) is reached. If the ALU is not used for calculations the action-bit 'time measurement' is cleared automatically now in the measurement modes 1, 3, 5 and 7.

In measurement mode 2 an automatic calibration measurement follows, performed on both channels, in measurement modes 0, 4 and 6 on the channel selected in the Control Register. When the calibration measurement is completed and the ALU is not used for calculations the action-bit 'time measurement' is cleared now.



**) Configuration allowed only when no action-bit is set within the Init Register*
***) Possibility of separate calibration measurements via direct command*

Figure 5.4: General Measurement Cycle Flow

If the ALU is used, now the first calculation according to the ALU-calculation rules and specifications within the Control-, ALU- and Multiplication Registers is executed and the result of this first calculation within a measurement cycle is always stored in *result register 0*. Afterwards the action-bit 'time measurement' is cleared automatically.

After modifying the ALU-calculation rules, repetitive activation of the action-bit 'ALU calculation' within the Init Register makes an unlimited number of calculations possible. The results are stored then alternately in the *result registers 1, 0, 1, ...* . After completion a calculation the action-bit 'ALU calculation' is cleared automatically each time.

For another time measurement the action-bit 'time measurement' has to be reactivated. The first ALU-calculation result for a new measurement is always stored in *result register 0.*

Please notice, that configuring the Control-, Hit-, ALU-, Multiplication-, Smart- and High-Resolution Registers is only allowed when no action-bit is set within the Init Register.

5.3.2 Measurement Modes 0 and 1

Mode's 0 and 1 measurements are executed within measurement range I using the measuring core. As shown in Figure 5.5, one channel with up to 10 hits and a double pulse resolution of 25ns (5V, 25°C) is available. Via software channel A or channel B is selectable. When the time measurement is completed in measurement mode 0 an automatic calibration measurement on the selected channel follows according to Chapter 5.2.

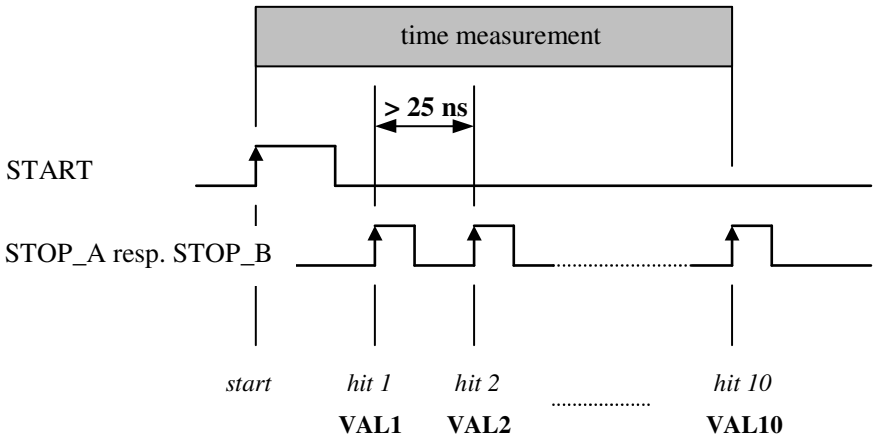


Figure 5.5: Measurement Modes 0 and 1

The time difference $\mathbf{t_{RES}}$ between *hit x* ($1 \le x \le 10$) and *start* is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$, the calibration values **CAL** and **OFFSET** and the measurement value **VALx** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\mathbf{(1)} \quad \mathbf{t_{RES}} = \frac{\mathbf{VALx - OFFSET}}{\mathbf{CAL - OFFSET}} * \mathbf{t_{CAL}}$$

The time difference $\mathbf{t_{RES}}$ between *hit y* ($1 \le y \le 10$) and *hit x* ($1 \le x \le 10$) is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VALy, VALx**, **CAL** and **OFFSET** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\mathbf{(2)} \quad \mathbf{t_{RES}} = \frac{\mathbf{VALy - VALx}}{\mathbf{CAL - OFFSET}} * \mathbf{t_{CAL}}$$

If the ALU is used for calculation the time difference $\mathbf{t_{RES}}$, the fraction of formulas 1 and 2 is computed during calibration. If the ALU is used not only for calibration but also for multiplication, $\mathbf{t_{CAL}}$ has to be set up within the *multiplication registers* to numbers between 0 and 2. If the multiplication is disabled via software, $\mathbf{t_{CAL}}$ remains 1 and no multiplication is executed.

If VALx is greater than VALy within formula 2, the measurement result $\mathbf{t_{RES}}$ becomes negative when using the TDC's ALU.

5.3.3 Measurement Modes 2 and 3

Mode's 2 and 3 measurements are executed within measurement range I using the measuring core. As shown in Figure 5.6, both channels with a *common start* and up to 4 hits each are available. The double pulse resolution is 25ns (5V, 25°C) for hits on the same channel and 0ns for hits on different channels. When the time measurement is completed in measurement mode 2 an automatic calibration measurement on both channels follows according to Chapter 5.2.

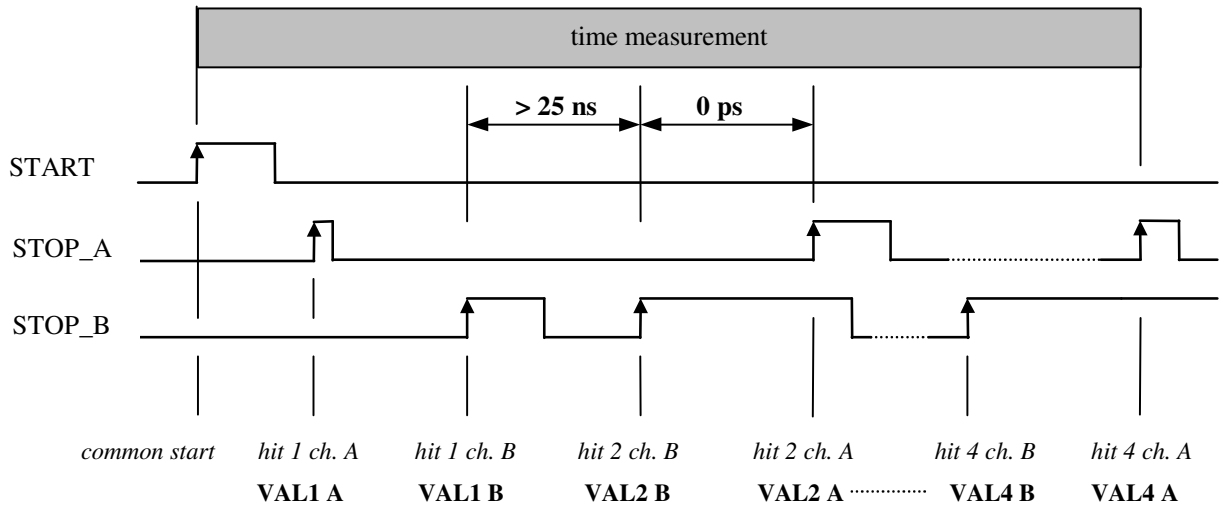


Figure 5.6: Measurement Modes 2 and 3

The time difference $\mathbf{t_{RES}}$ between *hit x* ($1 \le x \le 4$) on channel A (resp. channel B) and *common start* is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VALx A**, **CAL A** and **OFFSET A** (resp. **VALx B**, **CAL B** and **OFFSET B**) in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\textbf{(3)} \quad t_{RES} = \frac{\textbf{VALx A} - \textbf{OFFSET A}}{\textbf{CAL A} - \textbf{OFFSET A}} * t_{CAL}$$

resp.

$$\textbf{(4)} \quad t_{RES} = \frac{\textbf{VALx B} - \textbf{OFFSET B}}{\textbf{CAL B} - \textbf{OFFSET B}} * t_{CAL}$$

The time difference $\mathbf{t_{RES}}$ between *hit y* ($1 \le y \le 4$) and *hit x* ($1 \le x \le 4$) on the same channel is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VALy A, VALx A**, **CAL A** and **OFFSET A** for channel A (**VALy B, VALx B**, **CAL B** and **OFFSET B** for channel B) in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\textbf{(5)} \quad t_{RES} = \frac{\textbf{VALy A – VALx A}}{\textbf{CAL A – OFFSET A}} * t_{CAL}$$

resp.

$$\textbf{(6)} \quad t_{RES} = \frac{\textbf{VALy B – VALx B}}{\textbf{CAL B – OFFSET B}} * t_{CAL}$$

The time difference $\mathbf{t_{RES}}$ between *hit y* ($1 \le y \le 4$) on channel B and *hit x* ($1 \le x \le 4$) on channel A is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VALy B, VALx A**, **CAL B, OFFSET B** and **OFFSET A** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\textbf{(7)} \quad t_{RES} = \frac{\textbf{(VALy B – OFFSET B) – (VALx A – OFFSET A)}}{\textbf{CAL B – OFFSET B}} * t_{CAL}$$

The time difference $\mathbf{t_{RES}}$ between *hit y* ($1 \le y \le 4$) on channel A and *hit x* ($1 \le x \le 4$) on channel B is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VALy A, VALx B**, **CAL A, OFFSET A** and **OFFSET B** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\textbf{(8)} \quad t_{RES} = \frac{\textbf{(VALy A – OFFSET A) – (VALx B – OFFSET B)}}{\textbf{CAL A – OFFSET A}} * t_{CAL}$$

If the ALU is used for calculation the time difference $\mathbf{t_{RES}}$, the fraction of the formulas 3 to 8 is computed during calibration. If the ALU is used not only for calibration but also for multiplication, $\mathbf{t_{CAL}}$ has to be set up within the *multiplication registers* to numbers between 0 and 2. If the multiplication is disabled via software, $\mathbf{t_{CAL}}$ remains 1 and no multiplication is executed.

When using the TDC's ALU the measurement result $\mathbf{t_{RES}}$ may become negative.

Application Note:

When the stop-inputs STOP_A and STOP_B are combined the same time difference can be measured simultaneously on both channels. Averaging the two measurement results will improve the measurement's accuracy and double the TDC's resolution of up to 23ps at 5V resp. 33ps at 3.3V (typ).

5.3.4 Measurement Modes 4 and 5 (Burst Modes)

Mode's 4 and 5 measurements are executed within measurement range I using the measuring core. As shown in Figure 5.7, one channel with up to 10 burst mode measurements 'start-stop' is available. Via software channel A or channel B is selectable. For each burst mode measurement the whole measurement range (0ps – 10µs *)) is usable. The dead time between burst mode measurements is 100ns (5V, 25°C, see Appendix 8.10.3). When the last burst mode measurement is completed in measurement mode 4 an automatic calibration measurement on the selected channel follows according to Chapter 5.2.

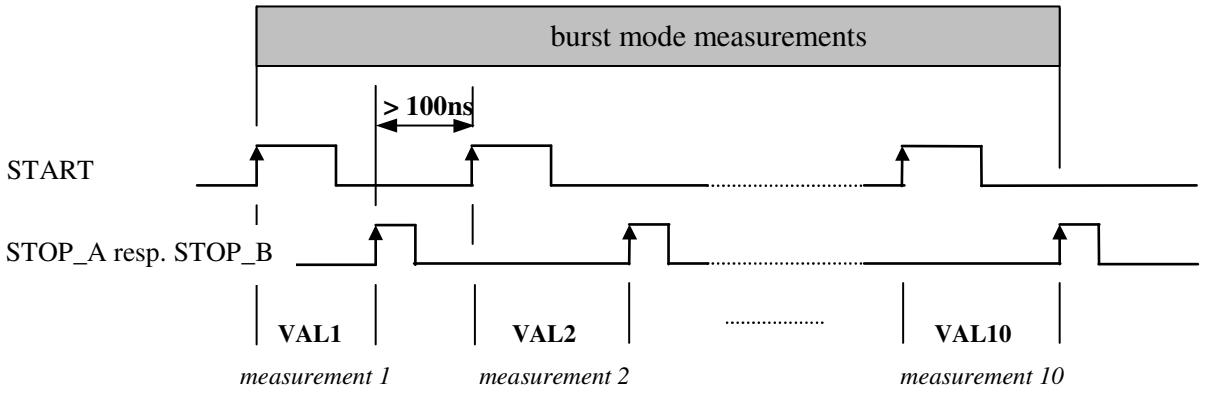


Figure 5.7: Burst Modes 4 and 5

The time difference $\mathbf{t_{RES}}$ of *burst mode measurement x* ($1 \le x \le 10$) is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$, the calibration values **CAL** and **OFFSET** and the measurement value **VALx** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\mathbf{(9)} \quad t_{RES} = \frac{VAL_X - OFFSET}{CAL - OFFSET} * t_{CAL}$$

If the ALU is used for calculation the time difference $\mathbf{t_{RES}}$, the fraction of formula 9 is computed during calibration. If the ALU is used not only for calibration but also for multiplication, $\mathbf{t_{CAL}}$ has to be set up within the *multiplication registers* to numbers between 0 and 2. If the multiplication is disabled via software, $\mathbf{t_{CAL}}$ remains 1 and no multiplication is executed.

When using the TDC's ALU the measurement result $\mathbf{t_{RES}}$ may become negative.

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*) *- typical at 5V, 25°C*
- High-Resolution: Maximum measurement period is shortened by half
- Smart-Resolution: Maximum measurement period is shortened to the fourth part

5.3.5 Measurement Modes 6 and 7

Mode's 6 and 7 measurements are executed within measurement range II using both, the measuring core and the precounter. As shown in Figure 5.8, one channel with up to 4 hits and a double pulse resolution of *1,5 * t_{CAL} + 105ns* (5V, 25°C) is available. In this formula $\mathbf{t_{CAL}}$ is the divided calibration clock period. Via software channel A or channel B is selectable. The minimum measurement period is *1,5 * t_{CAL} +105ns* (5V, 25°C), too. When the time measurement is completed in measurement mode 6 an automatic calibration measurement on the selected channel follows according to Chapter 5.2.

As shown in Figure 5.8 for each hit time measurements are divided into three stages:

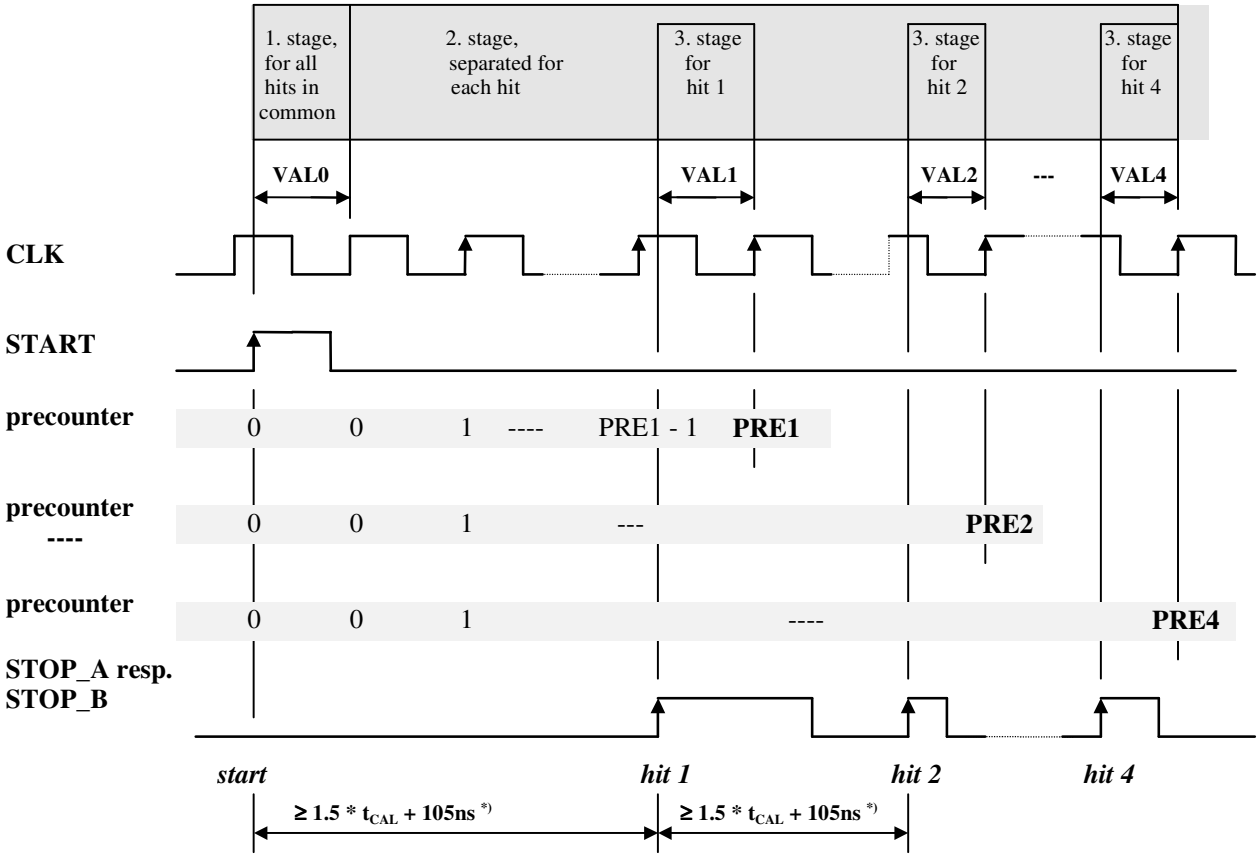


Figure 5.8: Measurement Modes 6 and 7

In the first stage of the measurement the measuring core determines the time difference between the start-signal and the following rising edge of the divided calibration clock for all hits in common. The output is stored as measurement value **VAL0** in a raw-value register. In the second stage of the measurement the *precounter* counts the clock periods t_{CAL} of the divided calibration clock CLK between the *start-signal* and *each hit*. The results are stored as precounter values **PREx (1 ≤ x ≤ 4)** in the raw-value registers. In the thirdstaget of the measurement the time between each hit and the following rising edge of the divided calibration clock is measured using the measuring core once again. The results are stored as measurement values **VALx (1 ≤ x ≤ 4)** in the raw-value registers.

The time difference $\mathbf{t_{RES}}$ between *hit x* ($1 \le x \le 4$) and *start* is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VAL0, VALx, PREx, CAL** and **OFFSET** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\mathbf{(10)}\quad \mathbf{t_{RES}} = \left[\frac{\mathbf{VAL0 - VALx}}{\mathbf{CAL - OFFSET}} + \mathbf{PREx} \right] * \mathbf{t_{CAL}}$$

The time difference $\mathbf{t_{RES}}$ between *hit y* and *hit x* ($1 \le x \le 3$, $2 \le y \le 4$, x < y) is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VALx, PREx, VALy, PREy, CAL** and **OFFSET** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\mathbf{(11)}\quad \mathbf{t_{RES}} = \left[\frac{\mathbf{VALx - VALy}}{\mathbf{CAL - OFFSET}} + \mathbf{PREy - PREx} \right] * \mathbf{t_{CAL}}$$

If the ALU is used for calculation the time difference $\mathbf{t_{RES}}$, the bracket term of formulas 10 and 11 is computed during calibration. If the ALU is used not only for calibration but also for multiplication, $\mathbf{t_{CAL}}$ has to be set up within the *multiplication registers* to numbers between 0 and 2. If the multiplication is disabled via software, $\mathbf{t_{CAL}}$ remains 1 and no multiplication is executed.

In measurement range II the TDC's ALU computes positive results only.

6 Functional Description

6.1 Calibration Clock Divider

Figure 6.1 shows the principle function of the calibration clock divider.

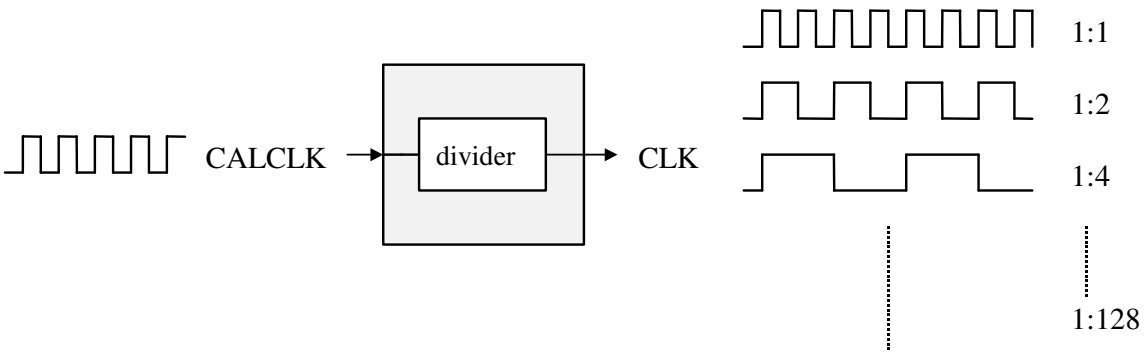


Figure 6.1: Calibration Clock Divider

The external calibration clock CALCLK is divided by the calibration clock divider. The division factors are programmable and can be set to 1, 2, 4, 8, 16, 32, 64 or 128.

Since a calibration measurement is always done by the TDC's measuring core, it is necessary to ensure that in measurement range I the clock period t_{CAL} of the divided calibration clock CLK is not larger than 10µs[*)] (5V, typ). Otherwise the measuement of the calibration clock period would cause a measuring core overflow OV_CORE (cp. formula A1 in Appendix 8.4.2). In measurement range II the divided calibration clock period t_{CAL} shouldn't be larger than 6.6µs[**)] (5V, typ) (cp. formula A4 in Appendix 8.5.2).

Depending on the power supply VDD the maximum frequency of the divided calibration clock CLK is limited as follows:

- 4.5V ≤ VDD ≤ 5.5 V: 20 MHz
- 3.0V ≤ VDD < 4.5 V: 10 MHz
- 2.7V ≤ VDD < 3.0 V: 6 MHz

In order to achieve high precision accuracy when measuring in measurement range I, the division factor should be selected in such a way, that the (largest) time difference to be measured is in the range of half the calibration clock period length. To achiev best measurement results in measurement range II the period of the divided calibration clock should be as long as possible.

---

*) *High-Resolution: 5µs, Smart-Resolution: 2.5µs*
**) *High-Resolution: 3.3µs, Smart-Resolution: 1.6µs*

6.2 Measurement Channels

Figure 6.2 shows the block diagram of the measurement channels.

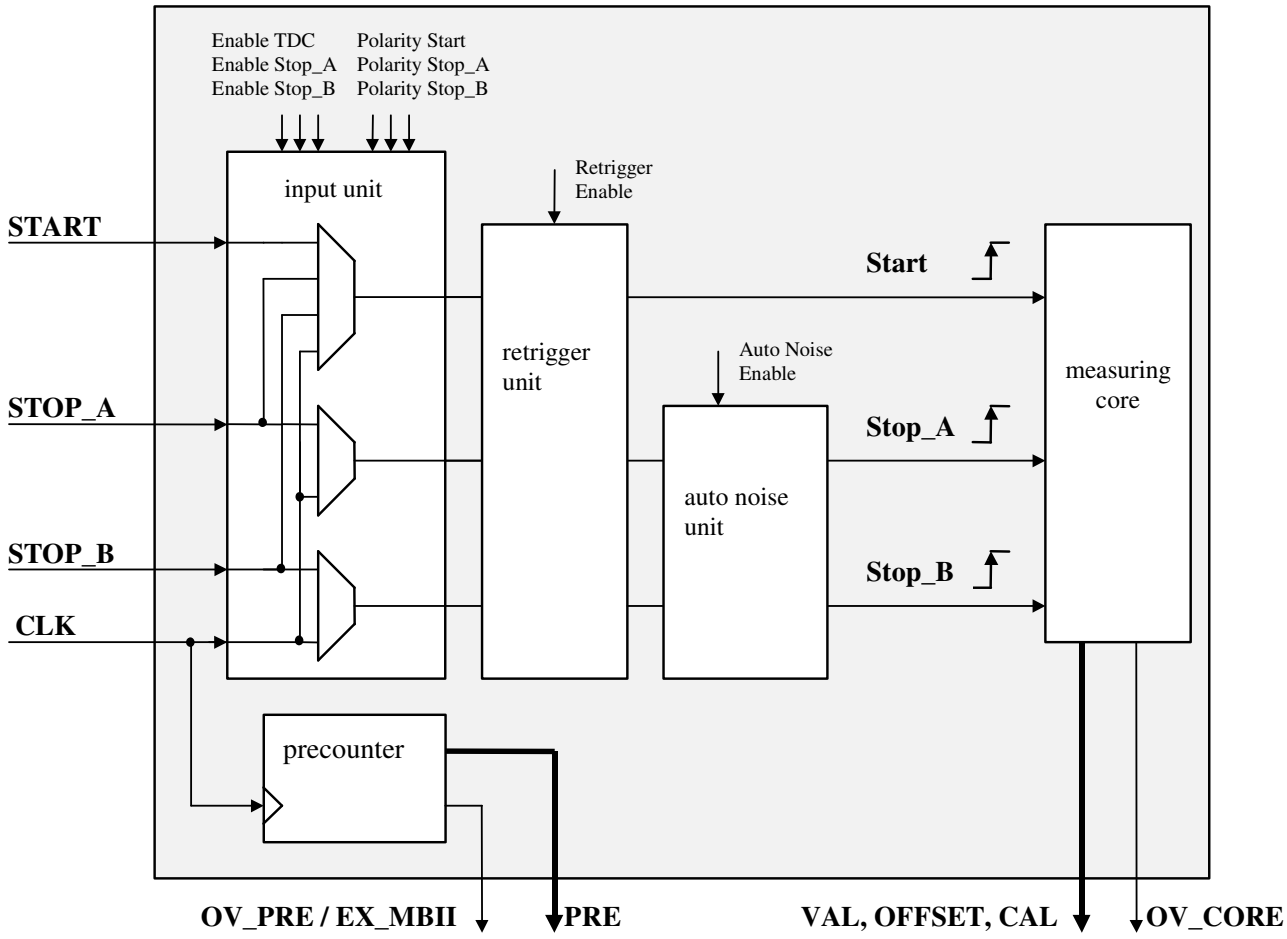


Figure 6.2: Measurement Channels Block Diagram

6.2.1 Input Unit

The input unit handles the incoming start-, stop- and calibration clock-signals using the following control signals:

- Enable TDC:

  The measurement channels are enabled by activating the action-bit ‘time measurement‘ within the Init Register. If the channels are disabled, no start-, stop- and calibration clock-signals will reach the measuring core and no measurement will take place. As an exception calibration measurements take place, no matter if the measurement channels are enabled or not.

- Enable Stop_A / Enable Stop_B:

  Using the pins EN_STOP_A and EN_STOP_B the stop-inputs STOP_A and STOP_B of the measurement channels can be disabled. No stop-signals will be passed to the measuring core. If the stop-inputs are enabled by EN_STOP_A or EN_STOP_B, they can also be enabled/disabled by software. Please notice, that in measurement range II the stop-input of the selected channel has to be enabled during the whole time measurement.

- Polarity Start / Polarity Stop_A / Polarity Stop_B:

  The edge-sensitivities of the TDC's start- and stop-inputs START, STOP_A and STOP_B are adjusted independently from each other by software. The input unit therefore triggers on rising or falling edges of the start- and stop-signals depending on the configuration.

Furthermore the input unit decides, which signal (start, stop or calibration clock) has to be passed on as a start- or stop-signal to the measuring core, depending on the measurement mode and on the partial step of the measurement cycle.

6.2.2 Precounter

In measurement range II the precounter counts the clock periods t_{CAL} of the divided calibration clock CLK between the start-signal and up to four hits. The precounter is enabled by the start-signal and disabled by the last hit, defined in the hit register (cp. Chapter 6.5.1.3). With every hit the current 15-bit counter reading PRE is stored as precounter value in a raw-value register. In doing so the maximum measurement period of measurement range II is $t_{MBIImax} = 2^{15} * t_{CAL}$ (cp. Appendix 8.5.2).

If the time difference the precounter has to measure exceeds the maximum measurement period, a precounter overflow OV_PRE will occur and - if enabled - the signal I_OV_PRE sets the TDC's interrupt request flag INTFAG (cp. Chapter 6.8.3.1). Thus, the ongoing measurement cycle is aborted including any automatic calibration measurement and ALU-calculations. All data (measurement and precounter values) already stored in the raw-value registers will remain unaffected.

Even if the expansion of measurement range II is enabled via software, a precounter overflow OV_PRE will occur and - if enabled - the signal I_OV_PRE will set the TDC's interrupt request flag INTFAG as well. The ongoing measurement cycle, however, is not aborted and the TDC's signal EX_MBII toggles at every overflow of the precounter: 1st overflow: 0 -> 1, 2nd overflow: 1 -> 0, 3rd overflow: 0->1 etc.

Remarks:

- *If the expansion is disabled, EX_MBII remains on high impedance.*
- *EX_MBII is only cleared on power-on and soft reset or by activating the action-bit 'time measurement', whereas it is not cleared by activating the action-bit 'separate calibration measurement', for example.*
- *If the expansion is enabled, ALU-calculations are only valid before 1st overflow.*

6.2.3 Retrigger Unit

If the retrigger unit is enabled, the measurement is re-started at the appearance of every start at the TDC's start-input START, as long as no stop (resp. hit) has been detected.

As shown in Figure 6.3, the determined time difference t_{RES} is the time between the *last* start and the stop/hit. If the retrigger unit isn't enabled then the time difference between the *first* start and the stop/hit is measured. The retrigger unit can be enabled by software for the measurement modes 0 to 5 (measurement range I).

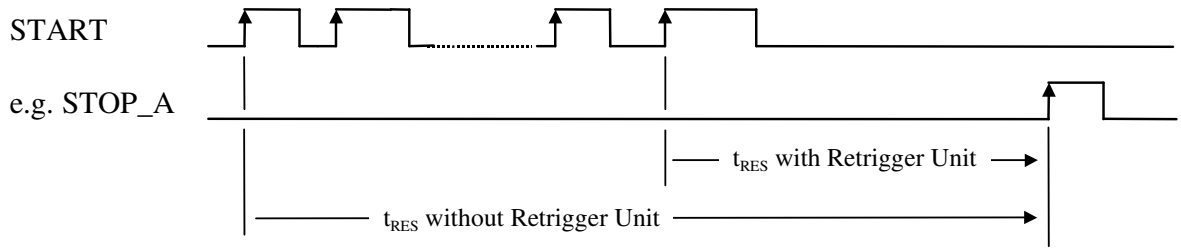


Figure 6.3 Measurement with and without Retrigger Unit

Remarks:

- *The maximum measurement period in measurement range I is 10µs (resp. 5 µs (High-Resolution), 2,5µs (Smart Resolution), (25°C, 5V), see Appendix 8.4.2), no matter if the retrigger unit is enabled or not. So if the time difference between a retriggering start and the start before exceeds the maximum measurement period, a measuring core overflow OV_CORE will occur and - if enabled - the signal I_OV_CORE sets the TDC's interrupt request flag INTFLAG (cp. Chapter 6.8.3). Thus, the ongoing measurement cycle is aborted including any automatic calibration measurement and ALU-calculations and the retriggering start will <u>not</u> restart the measurement.*
- *After the first start the minimum measurement period is 0,8 * t_s. The time t_s is the minimum pulse width of start- and stop-signals (cp. Appendix 8.7). After any retriggering start the minimum measurement period is 0ps as usual.*

6.2.4 Auto Noise Unit

The characteristic of the TDC is a straight line with offset and upward gradient, which due to the digital measurement procedure possesses quantisation stages – so called LSBs (Least Significant Bits) - with the width of the resolution. For a single measurement one therefore gets a quantisation error of up to one quantisation stage at ideal quantisation. This precision is sufficient for most applications.

A higher precision can be achieved when the measurement of the same time is repeated several times and statistical methods are used:

Changing the existing offset of the characteristic for each single measurement by delaying the stop-signal according to Figure 6.4 causes sampling at different positions of the characteristic, especially when measuring very constant time differences of a low noise signal. If the same offset shift is still present during the generation of the calibration values for the associated measurement value, the total offset is eliminated during the time difference calculation according to the formulas 1 to 11

(see Chapter 5.3). When averaging all the single measurements, there quantisation errors are averaged as well.

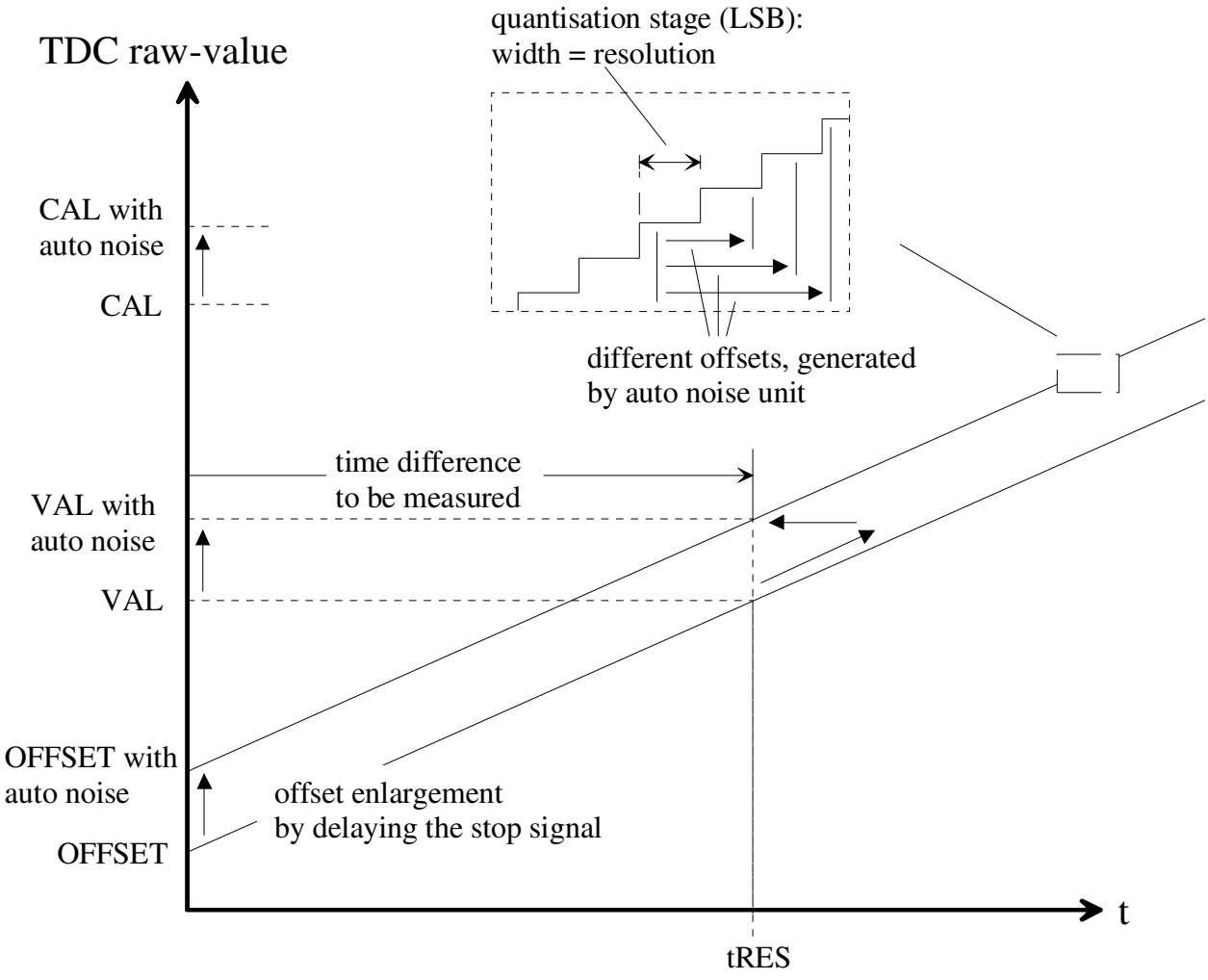


Figure 6.4: Influence of the Auto Noise Unit on the Characteristics of the TDC Measuring Core

If the auto noise unit is enabled a channel-specific delay is generated by a pseudo-random number generator. This delay is added to the already existing offset of the respective channel and can be changed with every activation of the action-bit 'clock auto noise' within the Init Register. The pseudo-random number generator provides 32 different states each generating another delay. The pseudo-random number generator is cleared on power-on reset only.

Remarks:

- *Maximum auto noise delay: 11ns (5V, typ, see Appendix 8.10.5).*
- *The auto noise unit is available only in the measurement modes 0 to 5 (measurement range I).*
- *For accuracy reasons averaging over 32, 64, 96, etc. measurements is recommended.*

6.2.5 Measuring Core

The measuring core determines the time difference between the start-signal and the hits with a programmable resolution of 45ps (Smart-Resolution), 90ps (High-Resolution), 180ps (Normal-Resolution) or 360ps (Half-Resolution) (25°C, 5V). The measuring core stores the measurement- and calibration values in the raw-value registers for further processing.

If the time difference the core has to measure exceeds the maximum measurement period (cp. Chapter 8.4.2), a measuring core overflow OV_CORE will occur and - if enabled - the signal I_OV_CORE sets the TDC's interrupt request flag INTFAG (cp. Chapter 6.8.3.1). Thus, the ongoing measurement cycle is aborted including any automatic calibration measurement and ALU-calculations.

To achieve a high precision accuracy electrical coupling effects can be minimized applying the TDC's separated power supply pins for the measuring core.

6.3 Hitcounter

Two hitcounters are provided, one for each channel.

Depending on the measurement mode and the channel selector bit within the Control Register CTRL_REG_1 the hitcounters register the hits detected on the respective channel. If the number of hits (resp. burst mode measurements) defined in the Hit Register (cp. Chapter 6.5.1.3) is reached, the time measurement is completed and an automatic calibration measurement or ALU-calibration may follow.

The Hit-Status Register HIT_STATUS_REG (cp. Chapter 6.5.2.1), readable via the processor interface, reflects the current state of the hitcounters.

Remarks:

- *The hitcounters are cleared on power-on and soft reset or by activating the action-bits 'time measurement' or 'separate calibration measurement'.*
- *The hitcounters are disabled during any kind of calibration measurements.*

6.4 Arithmetical Logic Unit (ALU)

The ALU executes time difference calculations (hit to start / hit to another hit, calibration and multiplication using a 24 bit unsigned integer number, negative results are possible!) on the measurement-, calibration- and precounter values of the raw-value registers in accordance with the formulas 1 to 11 (see Chapter 5.3).

For doing calculations the ALU requires calculation rules defined via software in the Control-, ALU- and Multiplication Registers.

If the ALU is enabled via software, the first ALU-calculation within a measurement cycle starts automatically following a time- or calibration measurement. The result of the first ALU-calculation within a measurement cycle is always stored in result register 0. After modifying the calculation rules an unlimited number of calculations can be initiated by activating the action-bit 'ALU calculation' again and again. The results are stored then alternating in the result registers 1, 0, 1, 0, .. .

During ALU-calculations the status flag ALU_BUSYN is active (low). When the result is calculated and stored in one of the two result registers, the status signal ALU_BUSYN is cleared (reset to '1') and - if enabled - the signal I_ALU_END sets the TDC's interrupt request flag INTFAG (cp. Chapter 6.8.3.1).

The ALU is provided with its own clock generator and is independent from TDC-external clocks. A calibration takes approx. 1,2µs (25°C, 5V) and the following multiplication approx. 2µs (25°C, 5V). Please see Appendix 8.11 for exact ALU-calculation times (calibration / multiplication).

6.5 TDC Registers

The width of all TDC registers is 8 bit. They are accessible via the processor interface (see Chapter 6.8). For addressing the registers refer to Chapter 7.1.

6.5.1 Read/Write Registers

All read/write registers are written with the rising edge of the signal WRN.

Please notice that it's only allowed to write the Control-, Hit-, Highresolution-, Smartresolution-, ALU- and Multiplication Registers when no action-bit is set within the Init Register (cp. Chapter 5.3.1).

6.5.1.1 Init Register

The Init Register provides direct commands which are executed by setting the register's bits to '1' (= activation of the action-bits). In doing so a time measurement, a separate calibration measurement or a ALU calculation is started or a soft reset is executed. For detailed information on the individual register bits refer to Chapter 7.2.1.1, Init Register (INIT_REG).

6.5.1.2 Control Registers

There are three Control Registers all in all. Here the measurement mode, the division factor for the calibration clock divider as well as the edges of the start- and stop-signals, on which the TDC will trigger, are selected. A detailed description of the individual register bits is given in Chapter 7.2.1.2, Control Registers (CRTL_REG_1 / CRTL_REG_2 / CTRL_REG_3).

6.5.1.3 Hit Register

In the Hit Register the number of hits for both channels is defined a measurement cycle consists of. In the burst mode the number of burst mode measurements 'start – stop' is defined. For detailed information on the individual register bits refer to Chapter 7.2.1.3, Hit Register (HIT_REG).

6.5.1.4 ALU Register

In this register the ALU-calculation rules are defined, according to the formulas 1 to 11 (see Chapter 5.3).

ALU-calculation rule format:

Calculate the time difference between the event of the register's HIGH_NIBBLE (hit, burst mode measurement) and the event of the register's LOW_NIBBLE (hit, start, common start).

In short: ***HIGH_NIBBLE – LOW_NIBBLE***

For detailed information on the individual register bits refer to Chapter 7.2.1.8, ALU Register (ALU_REG).

6.5.1.5 Multiplication Registers

In these three registers a 24 bit unsigned integer number (value range: 0 to 2) is specified. If the multiplication is enabled via software the ALU uses this value for multiplication according to the formulas 1 to 11 (see Chapter 5.3). For detailed information on the individual register bits refer to Chapter 7.2.1.9, Multiplication Registers (MULT_REG_1 / MULT_REG_2 / MULT_REG_3).

6.5.1.6 Interrupt Enable Register

In this register up to six IRQ flag set signals can be enabled for interrupt generation on pin INTFLAG. For detailed information on the individual register bits refer to Chapter 7.2.1.4, Interrupt Enable Register (INT_EN_REG).

6.5.1.7 High-Resolution Registers

There is a High-Resolution Register for each channel. In order to achieve an minimized differential non-linearity fine-tuning for High- and Smart-Resolution is done in these registers. For detailed information on the individual register bits refer to Chapter 7.2.1.6, High-Resolution Registers (HIGH_REG_A / HIGH_REG_B).

6.5.1.8 Smart-Resolution Registers

There is a Smart-Resolution Register for each channel. In order to achieve an minimized differential non-linearity fine-tuning for Smart-Resolution is done in these registers. A detailed description of the individual register bits is given in Chapter 7.2.1.7, Smart-Resolution Registers (SMART_REG_A / SMART_REG_B).

6.5.1.9 GPIO Configuration Register

The TDC provides four general purpose I/O-pins GPIO0, GPIO1, GPIO2 and GPIO3, individually configurable as input or output via this register. A pin configured as output drives a ‘0’ or ‘1’, according to the level specified also in this register. A detailed description of the individual register bits is given in Chapter 7.2.1.5, GPIO Configuration Register (GPIO_REG).

6.5.2 Read-only Registers

6.5.2.1 Hit-Status Register

The Hit-Status Register reflects the current number of hits or burst mode measurements detected for each channel. A detailed description of the individual register bits is given in Chapter 7.2.2.1, Hit-Status Register (HIT_STATUS_REG).

6.5.2.2 GPIO Input Register

The levels of all four general purpose I/O-pins GPIO0, GPIO1, GPIO2 and GPIO3 can be read via the GPIO Input Register. A detailed description of the individual register bits is given in Chapter 7.2.2.2, GPIO Input Register (GPIO_IN_REG).

6.5.2.3 Status Register

The Status Register reflects the current state of the TDC. The Status Register contains six status flags, which are described in detail in Chapter 6.8.3.1, Status Flags and Chapter 7.2.2.3, Status Register (STATUS_REG).

6.6 Raw-Value Registers

The TDC provides 12 read-only raw-value registers, in which the measurement values VAL of each hit (resp. each burst mode measurement), the calibration values OFFSET and CAL and the pre-counter values PRE of each hit in the measurement range II are stored for further processing. The width of all raw-value registers is 16 bit. The registers can be read out via the processor interface. For addressing the raw-value registers see Chapter 7.1 and Chapter 7.3.

6.7 Result Registers

The TDC provides two read-only result registers, in which the measurement results RES of the ALU-calculations are stored alternately within a measurement cycle beginning with result register 0. The width of the result registers is 32 bit. The registers can be read out via the processor interface. For addressing the result registers see Chapter 7.1.

6.8 Processor Interface

Figure 6.5 shows the block diagram of the processor interface.

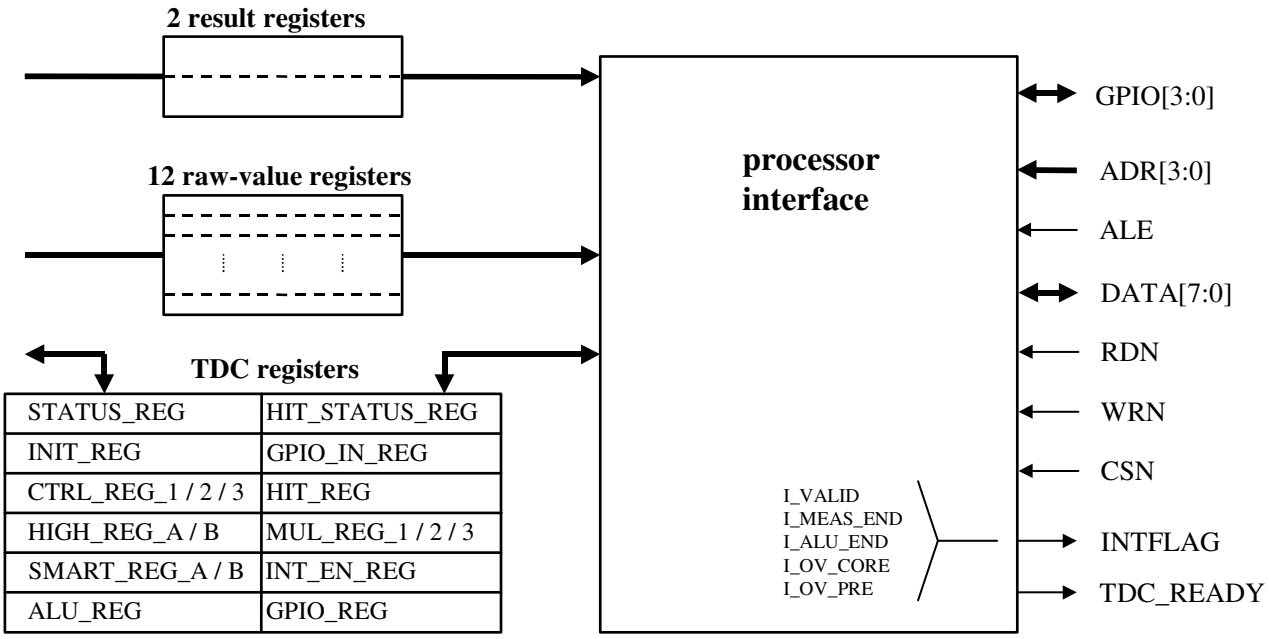


Figure 6.5: Block Diagram Processor Interface

Via the processor interface the access to all TDC registers is performed as well as the access to the raw-value and result registers.

In addition to data- and control lines the processor interface provides a status flag, an interrupt request flag and four general purpose I/O-pins, individually configurable as input or output.

6.8.1 General Purpose I/O-Pins

The TDC provides four general purpose I/O-pins, individually configurable as input or output via the GPIO Configuration Register GPIO_REG. A pin configured as output drives a '0' or '1', according to the level specified in the same register. The level of each pin can be read via the GPIO Input Register GPIO_IN_REG, regardless whether configured as input or output.

6.8.2 Data- and Control Lines

6.8.2.1 Overview

The TDC502 provides the following data- and control lines:

- DATA[7:0]: Bi-directional data bus
- CSN: Chip select (low active)
- RDN: Read strobe (low active)
- WRN: Write strobe (low active)
- ADR[3:0]: Address bus
- ALE: Address latch enable (high active)

The processor interface provides an address latch, controlled by ALE, in order to make various applications for connecting diverse processors resp. controllers possible:

- Separated data/address bus: The address latch is transparent (ALE = 1). Thus, in principle, all controllers addressing a SRAM directly are connectable, e.g. RENESAS H8-Controller.
- Shared data/address bus: Using ALE, in principle all 8051-compatible 8-bit controllers are directly connectable, e.g. ATMEL AT89S53. 16-bit controller such as SIEMENS C167SR are possible, too.

6.8.2.2 Timing Diagrams

Figure 6.6 and Figure 6.7 show the read and write cycle timings for applications with separated data/address bus. In Figure 6.8 and Figure 6.9 the read and write cycle timings for applications with shared data/address bus are shown. In Table 6.1 and Table 6.2 the associated read and write cycle timing characteristics are specified.

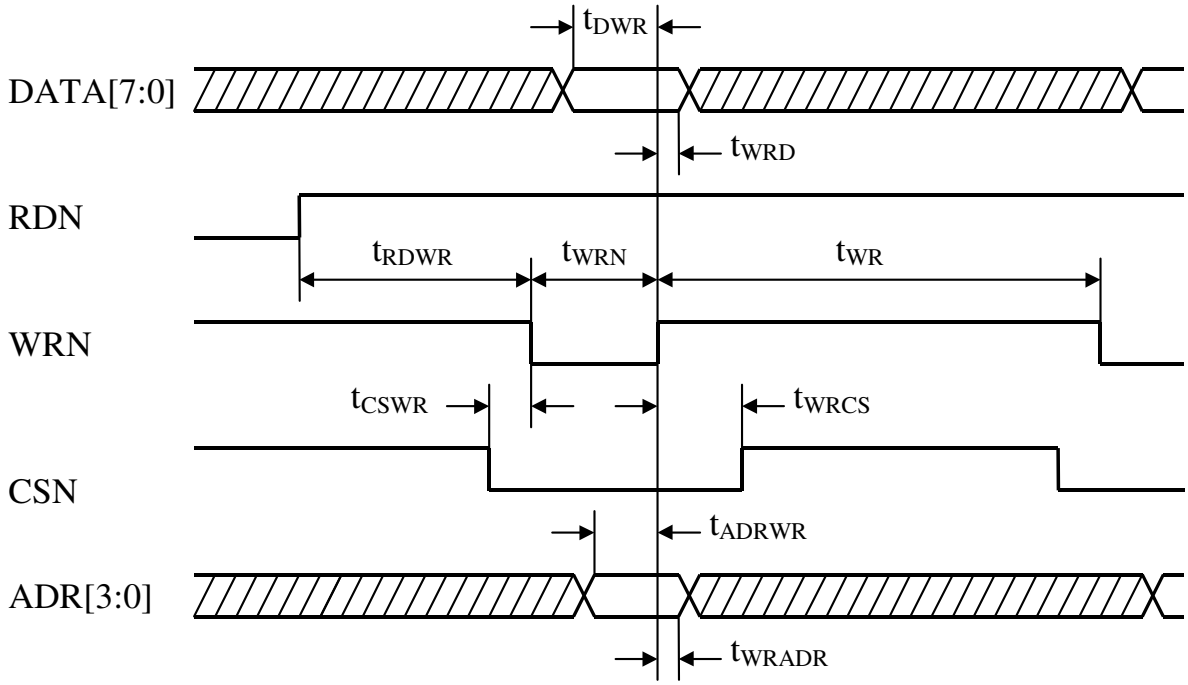


Figure 6.6: Separated Data/Address Bus: Write Cycle Timing (ALE = 1)

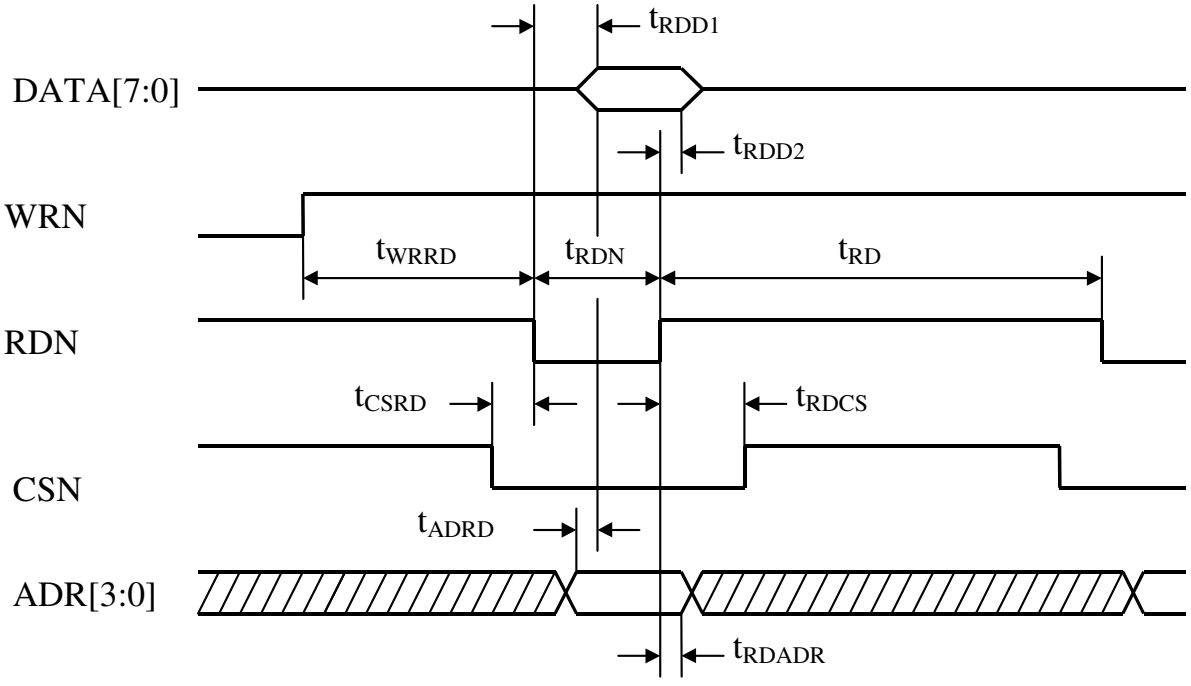


Figure 6.7: Separated Data/Address Bus: Read Cycle Timing (ALE = 1)

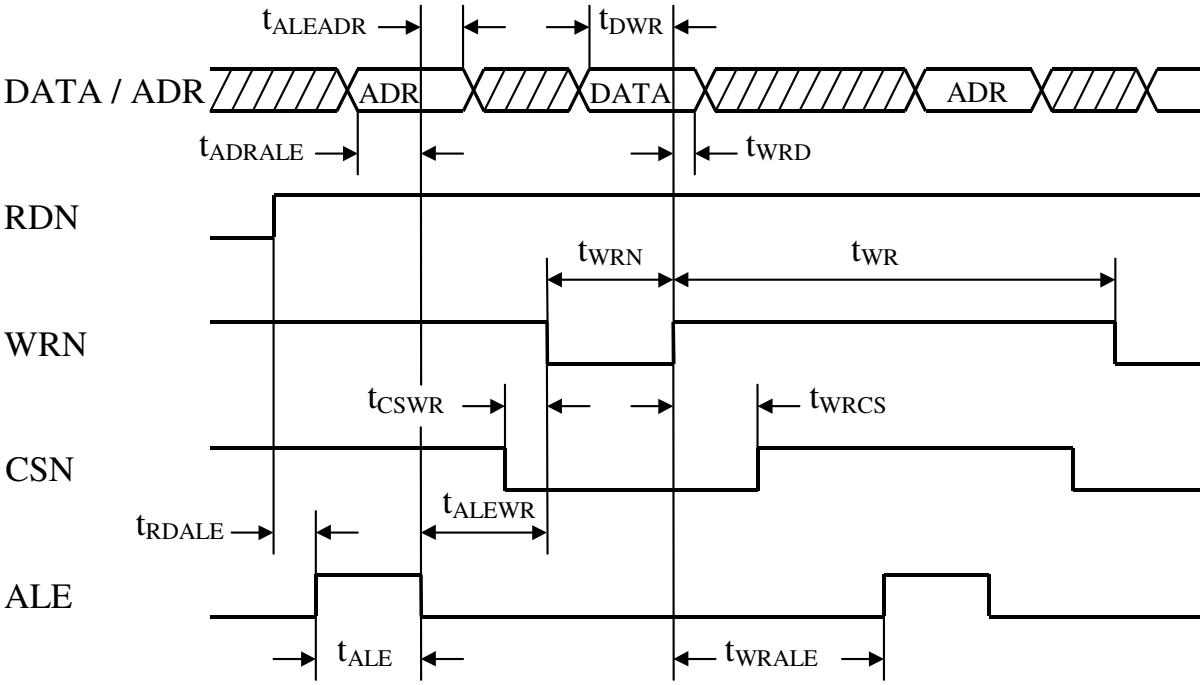


Figure 6.8: Shared Data/Address Bus: Write Cycle Timing

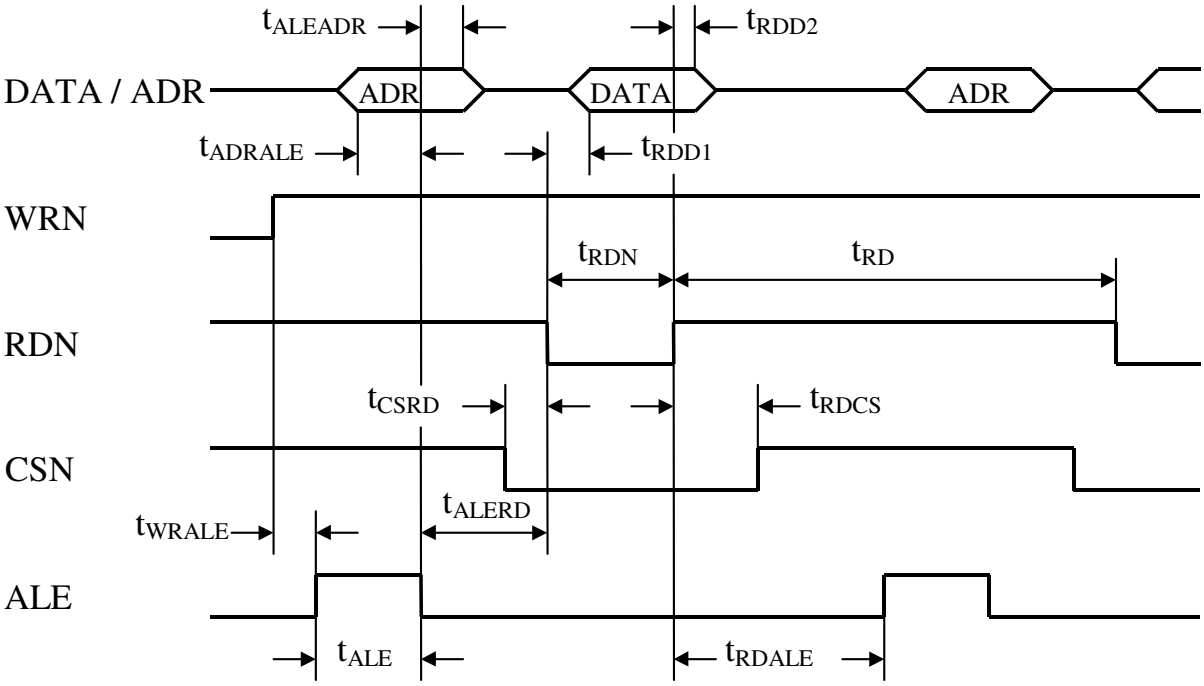


Figure 6.9: Shared Data/Address Bus: Read Cycle Timing

Parameter	Min	Max	Unit
t_{WRN}	25	-	ns
t_{WR}	25	-	ns
t_{DWR}	8	-	ns
t_{WRD}	0	-	ns
t_{ADRWR}	8	-	ns
t_{WRADR}	2	-	ns
t_{CSWR}	0	-	ns
t_{WRCS}	0	-	ns
t_{RDWR}	25	-	ns
t_{ADRALE}	3	-	ns
t_{ALEADR}	3	-	ns
t_{ALE}	17	-	ns
t_{ALEWR}	3	-	ns
t_{WRALE}	5	-	ns
t_{RDALE}	5	-	ns

- VDD = 5V ± 10%, T_A = -40 to +85°C, Load = 30pF
- 3.0V ≤ VDD < 4.5 V: All times listed above have to be multiplied by 1.5
- 2.7V ≤ VDD < 3.0V: All times listed above have to be multiplied by 2

Table 6.1: Write Cycle Timing Characteristics

Parameter	Min	Max	Unit
t_{RDN}	25	-	ns
t_{RD}	25	-	ns
t_{RDD1}	3	15	ns
t_{RDD2}	2	15	ns
t_{ADRD}	-	15	ns
t_{RDADR}	3	-	ns
t_{CSRD}	0	-	ns
t_{RDCS}	0	-	ns
t_{WRRD}	25	-	ns
t_{ADRALE}	3	-	ns
t_{ALEADR}	3	-	ns
t_{ALE}	17	-	ns
t_{ALERD}	3	-	ns
t_{RDALE}	5	-	ns
t_{WRALE}	5	-	ns

- VDD = 5V ± 10%, T_A = -40 to +85°C, Load = 30pF
- 3.0V ≤ VDD < 4.5 V: All times listed above have to be multiplied by 1.5
- 2.7V ≤ VDD < 3.0V: All times listed above have to be multiplied by 2

Table 6.2: Read Cycle Timing Characteristics

6.8.3 Status and Interrupt Request Flags

6.8.3.1 Status Flags

Six status flags are provided, reflecting the current state of the TDC. The status flags are accessible via the Status Register (see Chapter 7.2.2.3). In Table 6.3 all status flags are described in detail.

Status Flag		Description
TDC_READY	0:	TDC not ready, measurement channels are disabled (default).
	1:	Set by activation of action-bit 'time measurement': TDC is ready for measurement and waits for a start-signal on the start-input START. After start has taken place TDC_READY is cleared until the next activation of action-bit 'time measurement'. If the retrigger unit is enabled, the TDC remains ready as long as no stop (resp. hit) is detected. In the burst measurement modes 4 and 5 the TDC will be also ready between the burst mode measurements until the number of burst mode measurements specified in the Hit Register (cp. Chapter 6.5.1.3) is reached.
VALID	0:	Raw-value register empty: No valid data for readout (default).
	1:	At least one raw-value register contains valid data for readout: VALID is set to '1' when the first raw-value of a time- or calibration measurement is generated. VALID remains '1' until it's cleared. VALID is cleared only on power-on and soft reset or by activating the action-bits 'time measurement' or 'separate calibration measurement'.
MEAS_BUSYN	0:	After the (first) start on the start-input the flag MEAS_BUSYN is set to '0', no matter if the retrigger unit is enabled or not: Time measurement or calibration measurement (automatic, separate) is in action, since the measuring core and/or the precounter is busy. In the burst measurement modes 4 and 5 MEAS_BUSYN remains '0' between the burst mode measurements. In the measurement modes with automatic calibration measurement (modes 0, 2, 4 and 6) MEAS_BUSYN remains '0' between time- and calibration measurement.
	1:	No time- or calibration measurement is in action (default).
ALU_BUSYN	0:	ALU is in action (calibration / multiplication).
	1:	ALU is idle (default).
OV_CORE	0:	No measuring core overflow (Default).
	1:	Measuring core overflow. OV_CORE is cleared on power-on and soft reset or by activating the action-bits 'time measurement' or 'separate calibration measurement'.
OV_PRE	0:	No precounter overflow (Default).
	1:	Precounter overflow: No matter if the expansion of measurement range II is enabled or not, OV_PRE is set to '1' at the first overflow of the precounter. OV_PRE is cleared on power-on and soft reset or by activating the action-bits 'time measurement' or 'separate calibration measurement'.

Table 6.3: Status Flags

TDC_READY is the only status flag also accessible via pin [*)].

[*)] *For timing characteristics of pin TDC_READY refere to Appendix 8.9.*

6.8.3.2 Interrupt Request Flag

For interrupt generation at the connected processor the TDC provides an interrupt request flag on pin INTFLAG. Via software up to six IRQ flag set signals can be enabled at the same time:

- I_VALID: Set to '1', when the first raw-value register is filled with valid data.
- I_MEAS_END: Set to '1', when separate calibration measurement or time measurement (with/without automatic calibration measurement) is finished. All relevant raw-value registers are filled with valid data if the measurement was correct.
- I_ALU_END: Set to '1', when ALU-calculations are completed and the relevant result register is filled with valid data.
- I_OV_CORE: Set to '1', when a measuring core overflow occurs.
- I_OV_PRE: Set to '1', when (the first) precounter overflow occurs.

INTFLAG and all IRQ flag set signals are cleared on power-on reset on pin RSTN or by activating one of the following action-bits within the Init Register:

- 'reset INTFLAG' - 'ALU calculation' - 'soft reset'
- 'separate calibration measurement' - 'time measurement'

6.8.3.3 Correlation of Status Flags and Interrupt Request Flag set Signals

Figure 6.10 shows exemplarily the correlation of status flags and IRQ flag set signals on the base of a correct and two faulty measurement cycles. The status flags are represented as time dependant characteristics. Setting IRQ flag set signals to '1' is marked as events.

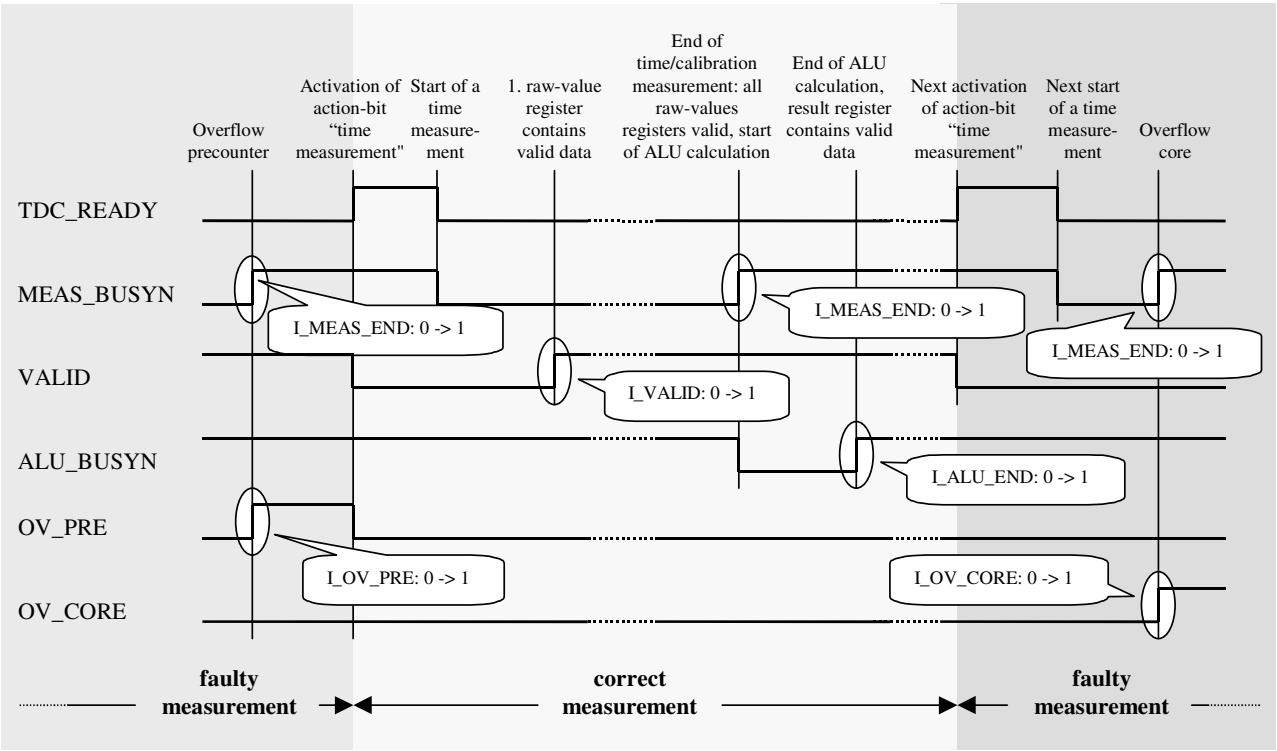


Figure 6.10: Correlation of Status Flags and Interrupt Request Flag set Signals

7 Programming of the TDC502

Programming the TDC, configuring and reading out the TDC's status and measurement results is done via the processor interface. The relevant data is read and written via the bi-directional data bus DATA[7:0].

7.1 Addressing

As shown in Table 7.1, the TDC provides four address spaces for addressing the TDC registers, the raw-value registers and the result registers via the address bus ADR[3:0]. The address spaces are selectable via the bits 6 and 7 of the Init Register.

The Init Register, the Hit-Status Register, the GPIO Input Register and the Status Register are visible within all address spaces. In Table 7.1 all read/write registers are marked in gray color, all read-only registers are unmarked.

	Address space 0 *) INIT_REG[7:6] = 00	**Address space 1** INIT_REG[7:6] = 01	**Address space 2** INIT_REG[7:6] = 10	**Address space 3** INIT_REG[7:6] = 11
ADR[3:0]	D7 D0	D7 D0	D7 D0	D7 D0
0x0	INIT_REG	INIT_REG	INIT_REG	INIT_REG
0x1	CTRL_REG_1	MULT_REG_1	ROH_REG_0[7:0]	ROH_REG_6[7:0]
0x2	CTRL_REG_2	MULT_REG_2	ROH_REG_0[15:8]	ROH_REG_6[15:8]
0x3	CTRL_REG_3	MULT_REG_3	ROH_REG_1[7:0]	ROH_REG_7[7:0]
0x4	HIT_REG	ALU_REG	ROH_REG_1[15:8]	ROH_REG_7[15:8]
0x5	INT_EN_REG	ERG_REG_0[7:0]	ROH_REG_2[7:0]	ROH_REG_8[7:0]
0x6	GPIO_REG	ERG_REG_0[15:8]	ROH_REG_2[15:8]	ROH_REG_8[15:8]
0x7	--	ERG_REG_0[23:16]	ROH_REG_3[7:0]	ROH_REG_9[7:0]
0x8	HIGH_REG_A	ERG_REG_0[31:24]	ROH_REG_3[15:8]	ROH_REG_9[15:8]
0x9	HIGH_REG_B	ERG_REG_1[7:0]	ROH_REG_4[7:0]	ROH_REG_10[7:0]
0xA	SMART_REG_A	ERG_REG_1[15:8]	ROH_REG_4[15:8]	ROH_REG_10[15:8]
0xB	SMART_REG_B	ERG_REG_1[23:16]	ROH_REG_5[7:0]	ROH_REG_11[7:0]
0xC	--	ERG_REG_1[31:24]	ROH_REG_5[15:8]	ROH_REG_11[15:8]
0xD	GPIO_IN_REG	GPIO_IN_REG	GPIO_IN_REG	GPIO_IN_REG
0xE	HIT_STATUS_REG	HIT_STATUS_REG	HIT_STATUS_REG	HIT_STATUS_REG
0xF	STATUS_REG	STATUS_REG	STATUS_REG	STATUS_REG
	MSB LSB	MSB LSB	MSB LSB	MSB LSB

**) Default address space after power-on or soft reset*

Table 7.1: Address Spaces and Register Addresses

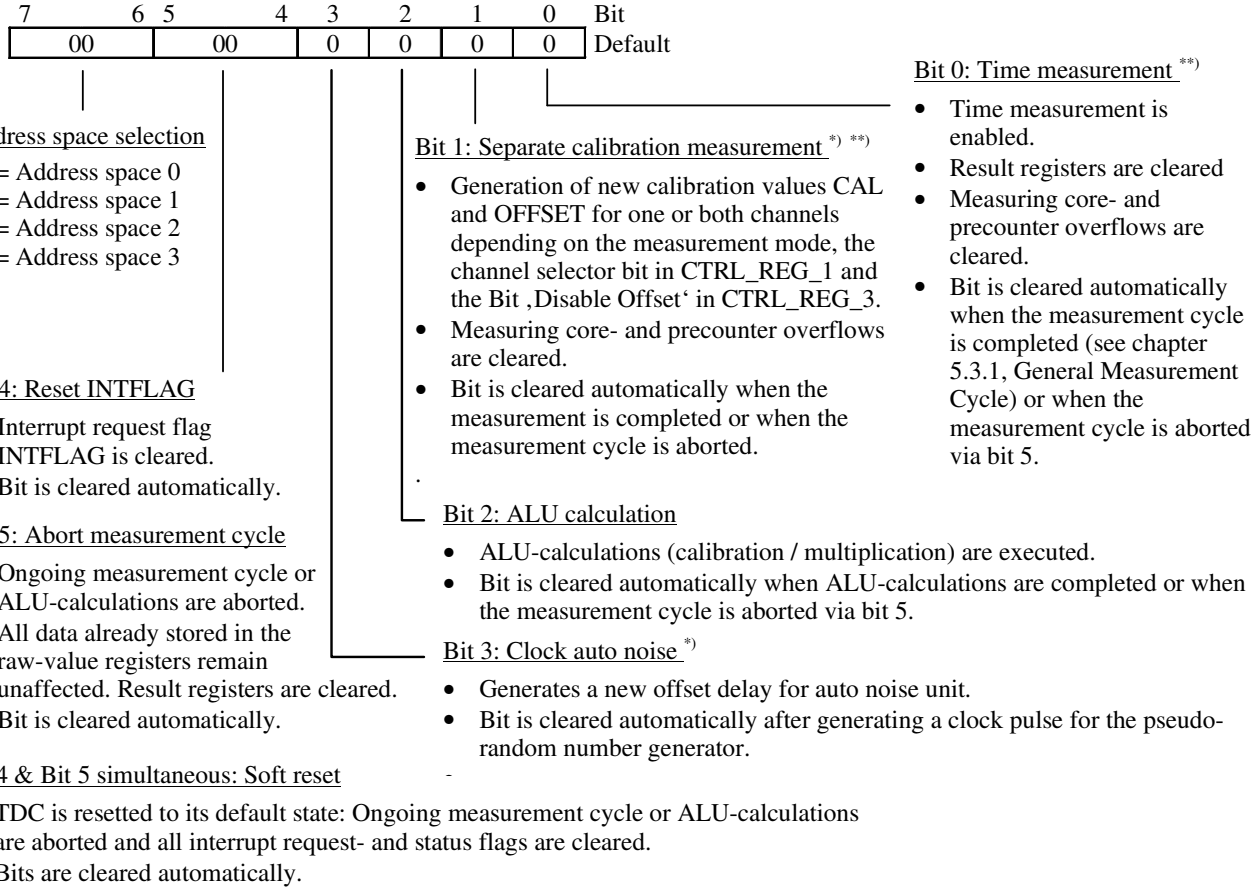
7.2 TDC Registers

The TDC provides 15 read/write registers and 3 read-only registers.

7.2.1 Read/Write Register Formats

7.2.1.1 Init Register (INIT_REG)

Figure 7.1 shows the format of the Init Register. Via the bits 6 and 7 the address spaces for addressing all registers of the TDC are selectable. Setting the other bits to '1' (= activation of action-bits) starts direct commands. When the direct commands are completed the relevant bits are cleared to '0' automatically.



*) *Execution of this direct command allowed only when the action-bit 'time measurement' is not set!*

**) *Do not clear this bit manually! In doing this anyhow (e.g. when resetting INTFLAG via bit 4 during a time measurement) the measurement cycle is aborted irregularly and immediately.*

Figure 7.1: Init Register INIT_REG Format

7.2.1.2 Control Registers (CRTL_REG_1 / CRTL_REG_2 / CTRL_REG_3)

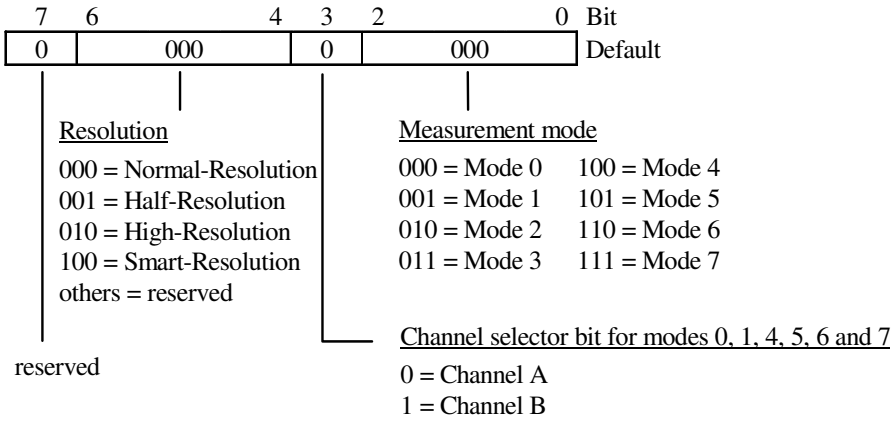
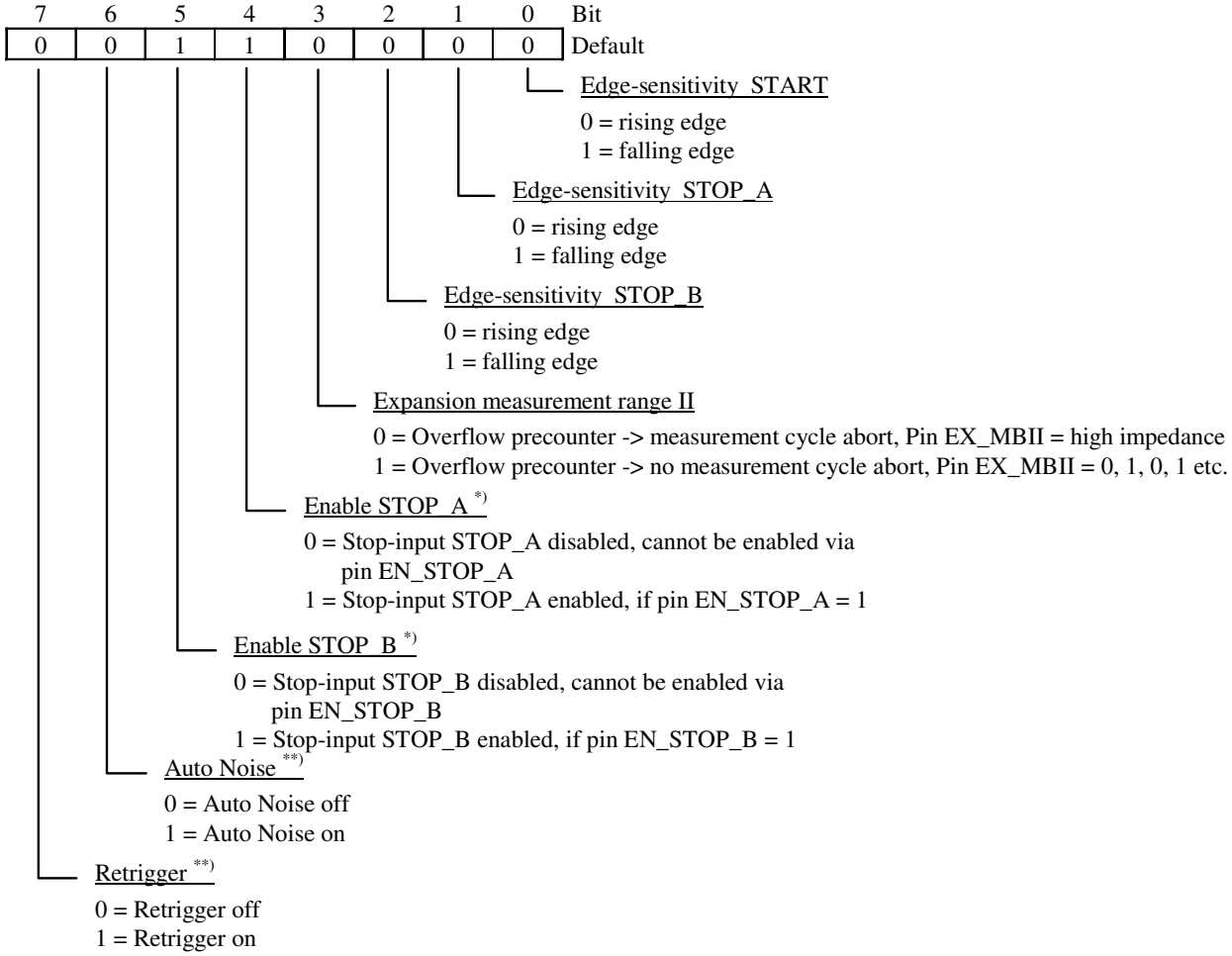


Figure 7.2: CTRL_REG_1 Format



**) In measurement range II the stop-input of the selected channel has to be enabled during the whole time measurement.*
***) Bits relevant only for measurement modes 0 up to 5. Have to be set to'0' for modes 6 and 7.*

Figure 7.3: CTRL_REG_2 Format

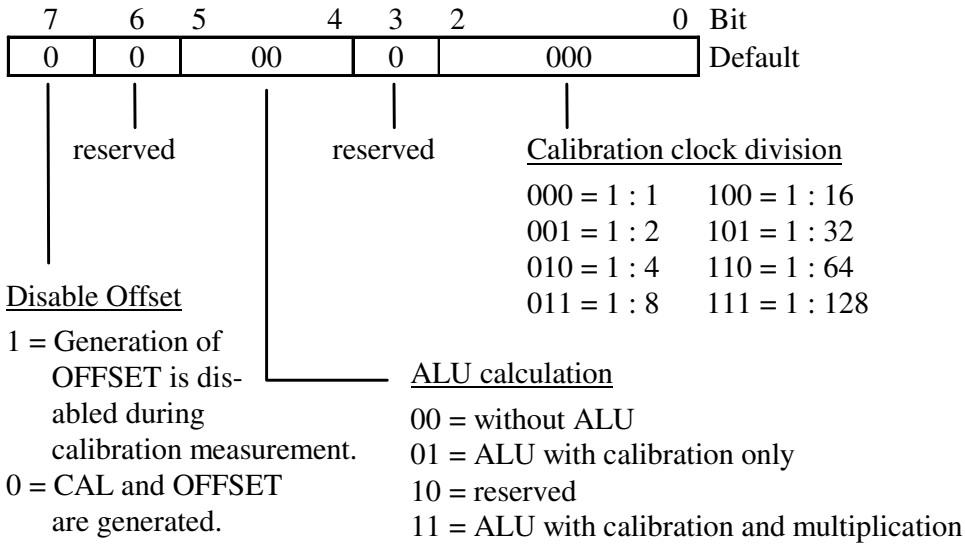


Figure 7.4: CTRL_REG_3 Format

7.2.1.3 Hit Register (HIT_REG)

Figure 7.5 shows the format of the Hit Register. Be sure to enable not more hits/burst mode measurements than allowed within the selected measurement mode (see Table 5.1). Within the measurement modes 0, 1, 4, 5, 6 and 7 only four bits of the Hit Register are relevant depending on the channel selector bit of CTRL_REG_1. Within the measurement modes 2 and 3 all bits are relevant.

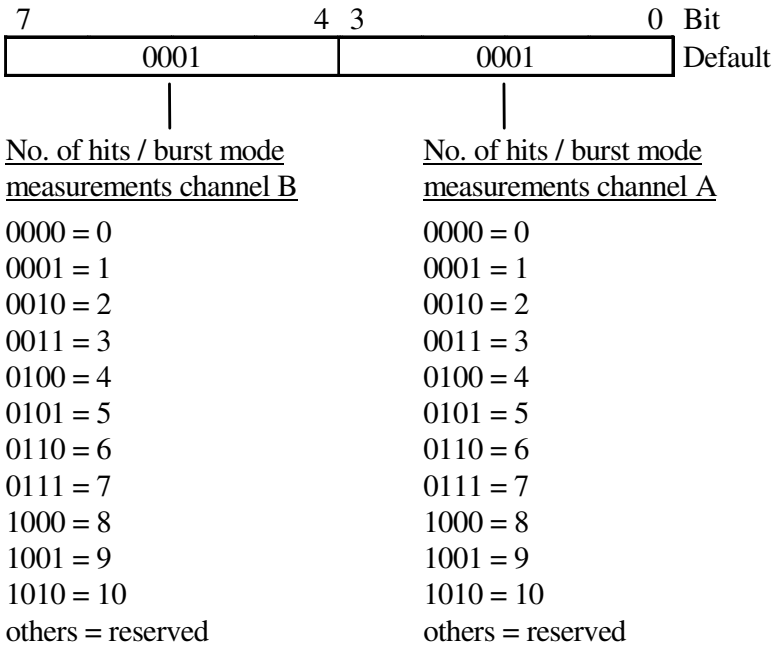


Figure 7.5: HIT_REG Format

7.2.1.4 Interrupt Enable Register (INT_EN_REG)

Figure 7.6 shows the format of the Interrupt Enable Register. A detailed description of the register bits, representing the enabling of the interrupt request flag set signals, is given in Chapter 6.8.3.2.

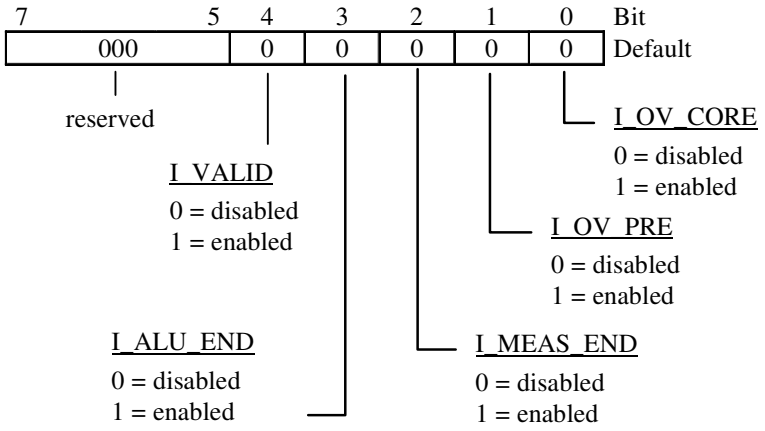


Figure 7.6: INT_EN_REG Format

7.2.1.5 GPIO Configuration Register (GPIO_REG)

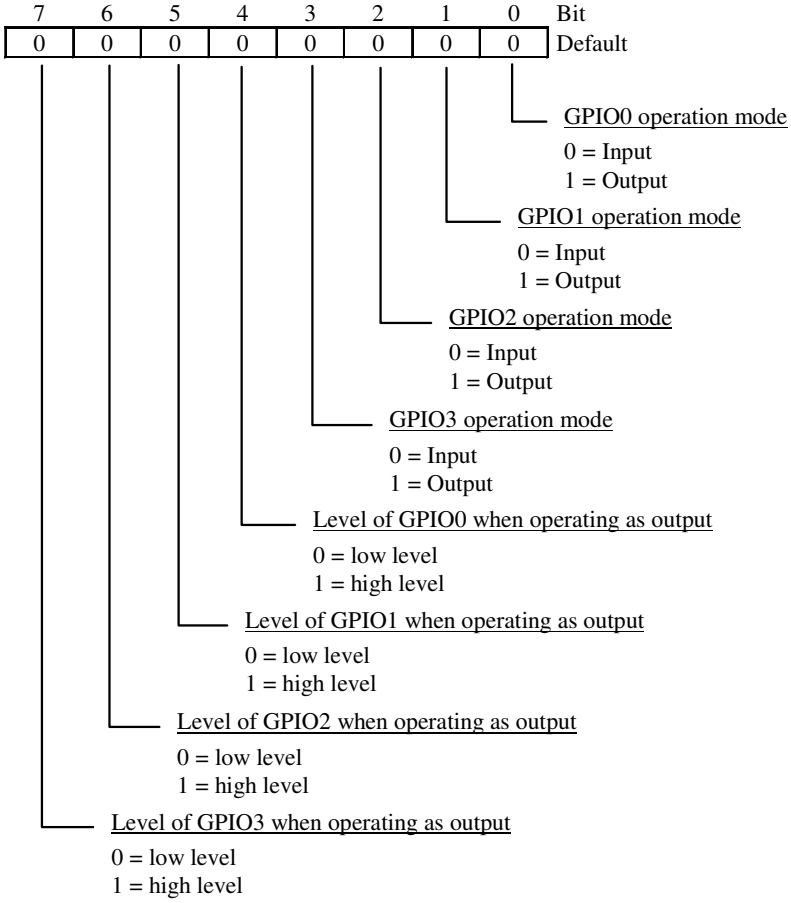


Figure 7.7: GPIO_REG Format

7.2.1.6 High-Resolution Registers (HIGH_REG_A / HIGH_REG_B)

The format of the High-Resolution Registers is shown in Figure 7.8. Optimal configurations of theses registers are shown in Table 7.2.

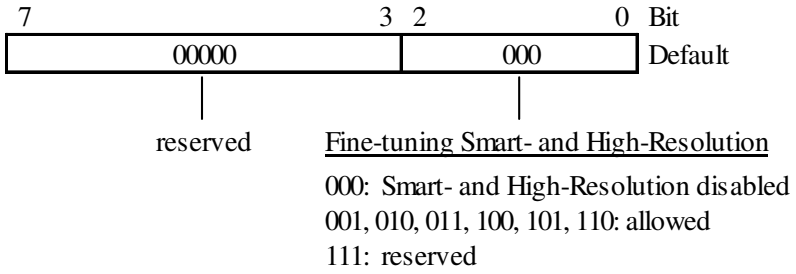


Figure 7.8: HIGH_REG_A and HIGH_REG_B Format

7.2.1.7 Smart-Resolution Registers (SMART_REG_A / SMART_REG_B)

Figure 7.9 shows the format of the Smart-Resolution Registers. Optimal configurations of theses registers are shown in Table 7.2.

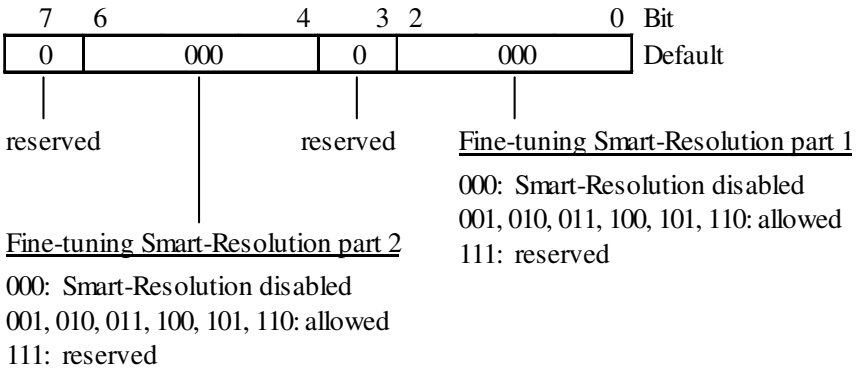


Figure 7.9: SMART_REG_A and SMART_REG_B Format

Resolution	HIGH_REG_A/B	SMART_REG_A/B
Half	0x00	0x00
Normal	0x00	0x00
High	0x04	0x00
Smart	0x04	0x65

Table 7.2: Optimal Configuration of High- and Smart-Resolution Registers

7.2.1.8 ALU Register (ALU_REG)

Figure 7.10 shows the ALU Register's format for each measurement mode, according to the ALU-calculation rule format (see Chapter 6.5.1.4) :

HIGH_NIBBLE – LOW_NIBBLE

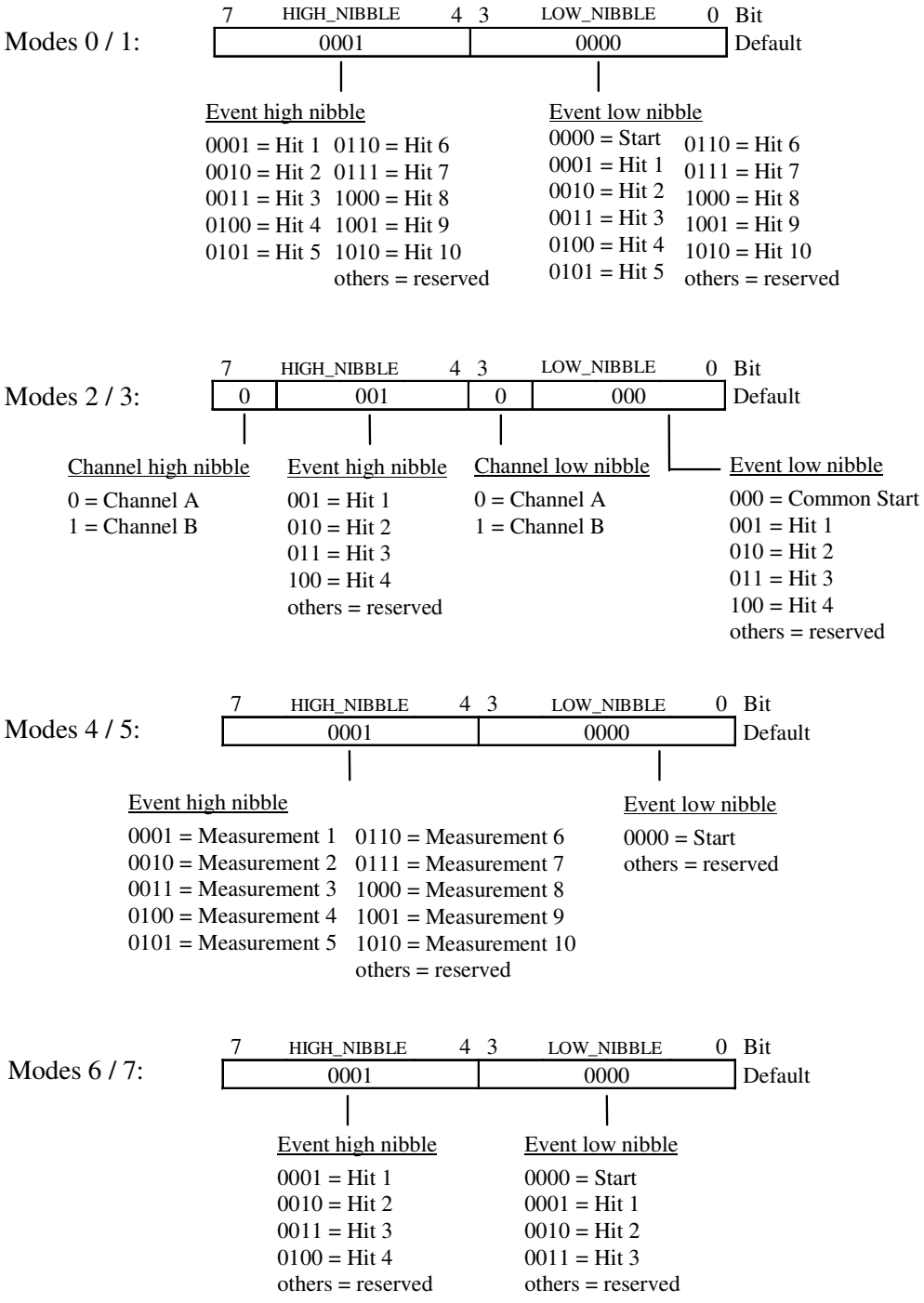


Figure 7.10: ALU_REG Formats

I the following some examples for configuration the ALU register are shown:

- Measurement mode 0: Calculation of the time difference between the 3rd hit and start on the channel selected via CTRL_REG_1: 0011 0000
- Measurement mode 1: Calculation of the time difference between the 6th hit and the 2nd hit on the channel selected via CTRL_REG_1: 0110 0010
- Measurement mode 2: Calculation of the time difference between the 1st hit on channel B and the 3rd hit on channel A: 1001 0011
- Measurement mode 2: Calculation of the time difference between the 4th hit on channel A and Common Start: 0100 0000
- Measurement mode 3: Calculation of the time difference between the 2nd hit on channel B and Common Start: 1010 1000
- Measurement mode 5: Calculation of the 10th burst mode measurement 'start-stop' on the channel selected via CTRL_REG_1: 1010 0000
- Measurement mode 7: Calculation of the time difference between the 2nd hit and the 1st hit on the channel selected via CTRL_REG_1: 0010 0001

7.2.1.9 Multiplication Registers (MULT_REG_1 / MULT_REG_2 / MULT_REG_3)

The formats of the Multiplication Registers are shown in Figure 7.11. MULT_REG_1 is the low byte, MULT_REG_2 is the middle byte and MULT_REG_3 is the high byte of the 24 bit unsigned integer number, the ALU uses for multiplication. Bit 7 of MULT_REG_3 is 1, Bit 6 is ½, Bit 5 is ¼, etc. .

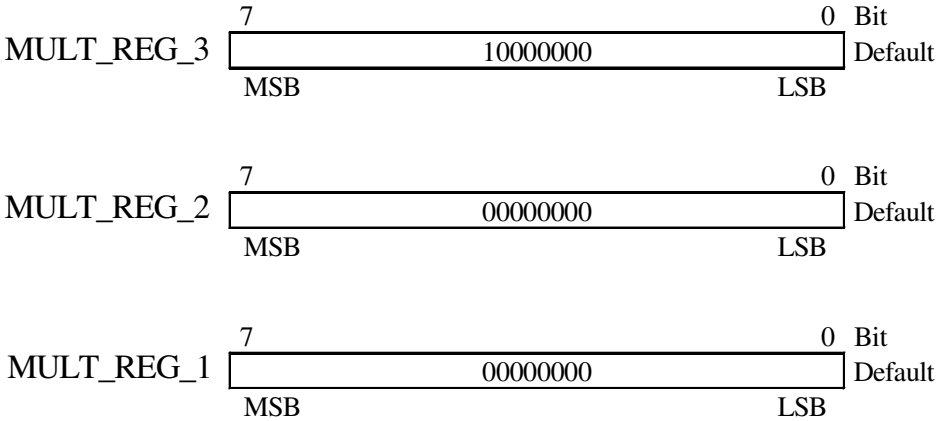


Figure 7.11: MULT_REG_1, MULT_REG2 and MULT_REG_3 Formats

7.2.2 Read-only Register Formats

7.2.2.1 Hit-Status Register (HIT_STATUS_REG)

Figure 7.12 shows the format of the Hit-Status Register.

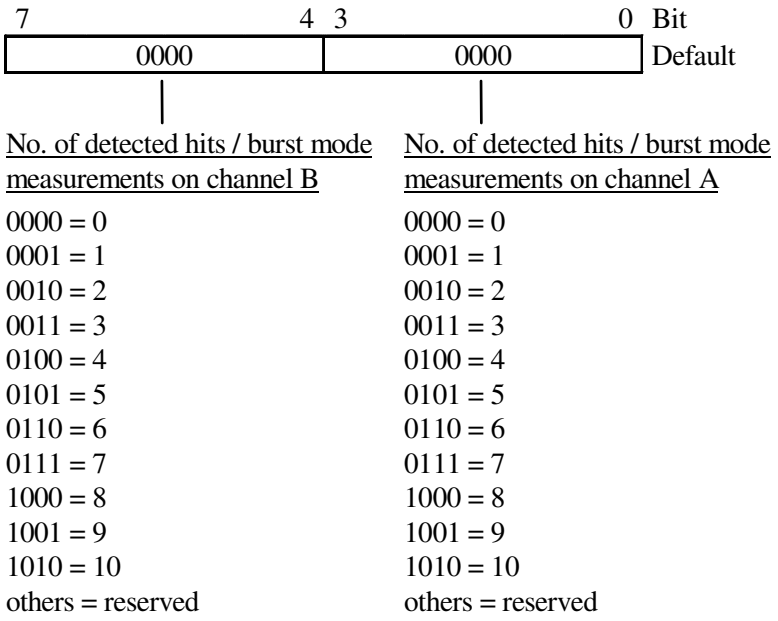


Figure 7.12: HIT_STATUS_REG Format

7.2.2.2 GPIO Input Register (GPIO_IN_REG)

The format of the GPIO Input Register is shown in Figure 7.13.

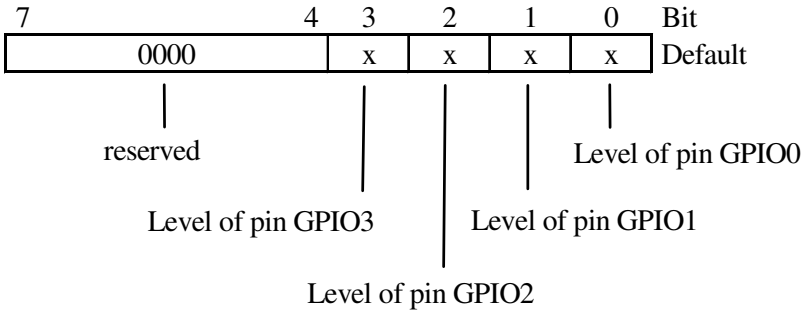


Figure 7.13: GPIO_IN_REG Format

7.2.2.3 Status Register (STATUS_REG)

Figure 7.14 shows the flags of the Status Register. TDC_READY is the only flag accessible via pin, too. A detailed description of the status flags is given in Chapter 6.8.3.1.

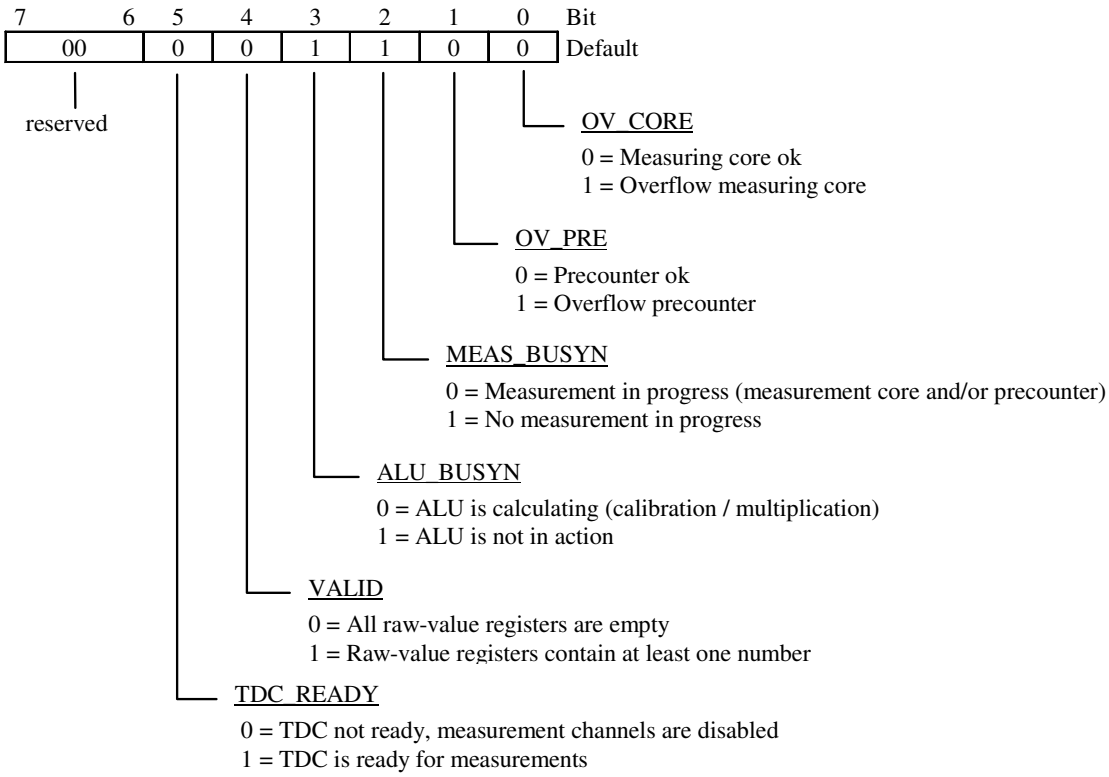


Figure 7.14: STATUS_REG Format

7.3 Raw-Value Registers

The TDC provides 12 read-only raw-value registers ROH_REG_0 to ROH_REG_11.

7.3.1 Raw-Value Register Format

As shown in Figure 7.15 the width of all raw-value registers is 16 bit. Therefore two read cycles are necessary to read out a complete raw-value via the 8-bit processor interface (see Table 7.1). The raw-value registers are not resettable, so there default state is undefined after power-on or soft reset.

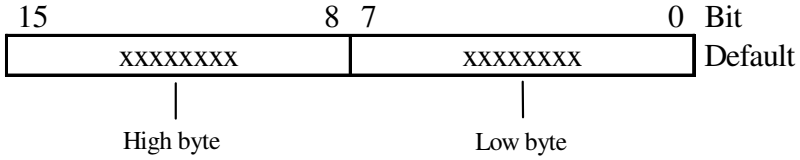


Figure 7.15: Raw-Value Register Format

Table 7.3 shows the raw-value register mapping, which depends on the measurement mode.

Register	Modes 0 / 1	Modes 2 / 3	Modes 4 / 5	Modes 6 / 7
ROH_REG_0	OFFSET	OFFSET A	OFFSET	OFFSET
ROH_REG_1	CAL	CAL A	CAL	CAL
ROH_REG_2	VAL1	VAL1 A	VAL1	VAL0
ROH_REG_3	VAL2	VAL2 A	VAL2	VAL1
ROH_REG_4	VAL3	VAL3 A	VAL3	PRE1
ROH_REG_5	VAL4	VAL4 A	VAL4	--
ROH_REG_6	VAL5	OFFSET B	VAL5	VAL2
ROH_REG_7	VAL6	CAL B	VAL6	PRE2
ROH_REG_8	VAL7	VAL1 B	VAL7	VAL3
ROH_REG_9	VAL8	VAL2 B	VAL8	PRE3
ROH_REG_10	VAL9	VAL3 B	VAL9	VAL4
ROH_REG_11	VAL10	VAL4 B	VAL10	PRE4

Table 7.3: Raw-Value Register Mapping

7.3.2 Raw-Value Data Format

All raw-values are 16 bit ***unsigned integer*** numbers. Thus, the maximum number for measurement- and calibration values is 0xffff = 65535. Because the MSB of precounter values is fixed to ‘0’ at all times, there maximum number is 0x7fff = 32767.

7.4 Result Registers

The TDC provides two read-only result registers ERG_REG_0 and ERG_REG_1, which are filled with ALU-calculation results alternately within a measurement cycle, beginning with ERG_REG_0.

7.4.1 Result Register Format

The width of the result registers is 32 bit. Therefore four read cycles are necessary to read out a complete measurement result via the 8-bit processor interface (see Table 7.1).

Figure 7.16 shows the format of the result registers.

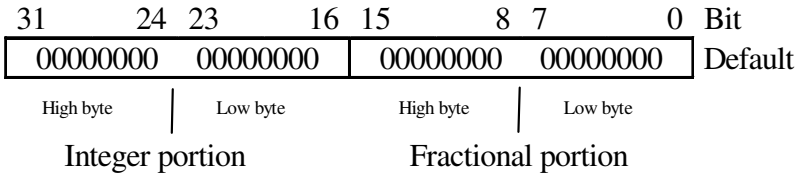


Figure 7.16: Result Register Format

7.4.2 Result Data Formats

The measurement results are 32 bit fixed point numbers with a 16 bit integer portion and a 16 bit fractional portion. In measurement range I the four most significant bits of the integer portion are either '0' (→ result is positive) or '1' (→ result is negative). In addition negative results are represented via the ones complement only of the integer portion. In measurement range II the measurement results are positive at all times.

Examples:

- Pos. result in measurement range I: 0x 0A1E 4F71 = 2590 + 20337 / 65536 = 2590.310318
- Neg. result in measurement range I: 0x FEC2 F432 = – 317 – 62514 / 65536 = – 317.953888
- Result in measurement range II: 0x C02B 2723 = 49195 + 10019 / 65536 = 49195.152878

8 Appendix

8.1 Electrical Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IL_CMOS}	Input Low Voltage		GND - 0.3		0.3 V_{DD}	V
V_{IH_CMOS}	Input High Voltage		0.7 V_{DD}		V_{DD} + 0.3	V
I_{IN}	Input Current	V_{IN} =V_{DD} or GND	-10		10	µA
V_{OH_CMOS}	Output High Voltage	I_{OH} = -4mA	V_{DD} - 0.8			V
V_{OL_CMOS}	Output Low Voltage	I_{OL} = 4mA			0.4	V
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{DD} or GND	-10		10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or GND	Design Depend			µA

***NOTE**: Junction temperature range –55°C to +125°C*

Table 8.1: DC Characteristics @ V_{DD} = 5V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IL_CMOS}	Input Low Voltage		GND - 0.3		0.3 V_{DD}	V
V_{IH_CMOS}	Input High Voltage		0.7 V_{DD}		V_{DD} + 0.3	V
I_{IN}	Input Current	V_{IN} =V_{DD} or GND	-10		10	µA
V_{OH_CMOS}	Output High Voltage	I_{OH} = -4mA	V_{DD} - 0.8			V
V_{OL_CMOS}	Output Low Voltage	I_{OL} = 4mA			0.4	V
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{DD} or GND	-10		10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or GND	Design Depend			µA

***NOTE**: Junction temperature range –55°C to +125°C*

Table 8.2: DC Characteristics @ V_{DD} = 3.3V

Symbol	Parameter	Rating	Unit	Note
V_{DD}	DC Supply Voltage	-0.3 to +7.0	V	
V_{IN}	Input Pin Voltage	-0.3 to V_{DD} + 0.3	V	
I_{IN}	Input Current on any Pin	-100 to +100	mA	25°C
T_{STRG}	Storage Temperature	-65 to +150	°C	
H	Humidity Noncondensing	5 to 85	%	Noncond.
	Electrostatic Discharge	1000	V	R=1.5kOhm, C=100pF
	Lead Temperature	260	°C	T=10s

***NOTE**: Stresses above these values may cause permanent damage to the device.*

Table 8.3: Absolute Maximum Ratings

8.2 Resolution

8.2.1 How to calculate the Resolution

The TDC's resolution **RES** is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the calibration values **CAL** and **OFFSET**:

$$\mathbf{RES = t_{CAL} / (CAL - OFFSET)} \quad \mathbf{(A0)}$$

8.2.2 Voltage Dependence

Table 8.4 shows the voltage dependence of the Normal-Resolution at normal conditions (typical process, ambient temperature approx. 28°C), arised from averaging the measured resolution of several TDCs.

Supply Voltage [V]	Normal-Resolution [ps]
2,7	335
3,0	293
3,3	264
3,6	242
4,0	220
4,5	201
5,0	186
5,5	177

Table 8.4: Resolution Voltage Dependence ($T_A \approx 28°C$, typ.)

At Half-Resolution the specified values of Table 8.4 have to be doubled, at High-Resolution the values have to be shortened by half and at Smart-Resolution they have to be shortened to the fourth part.

8.2.3 Temperature Dependence

The Normal-Resolution increases by factors of approx. 0,6 ps/K at V_{DD} = 3,3V and approx. 0,4 ps/K at 5V. At Half-Resolution the factors have to be doubled, at High-Resolution the factors have to be shortened by half and at Smart-Resolution they have to be shortened to the fourth part.

8.3 Differential Non-Linearity

The quality of a measurement not only depends on the TDC's resolution but also on its so called *differential non-linearity (DNL)*. The DNL is a criterion for the variation of the quantisation stage's width (LSB-width).

Figure 8.1 shows a typical histogram of the TDC's LSB-widths for 'Normal Resolution' at V_{DD} = 5V, where the average LSB-width is identical with the resolution RES. Furthermore the figure illustrates the definition of the DNL.

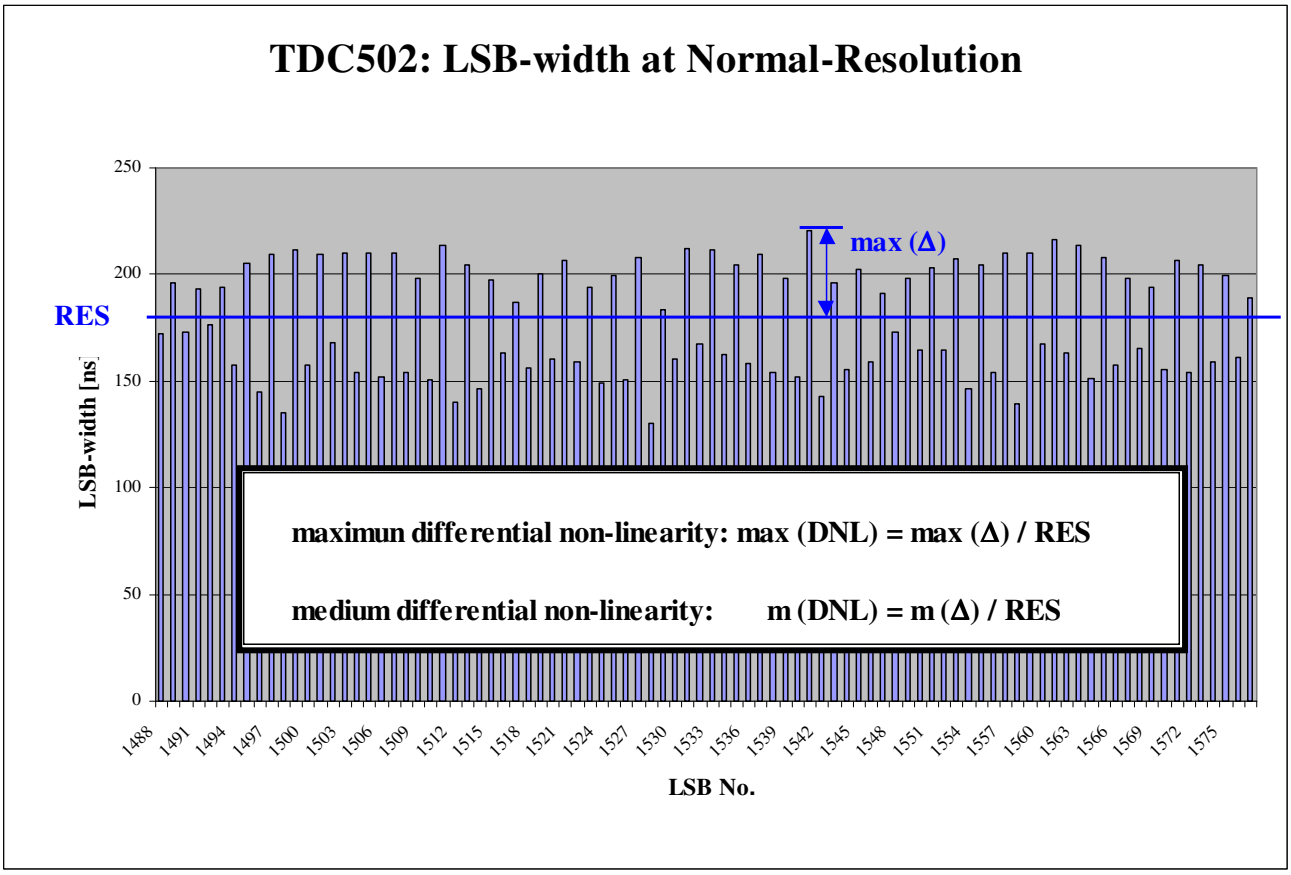


Figure 8.1: Resolution, LSB-Width and Differential Non-Linearity

Table 8.5 shows the differential non-linearity for all kinds of resolution, based upon measurements of several TDCs at V_{DD} = 5V and 3,3V and using the configurations of Table 7.2 for High- and Smart-Resolution Registers.

Resolution	m (DNL)		max (DNL)	
	3.3V	5V	3.3V	5V
Half	2 %	2 %	5 %	5 %
Normal	12 %	14 %	21 %	24 %
High	16 %	16 %	48 %	47 %
Smart	25 %	25 %	92 %	85 %

Table 8.5: Differential Non-Linearity

8.4 Measurement Range I: Minimum/maximum Measurement Period

8.4.1 Minimum Measurement Period

If the retrigger unit is disabled, the minimum measurement period is $\mathbf{t_{MBImin} = 0ps}$. If the retrigger unit is enabled, the minimum measurement period after the first start is $t_{MBImin} = 0{,}8 * t_s$. The time $\mathbf{t_s}$ is the minimum pulse width of start- and stop-signals (cp. Appendix 8.7). After any retriggering start the minimum measurement period is 0ps as usual.

8.4.2 Maximum Measurement Period

The maximum measurement period $\mathbf{t_{MBImax}}$ depends on the resolution. At Normal- and Half-Resolution the maximum measurement period is approximately:

$$\mathbf{t_{MBImax} = 2^{11} * t_U.} \qquad \mathbf{(A1)}$$

The time $\mathbf{t_U}$ in formula A1 is a specific internal parameter of the measurement range I. In Table 8.6 t_U is given for different conditions.

Conditions (voltage, temperature, process)	**t_U [ns]**
5.5V, -40°C, best	3
5.0V, +25°C, typ	5
4.5V, +85°C, worst	11
3.6V, -40°C, best	3,5
3.3V, +25°C, typ	7
3.0V, +85°C, worst	17

Table 8.6: Time t_U in Measurement Range I

At High-Resolution t_{MBImax} has to be shortened by half and at Smart-Resolution t_{MBImax} has to be shortened to the fourth part.

Using the typical value of Table 8.6 at 5V, the maximum measurement period for Normal- and Half-Resolution is approx. $\mathbf{t_{MBImax} = 10\mu s}$, for High-Resolution approx. 5µs and for Smart-Resolution approx. 2.5µs.

8.5 Measurement Range II: Minimum/maximum Measurement Period

The minimum and maximum measurement periods depend on the divided calibration clock period $\mathbf{t_{CAL}}$ (cp. Chapter 5.2, Generating Calibration Values).

8.5.1 Minimum Measurement Period

The minimum measurement period is approximately:

$$\mathbf{t_{MBIImin} = 1{,}5 * t_{CAL} + t_D} \qquad \mathbf{(A2)}$$

The time $\mathbf{t_D}$ in formula A2 is a specific internal parameter of the measurement range II. In Table 8.7 t_D is given for different conditions.

Conditions (voltage, temperature, process)	t_D [ns]
5.5V, -40°C, best	65
5.0V, +25°C, typ	105
4.5V, +85°C, worst	210
3.6V, -40°C, best	70
3.3V, +25°C, typ	135
3.0V, +85°C, worst	325

Table 8.7: Time t_D in Measurement Range II

Using the typical value of Table 8.7 at 5V, an external calibration clock of 20MHz and the division factor 1:1, the minimum measurement period is approx. $\mathbf{t_{MBIImin} = 180ns}$.

8.5.2 Maximum Measurement Period

The maximum measurement period is approximately:

$$\mathbf{t_{MBIImax} = 2^{15} * t_{CAL}.} \quad \mathbf{(A3)}$$

In measurement range II the measuring core has to measure 1.5 calibration clock periods at the most. Therefore the following condition has to be satisfied, too:

$$t_{CAL} \leq 2/3 * t_{MBImax} \qquad \textbf{(A4)}$$

The time t_{MBImax} in formula A4 is the minimum measurement period of measurement range I (cp. formula A1, Chapter 8.4.2).

Example:
As calculated in Chapter 8.4.2 for Normal- and High-Resolution at 5V, the maximum measurement period of measurement range I is approx. t_{MBImax} **= 10µs** typically. According to formula A4, the divided calibration clock has to be 150kHz at least. Using formula A3, this results in a maximum measurement period of approx. $t_{MBIImax}$ **= 210ms**.

8.6 Double Pulse Resolution

The double pulse resolution of a TDC with multi-hit capability is defined as the minimum possible time difference between two hits on the same stop-input, so that the second hit is definitely detected.

8.6.1 Measurement Range I

Table 8.8 shows the double pulse resolution t_{DPRI} for different conditions in measurement range I.

Conditions (voltage, temperature, process)	t_{DPRI} [ns]
5.5V, -40°C, best	17
5.0V, +25°C, typ	25
4.5V, +85°C, worst	55
3.6V, -40°C, best	18
3.3V, +25°C, typ	35
3.0V, +85°C, worst	80

Table 8.8: Double Pulse Resolution t_{DPRI} in Measurement Range I

8.6.2 Measurement Range II

In measurement range II the double pulse resolution t_{DPRII} depends on the divided calibration clock period t_{CAL} and is identical with the minimum measurement period $t_{MBIImin}$ (see Chapter 8.5.1).

8.7 Minimum Pulse Width of Start- and Stop-Signals

Table 8.9 shows the minimum pulse width $\mathbf{t_s}$ of signals on the start- and stop-inputs START, STOP_A and STOP_B as well as on the inputs EN_STOP_A and EN_STOP_B for different conditions. The time t_s is relevant for both, high- and low-level of the signals.

Conditions (voltage, temperature, process)	t_S [ns]
5.5V, -40°C, best	5
5.0V, +25°C, typ	7
4.5V, +85°C, worst	14
3.6V, -40°C, best	5
3.3V, +25°C, typ	9
3.0V, +85°C, worst	21

Table 8.9: Minimum Pulse Width t_s of Start- and Stop-Signals

8.8 Setup and Hold Time EN_STOP_A/B to STOP_A/B

Figure 8.2 shows the timing diagram of setup- and hold times $\mathbf{t_{ENS}}$ and $\mathbf{t_{ENH}}$ for EN_STOP_A (resp. EN_STOP_B) to STOP_A (resp. STOP_B). In Table 8.10 the associated timing characteristics are specified for different conditions.

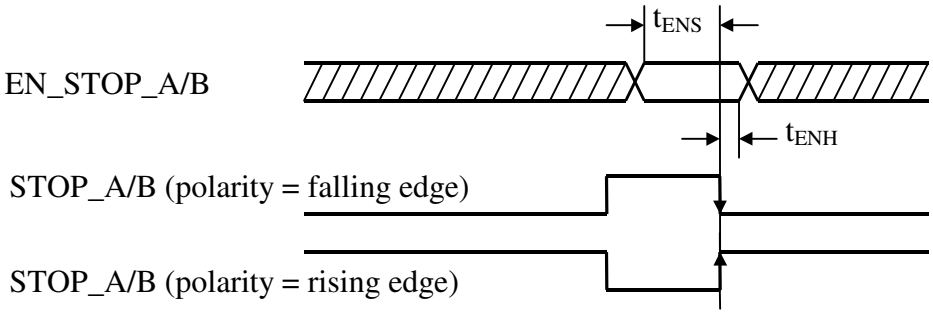


Figure 8.2: Setup and Hold Time EN_STOP_A/B to STOP_A/B

Conditions (voltage, temperature, process)	t_{ENS} [ns]	t_{ENH} [ns]
5.5V, -40°C, best	0,2	1,1
5.0V, +25°C, typ	0,3	1,5
4.5V, +85°C, worst	0,4	2,6
3.6V, -40°C, best	0,1	1,2
3.3V, +25°C, typ	0,0	2,1
3.0V, +85°C, worst	-0,3	4,1

Table 8.10: Setup and Hold Time EN_STOP_A/B to STOP_A/B Timing Characteristics

8.9 Timing when initiating and starting a Time Measurement

Figure 8.3 shows the timing of the TDC's pins WRN, START and TDC_READY when initiating and starting a time measurement. In Table 8.11 the associated characteristics are specified. They are relevant for falling edge triggered start-signals, too.

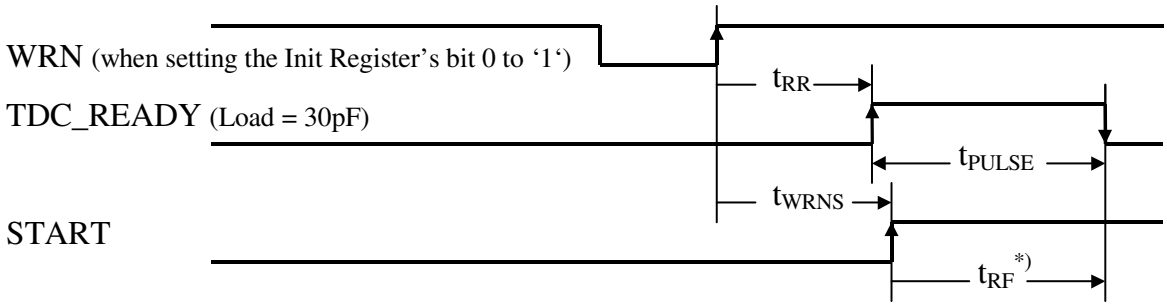


Figure 8.3: Timing when initiating and starting a Time Measurement

Conditions (voltage, temperature, process)	t_{RR} **) [ns]	t_{RF} *) **) [ns]	Setup time for start detection: t_{WRNS} [ns]	Minimum pulse width t_{PULSE} [ns]
5.5V, -40°C, best	5,4	7,3	4,9	6,7
5.0V, +25°C, typ	8,4	11,6	7,5	10,7
4.5V, +85°C, worst	14,5	20,5	13,3	19,1
3.6V, -40°C, best	6,5	8,4	5,6	7,4
3.3V, +25°C, typ	11,2	15,0	10,0	13,7
3.0V, +85°C, worst	21,4	31,1	21,0	30,4

**) t_{RF} is relevant only when the retrigger unit is not enabled.*

***) Maximum values*

Table 8.11: Timing Characteristics when initiating and starting a Time Measurement

8.10 Dead Times

Due to the measurement principle a TDC has got a dead time t_{TOT} after the execution of a time measurement. Depending on the configuration and the measurement mode this time period differs within a wide range. During the dead time the start and stop detection of the TDC's measuring core is disabled because of post-processing. Trying to re-initiate the TDC for another time measurement by re-setting the Init Register's bit 0 to '1' before the end of dead time is not legal and will be ignored.

Due to the fact that the TDC's measuring core is not available for time measurements during automatic or separate calibration measurements, this time periods are also considered as dead times. ALU-calculation times (see Table 8.17) are considered as dead times as well.

8.10.1 Dead Time at the End of a Time Measurement in Measurement Range I

The dead time at the end of a time measurement in measurement range I is defined as the time period between the last hit of a time measurement (resp. the stop of the last burst mode measurement) and the rising edge of the status flag MEAS_BUSYN (resp. the rising edge of the interrupt request flag INTFLAG, set by I_MEAS_END if enabled).

For the measurement modes 1, 3 and 5 (modes without automatic calibration measurement) the maximum dead time $\mathbf{t_{TOT\_MBI\_O}}$ at the end of a time measurement is specified in Table 8.12.

Conditions (voltage, temperature, process)	$t_{TOT\_MBI\_O}$ *) [ns]
5.5V, -40°C, best	60
5.0V, +25°C, typ	95
4.5V, +85°C, worst	190
3.6V, -40°C, best	65
3.3V, +25°C, typ	120
3.0V, +85°C, worst	295

**) Values for pin INTFLAG, Load = 30pF*

Table 8.12: Maximum Dead Time $t_{TOT\_MBI\_O}$ within the Measurement Modes 1, 3, 5

Because of the automatic calibration measurement this dead time is increased for the measurement modes 0, 2 and 4 to

$$\mathbf{t_{TOT\_MBI\_M} = t_{TOT\_MBI\_O} + 2{,}5 * t_{CAL} + t_{AC}} \qquad \mathbf{(A5)}$$

The time $\mathbf{t_{AC}}$ in formula A5 is a specific parameter of the automatic calibration measurement. In Table 8.13 t_{AC} is given for different conditions.

Conditions (voltage, temperature, process)	t_{AC} [ns]
5.5V, -40°C, best	60
5.0V, +25°C, typ	100
4.5V, +85°C, worst	200
3.6V, -40°C, best	65
3.3V, +25°C, typ	110
3.0V, +85°C, worst	305

Table 8.13: Time t_{AC} for Measurement Modes 0, 2, 4 and 6

8.10.2 Dead Time at the End of a Time Measurement in Measurement Range II

The dead time at the end of a time measurement in measurement range II is defined as the time period between the last hit of a time measurement and the rising edge of the status flag MEAS_BUSYN (resp. the rising edge of the interrupt request flag INTFLAG, set by I_MEAS_END if enabled).

For the measurement mode 7 (= mode without automatic calibration measurement) the maximum dead time $\mathbf{t_{TOT\_MBII\_O}}$ at the end of a time measurement depends on the divided calibration clock period $\mathbf{t_{CAL}}$ and is identical with the minimum measurement period $\mathbf{t_{MBIImin}}$ (see Chapter 8.5.1).

Because of the automatic calibration measurement this dead time is increased for the measurement mode 6 to

$$\mathbf{t_{TOT\_MBII\_M} = t_{TOT\_MBII\_O} + 2{,}5 * t_{CAL} + t_{AC}} \qquad \mathbf{(A6)}$$

The time $\mathbf{t_{AC}}$ in formula A6 is – similar to measurement range I - the specific parameter of the automatic calibration measurement. In Table 8.13 t_{AC} is given for different conditions.

8.10.3 Dead Time between Burst Mode Measurements

The dead time between burst mode measurements is defined as the time period between the stop of a burst mode measurement 'start-stop' and the following rising edge of the status flag TDC_READY on pin TDC_READY, enabling the next burst mode measurement 'start-stop'.

Table 8.14 shows the maximum dead time $\mathbf{t_{TOT\_B}}$ between burst mode measurements for different conditions.

Conditions (voltage, temperature, process)	$\mathbf{t_{TOT\_B}}$ *) **[ns]**
5.5V, -40°C, best	60
5.0V, +25°C, typ	100
4.5V, +85°C, worst	200
3.6V, -40°C, best	65
3.3V, +25°C, typ	125
3.0V, +85°C, worst	305

**) Pin TDC_READY with Load = 30pF*

Table 8.14: Maximum Dead Time t_{TOT_B} between Burst Mode Measurements

8.10.4 Dead Time of a Separate Calibration Measurement

The dead time of a separate calibration measurement is defined as the time period between the rising edge of WRN when activating the action-bit 'separate calibration measurement' within the Init Register and the rising edge of the status flag MEAS_BUSYN (resp. the rising edge of the interrupt request flag INTFLAG, set by I_MEAS_END if enabled).

The dead time $\mathbf{t_{TOT\_SC}}$ of a separate calibration measurement depends on the divided calibration clock period $\mathbf{t_{CAL}}$ (cp. Chapter 5.2) and is calculated as follows:

$$\mathbf{t_{TOT\_SC} = 2{,}5 * t_{CAL} + t_{SC}} \qquad \mathbf{(A7)}$$

The time $\mathbf{t_{SC}}$ in formula A7 is a specific parameter of the separate calibration measurement. Table 8.15 t_{SC} is given for different conditions.

Conditions (voltage, temperature, process)	t_{SC} *) [ns]
5.5V, -40°C, best	65
5.0V, +25°C, typ	100
4.5V, +85°C, worst	200
3.6V, -40°C, best	70
3.3V, +25°C, typ	130
3.0V, +85°C, worst	315

**) Values for pin INTFLAG, Load = 30pF*

Table 8.15: Time t_{SC} for Dead Time of a Separate Calibration Measurement

8.10.5 Dead Time Increase due to Auto Noise and Retrigger Unit

If the auto noise unit is enabled all dead times in Chapters 8.10.4 and 8.10.3 are increased by $\mathbf{t_{AN}}$. If the retrigger unit is enabled the dead times in theses chapters are increased by $\mathbf{t_{RT}}$. In Chapter 8.10.1 the dead times for measurement modes 1, 3 and 5 are increased by $\mathbf{t_{AN}}$ and/or $\mathbf{t_{RT}}$, for measurement modes 0, 2 and 4 by $\mathbf{2*t_{AN}}$ and/or $\mathbf{2*t_{RT}}$. The maximum values for t_{AN} and t_{RT} are specified in Table 8.16.

Conditions (voltage, temperature, process)	t_{AN} [ns]	t_{RT} [ns]
5.5V, -40°C, best	7	7
5.0V, +25°C, typ	11	10
4.5V, +85°C, worst	23	18
3.6V, -40°C, best	8	7
3.3V, +25°C, typ	15	13
3.0V, +85°C, worst	36	29

Table 8.16: Auto Noise Unit Offset t_{AN} and Retrigger Unit Offset t_{RT}

8.11 ALU-Calculation Times

Depending on the measurement mode in Table 8.17 the maximum times $\mathbf{t_{ALU\_CAL}}$ and $\mathbf{t_{ALU\_MUL}}$ the ALU needs for a calibration and the following optional multiplication are specified.

Conditions (voltage, temperature, process)	t_{ALU_CAL} [ns]		t_{ALU_MUL} [ns]
	Measurement Modes 0 / 1 / 4 / 5	Measurement Modes 2 / 3 / 6 / 7	
5.5V, -40°C, best	625	725	1245
5.0V, +25°C, typ	965	1130	1930
4.5V, +85°C, worst	1815	2115	3625
3.6V, -40°C, best	665	780	1330
3.3V, +25°C, typ	1235	1440	2465
3.0V, +85°C, worst	2895	3380	5790

Table 8.17: ALU-Calculation Times for Calibration t_{ALU_CAL} and Multiplication t_{ALU_MUL}

8.12 Timing when the first Raw-Value of a Measurement is generated

Using the status flag VALID or the IRQ flag set signal I_VALID for pin INTFLAG, allows to detect the moment when the first raw-value of a time- or calibration measurement is generated and written to the raw-value registers for readout. Depending on the TDC's operation mode this moment can be a long time before the end of the measurement: When executing a time measurement in measurement range I the first hit (resp. the stop of the first burst mode measurement) generates the first raw-value (VAL1 resp. VAL1 A or VAL1 B). When executing a time measurement in measurement range II the first raw-value to be generated is VAL0. Executing a separate calibration measurement with offset generation generates the raw-value OFFSET (resp. both raw-values OFFSET A and OFFSET B) at first. When executing a seperate calibration measurement without offset generation the first raw-value to be ready for readout will be the calibration value CAL (resp. both calibration values CAL A and CAL B).

In Table 8.18 the following maximum time periods for raw-value detection are given for different conditions:

- $\mathbf{t_{V\_MBI}}$: Time period between the first hit of a time measurement (resp. the stop of the first burst mode measurement) in measurement range I and the rising edge of the interrupt request flag INTFLAG.
- $\mathbf{t_{V\_MBII}}$: Time period between the start of a time measurement in measurement range II and the rising edge of the interrupt request flag INTFLAG.
- $\mathbf{t_{V\_SC\_M}}$: Time period between the rising edge of WRN when activating the action-bit 'separate calibration measurement' within the Init Register and the rising edge of the interrupt request flag INTFLAG. The calibration measurement's offset generation is enabled.
- $\mathbf{t_{V\_SC\_O}}$: Time period between the rising edge of WRN when activating the action-bit 'separate calibration measurement' within the Init Register and the rising edge of the interrupt request flag INTFLAG. The calibration measurement's offset generation is disabled.

Conditions (voltage, temperature, process)	t_{V_MBI}	t_{V_MBII}	$t_{V\_SC\_M}$	$t_{V\_SC\_O}$
5.5V, -40°C, best	50ns	1,5 * t_{CAL} + 60ns	1,5 * t_{CAL} + 55ns	2,5 * t_{CAL} + 55ns
5.0V, +25°C, typ	85ns	1,5 * t_{CAL} + 95ns	1,5 * t_{CAL} + 90ns	2,5 * t_{CAL} + 90ns
4.5V, +85°C, worst	165ns	1,5 * t_{CAL}+ 185ns	1,5 * t_{CAL} + 175ns	2,5 * t_{CAL} + 175ns
3.6V, -40°C, best	55ns	1,5 * t_{CAL} + 65ns	1,5 * t_{CAL} + 60ns	2,5 * t_{CAL} + 60ns
3.3V, +25°C, typ	105ns	1,5 * t_{CAL} + 120ns	1,5 * t_{CAL} + 110ns	2,5 * t_{CAL} + 110ns
3.0V, +85°C, worst	255ns	1,5 * t_{CAL} + 285ns	1,5 * t_{CAL} + 270ns	2,5 * t_{CAL} + 270ns

Notes:

- *Pin INTFLAG with Load = 30pF.*
- *t_{CAL} = divided calibration clock period.*
- *If the auto noise unit is enabled the time t_{AN}, shown in Table 8.16, has to be added to t_{V_MBI} , $t_{V\_SC\_M}$ and $t_{V\_SC\_O}$.*
- *If the retrigger unit is enabled the time t_{RT}, shown in Table 8.16, has to be added to t_{V_MBI} , $t_{V\_SC\_M}$ and $t_{V\_SC\_O}$.*

Table 8.18: Timing when the first raw-value of a measurement is generated

When using the status flag VALID or the IRQ flag set signal I_VALID for pin INTFLAG please be sure not to re-initiate the TDC for another time measurement or to start a separate calibation measurement before the end of the measurement's dead time (see Appendix 8.10).

8.13 Current Consumption

The current consumption of the TDC502 is one of the most important criteria, if it is to be used in battery-operated devices. The current consumption basically depends on the runtime of the measuring core, shown in Table 8.20 and the ALU-calculations times, shown in Table 8.17. If there are no measurements, calculations or I/O activities, then the TDC only needs its quiescent supply current. Table 8.19 shows the typical current consumption for each relevant component of the TDC at V_{DD} = 5V, T_A = 25°C.

Component	Duration of Current Consumption	Current Consumption
Quiescent current *)	all the time	150nA
Measuring core	during measuring core runtime	32mA
ALU	during calculations	8mA
Precounter	between start and last hit resp. stop of a measurement within measurement range II	100µA/MHz
Calibration clock input	during calibration clock runtime	45µA/MHz
Read- and write cycles	during read- and write cycles	1.7µA/1000 cycles

**) - Measurement conditions: Inputs WRN, RDN and CSN = V_{DD}, all other inputs and bidis = GND, all outputs = open.*
- Please refere also to Table 8.1 and Table 8.2.
- The quiescent current increases exponentially to the temperature.

Table 8.19: Typical Current Consumption of TDC502 components at V_{DD} = 5V, T_A = 25°C

When operating with supply voltages other than 5V the following voltage dependence have to be taken into account:

- The quiescent current drops/increases linearly to the supply voltage.
- The current consumption of all other components drops/increases squarely to the supply voltage.

Kind of measurement	Measuring core runtime	Comment
Time measurement in range I	Time between start and last hit resp. stop + 0.8 * $t_{TOT\_MBI\_O}$	$t_{TOT\_MBI\_O}$: see Table 8.12
Burst mode measurement	Time between start and stop + 0.8 * t_{TOT_B}	t_{TOT_B} : see Table 8.14
Time measurement in range II	About 2 calibration clock periods t_{CAL} + 1.6 * t_D	t_D : see Table 8.7
Automatic calibration measurement	1 calibration clock period t_{CAL} + 0.8 * t_{AC}	t_{AC} : see Table 8.13
Separate calibration measurement	1 calibration clock period t_{CAL} + 0.8 * t_{SC}	t_{SC} : see Table 8.15

***Note**: If the auto noise unit is enabled the time t_{AN}, shown in Table 8.16, has to be added to the runtime of the measuring core.*

Table 8.20: Runtime of the Measuring Core

Example:

2500 start-stop measurements/sec in measurement mode 6, each with a measurement period of 0.1ms on the average, followed by ALU-calculations for calibration and multiplication operating at V_{DD} = 3.3V. The external calibration clock CALCLK is 4 MHz, which is divided by the calibration clock divider down to a 2MHz internal clock CLK. After each measurement the result registers are read out (4 read cycles) and the next measurement is initiated by activating the action-bit 'time measurement' (1 write cycle).

=> Calculation of the current consumption:

Quiescent current:	150nA*(3.3V/5V) =	99nA
Meas. core:	32mA*(3.3V/5V)² *[(2*500ns+1.6*135ns)+(500ns+0.8*110ns)]*2500/s =	62.866µA
ALU:	8mA*(3.3V/5V)²*(1440ns+2465ns)*2500/s =	34.02µA
Precounter:	100µA/MHz*(3.3V/5V)²*2MHz*0.1ms*2500/s =	21.78µA
Calibration clock input:	45µA/MHz*(3.3V/5V)² *4MHz =	78.408µA
Read- and write cycles:	1.7µA/1000*(3.3V/5V)² *2500*(4+1) =	9.257µA
Over-all current consumption:		206.43µA

8.14 Power-On Characteristics

The minimum pulse width of a low active power-on reset pulse connected to pin RSTN is 100µs. Figure 8.4 shows a possible reset circuit (RC-circuit).

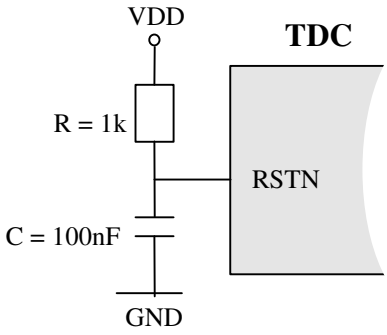


Figure 8.4: Reset Circuit

After power-on reset the TDC is in the default state: The TDC is not ready for measurements, because the measurement channels are disabled. After activating the action-bit 'time measurement' within the Init Register (see Chapter 7, Programming of the TDC502) the TDC is ready for a time measurement in measurement mode 0 and waits for a rising edge on the start-input START and a rising edge on the stop-input STOP_A (channel A).

8.15 Measurement Results

8.15.1 Singleshot Measurements and RMS Resolution

Table 8.21 and Table 8.22 show the time-based **singleshot standard deviation** "**σ [ps]**" also referred to as **rms resolution** and the resolution-based singleshot standard deviation "**σ [LSB]**". All singleshot standard deviations are averaged values derived from measurements on both channels of a TDC502 at the conditions given below. In a normal distribution the so called one-sigma area ±σ contains about 68% of the measurement results. About 95,5% will fall within the two-sigma area ±2σ.

- Measurement period: 100 - 300ns (Mode 0); 9 - 10µs (Mode 6).
- Increment: 1ns.
- Sampling rate: One measurement per measuring point.
- Calibration clock = 4 MHz / 2 = 2 MHz (Division factor of the calibration clock divider = 2).
- Automatic calibration measurement without offset generation.
- Offset generation via separate calibration measurement before overall measurement.
- Supply voltage: 3.3V and 5V.
- Temperature: approx. 28°C.
- Reference Measurements: Universal Time Interval Counter SR620 (Stanford Research Systems).

Measurement Mode	Kind of Resolution	Resolution [ps]	σ [ps]	σ [LSB]
0	half	360	125	0.4
0	normal	180	65	0.4
0	high	90	40	0.5
0	smart	45	35	0.8
6	half	360	170	0.5
6	normal	180	85	0.5
6	high	90	55	0.6
6	smart	45	45	1.0

Table 8.21: RMS Resolution σ at 5V, Measurement Modes 0 and 6

Measurement Mode	Kind of Resolution	Resolution [ps]	σ [ps]	σ [LSB]
0	half	520	155	0.3
0	normal	260	80	0.3
0	high	130	50	0.4
0	smart	65	40	0.7
6	half	520	215	0.4
6	normal	260	115	0.4
6	high	130	80	0.6
6	smart	65	55	0.8

Table 8.22: RMS Resolution σ at 3.3V, Measurement Modes 0 and 6

Figure 8.5 shows exemplarily the measurement errors of singleshot measurements on channel A with measurement mode 6 and Smart-Resolution selected at 5V. The offset of the diagram is approx. 700ps. This systematic error results from a different length of cables for start and stop and is irrelevant here.

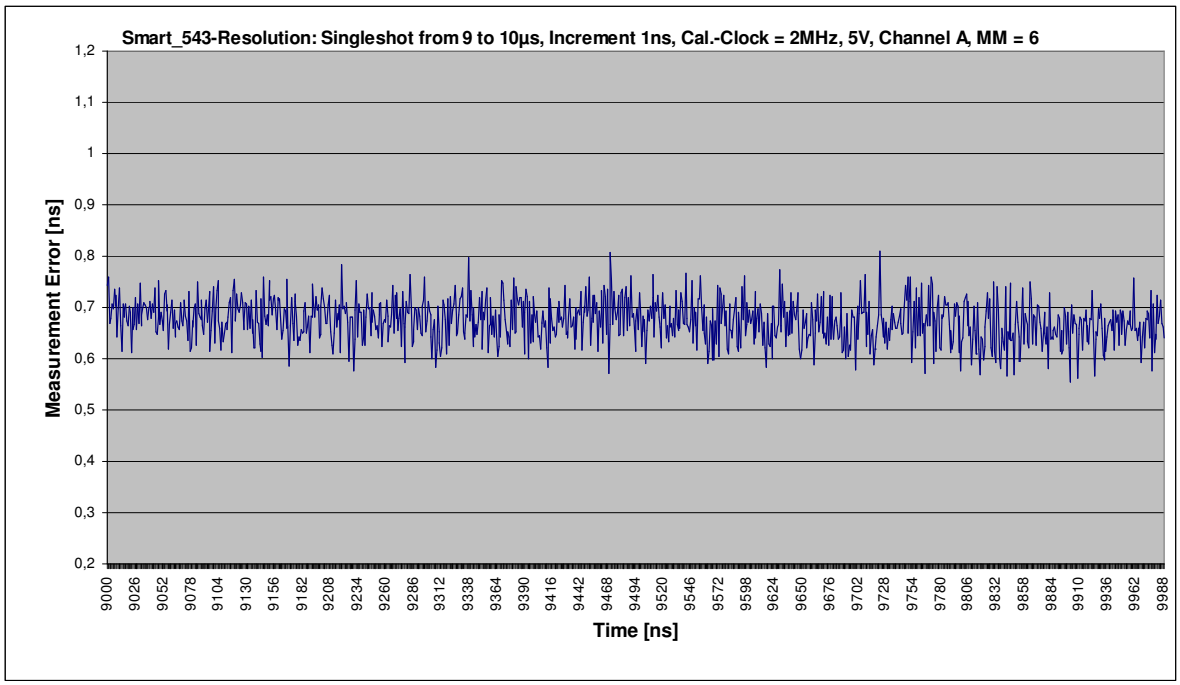


Figure 8.5: Measurement Errors of Singleshot Measurements at 5V, Measurement Mode 6

8.15.2 Simultaneous Singleshot Measurements on both Channels

When measurement mode 2 or 3 is selected and the stop-inputs STOP_A and STOP_B are combined the same time difference can be measured simultaneously on both channels. Averaging the two measurement results will improve the measurement's accuracy by up to approx. 30% and double the TDC's resolution of up to 23ps at 5V resp. 33ps at 3.3V (typ).

Table 8.23 shows the **doubled resolution [ps]** of simultaneous singleshot measurements of a TDC at 5V in measurement mode 2 as well as the **singleshot standard deviation** resp. **rms resolution** "**σ [ps]**". The measurement period is from 100 to 300ns. All other conditions are the same as given in the previous Chapter 8.15.1. The one-sigma area ±σ contains about 68% of the simultaneous singleshot measurement results. About 95,5% will fall within the two-sigma area ±2σ.

Measurement Mode	Kind of Resolution	Doubled Resolution [ps]		σ [ps]	
		5V	3.3V	5V	3.3V
2	half	180	260	85	135
2	normal	90	130	45	65
2	high	45	65	35	45
2	smart	23	33	25	35

Table 8.23: RMS Resolution σ[ps] of simultaneous Singleshot Measurements, MM 2

Figure 8.6 shows exemplarily the measurement errors of simultaneous singleshot measurements on both channels with measurement mode 2 and Smart-Resolution selected at 5V. The measurement period is from 100 to 300ns. The systematic offset error of approx. 575ps is irrelevant here, too.

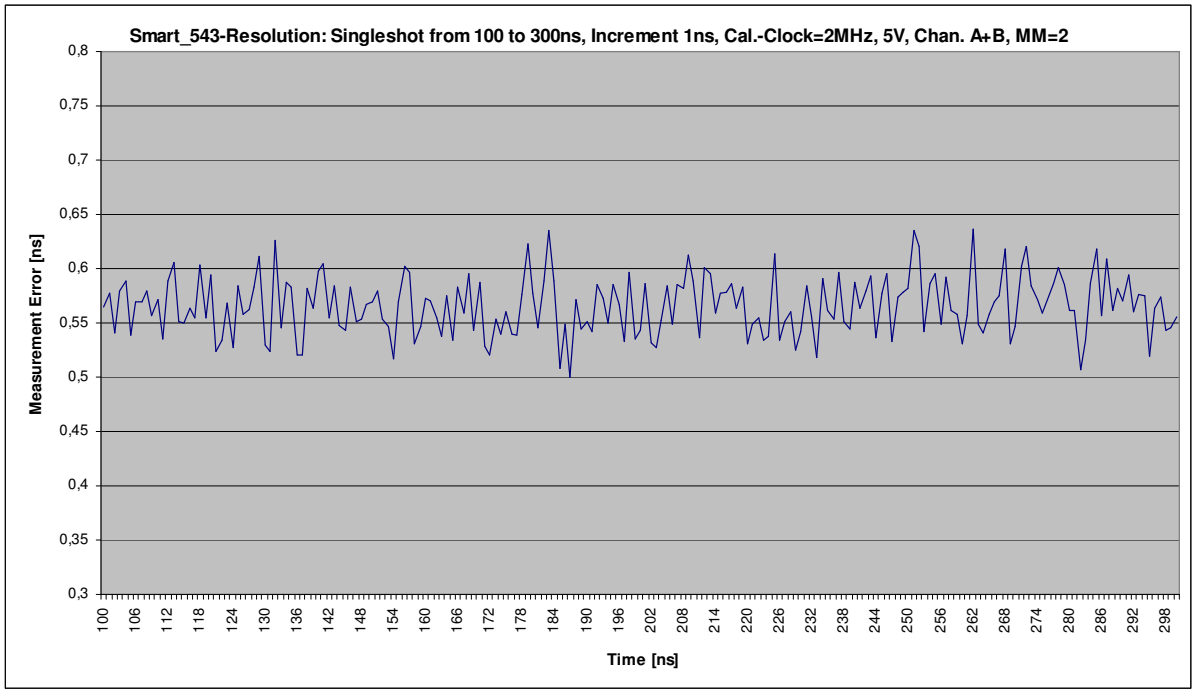


Figure 8.6: Measurement Errors of simultaneous Singleshot Measurements at 5V, Mode 2

8.15.3 Auto Noise Unit: Effect on Measurement Error and Standard Deviation

If there is the possibility to measure the same time difference several times a higher precision can be achieved by calculating the average measurement result. With an increasing number of measurements and taking into account all systematic errors such as the TDC's quantisation error (see Chapter 6.2.4) or offsets, caused by different length of cables for start and stop, the average measurement result will converge the real time difference which has to be measured. So the measurement error of the average measurement result is getting smaller and smaller.

In doing so the standard deviation is a good measure of the variation of the individual measurement results around the average. Comparing Figure 8.7 with Figure 8.8 shows which effects the auto noise unit has on the measurement error and the standard deviation: Every time difference was measured 64 times within measurement mode 0 at the following conditions, once with and another time without using the auto noise unit:

- Measurement period: 100 - 400ns.
- Increment: 1ns.
- Sampling rate: 64 measurements per measuring point.
- Calibration clock = 4 MHz / 2 = 2 MHz (Division factor of the calibration clock divider = 2).
- Automatic calibration measurement without offset generation.
- Offset generation via separate calibration measurement before every single measurement.
- Supply voltage: 5V.
- Resolution: Half-Resolution.
- Reference measurements: Universal Time Interval Counter SR620 (Stanford Research System).

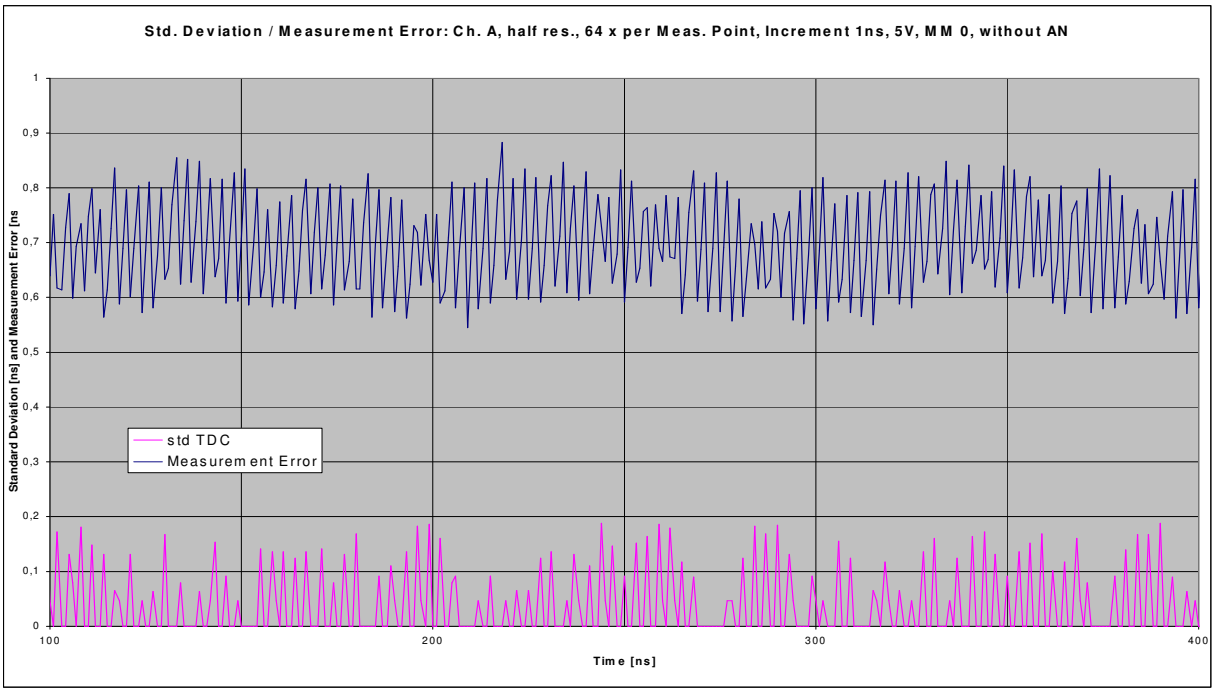


Figure 8.7: Standard Deviation and Measurement Error without Auto Noise Unit

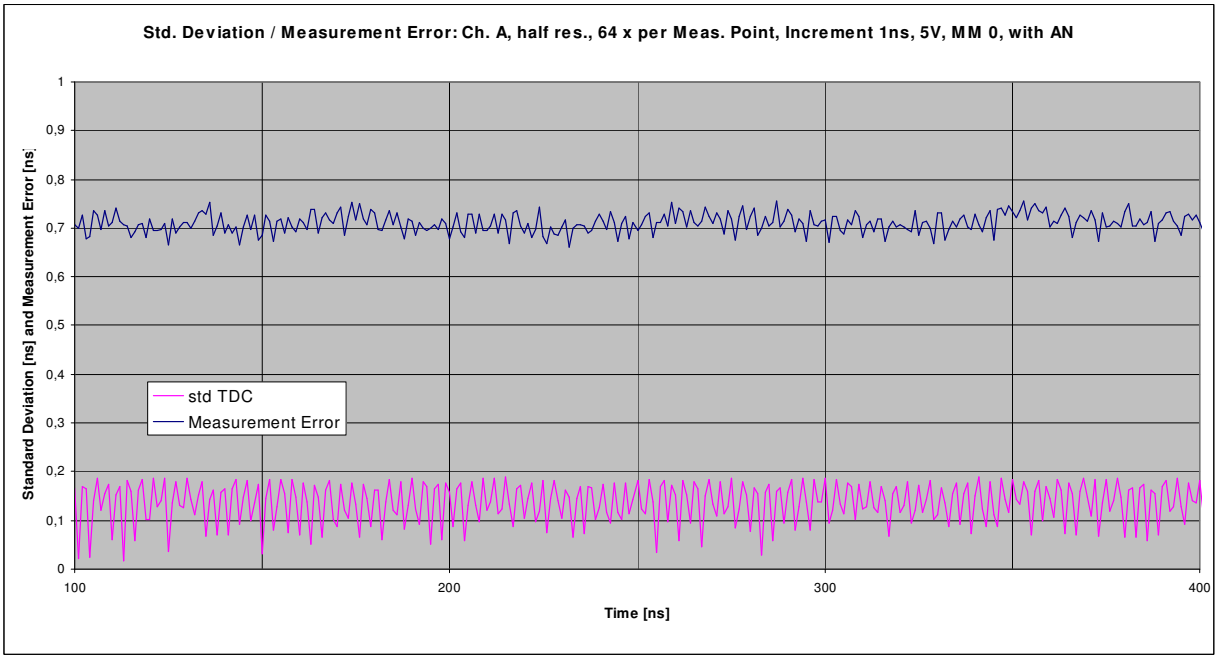


Figure 8.8: Standard Deviation and Measurement Error with Auto Noise Unit

The comparison of the figures shows that on average the standard deviation is smaller when operating without auto noise unit: When measuring the same time difference several times then the same quantisation stage (LSB) of the TDC is hit very often or permanently. So the standard deviation becomes small whereas the measurement error (approx. 1 LSB) remains huge. Since this error is mainly based upon the TDC's quantisation it can be minimized when operating with auto noise unit which cuts off the peaks of the characteristics. So the measurement errors become smaller. Furthermore the standard deviation of the average measurement results is improved by about $1/\sqrt{64}$ from σ=125ps (singleshot measurement, see Table 8.21) down to σ_{64}=17ps. The systematic offset error of approx. 700ps is irrelevant here, too.