Modicon TSX Momentum

170 AEC 920 00

I/O Base with 2 High–Speed Counters

User Manual

870 USE 008 00

7/99

330 01466.00

GROUPE SCHNEIDER

■ Merlin Gerin ■ Modicon ■ Square D ■ Telemecanique

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Contents

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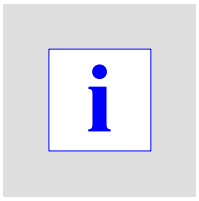
Info



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The relevant regulations must be observed for control applicatons involving safety requirements.
For reasons of safety and to ensure compliance with documented system data, repairs to components should be performed only by the manufacturer.

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Terminology

Note
This symbol emphasizes very important facts.

Caution
This symbol refers to frequently appearing error sources.

Warning
This symbol points to sources of danger that may cause financial and health damages or may have other aggravating consequences.

Expert
This symbol is used when a more detailed information is given, which is intended exclusively for experts (special training required). Skipping this information does not interfere with understanding the publication and does not restrict standard application of the product.

Tip
This symbol is used for Tips & Tricks.

Example This symbol emphasizes the begining of an example.

▶ **Proceed as follows:**
This marks the beginning of a series of applications that must execute in order to achieve a certain product function.

Related Documents:
This symbol indicates manuals or other sources which elaborate on the addressed topic in more detail.

Related Documentation

Title	Order–No.
I/O Module Bases for TSX Momentum, User Manual	870 USE 002 00
Interbus Communication Adapter	870 USE 003 00
Profibus DP Communication Adapter	870 USE 004 00
FIPIO Communication Adapter	870 USE 005 00
Modbus Plus Communication Adapter	870 USE 103 00
ControlNet Communication Adapter	870 USE 007 00
Ethernet Communication Adapter	870 USE 112 00

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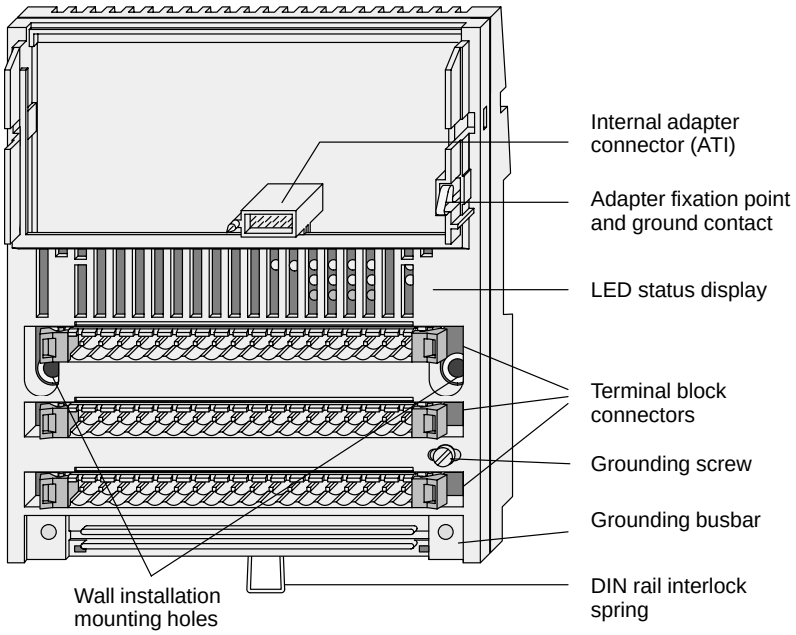
Introduction

1

The 170 AEC 920 00 I/O base is a high speed counter module for the TSX Momentum family. Together with a communications adapter or processor adapter it comprises a fully functional module. The 170 AEC 920 00 principles of operation are described in this document.

- Introduction (Chapter 1)
- Operating mode descriptions (Chapter 2)
- 170 AEC 920 00 I/O base hardware description (Chapter 3)
- Counter configuration (Chapter 4)
- Status information and counted values (Chapter 5)
- DFB parameterization (Appendix A)



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1.1 TSX Momentum Adapters

1.1.1 TSX Momentum Communications Adapters

The communications adapters serve the I/O bases as interfaces to numerous industry standard open communication networks. The following communications adapters are available:

Table 1 Available communications adapters

Type	Communications adapter for
170 INT 110 00	INTERBUS
170 NEF 110 21	Modbus Plus, 984 data format over single network cable
170 NEF 160 21	Modbus Plus, 984 data format over dual network cable
170 PNT 110 20	Modbus Plus, IEC data format over single network cable
170 PNT 160 20	Modbus Plus, IEC data format over dual network cable
170 DNT 110 00	ProfiBus DP
170 FNT 110 00	FIPIO for TSX 7 and April
170 FNT 110 01	FIPIO for TSX Premium
170 LNT 710 00	DeviceNet
170 LNT 810 00	ControlNet
170 ENT 110 00	Ethernet

Additional Documentation: Detailed information for the individual communications adapters can be found in the specific manuals (refer to the ”Additional Documentation” section in the foreword).

The procedure to join the communications adapter and I/O base is described in the 870 USE 002 00 User Manual.

1.1.2 TSX Momentum Processor Adapters and Interface Adapters

The processor adapter is comparable to a PLC's processor, in which a user program executes controlling the I/O points of a process. It can be plugged to the I/O base, controlling its I/O points as local I/O.

The following processor adapters are available:

Table 2 TSX Momentum processor adapter

Type	Internal memory	Flash RAM	Clock speed	Interfaces
171 CCS 700 00	64 KB	256 KB	20 MHz	1 x RS–232C
171 CCS 700 10	64 KB	256 KB	32 MHz	1 x RS–232C
171 CCS 760 00	256 KB	256 KB	20 MHz	1 x RS–232C
				1 x I/O bus
171 CCS 780 00	64 KB	256 KB	20 MHz	1 x RS–232C
				1 x RS–485
171 CCC 780 10	512 KB	–	32 MHz	1 x RS–232C 1 x RS–485
171 CCC 760 10	512 KB	–	32 MHz	–

Processor adapter functionality can be enhanced by an interface adapter. The interface adapter is plugged directly between the processor adapter and the I/O base. Interface adapters offer:

- Time of day
- Battery backup
- Additional communications interfaces

☞ **Note:**
Interface adapters can only be utilized in combination with a processor adapter, and not with a communications adapter.

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Three different interface adapters are available:

Table 3 TSX Momentum interface adapters

Type	Interfaces
172 JNN 210 32	Modbus port for either RS-232C or RS-485
172 PNN 210 22	Modbus Plus port
172 PNN 260 22	Two (redundant) Modbus Plus ports

Additional Documentation: Further information regarding the processor and interface adapters can be found in the 870 USE 101 00 manual.

Dimensions of the combined modules (with and without an interface adapter) are given in the 870 USE 002 00 User Manual.

1.2 Functional Details and Utilization

The 170 AEC 920 00 I/O base contains two 200 kHz hardware counters. Typical application areas would be:

- Event counting
- Frequency measurements
- Period measurements
- Pulse generator
- Position sensing through incremental encoders (quadrature mode)
- Position sensing through (SSI) absolute encoders

The module can also be employed for pulse and position operation. One of a possible 13 operating modes must be parameterized depending upon the particular application (refer to the overview of operating modes in Ch. 2).

Encoders perform the acquisition of pulses or positions and forward them to the I/O base. The I/O base firmware then interprets the incoming data as pulses, path increments, or ... based upon the operating mode, and compares them continuously with the prescribed command data values. These comparison results control two discrete hardware outputs for each counter. These outputs can consequently be utilized as first and final set–point cutoff output.

These operating modes often require a specific type of transmitter (pulse generator, absolute encoder, or incremental encoder). Encoder input signals are usually 5 Volt signals; however there are many application situations where 24 Volt signals are also authorized.

To facilitate control of the count and comparison functions, each of the two counters is further equipped with three discrete hardware inputs which are also available as software signals:

- Counter enable
- Accept preset value
- Hold current count

☞ **Note:**
Operating modes are described in Chapter 2. The diagnostic data and configuration of these functions is covered in Chapters 4 and 5. Configuration examples for counter operation mode are presented in Appendix A.

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1.2.1 Event Counting

The module is suitable for the operation of fast counting pulses and can provide explicit reaction, should the specified command data values be over or underrun.

1.2.2 Repetitive Counter

In this operating mode the module counts up to the previously registered modulo value, rolls back to a ”0” count, and continues from there. If a ”0” count is underrun while counting down, the count jumps back to the modulo value. Modulo values are always positive.

Expert
The repetitive function can be activated for every operating mode by transfer of a positive modulo value (code number 7). Exceptions are operating modes C, D, and E for absolute encoders.

1.2.3 Frequency Measurements

In this operating mode frequencies of up to 200 kHz can be measured. The time base can be varied in a range from 0.1 .... 1000 ms.

1.2.4 Period Measurements

In this operating mode the duration of a period can be measured. In this case pulses are registered for the duration of the gate time. Different time bases can be selected in accord with the period. Five time bases ranging from 1µs through 10,000 µs are available.

1.2.5 Pulse Generator

Pulses produced by the module can be output through the outputs Q1 (counter 1) and Q2 (counter 2). Pulse widths varying from 1 ms through 1000 s can be output (refer to 2.4.8).

1.2.6 Incremental Position Sensing

Position sensing through incremental encoders is performed according to a counting method. Therefore the encoder must be recalibrated (preset value acceptance) after turn–on or power failure. For this reason the encoder delivers a reference signal (zero pulse). In order to distinguish the direction of rotation during forward or reverse travel, the encoder provides two periodic square wave signals 90 degrees out of phase, which are evaluated and appropriately counted by the AEC.

To safeguard data transmission at higher frequencies, signals can also be conveyed as RS–422 differential signals, so that disturbing pulses can be recognized and common–mode interference eliminated. This requires a total of 6 conductors for data transfer (2 for each of the 3 counter inputs).

Reference zero (homing) execution (preset value acceptance)
Since the current actual position is lost with every power failure or at shut–down, the 170 AEC 920 00 must perform a reference zero (preset value acceptance) upon voltage recovery or turn–on. The encoder provides an appropriate reference signal (zero pulse).

7 different possibilities are made available to accept a preset value.

The acceptance of a preset value after every renewed enabling of the counter channel is necessary, since the discrete outputs will not otherwise be serviced.

The reference point switch should be installed close to a hardware limit switch such that the reference point is always approached from one direction.

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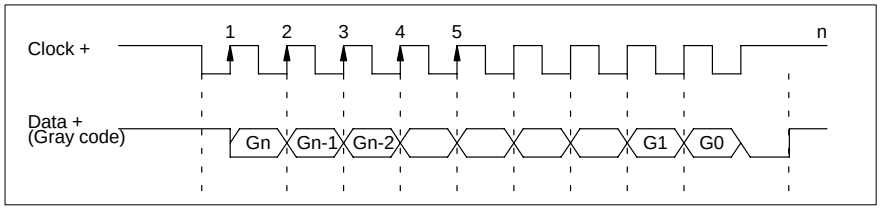
1.2.7 Absolute Position Sensing

In absolute displacement measurement each position is allocated a distinct numeric value. An absolute encoder performs this task. These numeric values exist in the encoder as code patterns (for instance on code disks in dual, Gray, or some other encoding). The great advantage to this encoder style is that the absolute position is available immediately upon turn–on.

Actual position determination is performed as follows:

The 170 AEC 920 00 requests the position value through a pulse sequence. The first 170 AEC 920 00 clock signal latches the absolute position present in the encoder and starts its clock–synchronous transfer as a serial data telegram (Gn ... G0) back to the 170 AEC 920 00 (see Figure 1). The length n of this transferred data stream is directly dependent upon the encoder resolution resp. data format, and can be parameterized through configuration words. The resolution of standard encoders is n=24.

Figure 1 SSI clock and data telegram



This data transfer takes place via a 4–wire (two each for clock and data) serial synchronous interface (SSI).

To safeguard data transmission, signals are conveyed as RS–422 differential signals, so that noise pulses can be recognized and common–mode interference eliminated.

Operating Mode Descriptions

2

A description of all valid operating modes (operation forms) in which the counter can operate can be found in the following chapter. The operating modes for each counter are parameterized individually through the output words 1 and 2 (refer to Chapter 3.3.1 on page 40).

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2.1 Overview of AEC 920 00 Operating Modes

The following table provides an overview of the valid operating modes:
(as defined in output words 1 and 2 (bits 11–8))

Operating mode	Transmitter type *)	Function
0		Channel not ready, parameters not reset, outputs = 0
1	Pulse	Down–counter
2	Pulse	Up–counter
3		Corresponds to operating mode ”0”
4	Inc	Up/down counter, position sensing, x 1 counter
5	Inc	Up/down counter, position sensing, x 4 counter
6	Pulse	Differential counter: A counter input = upcount; B counter input = downcount
7	Pulse	Up/down counter: A counter input = up/down; B counter input = direction (1 = up, 0 = down)
8	Pulse	Pulse counter with time base (e.g. for rotary speeds, flow rates etc.) a) with an external clock as time base to the B counter input or b) discrete output (Q) as time base to the B counter input
9	Pulse	Period meter with 5 time bases for full or half periods; full period: 0 = without time base, 1 = 1 , 2 = 10, 3 = 100, 4 = 1 000, 5 = 10 000 [microsec.]; half period: 9 = 1, A = 10, B = 100, C= 1 000, D = 10 000 [microsec.]

A	Pulse	frequency meter with 5 time bases for full or half periods; full period: 0 = without time base, 1 = 0.1 , 2 = 1, 3 = 10, 4 = 100, 5 = 1 000 [ms]; half period: 9 = 0.1, A = 1, B = 10, C= 100, D = 1 000 [ms]
B		Corresponds to operating mode ”0”
C	Abs	Position sensing with single-turn encoders (SSI), 12–bit resolution
D	Abs	Position sensing with multi-turn encoders (SSI), 24–bit resolution
E	Abs	Position sensing with multi-turn encoders (SSI), 25–bit resolution
F		Software reset. This always resets both counters, regardless of whether this operating mode has been invoked for counter 1 or 2.

*) Explanation of transmitter types:

Inc = incremental encoder

Abs = absolute encoder

Pul = pulse generator

☞ **Note:**
0, 3, and B are not true operating modes in the conventional sense. The counter is in a ”neutral mode”, i.e. in a secure state and inactive.

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2.2 Common Counter Characteristics

Both of the 170 AEC 920 00 I/O base counters are operated as a unit either with incremental, pulse, or absolute encoders.

2.2.1 Counter Resolution

Counter resolution is at most 24–bit + sign; equivalent to decimal values from –16 777 216 ... +16 777 215. The counting range utilized is dictated by the operating mode. 13 operating modes are selectable.

2.2.2 5 VDC/24 VDC Counter Inputs

The module can be connected to both 5 VDC differential signal (RS–422) encoders and 24 VDC signal (single–ended) encoders.

2.2.3 Preset Value

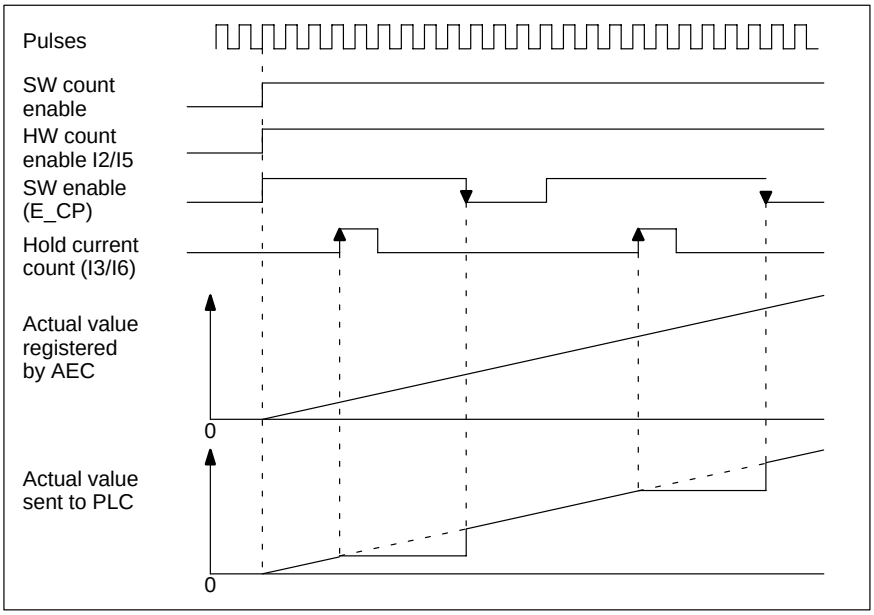
The counter can be loaded with a freely definable value from the PLC with the preset value. Preset value acceptance is dependent upon both the preset mode and the discrete inputs. Counter 1 is assigned discrete input 1 and counter 2 discrete input 4. When no preset value is transferred from the PLC, a default preset value of 0 is placed in the counter.

2.2.4 Software Limit Switch

A counter working range can be specified through the upper and lower software limit switches. When a software limit switch boundary is exceeded discrete outputs are deactivated and an error message is given. The software limit switches are only active after parameter values for both the upper and lower software limit switches have been transferred.

2.2.5 Hold the Current Counted Value (Capture Function)

With this function the current count value is placed in an additional internal register. Counting operations continue independent of this function. The function is required in particular for the measurement of pulses or paths. Counted value holding takes place after an enable through the software (E_CP bit) and an edge at either the I3 discrete input for counter 1 or I6 for counter 2. This held counted value continues to be transferred as the actual value to the PLC until the E_CP bit is reset by software. Transfers of the counter's true actual value are reinstated after the reset.



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2.2.6 Event Processing

The user has the option of assigning event–dependent functions to the outputs. The discrete outputs are set when the parameterized event has occurred.

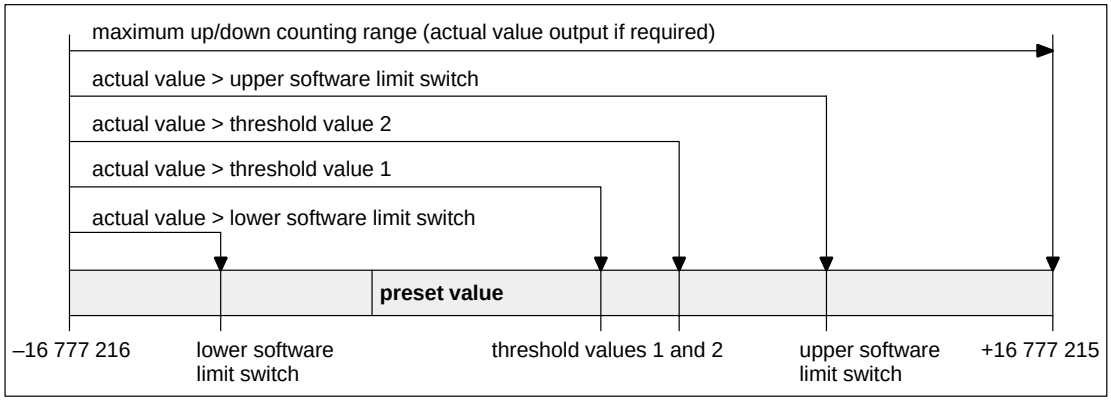
The following events can be parameterized:

- Counter value = threshold value
- Counter value >= threshold value
- Counter value < threshold value
- Counter value >= threshold value 1 and < threshold value 2

Additional information can be found in Chapter 4.2.3.

2.2.7 Definition of Terms

Explanations of terminology employed in this manual follow:



Counting pulse signals are dependent upon the type of transmitter. The I/O base can process signal levels of either 5 VDC or 24 VDC. Two counter inputs are provided for each of the two counters:

- 5 VDC differential signals (channels A+, A–; B+, B–; Z+, Z–)
- 24 VDC differential signals (channels A*, A–; B*, B–; Z*, Z–)
- 24 VDC single–ended signals (channels A*, B*, Z* connected to the transmitter’s ground. Be sure to turn off the encoder monitoring!)

2.2.8 Discrete Counter Control Inputs (I1 ... I6)

The discrete inputs (counter enable, accept preset value, and hold current count) are only effective in combination with the corresponding software signals.

☞ **Note:**
The counter inputs can be configured to operate with and without a filter for 5 VDC and 24 VDC signals. Filter activation (employed for mechanical contacts) reduces the counting frequency (max. 20 kHz).

2.2.9 Discrete Counter Outputs (Q1 ... Q4)

The discrete outputs can be operated in two fashions:

- through counter operations
- forcing discrete outputs via output words 1/2 (bits 1 ... 7) within the configuration tool (possible at any time)

Output activation functions are determined upon counter configuration (refer to Chapter 4.2.4, page 71).

2.2.10 Channel–Specific Error Messages

The user can obtain detailed references to the type of error reported at the counter input through the error word. These can be:

- Faults with the transmitter supply voltage
- Overshooting or undershooting of the measurement range
- Faulty transmitter
- Faulty transmitter connection

These errors are reported through the input words (refer to Chapter 5 ”Counted Values and Status Information”).

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2.2.11 Preset Value Acceptance (Preset Mode)

The counter can be loaded with a freely definable value from the PLC with the preset value. Preset value operation is dependent upon both the preset mode and the discrete inputs. Counter 1 is assigned discrete input 1 and counter 2 discrete input 4.

The following preset modes are available (words 1/2, (bits I4 ...I2)):

Preset mode	**Function**
0	Without preset
1	The preset value is activated by a positive edge at the ”preset” discrete input.
2	The preset value is activated by a negative edge at the ”preset” discrete input.
3	The preset value is activated by a positive edge at the ”preset” discrete input. The counter is then halted. A negative edge at the ”preset” discrete input starts the counter again.
4	The preset value is activated by a positive edge (for count up) or a negative edge (for count down) at the ”preset” discrete input.
5	The preset value is activated by a negative edge (for count up) or a positive edge (for count down) at the ”preset” discrete input.
6	Reference point with short cam signal
7	Reference point with long cam signal

The transmitter’s zero pulse (Z counter input) registers the preset value in preset modes 6 and 7. The transmitter provides this counting pulse with every full revolution.

The preset mode is configurable (also refer to Chapter 4.1.4, page 62). The preset modes are not available in all operating modes (frequency, period, and pulse counter).

2.3 Counter Channel for Counter Functions with Pulse Generators and Incremental Encoders

The software & hardware logic operations demonstrate the relationships for incremental encoders.

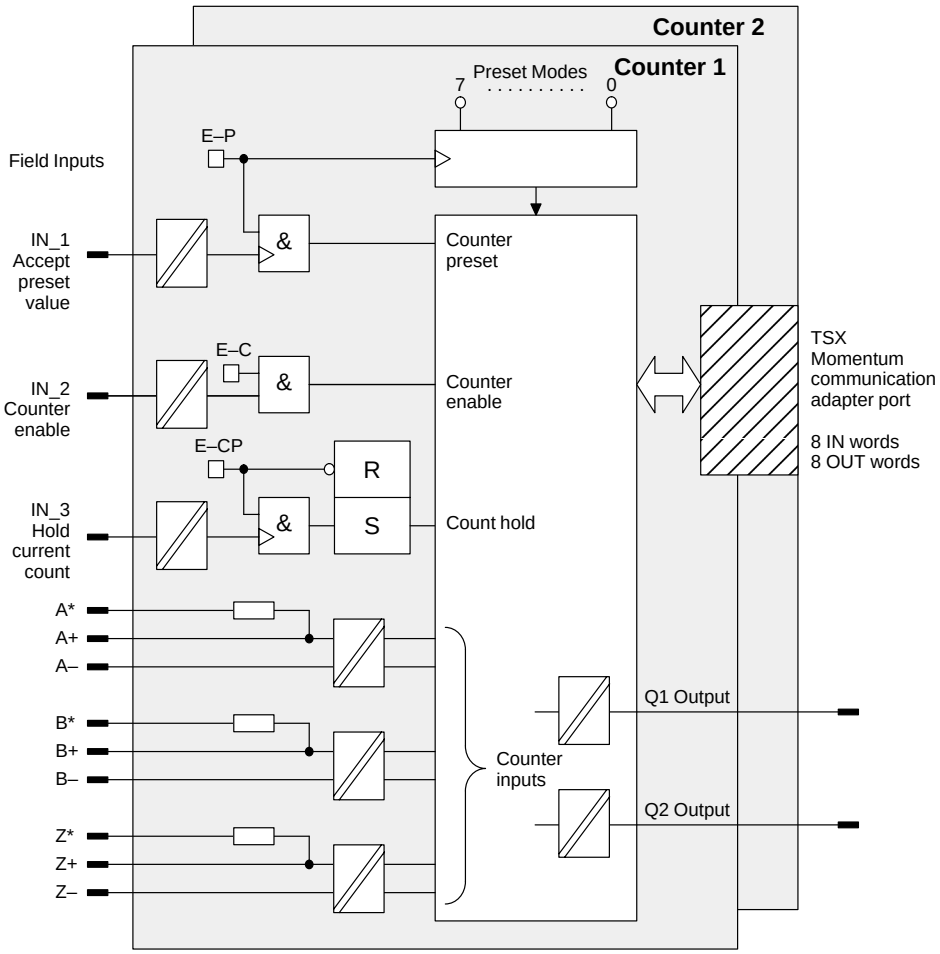

Figure 2 Incremental encoder functional diagram

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2.4 Pulse Generator & Incremental Encoder Modes

Operating Modes (Output words 1/2, (bits 8 ... 11))

2.4.1 Operating Mode 1: Pulse Down–Counter

In this operating mode all A input pulses count down, starting from a preset value (default = 0). The B input is functionless. Pulse generators with both 5 VDC differential output (RS–422) and 24 VDC single–ended output (24 VDC proximity switches) may be connected. The 2 discrete outputs can be controlled through 2 programmable threshold values.

2.4.2 Operating Mode 2: Pulse Up–Counter

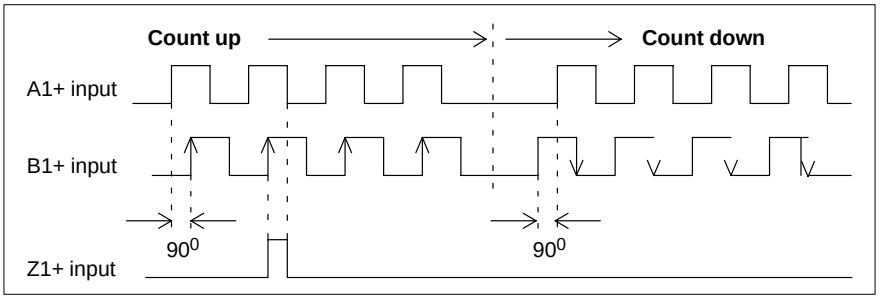
In this operating mode all A input pulses count up, starting from a preset value (default = 0). The B input is functionless. Pulse generators with both 5 VDC differential output (RS–422) and 24 VDC single–ended output (24 VDC proximity switches) may be connected. The 2 discrete outputs can be controlled through 2 programmable threshold values.

2.4.3 Operating Mode 3:

Reserved; Operating Mode ”0” Equivalent

2.4.4 Operating Mode 4: Counting with x1 Logic Incremental Encoders

Position sensing through incremental encoders is performed according to a counting method. Therefore the encoder must be calibrated after turn–on or after power failure. The encoder provides an appropriate reference signal (zero pulse). In order to distinguish the direction of rotation during forward or reverse travel, the incremental encoder provides two periodic square wave signals 90 ° out of phase, which are evaluated and appropriately counted by the AEC 920 00. The 2 discrete outputs can be controlled through 2 programmable threshold values.



2.4.5 Operating Mode 5: Counting with x4 Logic Incremental Encoders

Identical to operating mode 4, but offering 4 times the resolution since every edge of the A and B inputs can be evaluated (refer to the examples in Appendix B.1, page 102).

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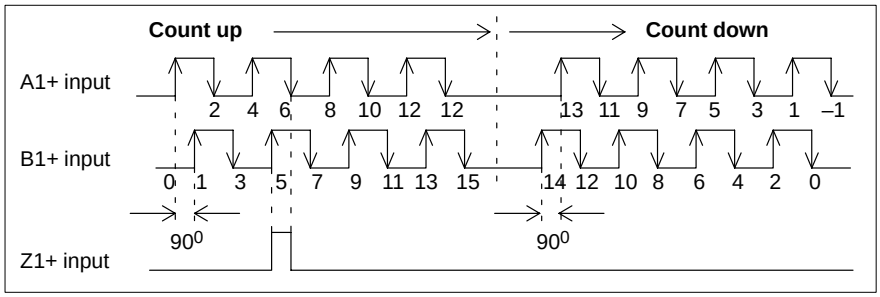
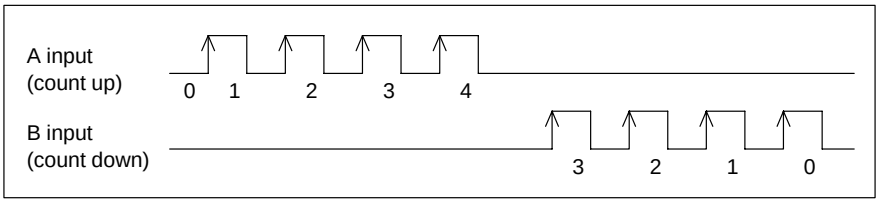


☞ **Note:**
The differential signal diagrams were omitted for operating modes 4 and 5 for clarity.

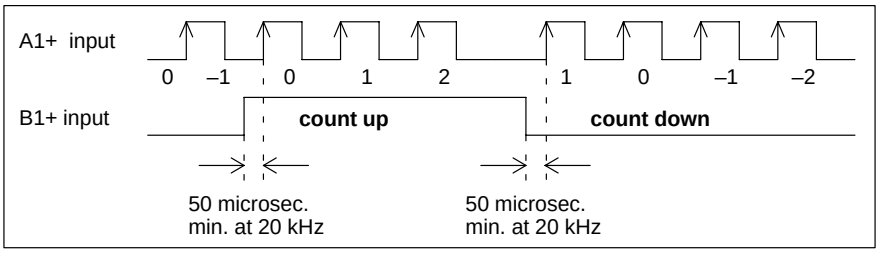
2.4.6 Operating Mode 6: Differential Counter

In this operating mode all pulses at the A input cause counting up, while all pulses at the B input invoke counting down. This means, that in this operating mode the pulse difference between the A and B inputs is formed.
The 2 discrete outputs can be controlled through 2 programmable threshold values.



2.4.7 Operating Mode 7: Up/Down Counter with Directional Signal

In this operating mode all pulses at the A input are counted up or down in accordance with the state of the B input. Counts are up for a B counter input ”1” signal, and down on a ”0” signal. The 2 discrete outputs can be controlled through 2 programmable threshold values.



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2.4.8 Operating Mode 8: Pulse Counter with Time Base (Rotary Speeds)

This operating mode is suitable for the determination of speeds, flow rates, or revolutions. Pulses during a selectable time base (gate time) are counted and saved. Thereafter the counter is reset and the counting procedure starts once again.

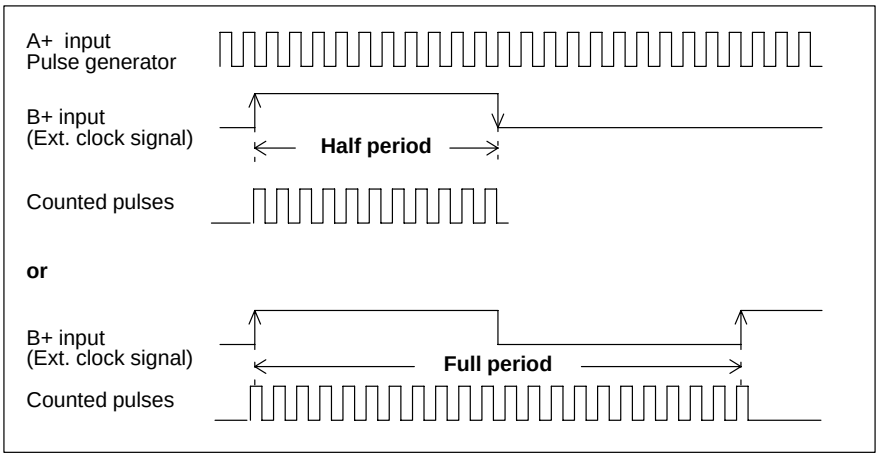
The gate time can be controlled in two ways:

- an external clock signal or
- an internal clock signal output through the Q1 or Q3 discrete outputs. These outputs must be configured (through output words 3 and 4) for frequency output (function D). In addition, the frequency must be chosen through code number B.

The count interval is from the positive to the negative edge of the clock signal **(half period)** or from one positive edge to the next **(full period)**. This is also parameterized through the output words 3 and 4.

☞ **Note:**
The discrete inputs (counter enable, accept preset value, and hold current count) are functionless in this operating mode. Only the frequency output function is made available for the discrete outputs (refer to 4.2.3).

Example 1: Pulse counting with an external clock signal (e.g. 5 VDC level)



☞ **Note:**
If an external clock signal with 24 VDC level is to be utilized, it must be connected to the B* input.

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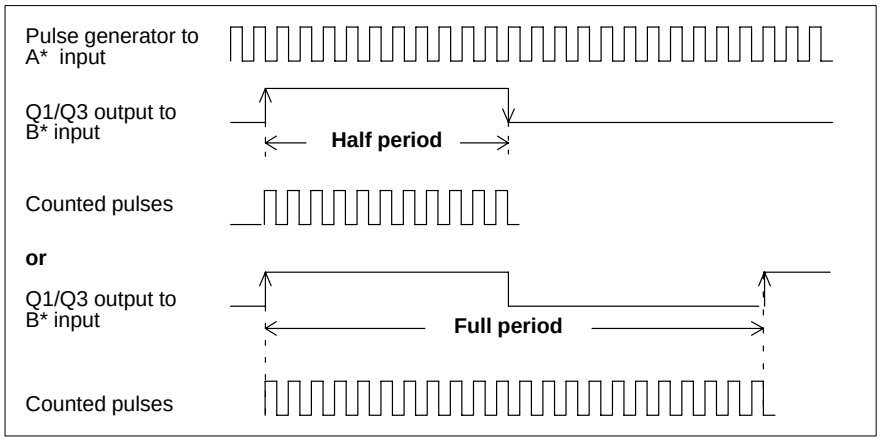
Example 2: Pulse counting with an internal clock signal (only 24 VDC level)

If an external clock signal is not available, the Q1/Q3 discrete outputs can be configured for frequency output. But since these outputs are only available as 24 VDC level, the corresponding Q1/Q3 output must be tied to the B* input, and B– with 1M–.



2.4.9 Operating Mode 9: Period Meter with 5 Time Bases

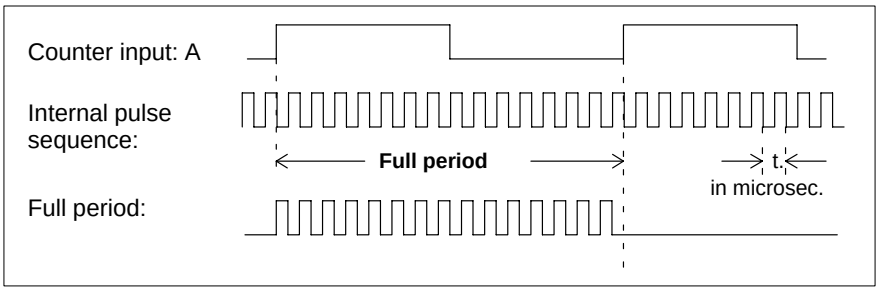
In this operating mode the duration of a period can be measured. In this case pulses are registered for the duration of the gate time. Different time bases can be selected in accord with the period. Five time bases ranging from 1µs through 10,000 µs are available.

This operating mode is applied to time measurements of processes.

☞ **Note:**
The time base is to be chosen such that the precision required is achieved, and that there is no counter overrun within the measurement period.

Depending upon the process, both full and half periods can be measured.

- Full period means: measurement of the input pulse sequence from one positive edge to the next.



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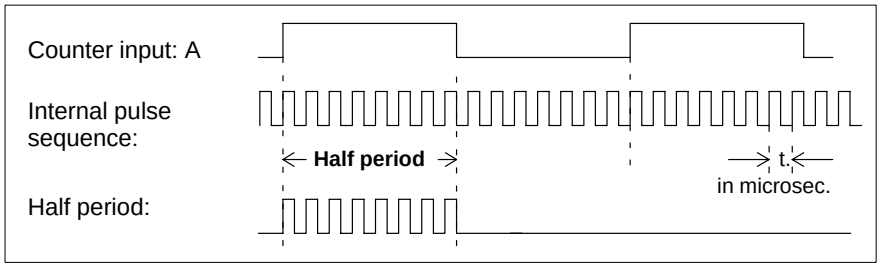


☞ **Note:**
Half period means: measurement of the input pulse sequence from one positive to the next negative edge.

2.4.10 Operating Mode A: Frequency Meter with 5 Time Bases

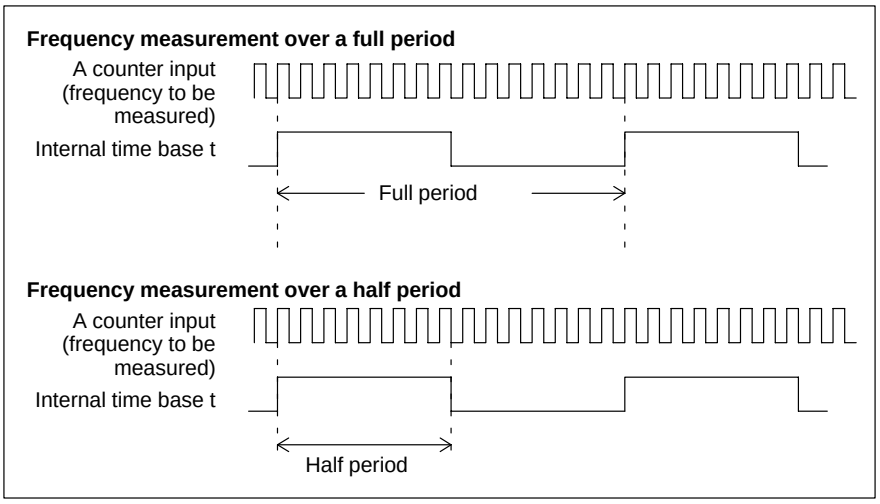
In this operating mode the number of pulses per unit time is measured. Different time bases can be selected in accord with the frequency to be measured. Five internal time bases ranging from 0.1 ms through 1000 ms are available.

This operating mode is applied to measurements of process frequencies.

☞ **Note:**
The time base is to be chosen such that the precision required is achieved, and that there is no counter overrun within the measurement period.

Depending upon the process, both full and half periods can be measured.

- Full period means: measurement of the input frequency from one positive time base edge to the next.
- Half period means: measurement of the input frequency from one time base positive to the next negative edge.



Width: 178 mm
Height: 216 mm

2.5 Operating Modes for Absolute Encoder

Both 170 AEC 920 00 counters can also be connected to absolute encoders using the SSI protocol.

☞ **Note:**
Mixed operation with incremental and absolute encoders is not supported.

Hereafter only the functions deviating from the incremental encoder will be described.

☞ **Note:**
The input filter must be disabled in the operating modes C, D, and E.

The following characteristics apply to absolute encoder operation:

2.5.1 Counter Resolution

The resolution of both counter channels can be chosen as 12–, 24–, or 25–bit. This is equivalent to decimal values from +4096 to +33 554 431.

The following operating modes are possible with absolute encoders:

- C = counting with 12–bit resolution (single-turn encoder)
- D = counting with 24–bit resolution (multi-turn encoder)
- E = counting with 25–bit resolution (multi-turn encoder)

2.5.2 Encoder Offset

The encoder’s absolute position value can be shifted through the encoder offset. Displacement is only allowed within the max. encoder resolution. The transferred offset is added to the current actual value through a 0–>1 edge of the E_P bit (word 1/2, (bit 0)).

In order to displace the encoder’s absolute value to the machine zero point, the negatively signed current actual position is transferred to the encoder as offset. Through the addition of absolute value and offset carried out within the module, the actual value is set to zero.

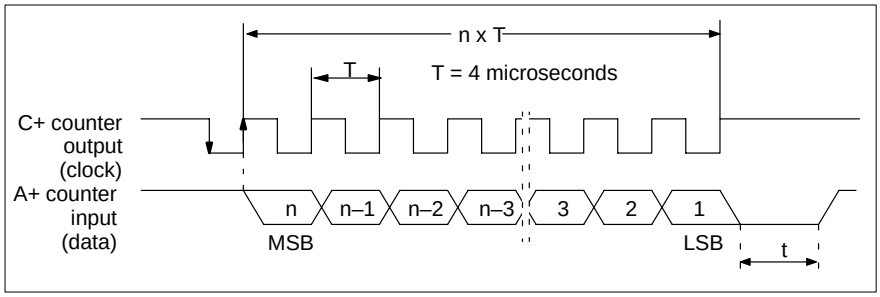
2.5.3 SSI = Serial synchronous Interface

Absolute position value (data) transfer begins with the ”most significant bit” (MSB) and in sync with a counter–provided clock output.

The data word length may be 12–bit for encoders with a single track (single-turn) and 24– or 25–bit for dual track encoders (multi-turn). An evaluation of parity or power failure bits is not foreseen.

Width: 178 mm
Height: 216 mm

Clock Cycles for the SSI Data Format



Each cycle edge triggers transfer of a single data bit. The 250 kHz clock frequency is dictated by the module.

Clock and data signals are at a high level when idle. The current measured value is latched through the first falling edge. Data transmission begins with the first rising edge.

The data signal output remains low after data word transfer until the absolute encoder is ready to provide a new measured value (t). This latency time depends upon the employed absolute encoder and is typically on the order of 30 microseconds.

2.6 Counter Channel for Counter Functions with Absolute Encoders

The software & hardware logic operations demonstrate the relationships for absolute encoders.

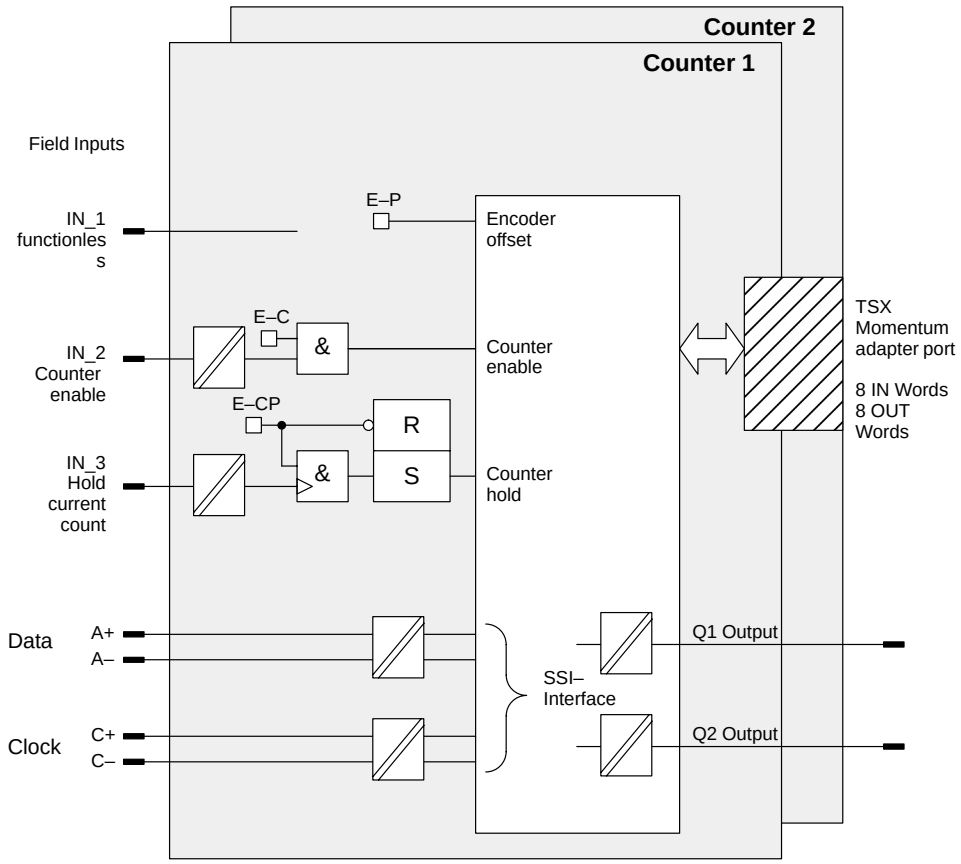


Figure 3 Absolute encoder functional diagram

Width: 178 mm
Height: 216 mm

2.6.1 Operating Mode C: Position Sensing with Single-Turn Encoders (SSI), 12–Bit Resolution

For connection of a SSI encoder with a single track. Resolution is 12–bit per revolution (single-turn encoder).

Single-turn encoders begin counting again from 0 after a full revolution. They are suitable for traversing ranges in which either the encoder does not make use of the entire revolution, or for those applications in which the number of revolutions is not important (turntable, ...).

An example of position sensing with a single-turn encoder can be found in the Appendix.

2.6.2 Operating Mode D: Position Sensing with Multi-Turn Encoders (SSI), 24–Bit Resolution

The multi-turn encoder with 24–bit resolution delivers 12–bit resolution per revolution (4096 pulses) and can count through 4096 revolutions before overflowing. The great advantage of absolute encoders is that the absolute position is available immediately upon turn–on.

An example of position sensing with a multi-turn encoder can be found in the Appendix.

2.6.3 Operating Mode E: Position Sensing with Multi-Turn Encoders (SSI), 25–Bit Resolution

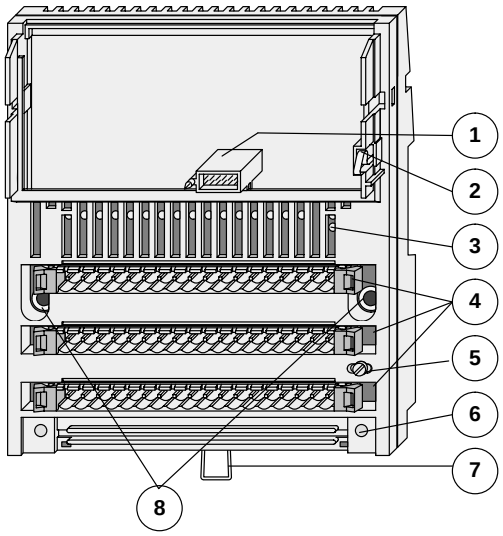
The multi-turn encoder with 25–bit resolution delivers 13–bit resolution per revolution (8192 pulses) and can count through 4096 revolutions before overflowing. The great advantage of absolute encoders is that the absolute position is available immediately upon turn–on.

An example of position sensing with a multi-turn encoder can be found in the Appendix.

170 AEC 920 00
Module Description

3

The 170 AEC 920 00 I/O base can count pulse frequencies of up to 200 kHz. To this end it is equipped with two hardware counters for counting pulse inputs (each with discrete inputs for counter enable, accept preset value, and hold current count as well as two independent discrete outputs).



Module elements:

1 Internal adapter connector (ATI)
2 Adapter fixation point and ground contact
3 LED status display
4 Terminal block connectors
5 Grounding screw
6 Grounding busbar
7 DIN rail interlock spring
8 Wall installation mounting holes

Width: 178 mm
Height: 216 mm

3.1 Momentum Adapter Selection

Select an appropriate communications adapter or processor adapter for your application and mount according to the 870 USE 002 00 User Manual instructions.

Caution:
Electrical voltages are present when the I/O base is connected to a supply voltage. Ensure that no voltage is applied as long as the I/O base is without an adapter.

This can be achieved by not attaching the terminal blocks to the I/O base until after adapter installation.

Always be sure to unplug the terminal blocks before separating the adapter from the I/O base. That should leave the I/O base without power.

Failure to observe these precautions will endanger personal safety or risk damage to the I/O base.

3.2 Terminal Block Selection

Suitable terminal blocks must be chosen for the connection of transmitters, sensors, and actuators to the I/O base. These can be found in the 870 USE 002 00 User Manual (refer to ”Terminal Block and Busbar Selection”).

3.3 Configuration

The 170 AEC 920 00 I/O base is equipped with two configurable hardware counters with discrete I/Os for high–speed counting procedures. Data exchange with the PLC is accomplished through contiguous word registers: eight IN and eight OUT.

- Output words – The configuration (parameterization) and value specification takes place through the output words
- Input words – The input words contain the status information, error messages, and counted values for each counter

Width: 178 mm
Height: 216 mm

3.3.1 Output Words

The eight counter output words with the following configuration data are sent to the I/O base:

Address 4x: Output word 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Counter 1 configuration

Address 4x + 1: Output word 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Counter 2 configuration

Address 4x + 2: Output word 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Configuration of the Q1, Q2 discrete outputs for counter 1

Code numbers for counter 1 command data and broken wire detect

Address 4x + 3: Output word 4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Configuration of the Q3, Q4 discrete outputs for counter 2

Code numbers for counter 2 command data and broken wire detect

Address 4x + 4: Output word 5 (low word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Counter 1 command data (low part)

Address 4x + 5: Output word 6 (high word)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Counter 1 command data (high part)

Address 4x + 6: Output word 7 (low word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Counter 2 command data (low part)

Address 4x + 7: Output word 8 (high word)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Counter 2 command data (high part)

☞ **Note:**
The individual word functions can be found in Chapter 4 from page 57 **"Counter Configuration".**

3.3.2 Input Words

8 input words from the I/O module with the following contents:

Address 3x: Input word 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Counter 1 module status bits								Counter 1 error bits							

Address 3x + 1: Input word 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Counter 2 module status bits								Counter 2 error bits							

Address 3x + 2: Input word 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Counter 1 output status								Code number for counter 1 command data							

Address 3x + 3: Input word 4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Counter 2 output status								Code number for counter 2 command data							

Address 3x + 4: Input word 5 (low word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Counter 1 current counted value (low part)															

Address 3x + 5: Input word 6 (high word)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Counter 1 current counted value (high part)															

Address 4x + 6: Input word 7 (low word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Counter 2 current counted value (low part)															

Address 4x + 7: Input word 8 (high word)

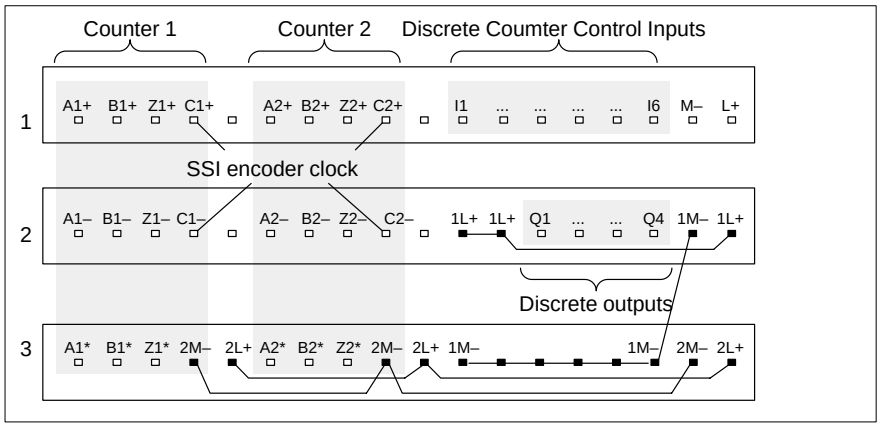
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Counter 2 current counted value (high part)															

☞ **Note:**
See page 85 for more details**”Diagnosis”.**

Width: 178 mm
Height: 216 mm

3.4 Internal Connections and Signal Functions

The following figure shows I/O base internal connections.



Caution:
A module without fuse protection can cause a short circuit and/or voltage spikes.

Protective measures should always provide external supply voltage fuses for module protection. Wiring diagrams specify the proper fuse values.

Failure to observe these precautions will endanger personal safety or risk damage to the I/O base.

Table 4 Terminal block mapping

Row	Terminal no.	Signal	Function
1	1, 6	A1+, A2+	Positive differential A input (5 VDC), counter channels 1, 2
	2, 7	B1+, B2+	Positive differential B input (5 VDC), counter channels 1, 2
	3, 8	Z1+, Z2+	Positive differential Z input (5 VDC), counter channels 1, 2
	4, 9	C1+, C2+	Positive SSI clock output, counter channels 1, 2
	11, 14	I1, I4	Discrete accept preset value inputs, counter channels 1, 2
	12, 15	I2, I5	Discrete counter enable inputs, counter channels 1, 2
	13, 16	I3, I6	Discrete hold current count inputs, counter channels 1, 2
	17	M–	Power supply – return
	18	L+	Module +24 VDC power supply
2	1, 6	A1–, A2–	Negative differential A input (5 VDC), counter channels 1, 2
	2, 7	B1–, B2–	Negative differential B input (5 VDC), counter channels 1, 2
	3, 8	Z1–, Z2–	Negative differential Z input (5 VDC), counter channels 1, 2
	4, 9	C1–, C2–	Negative SSI clock output, counter channels 1, 2
	13, 14	Q1, Q2	Counter channel 1 discrete outputs
	15, 16	Q3, Q4	Counter channel 2 discrete outputs
	17	1M–	24 VDC working voltage – return
	11, 12, 18	1L+	Discrete output + 24 VDC working voltage, discrete input supply voltage
3	1, 6	A1*, A2*	Positive differential A input (24 VDC), counter channels 1, 2
	2, 7	B1*, B2*	Positive differential B input (24 VDC), counter channels 1, 2
	3, 8	Z1*, Z2*	Positive differential Z input (24 VDC), counter channels 1, 2
	11 ... 16	1M–	24 VDC working voltage – return
	4, 9, 17	2M–	Transmitter supply voltage – return
	5, 10, 18	2L+	+5 ... +30 VDC transmitter supply voltage

Width: 178 mm
Height: 216 mm

Table 5 Incremental encoder cable lengths and cut–off frequencies

Transmitter type with signal level	Cable length	Cut–off frequency (kHz)
5 VDC RS–422	up to 100 m, shielded, twisted–pair	200 kHz
5 VDC RS–422	up to 300 m, shielded, twisted–pair	100 kHz
24 VDC	up to 300 m	10 kHz (w/filter active)

Table 6 Absolute encoder cable lengths and cut–off frequencies

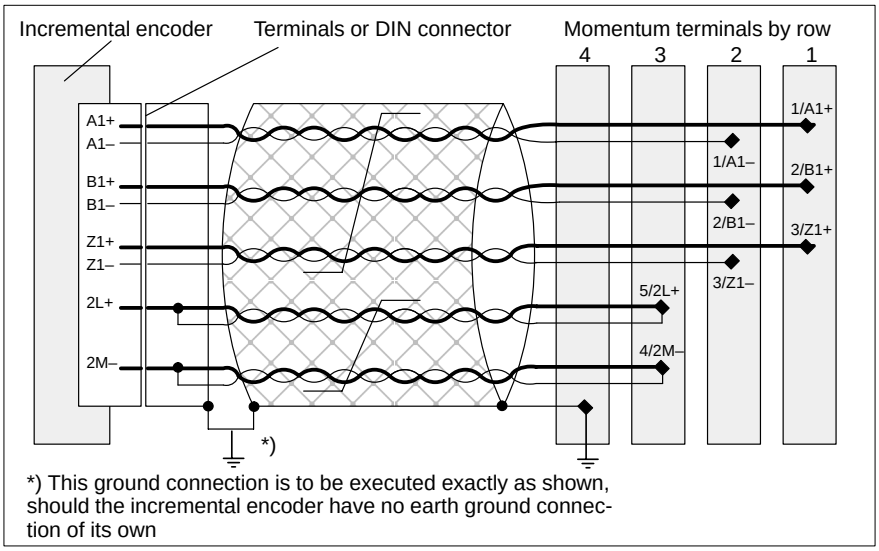
Trans. type	Cable length	Cut–off frequency (kHz)
RS–422	100 m max.	Each specified by the 170 AEC 920 00

3.5 Wiring Practices and Examples

The following measures are recommended to protect count signals from external push–pull or common mode disturbances:

- Use shielded, twisted–pair cable with a 0.22 mm^2 (AWG 24) minimum conductor cross section for all counter signal wiring.
- Ground the cable shield at both ends.
- Under the assumption that a common earth is applied, this I/O base's count signals can be connected to multiwire (twisted–pairs) cable which is also carrying the encoder supply.
- It should be taken into account for the encoder supply (mainly for 5 VDC), that a voltage drop of about 0.35 VDC results for an encoder current consumption of 100 mA, a wire cross section of 1 mm^2 (AWG 17) , and 100 m cable length.
- Separate the encoder cable from power lines or similar sources of electrical disturbances (at best a clearance >0.5 m).
- To attain full electrical isolation, the power for transmitters and peripherals should be drawn from separate sources.

5 VDC incremental encoder connection example (counter 1)



*) This ground connection is to be executed exactly as shown, should the incremental encoder have no earth ground connection of its own

Width: 178 mm
Height: 216 mm

Figure 4 Pulse generator (5 VDC) wiring example

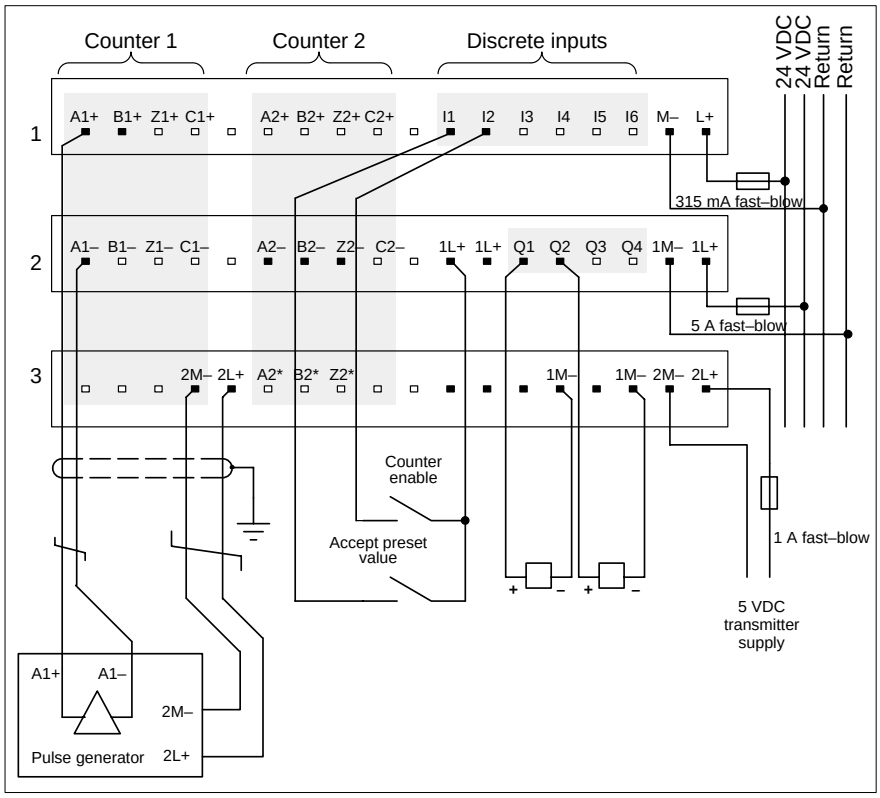
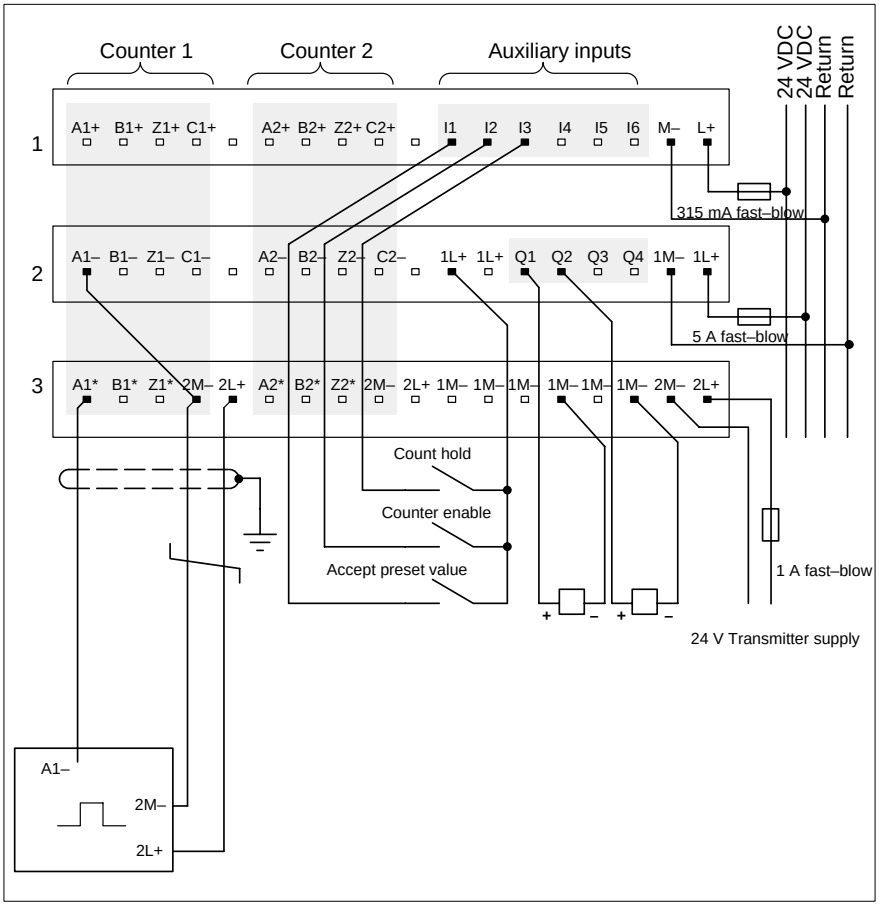


Figure 5 Pulse generator (24 VDC) wiring example



☞ **Note:**
The wiring example relates to operating mode 1: counting down.

Width: 178 mm
Height: 216 mm

Figure 6 Incremental encoder 5 V differential (RS–422) wiring example

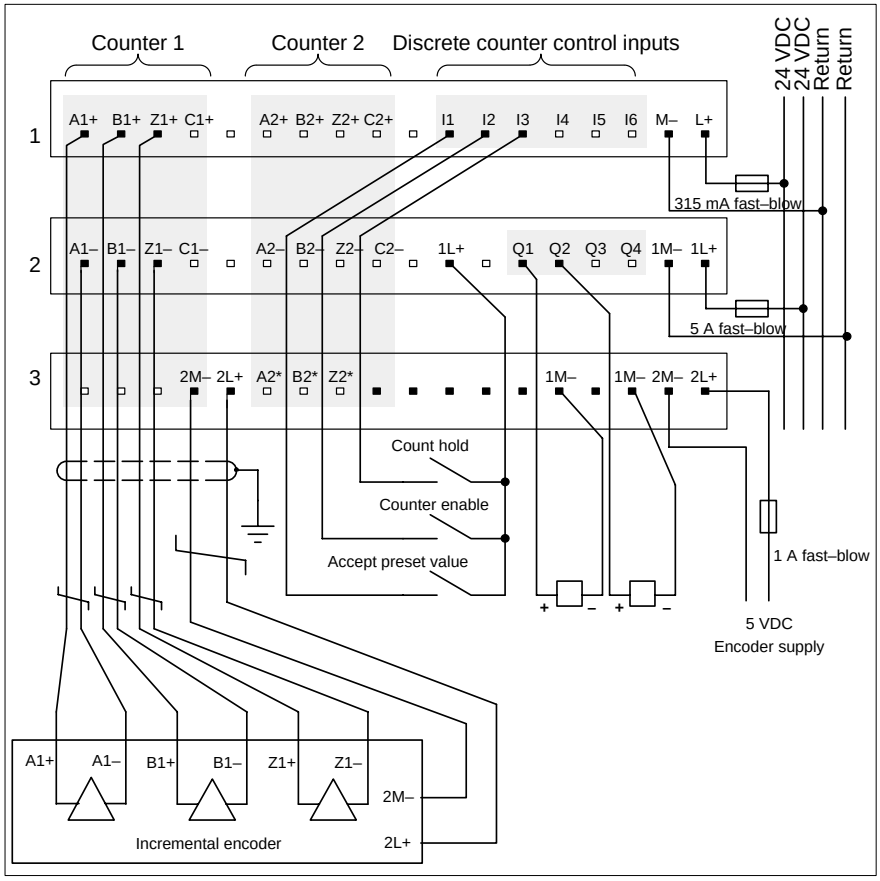
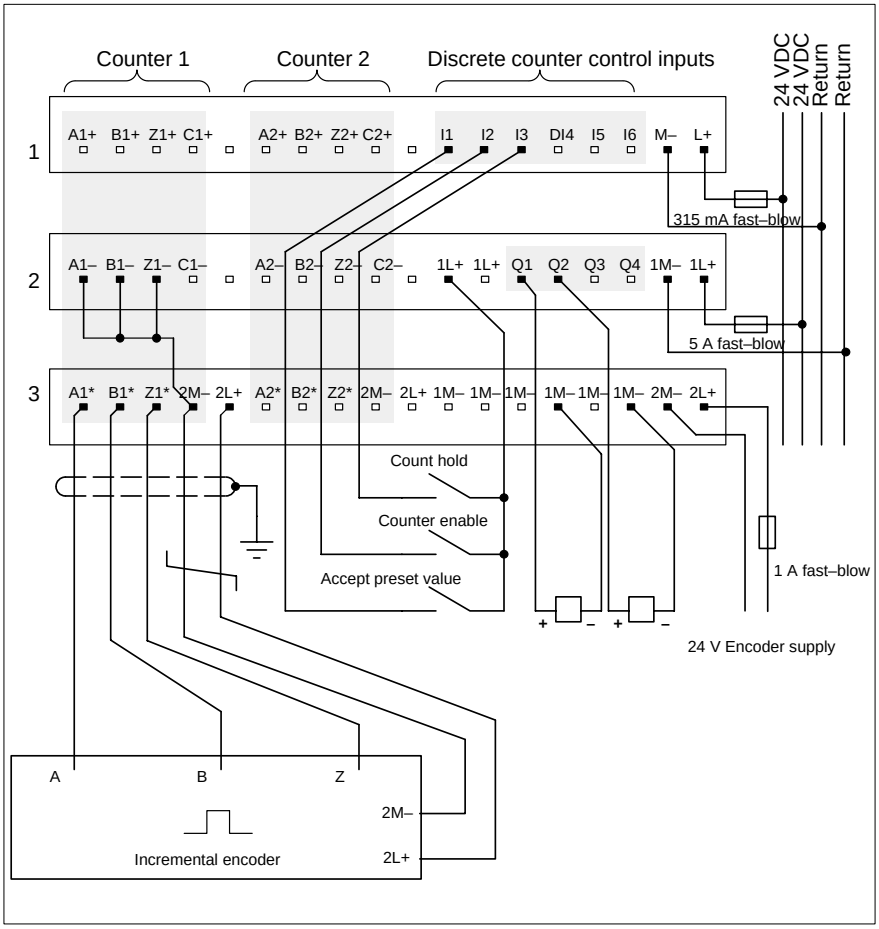


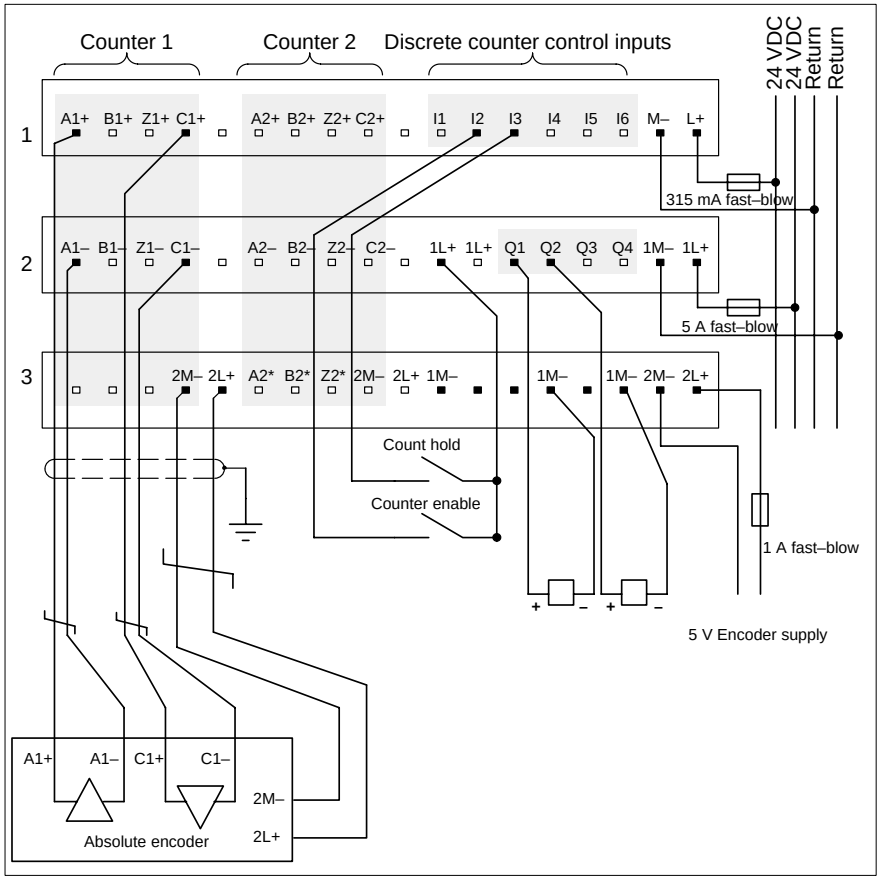
Figure 7 Wiring for 24 VDC incremental encoder for tracks A, B, and Z



Note:
The wiring example relates to operating modes 3, 4, and 5.

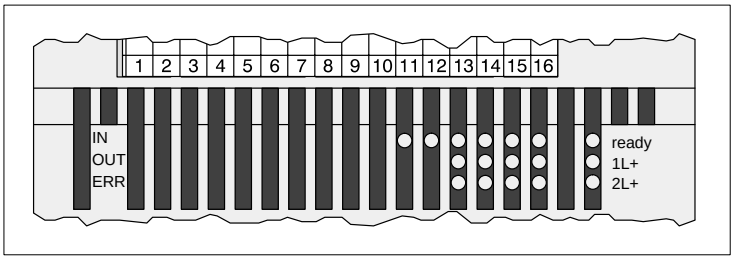
Width: 178 mm
Height: 216 mm

Figure 8 Wiring example for absolute encoder



☞ **Note:**
The wiring example relates to operating modes C, D, and E (SSI absolute encoder)

3.6 LED Status Display



LED	Status	Meaning
ready	Green	Ready for service; internal logic supply voltage (5 VDC) is present.
	Off	Module not ready.
1L+	Green	1L+ working voltage for Q1 ... 4 discrete outputs present.
	Off	1L+ working voltage for Q1 ... 4 discrete outputs not present.
2L+	Green	2L+ encoder supply voltage (5 ... 30 VDC) is present.
	Off	2L+ encoder supply voltage (5 ... 30 VDC) is not present.
Upper row IN	Green	Input status (one LED per discrete input); input active, i.e. ”1” signal at input (logical ”ON”).
11 ... 16	Off	Input status (one LED per discrete input); input inactive, i.e. ”0” signal at input (logical ”OFF”).
Middle row OUT	Green	Output status (one LED per discrete output); output active, i.e. ”1” signal at output (logical ”ON”).
13 ... 16	Off	Output status (one LED per discrete output); output inactive, i.e. ”0” signal at output (logical ”OFF”).
Bottom row ERR	Red	Discrete output overload (one LED per output); short circuit or overload of the corresponding output.
13 ... 16	Off	Normal Q1 ... Q4 output operation.

Width: 178 mm
Height: 216 mm

3.7 Technical Specifications

Module Type	2 high–speed counters (10 ... 200 kHz)
Supply voltage, sensor voltage, working voltage	24 VDC
Input current	6 mA @ 24VDC (type 1+ or 2)
Load current max.	0.5 A/output

Interbus ID–Code		hex 0633 decimal 1587
External Power Supply	Supply voltage	20 ... 24 ... 30 VDC
	Power consumption	Typically 200 mA at 24 VDC 350 mA max.
	Power dissipation	Typically 4 W 6 W maximum
Discrete Counter Control Inputs	Sensor supply	Typically 24 VDC 30 VDC max.
	Number of inputs	6 Sinking type
	Number of groups	2
	Input	3 for each counter with the functions: a) Accept preset value b) Counter enable c) Count hold
	Type of signal	True high
	IEC 1131 type	1+
	Signal level of ”1” signal	+11 ... +30 VDC
	Signal level of ”0” signal	–3 ... +5 VDC
	Input current	2.6 mA min. for ”1” signal 1.2 mA maximum for ”0” signal
	Input voltage range	–3 ... +30 VDC
	Surge	45 V pk for 10 ms
	Input delay (counter to output)	1 ms max. off to on 1 ms max. on to off

Counter Inputs (for pulses)	Input types	5 VDC differential (RS–422) or 24 VDC single–ended
	IEC 1131 type	2
	Counting range (incremental)	24–bit plus sign (–16 777 216 to +16 777 215)
	(Absolute)	25–bit (0 to 33 554 431) 12–bit (0 to 4095) 24–bit (0 to 16777215)
	5 VDC differential	
	Max. count frequency	200 kHz
	Input voltage of ”1” signal	Minimum 2.4 VDC
	Input current of ”1” signal	> 3.7 mA
	Input voltage of ”0” signal	Maximum 1.2 VDC
	Input current of ”0” signal	< 1 mA at 1.2 VDC
	24 VDC single–ended	
	Max. count frequency	10 kHz
	Input voltage of ”1” signal	Minimum 11 VDC
	Input current of ”1” signal	> 6 mA
	Input voltage of ”0” signal	–3 ... +5 VDC
	Input current of ”0” signal	< 2 mA at <= 5 VDC

Width: 178 mm
Height: 216 mm

Discrete Outputs	Output type	Solid–state
	Supply voltage range	20 ... 24 ... 30 VDC
	Number of outputs	4
	Output voltage	0.5 V
	Number of groups	2
	Current load	0.5 A max./output
	Type of signal	True high
	Leakage current	< 0.5 mA at 24 VDC
	Voltage drop in on–state	< 0.5 V DC at 0.5 A
	Overload protection	Outputs are protected against overload and short circuit (see below).
	Fault display	1 red LED per output (row 3) as short circuit/overload indicator
	Error message	Error message (I/O error) to the communications adapter if the module is defective (I/O base self–test)
	Output delay with resistive load	0.1 ms max. 0 –> 1 0.1 ms max. 1 –> 0
	Maximum switching cycles	1 000/h with inductive load 100/s with resistive load 8/s with 2.4 W bulb load
	Configurable functions	Refer to Chapter 4, page 57
Clock Outputs for Absolute Encoders	Output type	5 VDC differential (RS–422)
	Output voltage of ”1” signal	>+/– 2 VDC
	Output current of ”1” signal	> 20 mA

The output current of a shortenedoutput is limited to a nondestructive value. The short circuit heats the output driver and the output will switch off. The output will switch on again, if the driver leaves the over–temperature condition. If the short circuit still exists, the driver will reach the over–temperature condition again and will switch off again. As long as an output is overloaded the green LED is on and the red LED is on.

☞ **Note:**
An output load of at least 1 kOhm is necessary when the Q1 and/or Q3 outputs are utilized for frequency output.

Potential isolation from one another and PE	–Discrete I/O signals, –Counter inputs, –Clock outputs, –Supply voltage	500 VAC for 1 min.
Fusing	Internal	None
	External: L+ supply voltage	315 mA fast–blow
	External: 1L+ sensor– and actuator supply	In accordance with the designed power consumption of the connected sensors and actuators, but max. 5 A fast–blow
	External: 2L+ encoder / transmitter supply	In accordance with the designed power consumption of the connected encoders, but max. 1 A fast–blow
EMC in Industrial Use	Noise immunity	IEC 1131 Surge voltage in the mains supply 500 V, 12 Ohm
	Emissions	EN 50081–2
	Approvals	UL, CUL, CSA, CE,
Mechanical Design	Width	125 mm
	Depth (without an adapter)	40 mm
	Height	141.5 mm without or with 1–row busbar 159.5 mm with 2–row busbar 171.5 mm with 3–row busbar
	Weight	240 g

Width: 178 mm
Height: 216 mm

Counter Configuration

4

Together with a communication adapter or processor adapter, the 170 AEC 920 00 I/O base comprises a fully functional TSX Momentum System module. A bit–level explanation of output word functions is follows.

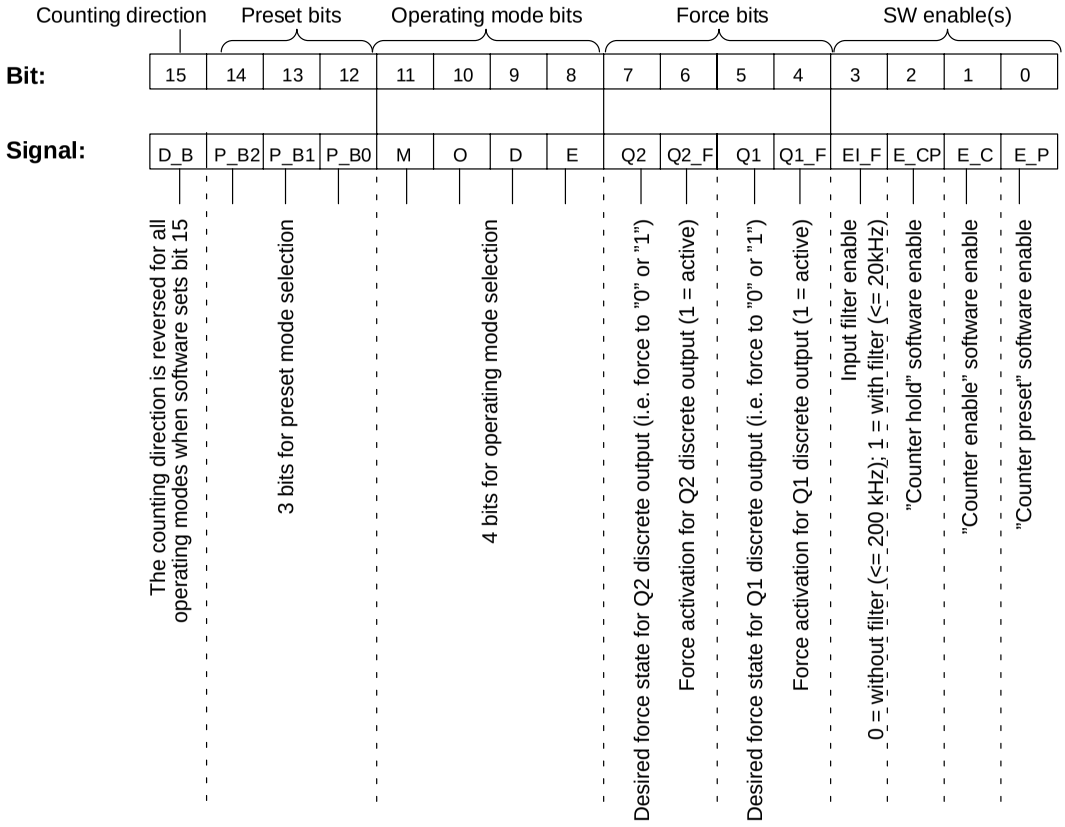
Settings for counter functions, output configuration, and counter channel preset values are made through output word parameters. This is accomplished for the two counters through the following output words:

Output word	Function High byte	Low byte
1	Counter 1 configuration bits	
2	Counter 2 configuration bits	
3	Counter 1 output configuration	Counter 1 command data code no.
4	Counter 2 output configuration	Counter 2 command data code no.
5	Counter 1 command data values (bits 0 ... 15)	
6	Counter 1 command data values (bits 16 ... 31)	
7	Counter 2 command data values (bits 0 ... 15)	
8	Counter 2 command data values (bits 16 ... 31)	

Width: 178 mm
Height: 216 mm

4.1 Configuration of Output Words 1 and 2

The following counter 1 functions are specified through output word 1:



After SSI encoder direction reversal, a transfer of the preset value and software limit switch values must be repeated.

Output word 2 specifies these same functions for counter 2 (relating however to Q3/Q4 discrete outputs instead of Q1/Q2).

4.1.1 Software Enable(s) and Filter Activation (Output words 1/2, (bits 0 ...4))

These bits can enable the following functions:

D0 = E_P
1 = Preset value enable. Preset value acceptance requires the E_P SW enable bit and an 0–>1 edge at the I1/I4 hardware input.

D1 = E_C
1 = Counter enable. To be enabled, the counter requires the E_C SW enable bit and a ”1” signal on the I2/I5 hardware input .

D2 = E_CP
1 = Counter hold enable (capture). Holding of the counted value given to the PLC requires the E_CP SW enable bit and an edge at the I3/I6 hardware input. This held counted value continues to be transferred to the PLC as the actual value until the E_CP bit is reset by software. Transfers of the counter’s true current actual value are reinstated after reset. Pulses at the counter inputs continue to be registered internally by the counter during counter hold enable.

D3 = EI_F
1 = Counter input filter activation. Input filter activation limits the counter input frequency to < 20 kHz.

☞ **Note:**
Filter activation is necessary to suppress noise disturbances with 24 VDC single–ended pulse generators.

Width: 178 mm
Height: 216 mm

4.1.2 Force the Discrete Outputs (Output words 1/2, (bits 4... 7)

The discrete outputs can be turned on or off (forced) by the PLC, independent of the assigned counter function.

D4 = Q1_F
1 = Force the Q1 discrete output. D5 determines the Q1 output state.

D5 = Q1
This bit contains the desired force state for Q1 discrete output.
0 = Output inactive, 1 = output active (24 VDC).

D6 = Q2_F
1 = Force the Q2 discrete output. D7 determines the Q2 output state.

D7 = Q2
This bit contains the desired force state for Q2 discrete output.
0 = Output inactive, 1 = output active (24 VDC).

4.1.3 Operating Mode Bits 8 ... 11 (output words 1/2)

Operating mode (hex)	Bits 11– 10– 9– 8	Trans. type *)	Function
0	0 0 0 0		Channel not ready, parameters not reset, outputs = 0
1	0 0 0 1	Pul	Down–counter
2	0 0 1 0	Pul	Up–counter
3	0 0 1 1		Corresponds to operating mode ”0”
4	0 1 0 0	Inc	Up/down counter, position sensing, x1 counting
5	0 1 0 1	Inc	Up/down counter, position sensing, x4 counting
6	0 1 1 0	Pul	Differential counter: A counter input = forward; B counter input = backward
7	0 1 1 1	Pul	Up/down counter: A counter input = up; B counter input = down (1 = up, 0 = down)
8	1 0 0 0	Pul	Pulse counter with external time base (e.g. for rotary speeds, flow rates etc.) a) with an external clock as time base to the B counter input or b) (Q1/Q3) frequency output as time base to the B counter input
9	1 0 0 1	Pul	Period meter with 5 time bases for full or half periods; 0 = without time base full period:, 1 = 1 , 2 = 10, 3 = 100, 4 = 1 000, 5 = 10 000 [µs]; half period: 9 = 1, A = 10, B = 100, C= 1 000, D = 10 000 [µs]
A	1 0 1 0	Pul	Frequency meter with 5 time bases for full or half periods; 0 = without time base full period: 1 = 0.1 , 2 = 1, 3 = 10, 4 = 100, 5 = 1 000 [ms]; half period: 9 = 0.1, A = 1, B = 10, C= 100, D = 1 000 [ms]
B	1 0 1 1		Corresponds to operating mode ”0”
C	1 1 0 0	Abs	Position sensing with single-turn encoders (SSI), 12–bit resolution
D	1 1 0 1	Abs	Position sensing with multi-turn encoders (SSI), 24–bit resolution
E	1 1 1 0	Abs	Position sensing with multi-turn encoders (SSI), 25–bit resolution
F	1 1 1 1		Software reset. This always resets both counters, regardless of whether this operating mode has been invoked for counter 1 or 2.

Width: 178 mm
Height: 216 mm

4.1.4 Preset Modes (Output words 1/2, (bits 12 ... 14)

Preset values are entered through the respective hardware inputs (I1 for counter 1, I4 for counter 2). When no preset value is transferred from the PLC, a default preset value of 0 is placed in the counter.

☞ **Note:**
The corresponding SW enable must be set.

Bits:	14	13	12	Function
Hex: 0	0	0	0	The preset value is entered when the SW enable bit E_P = ”1” signal (the I1/I4 hardware input is functionless)
Hex: 1	0	0	1	The preset value is entered by a 0/1 edge at the I1/I4 hardware input (refer to Figure 9) *
Hex: 2	0	1	0	The preset value is entered by a 1/0 edge at the I1/I4 hardware input. *
Hex: 3	0	1	1	The preset value is entered by a ”1” signal at the I1/I4 hardware input, halting further counting. The counter resumes when the I1/I4 hardware input = ”0” signal (refer to Figure 10) *
Hex: 4	1	0	0	The preset value is entered by a 0/1 edge (for count up) and a 1/0 edge (for count down) at the I1/I4 hardware input. Used for axis control. *
Hex: 5	1	0	1	The preset value is entered by a 1/0 edge (for count up) and a 0/1 edge (for count down) at the I1/I4 hardware input. *
Hex: 6	1	1	0	Reference point with short cam signal (refer to Chapter 4.1.6, page 65) *
Hex: 7	1	1	1	Reference point with long cam signal (refer to Chapter 4.1.6, page 65) *

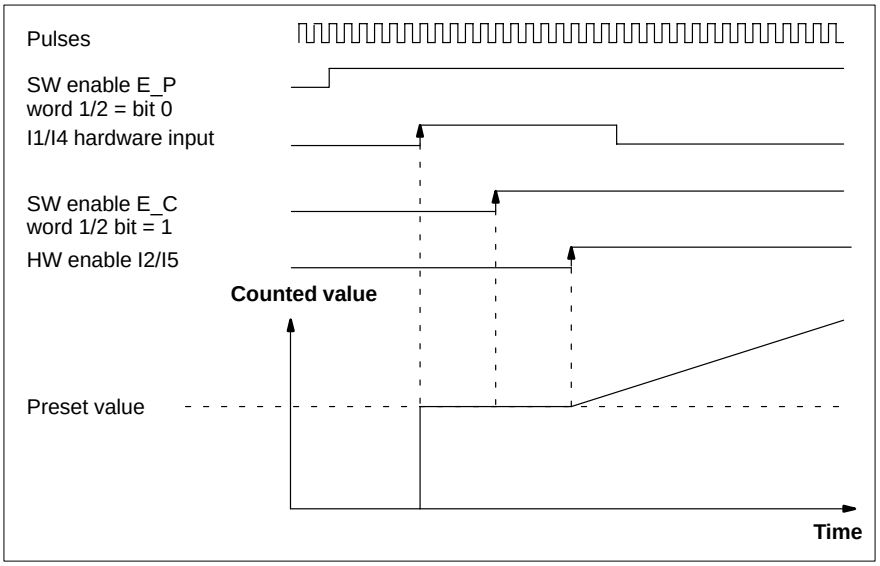
*) Only while SW enable bit E_P = ”1” signal.

4.1.5 Counting Direction Reversal

D15 = D_B
The counting direction is reversed for all operating modes when software sets bit 15.

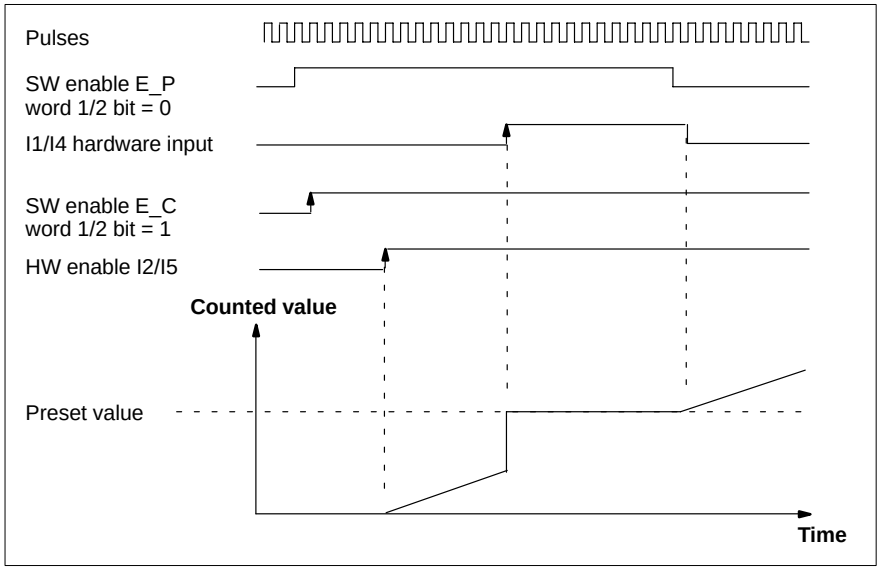
Caution:
After SSI encoder direction reversal, a transfer of the preset value and software limit switch values must be repeated.

Figure 9 Demonstration of preset mode 1 hex



Width: 178 mm
Height: 216 mm

Figure 10 Demonstration of preset mode 3 hex



4.1.6 Preset Value Acceptance for Short Cams

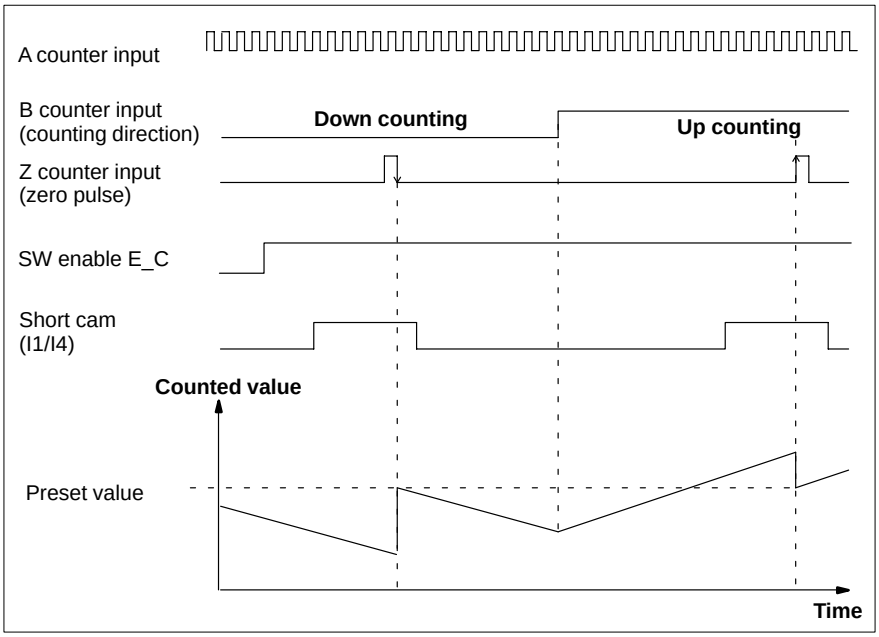
The preset value is entered when the SW enable bit E_P and I1/I4 hardware input both have ”1” signal, and a zero pulse is on the Z counter input.

This function can be used in those cases where the encoder provides only a single zero pulse over the cam length. Entry takes place on the zero pulse falling edge for down counters, and rising edge for up counters (refer to Figure 11). For incremental encoders entry always takes place on the zero pulse rising edge, since the zero pulse always coincides with a ”1” signal at the B counter input.

☞ **Note:**
Should the encoder provide several zero pulses during the cam signal, the counter is set to the preset value with each zero pulse.

The following timing diagram explains counter setting to the preset value with the short cam signal.

Figure 11 Short cam function



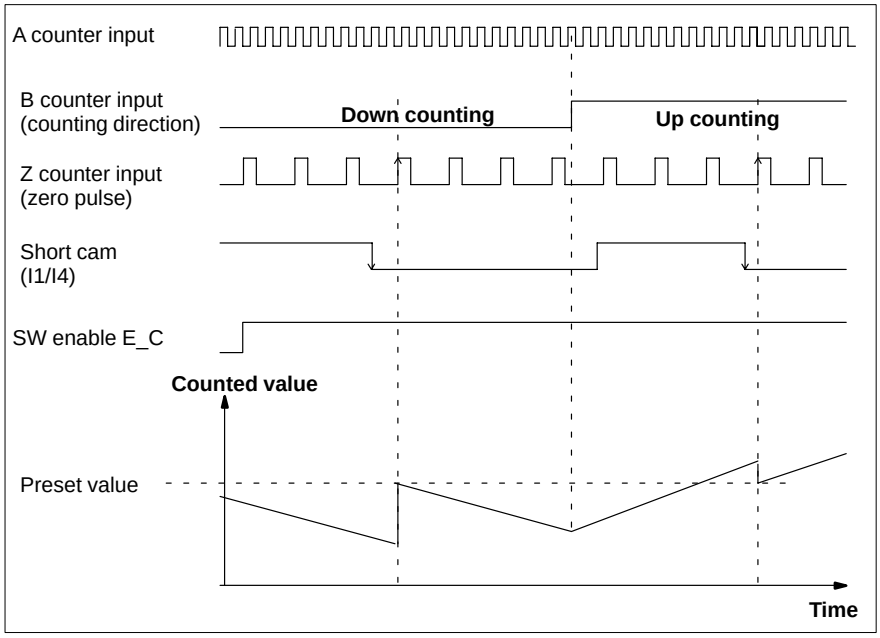
Width: 178 mm
Height: 216 mm

4.1.7 Preset Value Acceptance for Long Cams

Preset value entry takes place at the first rising edge of the zero pulse on the Z counter input, which follows an I1/I4 hardware input falling edge. Entry also requires the SW enable bit E_P to be set.

☞ **Note:**
Subsequent zero pulses have no effect.

The following timing diagram explains counter setting to the preset value with the long cam signal.



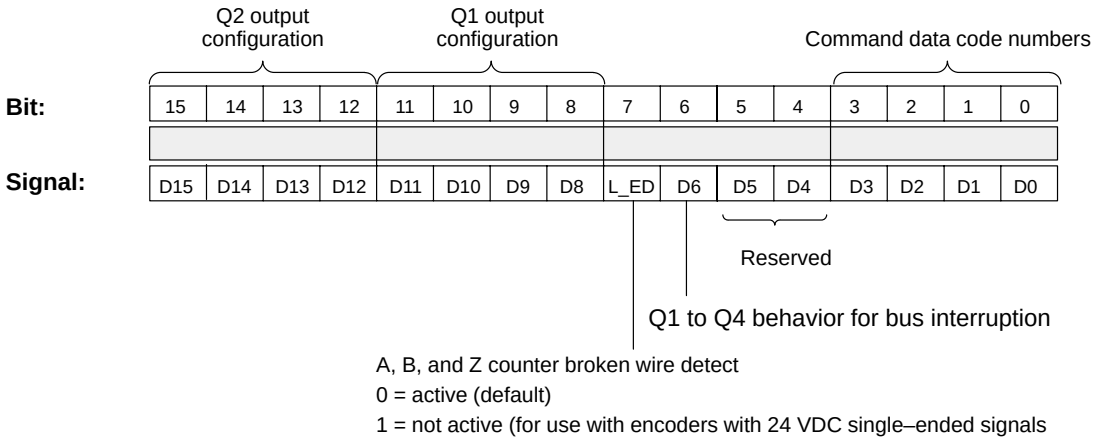
4.2 Configuration of Output Words 3 and 4

Output word 3 specifies the following functions for counter 1; output word 4 provides similiar functionality for counter 2.

4.2.1 Output Word 3

The following counter 1 functions are specified through output word 3:

- The significance of the parameters transferred through words 5 and 6 is determined by the command data code numbers (D0 ... D3).
- D4 and D5 are reserved
- D4 and D5 are reserved
- D6, D7 specify module behavior for bus interruption and counter input line breakage
- Output configuration for the Q1 discrete output (D8 ... D11)
- Output configuration for the Q2 discrete output (D12 ... D15)

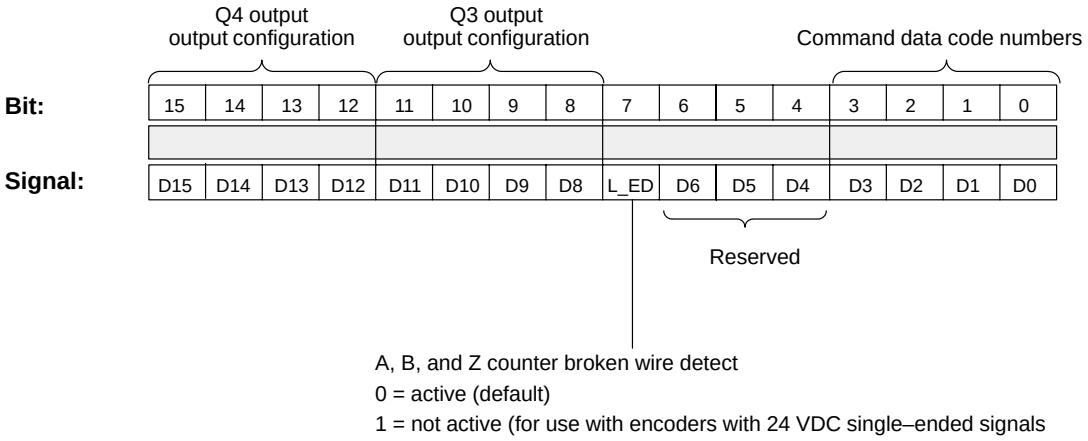


Width: 178 mm
Height: 216 mm

4.2.2 Output Word 4

The following counter 2 functions are specified through output word 4:

- The significance of the parameters transferred through words 7 and 8 is determined by the command data code numbers (D0 ... D3).
- D4, D5, and D6 reserved
- D7 specify counter 2 behavior for counter input line breakage
- Output configuration for the Q3 discrete output (D8 ... D11)
- Output configuration for the Q4 discrete output (D12 ... D15)



4.2.3 Command Data Code Numbers (Output words 3/4, (bits 0 ... 4))

By making use of the code numbers, different command data types can be transferred to the module. The functions are identical for output words 3 and 4, whereby the discrete outputs apply to the respective counter. In detail these are:

Code number	4	3	2	1	0	Function
Hex: 0	0	0	0	0	0	No code number selected
Hex: 1	0	0	0	0	1	Code number for preset value or SSI offset value
Hex: 2	0	0	0	1	0	Code number for threshold value 1 *)
Hex: 3	0	0	0	1	1	Code number for threshold value 2 *)
Hex: 4	0	0	1	0	0	Code number for upper software limit switch *) (outputs are disabled when counting pulses >= value)
Hex: 5	0	0	1	0	1	Code number for lower software limit switch *) (outputs are disabled when counting pulses >= value)
Hex: 6	0	0	1	1	0	Code number for counter 1 and 2 discrete output (Q) pulse width in ms
Hex: 7	0	0	1	1	1	Code number for modulo value of repetitive counters; function disabled by modulo value = 0.
Hex: 8	0	1	0	0	0	Code number for time base of counter operation mode ”period meter” (Mode 9) (Output words 1/2, bits 8...11)
Hex: 9	0	1	0	0	1	Code number for time base of counter operation mode ”frequency meter” (Mode A) (Output words 1/2, bits 8...11)
Hex: A	0	1	0	1	0	Code number for operating mode 8 (pulse counter with time base) (Output words 1/2, bits 8 ...11)
Hex: B	0	1	0	1	1	Code number for time base in ms of (half period) pulse on Q1/Q3 discrete outputs
Hex: C	0	1	1	0	0	Reserved
Hex: D	0	1	1	0	1	Reserved (corresponds to code number 0)
to F	0	1	1	1	1	

*) A HW or SW reset must be carried out to disable the functions. The ”0” value is a permissable parameter and does not deactivate these functions.

Width: 178 mm
Height: 216 mm

Default Values
If there are no command data defined (no code number chosen in output words 3/4, bits 0 ... 4) then the following command data default values are assigned:

Function	Default values
Preset value or SSI offset value	0
Threshold values 1 and 2	Inactive
Upper and lower software limit switches	Inactive
Pulse width of discrete outputs in ms	Value = 0; no output pulses
Modulo value	Value = 0; function inactive
Period and frequency meter	Without time base
Pulse counter mode	Full period
Pulse counter with time base in ms	Without time base
Transmitter line breakage monitoring	Active
Q discrete outputs	Inactive

D5 (output words 3/4)
Bit D5 is not currently used.

D6 = CLOA (output words 3/4)
This bit determines whether after an interruption of communications the outputs are to be disabled (CLOA = 0), or further operated by the module (CLOA = 1). This function can only be parameterized in the counter 1 output word, but is effective for both counter channels.

D7 = L_ED (output words 3/4)
The open–circuit monitoring of the counter inputs can be disabled with this bit. The meanings are:
0 = open–circuit monitoring active
1 = open–circuit monitoring disabled
In mode 1 and 2 (up and down counter) only the differencial 5 V inputs A+ and A– are line fault detected.
In mode C, D and E (absolut encoder) only the differencial 5 V inputs A+ and A– are line fault detected.
In all other modes (4, 5, 6, 7, 8, 9, A) all differential inputs A, B and Z are line fault detected.
If 24 V signle ended signals are used, the line fault detection have to disabled, or the error bits L_E have to be ignored.
If line fault detection is desired, the unused differential inputs have to be connected to the 5 V encode supply.

⚠ **Caution:**
The L_ED bit must be set for encoders with 24 VDC single–ended signals, disabling the open–circuit monitoring.

4.2.4 Discrete Output Configuration (Output words 3/4, (bits 8...15))

The discrete outputs can be assigned various functions; each output having 4 configuration bits for this purpose.

- Q1 output of counter 1 = bits 8 ... 11 in word 3
- Q2 output of counter 1 = bits 12 ... 15 in word 3
- Q3 output of counter 2 = bits 8 ... 11 in word 4
- Q4 output of counter 2 = bits 12 ... 15 in word 4

Width: 178 mm
Height: 216 mm

Discrete Output Functions (Output words 3/4, (bits 8...15))
The functions contained in the following table can be assigned to the discrete outputs:

Bits:	**11**	**10**	**9**	**8**	**Function (control of counter 1 Q1/Q3 discrete outputs)**
Bits:	**15**	**14**	**13**	**12**	**Function (control of counter 2 Q2/Q4 discrete outputs)**
Hex: 0	0	0	0	0	Outputs remain at ”0” signal
Hex: 1	0	0	0	1	The output is set to ”1” signal and remains set when the counted value = threshold value 1
Hex: 2	0	0	1	0	The output is set to ”1” signal and remains set when the counted value = threshold value 2
Hex: 3	0	0	1	1	The output is set to ”1” signal at counter enable, and returns to ”0” when the counted value = threshold value 1 (retentive)
Hex: 4	0	1	0	0	The output is set to ”1” signal at counter enable, and returns to ”0” when the counted value = threshold value 2 (retentive)
Hex: 5	0	1	0	1	The output is set to ”1” signal when the counted value = threshold value 1 (retentive). The output is set to ”0” signal when the counted value = threshold value 2 (retentive).
Hex: 6	0	1	1	0	The output is set to ”1” signal when the counted value >= threshold value 1. The output is set to ”0” signal when the counted value < threshold value 1.
Hex: 7	0	1	1	1	The output is set to ”1” signal when counter enabled and counted value < threshold value 1. The output is set to ”0” signal when the counted value >= threshold value 1.
Hex: 8	1	0	0	0	The output is set to ”1” signal when the counted value >= threshold value 2. The output is set to ”0” signal when the counted value < threshold value 2.
Hex: 9	1	0	0	1	The output is set to ”1” signal when counter enabled and counted value < threshold value 2. The output is set to ”0” signal when the counted value >= threshold value 2.
Hex: A	1	0	1	0	The output is set to ”1” signal when the counted value >= threshold value 1. The output is set to ”0” signal when the counted value >= threshold value 2.
Hex: B	1	0	1	1	Initiate a pulse when counted value = threshold value 1; pulse length is definable (1 ... 2 EXP 32 ms)
Hex: C	1	1	0	0	Initiate a pulse when counted value = threshold value 2; pulse length is definable (1 ... 2 EXP 32 ms)
Hex: D	1	1	0	1	Frequency output (only Q1/Q3 discrete outputs), a frequency must also be specified through the code number B
Hex: E	1	1	1	0	Reserved value (same as 0 hex, no acknowledgement to the communications adapter)
Hex: F	1	1	1	1	

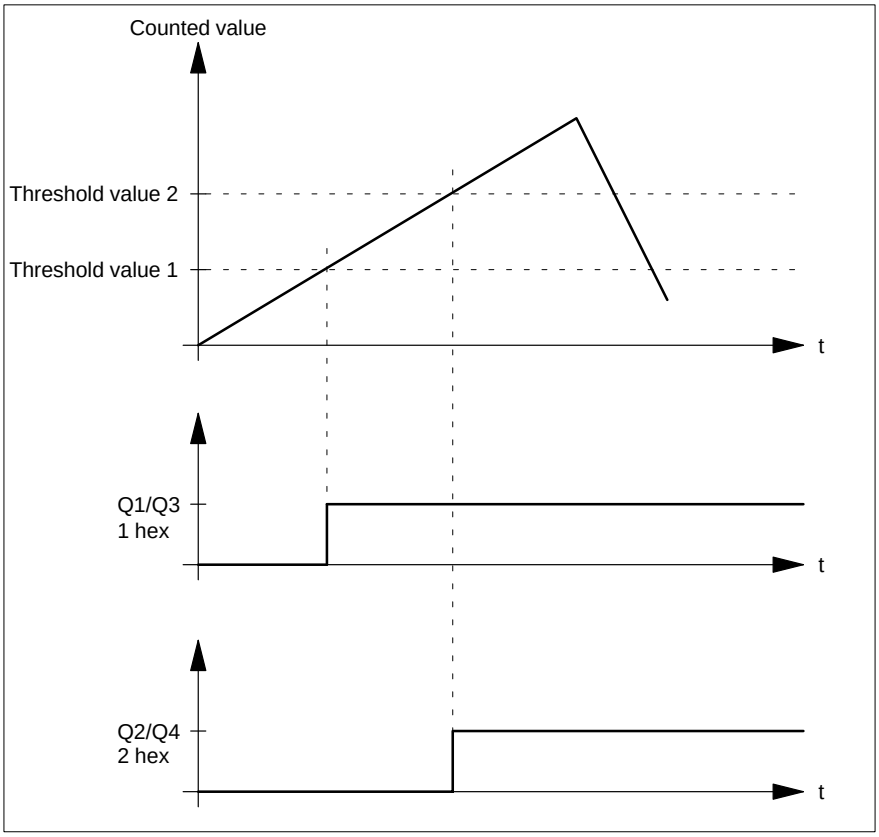
4.2.5 Timing Diagrams for Discrete Output Operation

Various output configurations for the Q1/Q3 and Q2/Q4 outputs can be found in the following timing diagrams.

1 hex and 2 hex output behavior
The Q1/Q3 output is set to ”1” signal and remains stored when the counted value = threshold value 1 (1 hex).

The Q2/Q4 output is set to ”1” signal and remains stored when the counted value = threshold value 2 (2 hex).

Figure 12 Function: 1 hex and 2 hex

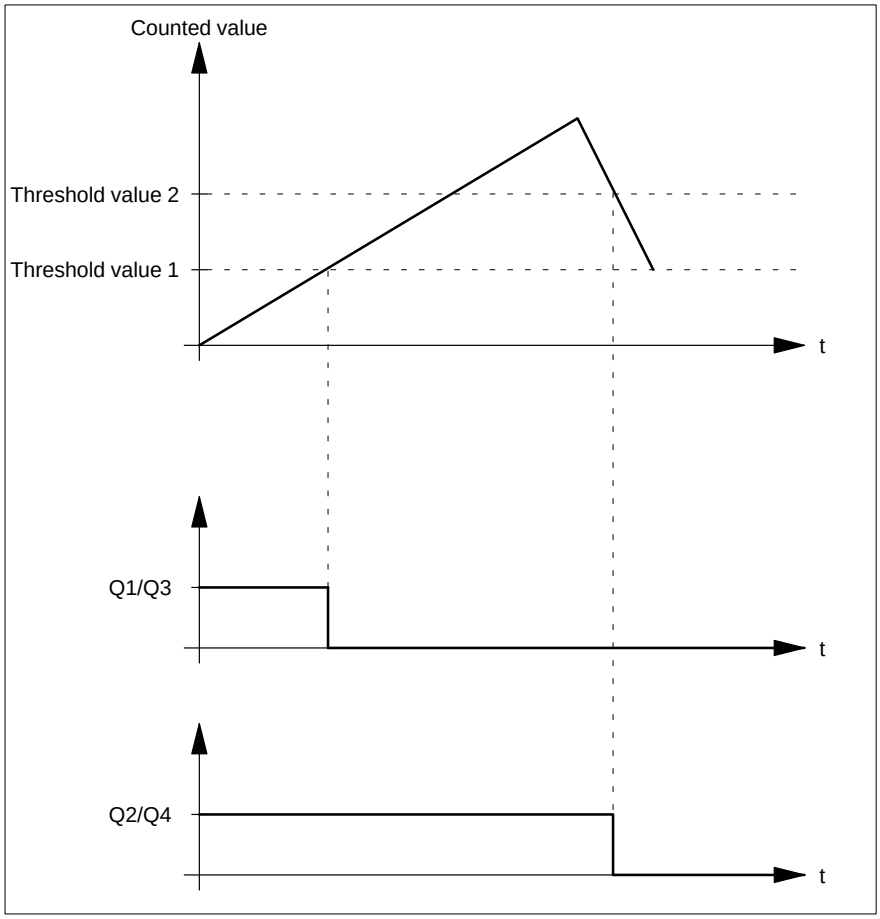


Width: 178 mm
Height: 216 mm

3 hex and 4 hex output behavior
The Q1/Q3 output is set to ”1” signal at counter enable, and returns to ”0” when the counted value = threshold value 1 (retentive).

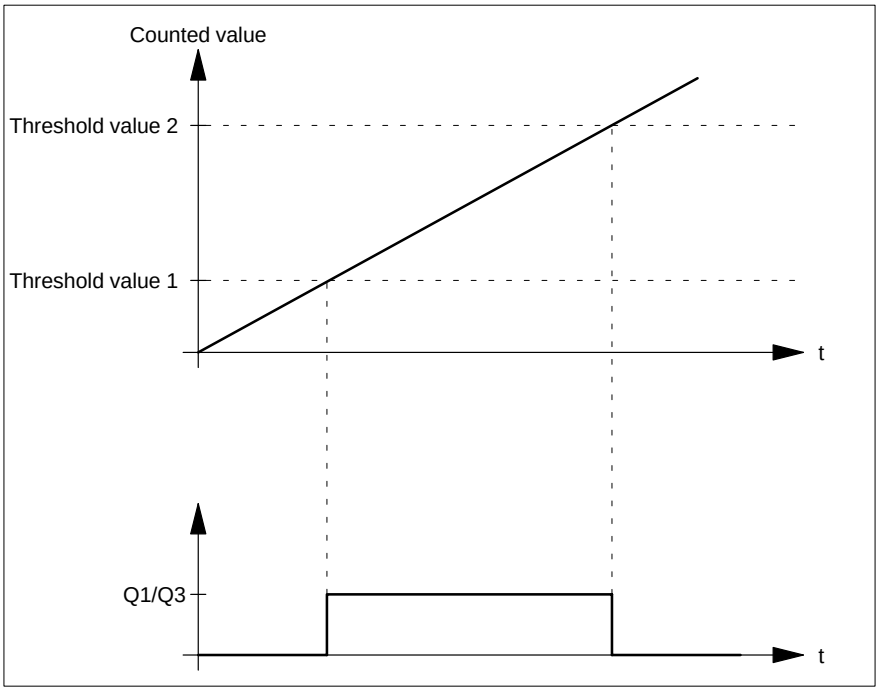
The Q2/Q4 output is set to ”1” signal at counter enable, and returns to ”0” when the counted value = threshold value 2 (retentive).

Figure 13 Function: 3 hex and 4 hex



5 hex output behavior
The Q1/Q3 output is set to ”1” signal when the counted value = threshold value 1 (retentive). The Q1/Q3 output is set to ”0” signal when the counted value = threshold value 2 (retentive).

Figure 14 Function: 5 hex

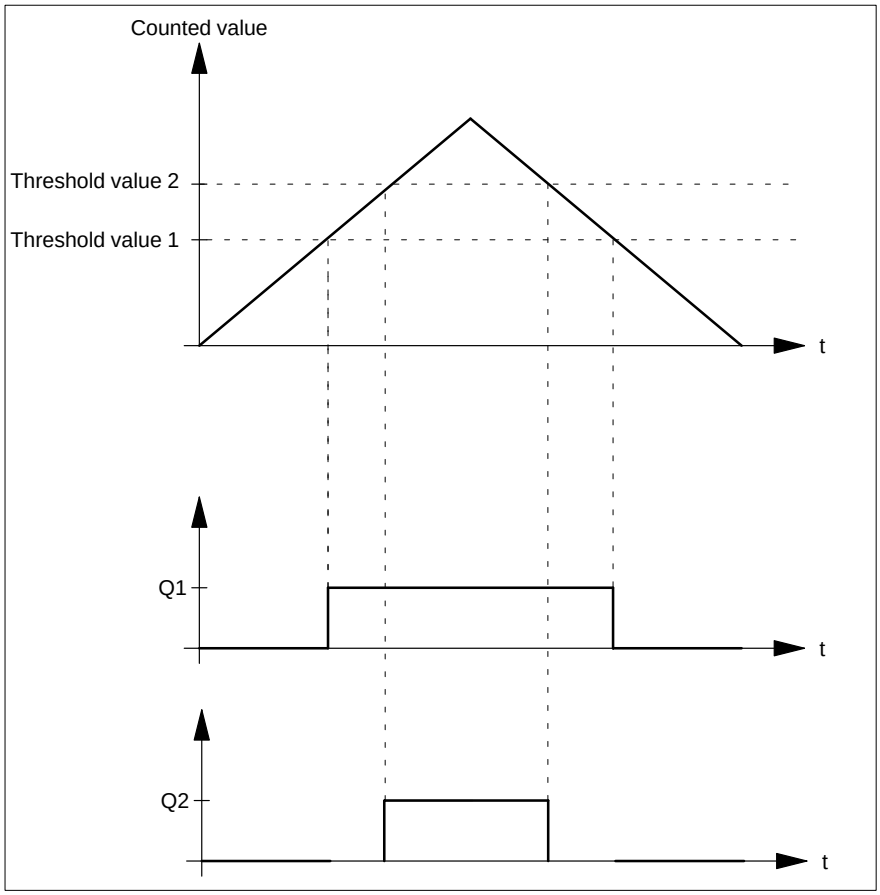


Width: 178 mm
Height: 216 mm

6 hex and 8 hex output behavior
The Q1 output is set to ”1” signal when the counted value >= threshold value 1.
The Q1 output is set to ”0” signal when the counted value < threshold value 1.

The Q2 output is set to ”1” signal when the counted value >= threshold value 2.
The Q2 output is set to ”0” signal when the counted value < threshold value 2.

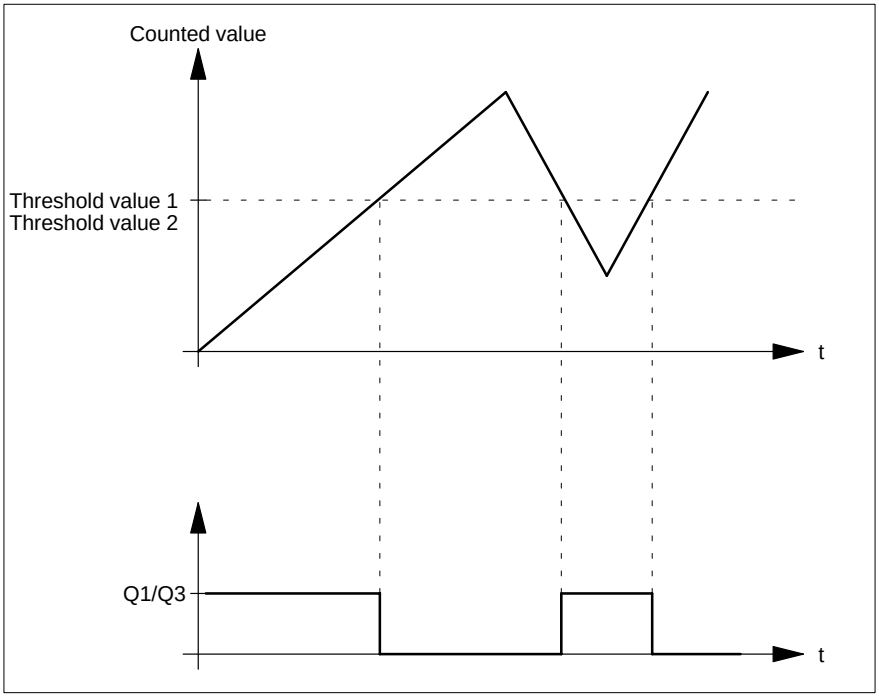
Figure 15 Function: 6 hex and 8 hex



7 hex and 9 hex output behavior
The Q1/Q3 output is set to ”1” signal when the counter is enabled and counted value < threshold value 1. The Q1/Q3 output is set to ”0” signal when counted value >= threshold value 1.

The Q1/Q3 output is set to ”1” signal when the counter is enabled and counted value < threshold value 2. The Q1/Q3 output is set to ”0” signal when counted value >= threshold value 2.

Figure 16 Function: 7 hex and 9 hex

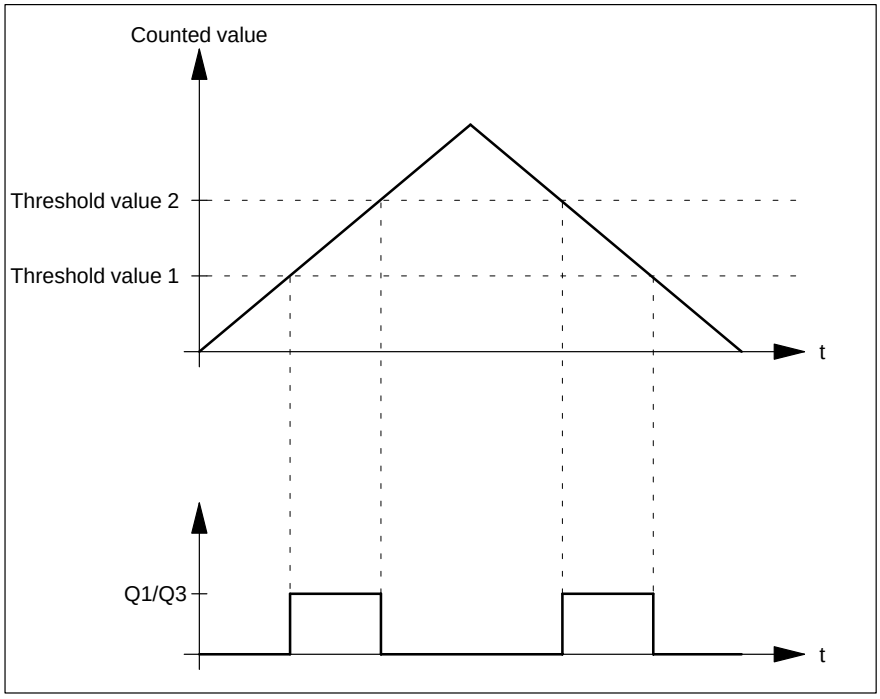


Width: 178 mm
Height: 216 mm

A hex output behavior

The Q1/Q3 output is set to ”1” signal when the counted value >= threshold value 1. The Q1/Q3 output is set to ”0” signal when the counted value >= threshold value 2.

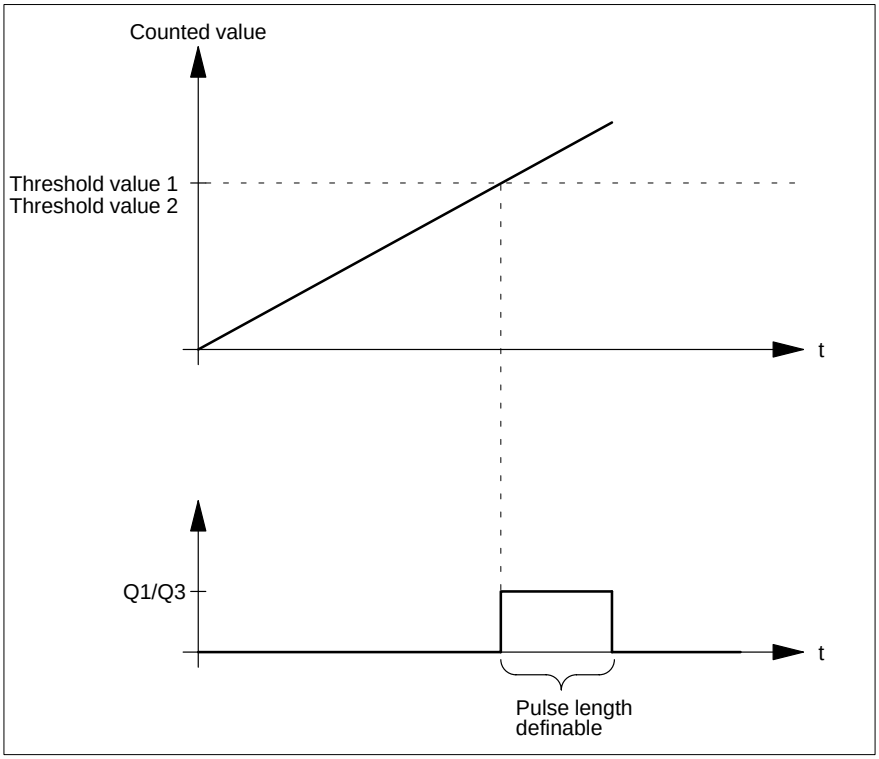
Figure 17 Function: A hex



B hex and C hex output behavior

Initiate a pulse when counted value = threshold value 1; pulse length is definable (1 ... 2 EXP 32 ms).

Figure 18 Function: B hex and C hex



Width: 178 mm
Height: 216 mm

Priorities
The following priorities apply to the setting of discrete outputs:

Highest priority	**A force through the PLC**
	**Frequency output active (D hex)**
	Software limit switches (min., max.)
Lowest priority	**Software configuration for threshold values 1 and 2**

4.3 Code Numbers and Meaning of the Parameters (Output Words 5/6 and 7/8)

Set points are handled in output words 5 and 6 (for counter 1), and in words 7 and 8 (for counter 2). Since only two words (one double word) are availible for each counter, the meaning of the set point is determined by their allocation to a particular code number.

Every set point must be sent in a data frame from the master to the I/O base. This can be done, for instance, using a function block. The code numbers are returned to the PLC during the parameterization. If the associated code number is indicated in the PLC, the next parameter and associated code number can be sent to the module.

- The code number for counter 1 is located in output word 3 (HEX 0)
- The code number for counter 2 is located in output word 4 (HEX 0)

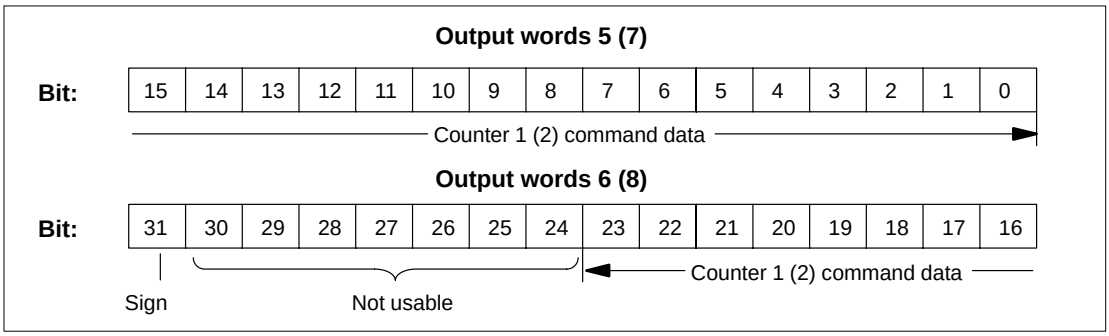
Code number refers to register 3/4, bits 0 ... 4	**Function** **This data is entered into output words 5/6 and 7/8**
Hex: 0	No command data value selected
Hex: 1	Preset value (24–bit + sign) or SSI offset value (max. encoder resolution)
Hex: 2	Threshold value 1 (24–bit + sign for inc. encoder; 25–bit for abs. encoder)
Hex: 3	Threshold value 2 (24–bit + sign for inc. encoder; 25–bit for abs. encoder)
Hex: 4	Counter 1 upper software limit switch (24–bit + sign for inc. encoder; 25–bit for abs. encoder)
Hex: 5	Counter 2 lower software limit switch 24–bit + sign for inc. encoder; 25–bit for abs. encoder)
Hex: 6	Q1/Q2 discrete outputs pulse width (1 .. 2 EXP 32 ms)
Hex: 7	Event counter (repetitive counter) modulo value (max. 24–bit); function disabled by modulo value = 0
Hex: 8	Time base for ”period meter” counter operation mode (operating mode 9 as found in output word 1/2, bits 8 ... 11) 0 = without time base: full period: 1 = 1 , 2 = 10, 3 = 100, 4 = 1 000, 5 = 10 000 (in microsec.); half period: 9 = 1, A = 10, B = 100, C= 1 000, D = 10 000 (in microsec.). Transfer of any other values sets the P_E bit and returns code number 1F.
Hex: 9	Time base for ”frequency meter” counter operation mode (operating mode A as found in output word 1/2, bits 8 ... 11) 0 = without time base: full period: 1 = 0.1 , 2 = 1, 3 = 10, 4 = 100, 5 = 1 000 (in ms); half period: 9 = 0.1, A = 1, B = 10, C= 100, D = 1 000 (in ms) Transfer of any other values sets the P_E bit and returns code number 1F.
Hex: A	Full/half period selection for pulse counter with time base (operating mode 8 as found in output word 1/2, bits 8 ... 11) (0 = unauthorized, sets the P_E bit 1 = full period, 2 = half period at the corresponding Bx counter input)
Hex: B	Clock output time base (1 .. 2 EXP 32 ms) only (half period) pulses on Q1/Q3 discrete outputs
Hex: C	Reserved
Hex: D to F	Reserved values (corresponds to code number 0)

Counter 1 code numbers are in output word 3

4.4 Command Data Format

4.4.1 Incremental Encoder Command Data

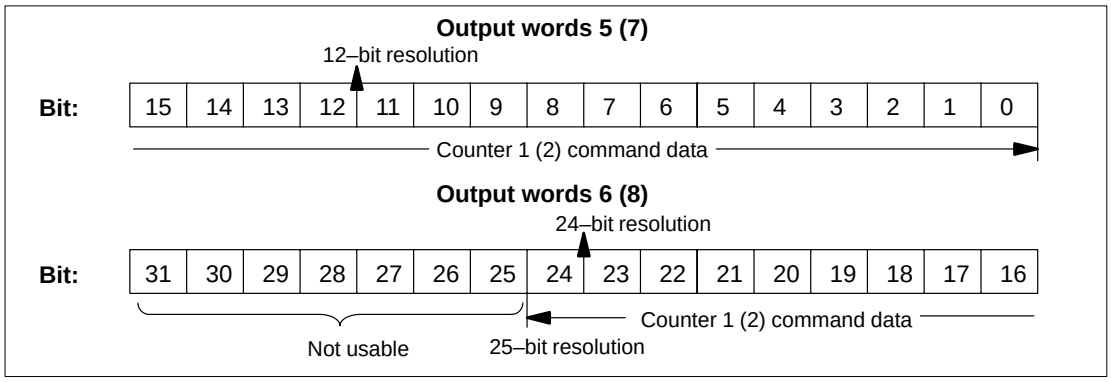
- The command data resolution is 24–bit + sign (–16 777 216 to +16 777 215).
- Modulo values only have a 24–bit unsigned resolution (0 to +16 777 215).



Width: 178 mm
Height: 216 mm

4.4.2 Absolute Encoder Command Data

Maximum command data resolution is 25–bit unsigned (0 to +33 554 431). This depends upon encoder resolution (from 0 to 4 095 for 12–bits; from 0 to 16 777 215 with 24–bits).



Status Information and Counted Values

5

Status information and counted values are transferred from the counter module to the PLC in 8 input words. The following data structure applies for both counter channels:

Input word	Function	
	High byte	**Low byte**
1	Counter 1 status bits	Counter 1 error bits
2	Counter 2 status bits	Counter 2 error bits
3	Reported counter 1 current status	Returned counter 1 code number
4	Reported counter 2 current status	Returned counter 2 code number
5	Counter 1 current counted value (bits 0 ... 15)	
6	Counter 1 current counted value (bits 16 ... 31)	
7	Counter 2 current counted value (bits 0 ... 15)	
8	Counter 2 current counted value (bits 16 ... 31)	

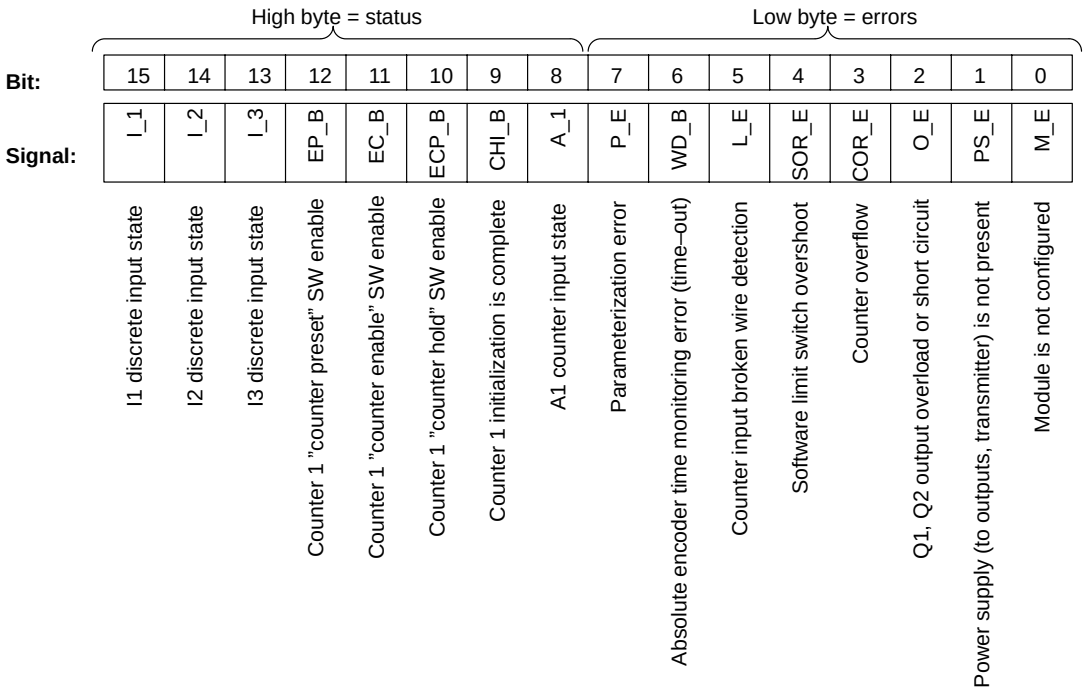
Width: 178 mm
Height: 216 mm

5.1 Status and Error Bits (Input Words 1 and 2)

Through the status bits, the counter is able to provide error messages and the current states of hardware inputs and associated software enable(s).

Counter 1 status information and error messages are transferred to the PLC in input word 1. The individual bits have the following significances:

Counter 2 status information and error messages are transferred to the PLC in input word 2. The significance of status and error bits correspond to word 1.



5.1.1 Error Bits (Low Byte) (Input words 1/2, (bits 0 ... 7))

The following errors can be reported with these bits:

D0 = M_E
1 = The module has not been configured, i.e. there has been no valid operating mode conveyed. This bit is set after a HW or SW reset.

D1 = PS_E
1 = Power supply to the discrete outputs or sensors is absent.

D2 = O_E
1 = A short circuit or overload has occurred on the discrete outputs.

D3 = COR_E
1 = The maximum permissable counting range has been exceeded. The bit can only be reset by a 0–>1 edge of the E_C SW enable bit. This function is inactive for absolute encoders.

D4 = SOR_E
1 = A SW limit switch setting has been exceeded. The discrete outputs are disabled by the error message. Once the counted value is again within the SW limit switch values, outputs assume their former state and the SOR_E bit is reset.

D5 = L_E
1 = Broken wire has occurred on the A, B, or Z counter inputs. Only the A counter input of absolute encoders is monitored.

D6 = WD_E
1 = The time monitoring for encoder absolute data transfer has tripped. This fault occurs for broken wire or with erroneously parameterized encoder resolution. The bit can only be reset by a 0–>1 edge of the E_C SW enable bit.

Width: 178 mm
Height: 216 mm

D7 = P_E
1 = Faulty counter 1 parameterization.
Causes might be:

- An unauthorized operating mode 3 or B.
- One channel is parameterized for an incremental encoder, the other for an absolute encoder.
- An incorrect output configuration has been selected (function E or F for Q1/Q3 output; function D, E, or F for Q2/Q4 output).
- A ”0” time has been chosen with output function D for the Q1/Q3 frequency output.
- An invalid command data code number (D ... 1F) has been selected.
- A valid cycle duration mode has not been chosen (code number A with an invalid value) in operating mode 8 (pulse counter with external time base).
- A valid time base has not been selected (code number 8 with an invalid value) in operating mode 9 (period meter).
- A valid time base has not been selected (code number 9 with an invalid value) in operating mode A (frequency meter).

5.1.2 Status Bits (High Byte) (Input word 1/2, bits 8 ... 15))

The following status can be reported with these bits:

D8 = A_1/A_2
1 = The A1+/A2+ (5 VDC) resp. A1*/A2* (24 VDC) counter input is at ”1” signal

D9 = CHI_B
1 = The counter has been properly configured, i.e. both counters are initialized for either absolute or incremental encoders. A ”0” signal indicates an incorrect operating mode or differing encoder configurations.

D10 = ECP_B
1 = The ”counter hold” SW enable is set.

D11 = EC_B
1 = The ”counter enable” SW enable is set.

D12 = EP_B
1 = The ”counter preset” SW enable is set.

D13 = I3/I6
1 = The ”Hold current count” hardware input is at ”1” signal.

D14 = I2/I5
1 = The ”Counter enable” hardware input is at ”1” signal.

D15 = I1/I4
1 = The ”Accept preset value” hardware input is at ”1” signal.

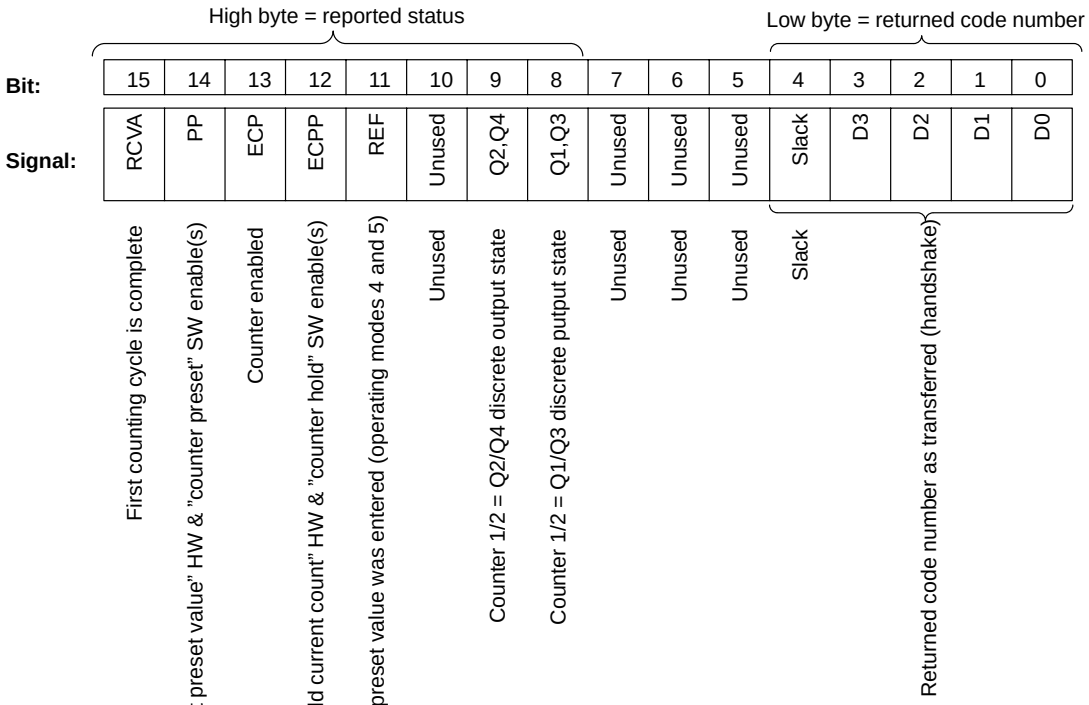
Width: 178 mm
Height: 216 mm

5.2 Status Return Information (Words 3 and 4)

The returned code numbers and reported counter bit–parameter status are transferred to the PLC in input words 3 and 4.

Counter 1 return information is conveyed in input word 3. The individual bits have the following significances:

Counter 2 return information is conveyed in input word 4. The significance of the status return information bits correspond to word 3.



5.2.1 Returned Code Number (Low Byte) (Input words 3/4, bits D0 ... D3)

The configured code numbers previously transferred to the module through output words 3 and 4, are reported back to the PLC through the D0 ... D3 bits. The returned code number serves as a command data transfer handshake (refer to 4.2.3).

☞ **Note:**
Should an invalid code number be conveyed, a 1F hex value is returned in the D0 ... D4 bits and the command data transferred in words 5/6 resp. 7/8 are not utilized by the module.

5.2.2 Reported Status (High Byte) (Input words 3/4, (bits 8 ... 15))

D8 = Q1/Q3
1 = Q1/Q3 discrete output is at ”1” signal.

D9 = Q2/Q4
1 = Q2/Q4 discrete output is at ”1” signal.

D10 = Unused

D11 = REF
1 = The preset value is registered (mode 4 or 5) and the outputs are enabled. There is no presetting necessary to enable outputs in all the other operating modes.
0 = The preset value has not been registered (mode 4 or 5) and the outputs are not enabled, resp. an invalid operating mode has been chosen.

D12 = ECPP
1 = The ”Counter hold” function is activated.

D13 = ECP
1 = The ”Counter enable” function is activated.

D14 = PP
1 = The ”Counter preset” function was executed by the counter.

D15 = RCVA
1 = The first counting cycle in the operating modes 8 (pulse counter), 9 (period meter) or A (frequency meter) is complete.

Width: 178 mm
Height: 216 mm

5.3 Actual Values for Counters 1 and 2 (Input Words 5, 6, 7, and 8)

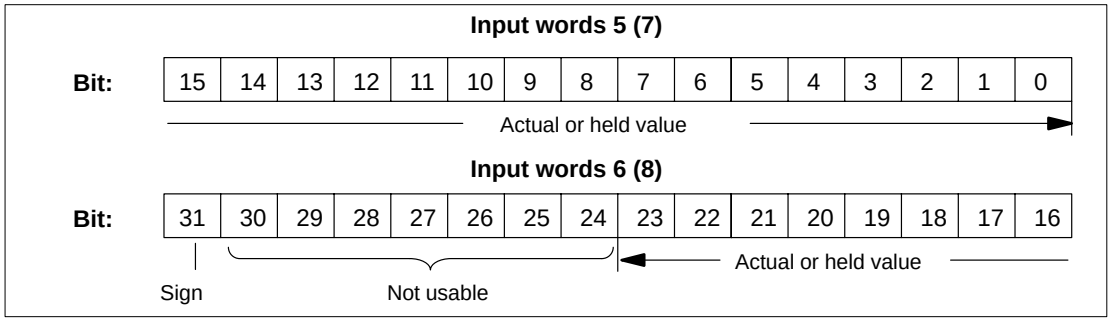
The current encoder values (actual data) are maintained in the input words 5 and 6 (for counter 1), resp. 7 and 8 (for counter 2). Two words (i.e. one double word) are available to each counter for this purpose.

☞ **Note:**
Only the counter's actual values are transferred in the input words 5/6 resp. 7/8. The previously transferred command data values cannot be read back.

Parameter values cannot be returned through the communications adapter.

5.3.1 Current Values for Incremental Encoders

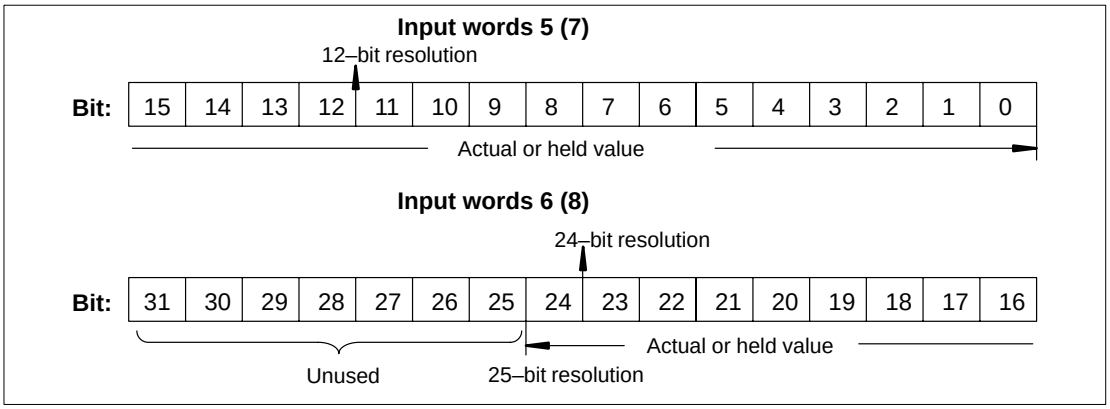
- Actual value resolution is 24–bit + sign (–16 777 216 to +16 777 215).
- Any specified modulo values only have a 24–bit unsigned resolution (0 to +16 777 215).



5.3.2 Current Values for Absolute Encoders (Input words 5, 6, 7, and 8)

Status reporting of current values for absolute encoders is made continuously. The values are maintained in the input words 5 and 6 (for counter 1) and 7 for 8 (for counter 2).The resolution offered:

- for 25 clock cycles – 25–bit unsigned, i.e. from 0 to 33,554,431.
- for 24 clock cycles – 24–bit unsigned, i.e. from 0 to 16,777,215.
- for 12 clock cycles – 12–bit unsigned, i.e. from 0 to 4,095.



Width: 178 mm
Height: 216 mm

Appendixes

The following appendixes provide additional information which may be helpful.

Breite: 178 mm
Höhe: 216 mm

DFB Parameterization

A

The AEC DFB is a 170 AEC 920 00 module aid to simple Concept configuration (from version 2.2). A DFB block is required each counter channel. The DFB block transfers several types of command data (stored in the ”par_arr” data structure) in succession, and provides the counter’s actual value. The data transmission of bytes, words, and double words are started through a 0–>1 edge at the ”send” input. All bits are transferred cyclically.

Width: 178 mm
Height: 216 mm

A.1 DFB Block

Figure 19 AEC function block

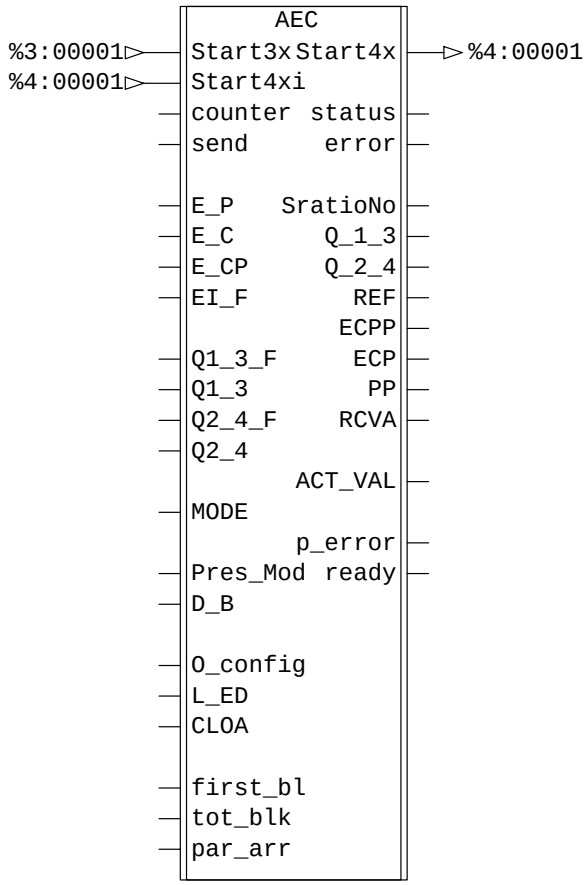


Table 7 DFB inputs

Inputs	Type	Function
Start3x	9 Word array	First address of the 8 input words
Start4xi	9 Word array	First address of the 8 output words
counter	Byte	Selects counter 1 or 2
send	Bool	A 0–>1 edge for data transmission of bytes, words, and double words (all bool values are transferred cyclically)
E_P	Bool	”Counter preset” SW enable
E_C	Bool	”Counter enable” SW enable
E_CP	Bool	”Counter hold” SW enable
EI_F	Bool	Input filter enable
Q1_3_F	Bool	Force the Q1/Q3 discrete output
Q1_3	Bool	Desired force state for Q1/Q3 discrete output
Q2_4_F	Bool	Force the Q2/Q4 discrete output
Q2_4	Bool	Desired force state for Q2/Q4 discrete output
MODE	Byte	4 bits for operating mode selection
Pres_Mod	Byte	3 bits for preset mode selection
D_B	Bool	Reverse counting direction; effective in all operating modes
O_config	Byte	Output configuration of the Q1/Q2 resp. Q3/Q4 outputs
L_ED	Bool	A, B, and Z counter broken wire detect
CLOA	Bool	Q1 to Q4 behavior for bus interruption
first_bl	INT	Number of the first data block to be transferred
tot_blk	INT	Number of data blocks to be transferred
par_arr	31 Word array	31 word data structure data block: word 1: code number word 2: command data value (low word) word 3: command data value (high word)

☞ **Note:**
The ”par_arr” data structure consists of 10 data blocks. Three words belong to each data block: the code number, command data value (low word), and command data value (high word).

Example **Example:**

first_bl = 3
tot_blk = 2
This means that the data blocks 3 and 4 of the ”par_arr” data structure will be transferred, i.e. words 7 through 12.

Width: 178 mm
Height: 216 mm

Table 8 DFB outputs

Outputs	Type	Function
Start4x	9 Word array	First address of the 8 output words
status	Byte	High byte of input word 1 or 2 (status bits)
error	Byte	Low byte of input word 1 or 2 (error bits)
SratioNo	Byte	Returned code numbers (failure = hex 1F)
Q_1_3	Bool	Q1 resp. Q3 output state
Q_2_4	Bool	Q2 resp. Q4 output state
REF	Bool	The preset value was registered
ECPP	Bool	”Hold current count” HW & ”counter hold” SW enable(s)
ECP	Bool	Counter enabled
PP	Bool	”Accept preset value” HW & ”counter preset” SW enable(s)
RCVA	Bool	First counting cycle is complete
ACT_VAL	DINT	Actual or held value
p_error	Bool	Transmission error (wrong value type sent)
ready	Bool	Data transmission indicator: 0 = transfer is in progress 1 = transfer is complete

Application Examples

B

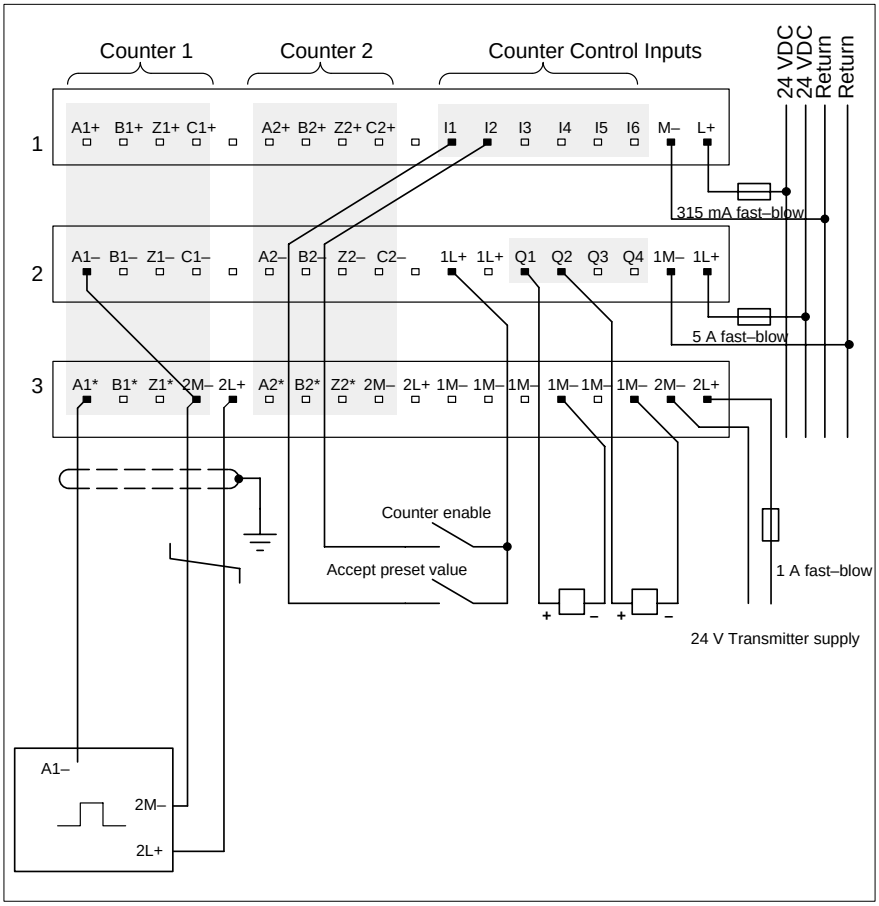
B.1 Example 1: Up Counter with 24 Vdc Pulse Encoder (Mode 2)

B.1.1 Task:

Counter 1 as up counter:

- Enable via hardware input 2
- Reset count value via hardware input 1 (positive edge)
- Start value of the counter is 0
- Threshold value 1 is 100
- Threshold value 2 is 200
- Output 1 switches on when counter is enabled and switches off when threshold value 1 is reached
- Output 2 switches on when threshold value 1 is reached and switches off when threshold value 2 is reached.

Figure 20 Wiring example 1: Up Counter with 24 VDC Pulse Encoder



Width: 178 mm
Height: 216 mm

B.1.2

Solution:

The parameterization of the counter is done in five steps:

1. Set counter mode and preset mode
2. Transfer of threshold value 1, configuration of output 1 and disable of the broken wire detection
3. Transfer of threshold value 1, configuration of output 2
4. Enable of the preset bit and the counter enable bit
5. Setting the preset input and the enable input

These steps are described on the following pages.

☞ **Note:**
We use a 24 V single ended pulse encoder. This means that we do not connect the terminal 2 and 3 of the encoder interface. The counter then generats a broken wire signal (bit 5 in input word 1) in this mode. To supress this signal we have to disable the broken wire detection (step 2).

Step 1: Set Counter Mode and Preset Mode
Counter mode (=2) and preset mode (=1) are set first. This happens with the output word 1.

Output word	Entry
400 101	1200 hex
400 102	0
400 103	0
400 104	0
400 105	0
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	220 hex
300 102	
300 103	800 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 2: Transfer of Threshold Value 1, Configuration of Output 1, and Disable of Broken Wire Detection

Next the threshold value 1 = 100 is transferred. Simultaneously output 1 is configured (output Mode 7). This happens with the output words 3 and 5. All other entries stay unchanged!

Output word	Entry
400 101	1200 hex
400 102	0
400 103	782 hex
400 104	0
400 105	100 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex
300 102	
300 103	802 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 3: Transfer of Threshold Value 2, Configuration of Output 2
The threshold value 2 = 200 is transferred next. Simultaneously output 2 is configured (output Mode A). This happens with the output words 3 and 5 again. All other entries stay unchanged!

☞ **Note:**
Change contents of register 400103 first before changing register 400105 contents. Otherwise the threshold value 1 will be overwritten.

Output word	Entry
400 101	1200 hex
400 102	0
400 103	A783 hex
400 104	0
400 105	200 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex
300 102	
300 103	803 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 4: Enable of the Preset Bit and the Counter Enable Bit
Now the counter gets enabled per software. This is done with the output word 1. All other entries stay unchanged!

Output word	Entry
400 101	1203 hex
400 102	0
400 103	A783 hex
400 104	0
400 105	200 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	5A00 hex
300 102	
300 103	803 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 5: Enable the Counter via Hardware
Enable the counter by setting the digital input 2 (input word = 2903 hex).

Output 1 gets on. Every pulse on the count input 1 gets counted. The actual count value is in word # 300 105. With a positive edge on the digital input 1 the count value (default value = 0) gets reset to 0.

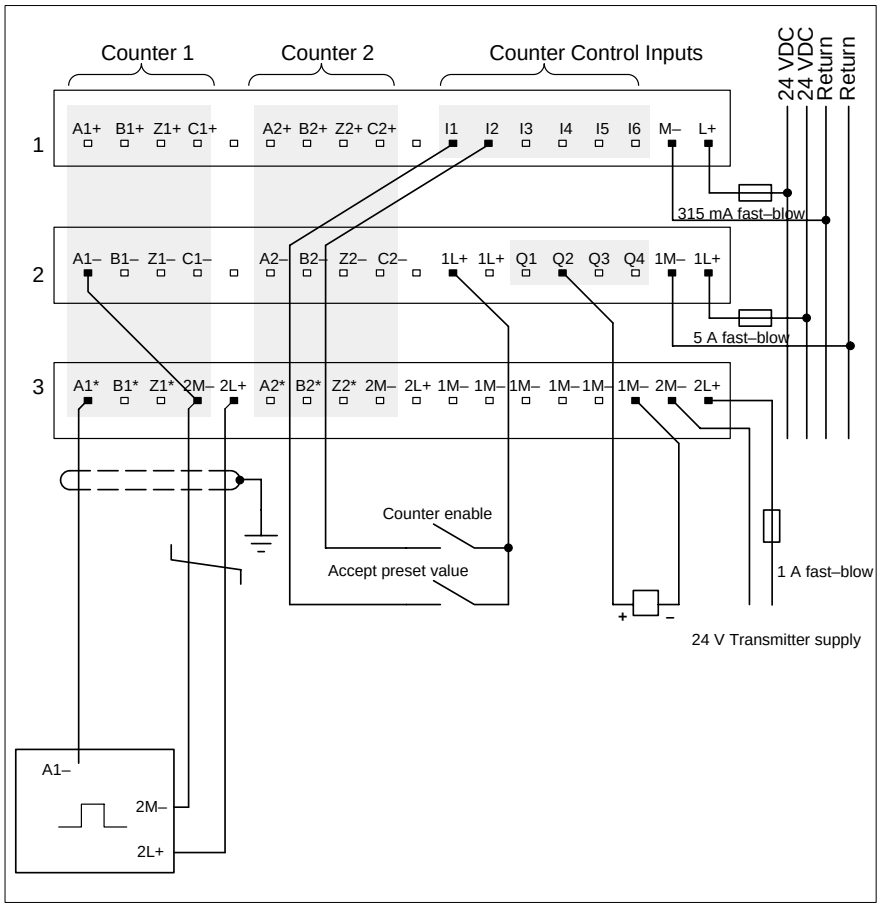
B.2 Example 2: Up Counter with 24 Vdc Pulse Encoder and Preset Value (Mode 2)

B.2.1 Task:

Counter 1 as up counter

- Enable via hardware input 2
- Reset count value via hardware input 1 (positive edge)
- Counter starts with count value 100
- Start value of the counter is 0
- Threshold value 1 is 200
- Threshold value 2 is 300
- Output 2 goes on when threshold value 1 is reached and goes off when threshold value 2 is reached.
- Output 1 stays unused

Figure 21 Wiring example 2: Up Counter with 24 Vdc Pulse Encoder and Preset Value



B.2.2 **Solution:**

The parameterization of the counter is done in seven steps:

1. Set counter mode and preset mode
2. Transfer of the preset value
3. Transfer of threshold value 1, configuration of output 2
4. Transfer of threshold value 2
5. Enable the counter via software
6. Setting the count value to the preset value
7. Enable the counter via hardware

These steps are described on the following pages.

Width: 178 mm
Height: 216 mm

Step 1: Set Counter Mode and Preset Mode
Counter mode (=2) and preset mode (=1) are set first. This with the output word 1.

Output word	Entry
400 101	1200 hex
400 102	0
400 103	0
400 104	0
400 105	0
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	220 hex
300 102	
300 103	800 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 2: Transfer of the Preset Value
Next the preset value 100 is transferred. This happens with the output words 3 and 5. All other entries stay unchanged

Output word	Entry
400 101	1200 hex
400 102	0
400 103	8 hex
400 104	0
400 105	100 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex
300 102	
300 103	801 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Note:
The steps 1 and 2 can be combined to one step.

Width: 178 mm
Height: 216 mm

Step 3: Transfer of Threshold Value 1, Configuration of Output 2
Next the threshold value 1 = 200 is transferred. Simultaneously output 2 is configured (Output Mode A). This happens with the output words 3 and 5. All other entries stay unchanged!

Output word	Entry
400 101	1200 hex
400 102	0
400 103	A082 hex
400 104	0
400 105	200 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex
300 102	
300 103	802 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 4: Transfer of Threshold Value 2
The threshold value 2 = 300 is transferred next. This happens with the output words 3 and 5. All other entries stay unchanged!

☞ **Note:**
Change contents of register 400103 first before changing register 400105 contents. Otherwise the threshold value 1 will be overwritten.

Output word	Entry
400 101	1200 hex
400 102	0
400 103	A083 hex
400 104	0
400 105	300 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex
300 102	
300 103	803 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 5: Enable the Counter via Software
Enable the preset bit and the counter enable bit with the output word 1. All other entries stay unchanged!

Output word	Entry
400 101	1203 hex
400 102	0
400 103	A083 hex
400 104	0
400 105	300 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	1A00 hex
300 102	
300 103	803 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 6: Set the Count Value to the Preset Value
Set the count value to the preset value. This is done by a positive edge on the digital input 1. The input word 300 105 feeds this value back.

Output word	Entry
400 101	1203 hex
400 102	0
400 103	A003 hex
400 104	0
400 105	300 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	9A00 hex
300 102	
300 103	4803 hex
300 104	
300 105	100 dec
300 106	
300 107	
300 108	

Step 7: Enable the Counter via Hardware
Enable the counter by setting the digital input 2 (input word 1= 5A00, input word 3= 2803).

Every pulse on the count input 1 gets counted as long as the digital input 1 is on. The actual count value can be red from word 300 105. Output 2 goes on when the count value reaches the threshold value 1 and goes off when it reaches threshold value 2. Output 1 is always off.

With a positive edge on the digital input 1 you reset the count value to the preset value.

☞ **Note:**
The firmware overtakes new preset values and new preset modes after a positive edge has been detected on bit E_P (bit 0 of the 1st output word).

New threshold values are overtaken directly.

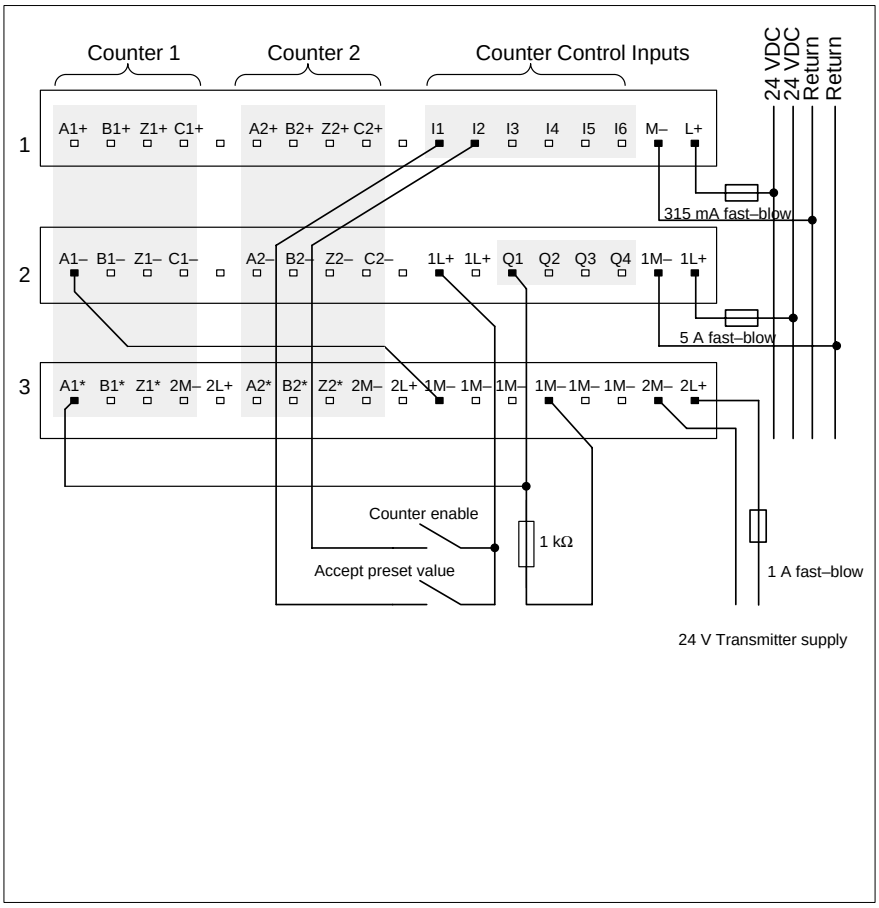
Width: 178 mm
Height: 216 mm

B.3 Example 3: Up Counter for 24 VDC Pulse and Internal Pulse Generator (Mode 2)

B.3.1 Task:

- Counter 1 as up counter
- Enable via hardware input 2
- Reset (preset) count value via hardware input 1 (positive edge)
- Counter starts with count value 100
- Start value of the counter is 0
- Threshold value 1 is 200
- Threshold value 2 is 300
- Output 1 is frequency output with 250 ms on/250 ms off. These pulses are to be counted
- Output 2 goes on when threshold value 1 is reached and goes off when threshold value 2 is reached.

Figure 22 Wiring example 3: Up Counter with 24 VDC Pulse Encoder and Internal Pulse Generator



Width: 178 mm
Height: 216 mm

B.3.2

Solution:

The parameterization of the counter is done in seven steps:

1. Set counter mode and preset mode, transfer the preset value and disable of the broken wire detection
2. Configuration of output 1 as frequency output
3. Transfer of threshold value 1, configuration of output 2
4. Transfer of threshold value 2
5. Enable the counter via software
6. Setting the count value to the preset value
7. Enable the counter via hardware

These steps are described on the following pages.

Step 1: Set Counter Mode and Preset Mode, Transfer the Preset Value
Counter mode (=2) and preset mode (=1) are set first disable protection wire detection. The transfer of the preset value 100 is done simultaneously (ratio no. 1). This is done with the output words 1, 3, and 5.

Output word	Entry
400 101	1200 hex
400 102	0
400 103	8 hex
400 104	0
400 105	100 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex
300 102	
300 103	801 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 2: Configuration of Output 1 as Frequency Output
Configure output 1 as frequency output (input Mode D) and transfer the time basis 250 ms (output words 3 and 5). After that, the output is blinking (250 ms on, 250 ms off).

Output word	Entry
400 101	1200 hex
400 102	0
400 103	D8B hex
400 104	0
400 105	250 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	80B hex / 90B hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 3: Transfer of Threshold Value 1, Configuration of Output 2
Next the threshold value 1 = 200 is transferred. Simultaneously output 2 is configured (Output Mode A). This happens with the output words 3 and 5.

Output word	Entry
400 101	1200 hex
400 102	0
400 103	AD82 hex
400 104	0
400 105	200 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	802 hex / 902 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 4: Transfer of Threshold Value 2
The threshold value 2 = 300 is transferred next. This happens with the output words 3 and 5.

☞ **Note:**
Change contents of register 400103 first before changing register 400105 contents. Otherwise the threshold value 1 will be overwritten.

Output word	Entry
400 101	1200 hex
400 102	0
400 103	AD83 hex
400 104	0
400 105	300 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	803 hex / 903 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 5: Enable the Counter via Software
Enable the preset bit and the counter enable bit with the output word 1.

Output word	Entry
400 101	1203 hex
400 102	0
400 103	AD83 hex
400 104	0
400 105	300 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	1B00 hex / 1A00 hex
300 102	
300 103	803 hex / 903 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 6: Set the Count Value to the Preset Value
Set the count value to the preset value. This is done by a positive edge on the digital input 1. The input word 300 105 feeds this value back.

Output word	Entry
400 101	1203 hex
400 102	0
400 103	AD83 hex
400 104	0
400 105	300 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	9B00 hex / 4903 hex
300 102	
300 103	4803 hex / 4903 hex
300 104	
300 105	100 dec
300 106	
300 107	
300 108	

Step 7: Enable the Counter via Hardware
Enable the counter by setting the digital input 2 (input word 1 = 5B00 hex / 5A00 hex, input word 3 = 2803 hex / 2903 hex).

Every pulse on the count input 1 gets counted as long as the digital input 1 is on. The actual count value can be red from word 300 105. Output 2 goes on when the count value reaches the threshold value 1 and goes off when it reaches threshold value 2. Output 1 is is blinking.

With a positive edge on the digital input 1 you reset the count value to the preset value.

☞ **Note:**
Make sure that a value > 0 is entered into output word 5/6 before entering the ratio no. B for a frequency output. Otherwise the value 0 will be overtaken and the output will be switched off!

Inverting the Bit D_B (Bit 15 in output word 1) changes the count direction of the counter

With the capture input the count value is held constant. Internally, however, the counter keeps on counting and serves the outputs correctly.

Width: 178 mm
Height: 216 mm

B.4 Example 4: Pulse rate Counter (Full Period) with external Time Base (Mode 8)

B.4.1 Task:

The counter has to count the number of pulses per second. The pulses to be counted are generated by the digital output 1 and the time base of 1sec by the digital output 3. This leads to the following settings:

- Counter 1 is configured as rate counter, full period (Mode 8)
- Output 1 is frequency output with e.g. 5 ms pulses (5 ms on, 5 ms off) and simulates the pulse to be counted
- Output 3 is frequency output with 500 ms pulses (500 ms on, 500 ms off). It simulates the time basis of 1 s when configured as ”full period”. (The counter then counts from one positive edge of output 3 to the next).

☞ **Note:**
In the operating mode ”rate counter” the preset mode and the digital inputs are without function. The digital outputs can be configured as ”frequency outputs” only.

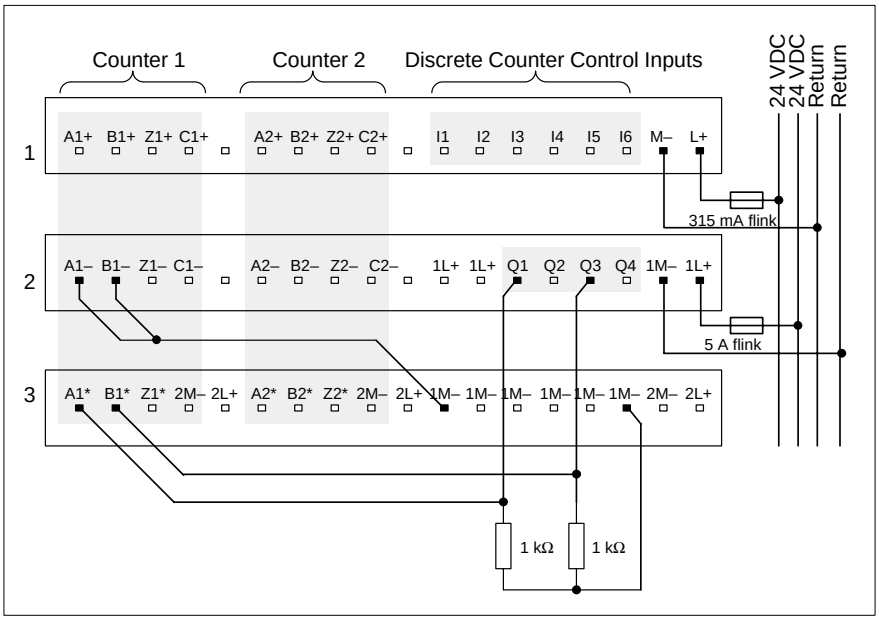
In this example we have 24 Vdc single ended signals. That is why the 20 kHz–Filter has to be activated.

Wire detection has to be disableed.

Wiring Notes:

- Output 1 to counter input A1* (row 2, pin 13 to row 3, pin 1)
- Output 3 to counter input B1* (row 2, pin 15 to row 3, pin 2)
- A1– to return of digital outputs (row 2, pin 1 to row 3, pin 11)
- B1– to return of digital outputs (row 2, pin 2 to row 3, pin 12)
- 1 kOhm resistor from each of the outputs 1 and 3 to the return of the digital outputs (recommended)

Figure 23 Wiring example 4: Pulse rate Counter (Full Period) with external Time Base



Width: 178 mm
Height: 216 mm

B.4.2

Solution:

The parameterization of the counter is done in five steps:

1. Set counter mode and activate the 20 kHz input filter
2. Configuration of output 1 as frequency output (to be counted) and disable of the broken wire detection
3. Configuration of output 3 as frequency output (for the time base)
4. Transfer of the setting ”full period”
5. Enable the counter via softwareThese steps are described on the following pages.

☞ **Note:**
We use a 24 V single ended pulse encoder. This means that we do not connect the terminal 2 and 3 of the encoder interface. The counter then generats a broken wire signal (bit 5 in word 1) in this mode. To supress this signal we have to disable the broken wire detection (step 2).

Step 1: Set Counter Mode and Activate the 20 kHz Input Filter
Counter mode (=8) and the 20 kHz filter are configured first in the output word 1.

Output word	Entry
400 101	808 hex
400 102	0
400 103	0
400 104	0
400 105	0
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	220 hex
300 102	
300 103	800 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 2: Configuration of Output 1 as Frequency Output and Disable of the Broken Wire Detection

Configure output 1 as frequency output (output Mode D), disable the broken wire detection, and transfer the time basis 5 ms for the output frequency (out words 3 and 5). After that output 1 is blinking (5 ms on, 5 ms off, ...)

☞ **Note:**

Note: In the reference data editor first enter the time basis (word 5) and then the ratio no. in word 3. Otherwise the value 0 is going to be transferred and the output will be switched off!!!

Output word	Entry
400 101	808 hex
400 102	0
400 103	D8B hex
400 104	0
400 105	5 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	80B hex / 90B hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 3: Configuration of Output 3 as Frequency Output for the Time Basis
Configure output 3 as frequency output (Output Mode D) and transfer the time basis 500 ms for the output frequency (out words 4 and 7). After that output 3 is blinking (500 ms on, 500 ms off, ...).

Output word	Entry
400 101	808 hex
400 102	0
400 103	D8B hex
400 104	D0B hex
400 105	5 dec
400 106	0
400 107	500 dec
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	80B hex / 90B hex
300 104	B hex / 10B hex
300 105	
300 106	
300 107	
300 108	

☞ **Note:**
Step 1 ... 3 may be combined to one step.

Width: 178 mm
Height: 216 mm

Step 4: Transfer of the Setting ”Full Period”
This is done with the output words 3 (ratio no.=A) and 5 (value = 1).

Output word	Entry
400 101	808 hex
400 102	0
400 103	D8A hex
400 104	D0B hex
400 105	1 dec
400 106	0
400 107	500 dec
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	80A hex / 90A hex
300 104	B hex / 10B hex
300 105	
300 106	
300 107	
300 108	

Step 5: Enable the counter via software
Set the counter enable bit (Bit 1 in output word 1).

Output word	Entry
400 101	80A hex
400 102	0
400 103	D8A hex
400 104	D0B hex
400 105	1 dec
400 106	0
400 107	500 dec
400 108	0

Input word	Counter feedback
300 101	A00 hex / B00 hex
300 102	
300 103	880A hex / 890A hex
300 104	B hex / 10B hex
300 105	100 dec
300 106	
300 107	
300 108	

The pulses on the counter input will be counted as long as the counter is enabled. After the first completed count period bit 15 (RCVA) of input word 3 will be set and the number of pulses per second is displayed in input word 5 (100 dec in this example).

☞ **Note:**
Bit positions are IEC. That is bit 15 is left most while bit zero (0) is right most when viewing register contents.

Make sure that a value > 0 is entered into output word 5/6 before entering the ratio no. B for a frequency output. Otherwise the value 0 will be overtaken and the output will be switched off!

Changes for the period definition are overtaken after a positive edge on the counter enable bit in output word 1 (this is bit 1 of word one).

For the operating mode 8 all digital inputs are without function.

Width: 178 mm
Height: 216 mm

B.5 Example 5: Period Meter (Mode 9) with internal Time Basis

B.5.1 Task:

In this operating mode the time length of a period can be measured.
This can be the time between:

- A positive edge to the next negative edge on the counter input A (= counter gate) half period
- A positive edge to the next positive edge on the counter input A (= counter gate) full period

During the gate time the counter counts internal clock signals generated by a selectable time base. The time base can be set as a parameter which also determines whether the counter gate is open during the half or the full period. There are 5 different time bases available with half or full period each. So you have the choice between 10 different codes.

In this example the time base (internally generated clock) shall be 10 µs. The period to be measured is simulated by the digital output #3 (frequency output with time base 50 ms). This leads to the following settings:

- Counter 1 is configured as period meter (Mode 9)
- Time basis 2 (10 ms, full period)
- Output 3 is frequency output with 50 ms–time base and generates the Counter gate (50 ms on, 50 ms off = 100 ms gate time at full period).

☞ **Note:**
In the operating mode ”Period meter” the preset mode and the digital inputs are without function. The digital outputs can be configured as ”frequency outputs” only.

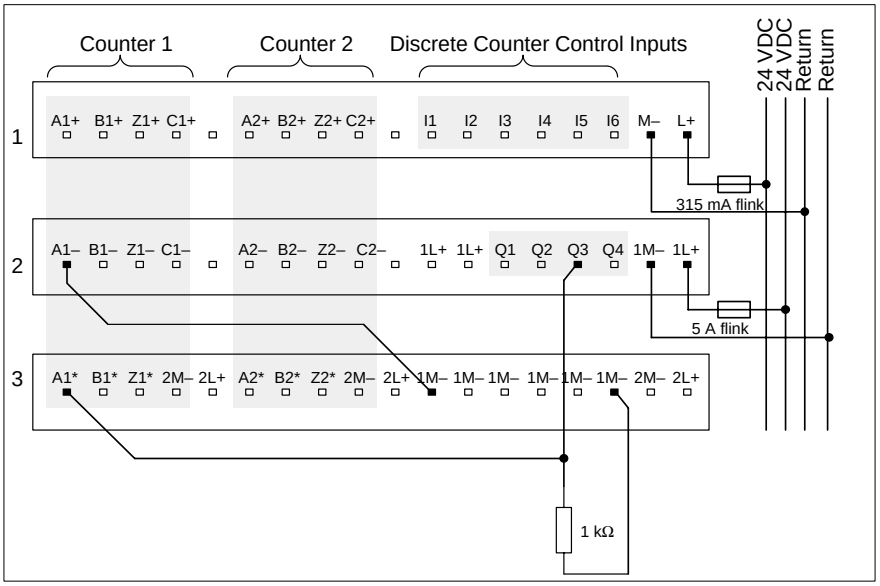
In this example we have 24 Vdc single ended signals. That is why the 20 kHz filter has to be activated.

Because there are no signals connected to the counter inputs B and C, broken wire detection must be disabled.

Wiring Notes:

- Output 3 to counter input A1* (row 2, pin 15 to row 3, pin 1)
- A1– to return of digital outputs (row 2, pin 1 to row 3, pin 11)
- 1 kOhm resistor from output 3 to the return of the digital outputs (recommended)

Figure 24 Wiring example 5: Period Meter (Mode 9) with internal Time Basis



Width: 178 mm
Height: 216 mm

B.5.2

Solution:

The parameterization of the counter is done in four steps:

1. Set counter mode and activate the 20 kHz input filter
2. Configuration of output 3 as frequency output (to be counted)
3. Transfer of the time base, setting ”full period”, and disable of the broken wire detection
4. Enable the counter via software

☞ **Note:**
We use a 24 V single ended pulse encoder. This means that we do not connect the terminal 2 and 3 of the encoder interface. The counter then generats a broken wire signal (bit 5 in word 1) in this mode. To supress this signal we have to disable the broken wire detection (step 2).

These steps are described on the following pages.

Step 1: Set counter mode and activate the 20 kHz input filter
Counter mode (=9) and the 20 kHz filter are configured in output word 1.

Output word	Entry
400 101	908 hex
400 102	0
400 103	0
400 104	0
400 105	0
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	220 hex
300 102	
300 103	800 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 2: Configuration of output 3 as frequency output
Configure output 3 as frequency output (ratio no. D) and transfer the time basis 50 ms for the clock frequency (output words 4 and 7). After that output 1 is blinking (50 ms on, 50 ms off, ...)

☞ **Note:**
First enter the value in reg 7/8 (other than zero else outputs switched off) then enter the command in register 4 (DOB hex).

Output word	Entry
400 101	908 hex
400 102	0
400 103	0
400 104	D0B hex
400 105	0
400 106	0
400 107	50 dec
400 108	0

Input word	Counter feedback
300 101	220 hex / 320 hex
300 102	
300 103	800 hex
300 104	B hex / 10B hex
300 105	
300 106	
300 107	
300 108	

Step 3: Transfer of the time base, setting ”full period”, and disable of the broken wire detection
This is done with the output words 3 and 5.

Output word	Entry
400 101	908 hex
400 102	0
400 103	88 hex
400 104	D0B hex
400 105	2 dec
400 106	0
400 107	50 dec
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	808 hex
300 104	B hex / 10B hex
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 4: Enable the counter via software
Set the counter enable bit (Bit 1 in output word 1).

Output word	Entry
400 101	90A hex
400 102	0
400 103	88 hex
400 104	D0B hex
400 105	2 dec
400 106	0
400 107	50 dec
400 108	0

Input word	Counter feedback
300 101	A00 hex / B00 hex
300 102	
300 103	8808 hex
300 104	B hex / 10B hex
300 105	9990 dec
300 106	
300 107	
300 108	

☞ **Note:**
Step 1 ... 4 may be combined to one step.

The clock signals of the internal clock are counted as long as the Counter gate is open and the counter enable bit is set. After the first completed count period bit 15

in input word 3 is set and input word 5 shows the counted value per gate time, in this case 9990. This means 9990 x 10 ms = 99.9 ms.

☞ **Note:**
Bit positions are IEC. That is bit 15 is left most while bit zero (0) is right most when viewing register contents.

Make sure that a value > 0 is entered into output word 5/6 before entering the ratio no. B for a frequency output. Otherwise the value 0 will be overtaken and the output will be switched off!

Changes of the time period definition are overtaken after a positive edge on the counter enable bit in output word 1.

For the operating mode 9 all digital inputs are without function.

Width: 178 mm
Height: 216 mm

B.6 Example 6: Frequency Meter (Full Period) with Internal Time Base (Mode A)

B.6.1 Task:

In this operating mode the number of pulses within a given time period can be counted. The time period is either:

- The whole length of the selected time base full period
- Half the length of the selected time base half period

The time base is generated internally and can be configured (length and period definition, 10 different possibilities).

In this example, we want to configure the digital output 1 as a frequency output and count its pulses per second. This leads to the following settings:

- Counter 1 is pulse counter
- Output 1 is configured as frequency output with 1 ms pulses (1 ms on, 1 ms off).
- Time basis for the frequency is set to 1000 ms, full period. (The counter then counts during the whole time period of 1 s).
- Broken wire detection must be disabled

☞ **Note:**
In the operating mode ”frequency meter” the preset mode and the digital inputs are without function. The digital outputs can be configured as ”pulse outputs” only.

In this example we have 24 Vdc single ended signals. That is why the 20 kHz–Filter has to be activated.

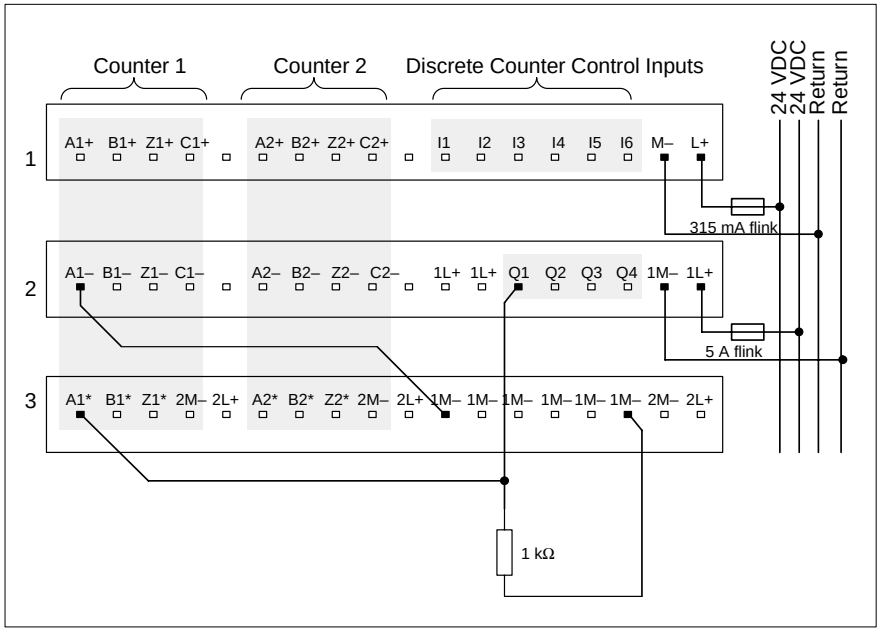
Wiring Notes:
Output 1 to counter input A1* (row 2, pin 13 to row 3, pin 1)

A1– to return of digital outputs (row 2, pin 1 to row 3, pin 11)

1 kOhm resistor from output 1 to the return of the digital outputs (recommended)

Width: 178 mm
Height: 216 mm

Figure 25 Wiring example 6: Frequency Meter (Full Period) with Internal Time Base



B.6.2 **Solution:**

The parameterization of the counter is done in four steps:

1. Set counter mode and activate the 20 kHz input filter
2. Configuration of output 1 as frequency output (to generate the frequency to be counted) and disable of the broken wire detection
3. Configuration of the internal time basis for frequency measuring
4. Enable the counter via software

☞ **Note:**
We use a 24 V single ended pulse encoder. This means that we do not connect the terminal 2 and 3 of the encoder interface. The counter then generats a broken wire signal (bit 5 in word 1) in this mode. To supress this signal we have to disable the broken wire detection (step 2).

These steps are described on the following pages.

Width: 178 mm
Height: 216 mm

Step 1: Set Counter Mode and Activate the 20 kHz Input Filter
Counter mode (=A) and the 20 kHz filter are configured first in the output word 1.

Output word	Entry
400 101	A08 hex
400 102	0
400 103	0
400 104	0
400 105	0
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	220 hex
300 102	
300 103	800 hex
300 104	
300 105	
300 106	
300 107	
300 108	

Step 2: Configuration of Output 1 as Frequency Output and Disable of the Broken Wire Detection

Configure output 1 as frequency output (Output Mode D), disable the broken wire detection and transfer the time basis 1 ms (ratio no. = B) for the output frequency (value = 1) to be counted (out words 3 and 5). After that output 1 is blinking (1 ms on, 1 ms off, ...)

☞ **Note:**

In the reference data editor first enter the time basis (word 5) and then the ratio no. in word 3. Otherwise the value 0 is going to be transferred and the output will be switched off!!!

Output word	Entry
400 101	A08 hex
400 102	0
400 103	D8B hex
400 104	0
400 105	1 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	80B hex / 90B hex
300 104	
300 105	
300 106	
300 107	
300 108	

Width: 178 mm
Height: 216 mm

Step 3: Configuration of the Internal Time Basis for Frequency Measuring
Transfer (ratio no = 9) the time basis 1000 ms and the setting ”full period” (value = 5).

Output word	Entry
400 101	A08 hex
400 102	0
400 103	D89 hex
400 104	0
400 105	5 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	200 hex / 300 hex
300 102	
300 103	809 hex / 909 hex
300 104	
300 105	
300 106	
300 107	
300 108	

☞ **Note:**
Step 1 ... 3 may be combined to one step.

Step 4: Enable the Counter via Software
Set the counter enable bit (Bit 1 in output word 1).

Output word	Entry
400 101	A0A hex
400 102	0
400 103	D89 hex
400 104	0
400 105	5 dec
400 106	0
400 107	0
400 108	0

Input word	Counter feedback
300 101	A00 hex / B00 hex
300 102	
300 103	8809 hex / 8909 hex
300 104	
300 105	500 dec
300 106	
300 107	
300 108	

The pulses on the counter input will be counted as long as the counter is enabled. After the first completed count period bit 15 of input word 3 will be set and the and

Width: 178 mm
Height: 216 mm

the number of pulses per second is displayed in input word 5 (500 in this example).

☞ **Note:**
Bit positions are IEC. That is bit 15 is left most while bit zero (0) is right most when viewing register contents.

For the operating mode A all digital inputs are without function.

Make sure that a value > 0 is entered into output word 5 before entering the ratio no. B for a frequency output. Otherwise the value 0 will be overtaken and the output will be switched off!

Changes for the period definition and/or time base are overtaken after a positive edge on the counter enable bit (this is bit 1 of output word one).

Changes of the frequency on output 1 can be performed directly (= without a positive edge on the counter enable bit)

Index

Index and keyword register are here.

Breite: 185 mm
Höhe: 230 mm

Breite: 178 mm
Höhe: 216 mm

Q

R

S

T

U

W

Breite: 178 mm
Höhe: 216 mm