CHAPTER 4

BIOS Setup Information

ROBO-618 is equipped with the AMI BIOS stored in Flash ROM. This BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, ROBO-618 communicates with peripheral devices and check its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start-up.

4.1 Entering Setup

Turn on or reboot the computer. When the message "Hit if you want to run SETUP" appears, press key immediately to enter BIOS setup program.

If the message disappears before you respond, but you still wish to enter Setup, please restart the system to try "COLD START" again by turning it OFF and then ON, or touch the "RESET" button. You may also restart from "WARM START" by pressing <Ctrl>, <Alt>, and <Delete> keys simultaneously. If you do not press the keys at the right time and the system will not boot, an error message will be displayed and you will again be asked to,

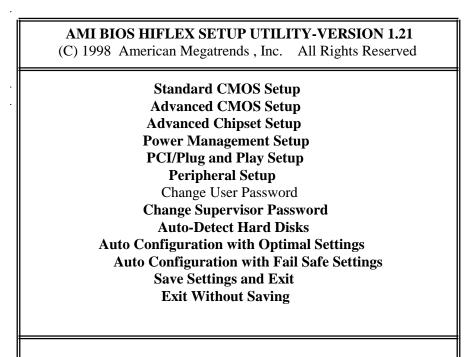
Press <F1> to Run SETUP or Resume

In HIFLEX BIOS setup, you can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table below will show you all of keystroke functions in BIOS setup.

EDITING KEYS	FUNCTION
<tab></tab>	Move to the next field
$\leftarrow \uparrow \rightarrow \downarrow$	Move the next field to the left, above, right, or below
<enter></enter>	Select in the current field
+ / -	Increments / Decrements a value
<esc></esc>	Close the current operation and return to previous level
<pgup></pgup>	Returns to the previous option
<pgdn></pgdn>	Advances to the next option
<f2>/<f3></f3></f2>	Select background color
<f10></f10>	Show "Save current settings and exit (Y/N)" in main menu

4.2 Main Menu

Once you enter AMI BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from ten setup functions and two exit choices. Use arrow keys to switch the items and press <Enter> to accept or enter the sub-menu.



Standard CMOS setup for changing time, date, hard disk type, etc. **ESC** : Exit $\uparrow \downarrow$: Sel **F2/F3** : Color **F10** : Save & Exit

NOTE : It is strongly recommended to reload Optimal Setting if CMOS is lost or BIOS is updated.

4.3 Standard CMOS Setup Menu

This setup page includes all the items in a standard compatible BIOS. Use the arrow keys to highlight the item and then use the $\langle PgUp \rangle / \langle PgDn \rangle$ or $\langle + \rangle / \langle - \rangle$ keys to select the value or number you want in each item and press $\langle Enter \rangle$ key to certify it.

Follow command keys in CMOS Setup table to change **Date**, **Time**, **Drive type**, and **Boot Sector Virus Protection Status**.

4.4 Advanced CMOS Setup Menu

This setup includes all of the advanced features in the system. The detail descriptions are specified as belows.

Quick Boot

Set "Disabled" for normal booting or select "Enabled" to skip minor BIOS test items to obtain quick boot response. The optimal default setting is *Enabled*.

Boot Up Sequence

This category includes six items to determine which drive computer searches first for the Disk Operating System (DOS). The reference default setting is :

* 1st Boot Device	IDE-0
* 2nd Boot Device	Floppy
* 3rd Boot Device	ATAPI ZIP
* 4th Boot Device	Disabled
* Try Other Boot Devices	Yes
* S.M.A.R.T. for Hard Disks	Disabled

The default ARMD (ATAPI Removable Media Device) emulation type is set to popular drive type LS-120 and ATAPI ZIP. There are many choices of booting devices to boot up system. User can select "Disabled", "IDE-0", "IDE-1", "IDE-2", "IDE-3", "Floppy", "LS-120", "ATAPI ZIP", "CDROM", "SCSI", or "NETWORK".

Boot Up Num-Lock

Select "On" (default setting) to enable numeric function of the numeric keypad , or "Off" to disregard it.

PS/2 Mouse Support

Select "Enabled" to enable PS/2 mouse function, or "Disabled" to release IRQ12 interrupt for other ISA-bus I/O devices. The optimal default setting is *Enabled*.

System Keyboard

This option will be used to neglect "keyboard error" while you choose *Absent* setting in your BIOS setup and system has no keyboard attached.

Primary Display

The default setting is VGA/EGA. Chooses Absent, VGA/EGA, CGA40x25, CGA80x25, or Mono to meet your monitor type. If you select Absent, the "CMOS Display Type Wrong" message will be ignored for mismatched display card in CMOS setting.

Password Check

This option enables the password checking when the system boots up or runs CMOS Setup. It only takes effect after setting Change Supervisor Password. The default setting is *Setup*.

- Setup : This option will force system to check password before running Setup if you have already entered the current user password in "Change User Password". By that time, the system will be only able to boot but deny accessing Setup.
- Always : Password prompt appears every boot-up. The system will not boot and deny access Setup with invalid password. The best way is to clear CMOS or try to reload BIOS Setup to boot up system.

Boot To OS/2 > 64MB

You should set this option to "Yes" to support OS/2 environment. The default setting is *No*.

System BIOS Cacheable

The default setting is *Enabled*. You can choose this option to enhance system performance by shadowing and caching function. The "Disabled" will ignore this BIOS shadow function.

Video BIOS Shadow

Select "Cached" option to get more higher display performance by shadowing and caching VGA BIOS. The default setting is set as "Cached". If user chooses "Enabled" option, only BIOS shadow function is active. The "Disabled" option will ignore this BIOS cacheable and shadowing function.

Shadow Memory (from address C000 – DFFF, 16K per segment)

Each of segments provides three options "Disabled", "Enabled", and "Cached" for faster adapter's ROM execution. However this shadow function is Chipset oriented and dependent on system hardware feature. The default setting for each of all segments are *Disabled* except for C000 and C400. In general, this area is allocated for VGA BIOS and set to *Cached* to get higher display performance by shadowing and caching feature. If user chooses "Enabled" setting, only BIOS shadow function is active.

4.5 Advanced Chipset Setup Menu

This setup is very important to keep system stability. If you are not technical person, do not attempt to change any parameters. The best way is to choose optimal default setting.

Configure SDRAM Timing by SPD

This option provides DIMM plug-and-play support by Serial Presence Detect (SPD) mechanism via the System Management Bus (SMBus) interface. You can disable this option to handle the following four SDRAM timing options. The optimal default setting is *Disabled*. In addition, SDRAM operating timings may follow serial presence from EEPROM content by setting this option to "Enabled", and all of SDRAM timing options will be not available and hidden.

SDRAM RAS# to CAS# delay

This option controls the number of SCLKs (SDRAM Clock) from a row activate command to a read or write command. If your system installs good quality of SDRAM, you can set this option to "2 SCLKs" to obtain better memory performance. The default setting is *3 SCLKs*.

SDRAM RAS# Precharge

This option controls the number of SCLKs for RAS# precharge. If your system

installs good quality of SDRAM, you can set this option to "2 SCLKs" to obtain better memory performance. The default setting is *3 SCLKs*.

SDRAM CAS# Latency

This option controls the number of SCLKs between the time a read command is sampled by the SDRAMs and the time the North Bridge, 82443BX, samples correspondent data from the SDRAMs. For a registered DIMM with CAS# Latency = 2, this option should be set to "2 SCLKs" to acquire better memory performance. The default setting is *3 SCLKs*.

SDRAM Leadoff Cmd Timing

This option is used to control when the SDRAM command pins (SRASx#, SCASx# and Wex#) and CSx# are considered valid on leadoffs for CPU cycles. The optimal default setting is *Auto*. It is automatically initialized and set by BIOS from CPU speed detection. For Desktop platforms, it might be set to "4 SCLKs". In general, another option "3 SCLKs" will be set to meet Mobile platforms.

DRAM Integrity Mode

There are three options *Non-ECC*, *EC-Only* (Error Check Only) and *ECC Hardware* (Error Checking and Correction) in this feature. The DRAM integrity mode will be implemented by the parity algorithm when this option is set to "Non-ECC". The optimal default setting is *Non-ECC*.

DRAM Refresh Rate

This option specifies the refresh rate frequency for the installed system memory SDRAM DIMMs. There are five options 15.6us, 31.2us, 62.4us, 124.8us, and 249.6us used to control DRAM refresh period. The default setting is 15.6 us. If you have good quality of DRAM, you can choose longer refresh rate to get better system performance.

Memory Hole

This option allows the end user to specify the location of a memory hole for

memory space requirement from ISA-bus cards. The settings are "Disabled", "512-640KB", or "15-16MB". The default setting is *Disabled*.

8bit I/O Recovery Time

This option specifies the length of the delay (in SYSCLKs) inserted between consecutive 8-bit I/O operations. The settings are *Disabled*, 1, 2, 3, 4, 5, 6, 7, or 8 Sysclk. The optimal default setting is 1 Sysclk.

16bit I/O Recovery Time

This option specifies the length of the delay (in SYSCLKs) inserted between consecutive 16-bit I/O operations. The settings are *Disabled*, *1*, *2*, *3*, or *4* Sysclk. The optimal default setting is *1 Sysclk*.

USB Passive Release

When enabled, this allows PIIX4 to use Passive Release to obtain better USB performance while transferring control information or data for USB transactions. When disabled, PIIX4 will perform PCI accesses for USB without using Passive Release. The optimal default setting is *Enabled*.

PIIX4 Passive Release

Choose the "Enabled" option to help raise the available bandwidth of the PCI bus for acquiring higher PCI bus performance. The optimal default setting is *Enabled*.

PIIX4 Delayed Transaction

Choose the "Enabled" option to obtain higher PCI bus performance for slower ISA bus application. The optimal default setting is *Disabled*.

USB Function

This option will enable on-chip USB function to support USB (Universal Serial Bus) peripheral devices if user chooses the "Enabled" setting. The default is *Disabled*.

USB Keyboard Legacy Support

This feature will be automatically disabled and hidden if user chooses the

"Disabled" setting from the foregoing USB Function option. Otherwise, enabling this option provides support for USB-keyboard or USB-Mouse without auxiliary driver under DOS environment.

CMOS RAM CLEAR FUNCTION

This option is default set to *Disabled*. If your system supports Y2K RTC, you should set this option to *Enabled* to support H/W CMOS clearing operation.

4.6 Power Management Setup Menu

This APM (Advanced Power Management) determines how much power energy can be saved by setting below items to handle system power resource. The following descriptions will specify the definition of each item in details.

Power Management/APM

Using this feature to control system power resources. The default setting is *Enabled* to enable power management function and effective based on following parameter settings.

Green PC Monitor Power State

This option is used to decide what kind of power states are effective. There are three options "Stand By", "Suspend", and "Off" in this feature. The "Stand By" option is to turn off light power by handling of Monitor signals. The other "Suspend" mode is to turn off heavy power. And the other one, "Off" state, is really to turn off the power of the monitor. The default setting is *Off*.

Video Power Down Mode

This option specifies the power conserving state that the VESA VGA video subsystem enters after the specified period of display inactivity has expired. There are three options "Disabled", "Stand By", and "Suspend" in this field. The default setting is *Disabled*. If user select another options, it will be controlled by "Stand by Time out" and "Suspend Time out".

Hard Disk Power Down Mode

This option specifies the power management state that the HDD enters after the

specified period of hard drive inactivity has expired. It is the same as video power control. The default setting is *Disabled*. If user chooses "Stand By" or "Suspend", it will depend on period of parameter "Stand By Time out" or "Suspend Time out".

Stand by Time out (Minute)

This option specifies the length of the period of system inactivity while the computer is in Full-On power state before the computer is placed in Standby mode. When this length of time expires, the computer enters Standby Timeout state. In Standby mode, some power use is curtailed. The settings are *Disabled*, 1, 2, 4, 8, 10, and all ten minute intervals up to and including 60 min. The default setting is *Disabled*.

Suspend Time out (Minute)

This option is the same as **Stand by Time out** function. These two features will be enabled to monitor power of sub-items "VGA display", "Serial port", "Parallel Port", "Floppy", "Pri-HDD", and "Sec-HDD" independently. It is also used to control CPU throttle running function. All of sub-items will be ineffective in selection of disabling "Stand by Time out" or "Suspend Time out" even if it can be choosed by user in BIOS setup menu. The settings are Disabled, 1, 2, 4, 8, 10, 20, 30, 40, 50, and 60 min. The optimal default setting is *Disabled*.

Throttle Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the throttle mode. The settings are 0-12.5%, 12.5-25%, 25-37.5%, 37.5-50%, 50-62.5%, 62.5-75%, and 75-87.5%. The default setting *50-62.5%*.

Display Activity

This option specifies if BIOS is to monitor activity on the display monitor for power conservation purposes. If set to *Monitor* and the computer is in a power saving state, BIOS watches for video display activity. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ lines. If set to *Ignore*, video display monitor activity is not monitored. The settings are *Monitor* (Enabled) or *Ignore* (Disabled). The default settings is *Ignore*.

Device 6/7/8/5/0/1/2/3 (Serial 1&2, Parallel, FDD, Pri/Sec HDD)

When set to *Monitor*, these options enable event monitoring on the specified hardware device. If set to *Monitor* and the computer is in a power saving state, BIOS watches for activity on the device with specified IRQ line. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified device. No Monitoring activity occurs if the option is set to *Ignore*. The settings for each of these options are Monitor or Ignore. The optimal default setting for Serial Port 1 & 2, Floppy disk, and Primary/Secondary master IDE are set to *Monitor*. The rest of Devices are default set to *Ignore*.

Power Button Function

This item is used to handle soft power on/off regardless of time countin (generally speaking, it is 4 sec) if you set it to *On/Off*. You can easily power on/off system by pressing power button (toggle switch) directly. This feature is only available on system with ATX power control interface. If you use standard AT power supply, this option will be ignored. However choose the "Suspend" setting , system will be forced into suspend mode when user turn it off unless you can consecutively press the power button for more than 4 second to get in Soft off function. The default setting is *Suspend*.

Ring Resume From Soft Off

This item will be used to wake up system from remote ringing control under Soft Off condition. If you choose "Disabled" setting, the system will be not resumed by modem ring. The default setting is *Disabled*.

4.7 PCI/Plug and Play Setup

This section describes configuring the PCI bus system. PCI (Peripheral Component Interconnect) is a system which allows I/O devices to operate at speeds nearing CPU's when they communicate with own special components.

All of options described in this section are important and technical and it is strongly recommended that only experienced users could make any changes to the default settings.

Plug and Play Aware O/S

Set this option to "Yes" if the operating system installed in the computer is Plug and Play-aware. BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to "No" if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. *You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly*. The optimal default setting is *No*.

Clear NVRAM

This option is used to clear NVRAM and check or update ESCD (Extended System Configuration Data) data after system power on. The default setting is *No* that will not clear NVRAM and the operation of update ESCD is effective in different ESCD data comparision. If you select the "Yes" setting, then the BIOS will update ESCD each time of power on.

PCI Latency Timer (PCI Clocks)

This option is used to control PCI latency timer period (follow PCI clocks). Based on PCI specification 2.1 or later and PCI bus frequency in system, user can select different timer to meet their PCI bus environment. The default setting is 64 PCI clocks.

PCI VGA Palette Snoop

The option are "Disabled" and "Enabled". Some display cards that are nonstandard VGA such as graphics accelerations or MPEG video cards may not show colors properly. User can choose "Enabled" setting to correct this display mismatch problem and support any ISA adapter card installed in the computer requires VGA palette snooping. The default setting is *Disabled*.

Allocate IRQ to PCI VGA

This option will be used to allocate IRQ for PCI VGA card. In general, some of PCI VGA cards need IRQ support.

PCI IDE BusMaster

Set this option to Enabled to specify that the IDE controller on the PCI local bus has bus mastering capability. The settings are *Disabled* or *Enabled*. The optimal default setting is *Disabled*.

Off Board PCI IDE Card

This option specifies if an offboard PCI IDE controller adapter card is used in the computer. You must also specify the PCI expansion slot on the SBC (Single Board Computer) where the offboard PCI IDE controller card is installed. If an offboard PCI IDE controller is used, the onboard IDE controller on the SBC is automatically disabled. The settings are *Auto*, *Slot 1*, *Slot 2*, *Slot 3*, or *Slot 4*. If *Auto* is selected, BIOS automatically determines the correct setting for this option. The optimal default setting is *Auto*. If you want to respectively control off board PCI IDE Primary/Secondary IRQ resources, you should set this option among *Slot 1* to *Slot 4*. Or all of these sub-options will be not available and hidden.

Off Board PCI IDE Primary/Secondary IRQ

This option specifies the PCI interrupt used by the primary/secondary IDE channel on the offboard PCI IDE controller. The settings are *Disabled*, *INTA*, *INTB*, *INTC*, *INTD*, or *Hardwired* for installing off-board non-compliant PCI IDE card. The optimal default setting is *Disabled*.

PCI Slot 1/2/3/4 IRQ Priority

These options specify the priority IRQ to be used for any PCI devices installed in PCI expansion slots 1 through 4. The settings are *Auto* (AMIBIOS automatically Determines the priority IRQ), (IRQ) *3*, *4*, *5*, *7*, *9*, *10*, or *11*. The default setting is *Auto*.

DMA Channel 0/1/3/5/6/7

These options specify if the named DMA channel is available for using on the ISA/EISA bus or PnP (Plug & Play). The settings are *ISA/EISA* or *PnP*. The optimal default setting is PnP.

IRQ 3/4/5/7/9/10/11/12/14/15

These options specify the bus that the named interrupt request lines (IRQs) are used on. These options allow you to specify IRQs for use by legacy ISA adapter cards. These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/PnP Setup to remove the IRQ by assigning the option to the ISA/EISA setting. All IRQs used by on-board I/O are configured as PCI/PnP. The settings are *PCI/PnP* or *ISA/EISA*.

4.8 Peripheral Setup

This section describes I/O resources assignment for all of on-board peripheral devices.

On Board FDC

Three options are "Auto", "Disabled", and "Enabled". If user wants to install different add-on super I/O card to connect floppy drives, set this field to *Disabled*. The default setting is *Auto*. It will call BIOS to automatically determine if the floppy controller should be enabled.

On Board Serial Port A/Port B

These fields control the resource assignments of two on-board serial interfaces SIO1 and SIO2. The following lists show current options in On Board Serial Port A/ Port B :

Auto (default setting) → cannot set serial I/O resources by manual operation Disabled → indicates on-board COM port function is ineffective 3F8h/COM1 → assign I/O address 3F8h to COM1 2F8h/COM2 → assign I/O address 2F8h to COM2 3E8h/COM3 → assign I/O address 3E8h to COM3 2E8h/COM4 → assign I/O address 2E8h to COM4

On Board IR Port

This option control the resource assignments of on-board serial port 3. The IR Mode Select has three settings IrDA, ASK IR, and FIR. The default setting is *Disabled*.

On Board Parallel Port

There are four optional items *Parallel Port Mode*, *EPP Version*, *Parallel Port IRQ*, and *Parallel Port DMA Channel* used to control on-board parallel port interface while user select I/O base address manually. The following lists are available options of on-board parallel port :

Auto (default setting) \rightarrow user can not control all of LPT port I/O resources **Disabled** \rightarrow on-board parallel port function is ineffective and N/A

378h \rightarrow locate IRQ7 for this default I/O address

278h \rightarrow assign this I/O address to LPT1

3BCh \rightarrow assign this I/O address to LPT1

O Parallel Port Mode :

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications. This Parallel Port Mode includes four options "Normal", "Bi-Dir", "EPP", and "ECP". The optimal default setting is *Bi-Dir*.

Setting	Description
Normal	Uni-direction operation at normal speed
Bi-Dir	Bi-direction operation at normal speed
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.

ECP	The parallel port can be used with devices that adhere to the
	Extended Capabilities Port (ECP) specification. ECP uses the
	DMA protocol to achieve data transfer rates up to 2.5 Megabits
	per second. ECP provides symmetric bidirectional
	communication.

\odot EPP Version :

This option is only valid if the **Parallel Port Mode** option is set to *EPP*. This option specifies the version of the Enhanced Parallel Port specification that will be used by AMIBIOS. The settings are *1.7* or *1.9*. The optimal default setting is *1.9*.

O Parallel Port IRQ :

This option is only valid if the **Onboard Parallel Port** option is not set to *Disabled*. This option sets the IRQ used by the parallel port. The settings are 5 and 7. The optimal default setting is 7.

O Parallel Port DMA Channel :

This option is only available if **On Board Parallel Port** is set to fixed I/O address and the setting of **Parallel Port Mode** is ECP. This option sets the DMA channel used by ECP-capable parallel port. The settings are 0, 1, or 3 (DMA channel 3). The optimal default setting is 3.

On Board IDE

This option specifies the onboard IDE controller channels that will be used. The settings are *Disabled*, *Primary*, *Secondary*, or *Both*. The optimal default setting is *Both*.

4.9 BIOS POST Check Point List

AMIBIOS provides all IBM standard Power On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. The POST routines support CPU internal diagnostics. The POST checkpoint codes are accessible via the Manufacturing Test Port (I/O port 80h).

Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the message and explaining the problem in detail so that the problem can be corrected.

During the POST, the BIOS signals a checkpoint by issuing one code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power-on sequence and what test is currently being performed. This is done to help troubleshoot faulty system board.

If the BIOS detects a terminal error condition, it will halt the POST process and attempt to display the checkpoint code written to port 80H. If the system hangs before the BIOS detects the terminal error, the value at port 80H will be the last test performed. In this case, the terminal error cannot be displayed on the screen. The following POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 07/15/95 version 6.27 (Enhanced).

Uncompressed Initialization Codes — The uncompressed initialization checkpoint hex codes are listed in order of execution :

Code	Description
D0	NMI is disabled. CPU ID saved. INIT code checksum verification will be
	started.
D1	Initializing the DMA controller, performing the keyboard controller BAT
	test, starting memory refresh, and going to 4GB flat mode.
D3	To start memory sizing.
D4	Returning to real mode. Executing any OEM patches and setting the stack
	next.
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h.
	The INIT code is copied to segment 0 and control will betransferred to
	segment 0.
D6	Control is in segment 0. Next, checking if <ctrl><home> was pressed and</home></ctrl>
	verifying the system BIOS checksum.
	If either <ctrl><home> was pressed or the system BIOS checksum is bad,</home></ctrl>
	next will go to checkpoint code E0h.
	Otherwise, going to checkpoint code D7h.
D7	To pass control to interface module.
D8	Main BIOS runtime code is to be decompressed.
D9	Passing control to the main system BIOS in shadow RAM next.

Bootblock Recovery Codes — The bootblock recovery checkpoint hex codes are listed in order of execution :

Code	Description
E0	The onboard floppy controller if available is initialized. Next, beginning the
	base 512KB memory test.
E1	Initializing the interrupt vector table next.
E2	Initializing the DMA and Interrupt controllers next.

Code	Description
E6	Enabling the floppy drive controller and Timer IRQs. Enabling internal
	cache memory.
ED	Initializing the floppy drive.
EE	Start looking for a diskette in drive A: and read first sector of the diskette.
EF	A read error occurred while reading the floppy drive in drive A: .
F0	Next, searching for the AMIBOOT.ROM file in the root directory.
F1	The AMIBOOT.ROM file is not in the root directory.
F2	Next, reading and analyzing the floppy diskette FAT to find the clusters
	occupied by the AMIBOOT.ROM file.
F3	Start reading AMIBOOT.ROM file, cluster by cluster.
F4	The AMIBOOT.ROM file is not the correct size.
F5	Next, disabling internal cache memory.
FB	Next, detecting the type of Flash ROM.
FC	Erasing the Flash ROM.
FD	Programming the Flash ROM
FF	Flash ROM programming was successful. Next, restarting the system BIOS.

Uncompressed Initialization Codes — The following runtime checkpoint hex codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Code	Description
03	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the POST code next.
07	Next, initializing the CPU and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before the keyboard BAT command is issued.
0C	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary INIT after the K/B controller BATcommand test.
0F	The keyboard command byte is written next.
10	Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <end> or <ins> keys were pressed during power on.</ins></end>
12	To initialize CMOS if the <i>initialize CMOS RAM in every boot</i> is set or the <end> key is pressed. Going to disable DMA and Interrupt controllers.</end>
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh line is toggling. Checking the 15us on/off time next.

Code	Description
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature
	next. Making the BIOS code segment writable and performing any necessary
	configuration before initializing the interrupt vectors.
24	The configuration or setup required before interrupt vector initialization has
	completed. Interrupt vector init. is about to begin
25	Interrupt vector initialization is done. Clearing the password if the POST
	DIAG switch is on.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration
	before the video ROM test.
2C	To look for optional video ROM and give control.
2D	The video ROM has returned control to BIOS POST. Performing any
	required processing after the video ROM had control.
2E	Completed podt-video ROM test processing. If the EGA/VGA controller is
	not found, performing the display memory read/write test next.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. Look for retrace checking next.
31	Display memory R/W test or retrace checking failed. To do alternate display
	retrace checking.
32	Alternate display memory R/W test passed. To look for the alternate display
	retrace checking.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error message.
3A	The new cursor position has been read and saved. Displaying the <i>Hit </i>
40	message next.
40	Preparing the descriptor tables next.
42	Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check
	memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the
43	total system memory size next.
46	The memory wraparound test has completed. The memory size calculation
40	has been done. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns
+/	to the base 640 KB memory test.
48	Patterns written in base memory. Determining the amount of memory below
70	1MB next.
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Code Description 49 The amount of memory below 1MB has been found and verified. Determining the amount of memory above 1MB memory next. 4B The amount of memory above 1MB has been found and verified. Checkir for a soft reset and clearing the memory below 1MB for the soft reset nex If this is a power on situation, going to checkpoint 4Eh next. 4C The memory below 1MB has been cleared via a soft reset. Clearing the memory above 1MB next. 4D The memory test started, but not as the result of a soft reset. Displaying th first 64KB memory size next. 4E The memory size next. 4F Memory size display started. This will be updated during memory test. Performing the sequential and random memory test next. 50 Memory testing/initialization below 1MB completed. Going to adjust displayed memory size for relocation and shadowing. 51 The memory above 1MB has been tested and initialized. Saving the mem size information next. 52 The memory size display was adjusted for relocation and shadowing. Testing the memory size information and the CPU registers are saved. Entering real mode next. 53 The memory size information and the CPU registers are saved. Entering real mode next. 54 Shutdown was successful. The CPU is in real mode. Disabling the Gate A line, parity, and the NMI next. 57 The A20 address line, parity, and the NMI are disabled. Adjusting the memory size dependi	
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	0
59 The <i>Hit <del< i="">> message is cleared. The <i><wait< i="">> message is displayed</wait<></i></del<></i>	d.
Staring the DMA and interrupt controller test next.	.
60 The DMA page register test passed. To do DMA#1 base register test.	
62 DMA#1 base register test passed. To do DMA#2 base register test.	
65 DMA#2 base register test passed. To program DMA unit 1 and 2.	
66 DMA unit 1 and 2 programming over. To initialize 8259 interrupt control	ler.
7F Extended NMI sources enabling is in progress.	
80 The keyboard test has started. Clearing the output buffer and checking for	r
stuck keys. Issuing the keyboard reset command next.	
81 A keyboard reset error or stuck key was found. Issuing the keyboard	
Controller interface test command next.	
82 The keyboard controller interface test completed. Writing the command b	yte
and initializing the circular buffer next.	
83 Command byte written, Global data init done. To check for lock-key.	
84 Locked key checking is over. Checking for a memory size mismatch with	1
CMOS RAM data next.	

Code	Description
85	The memory size check is done. Displaying a soft error and checking for a
	password or bypassing Setup next.
86	Password checked. About to do programming before setup.
87	The programming before Setup has completed. Uncompressing the Setup
	code and executing the AMIBIOS Setup utility next.
88	Returned from CMOS setup program and screen is cleared. About to do
	programming after setup.
89	The programming after Setup has completed. Displaying the power on
	Screen message next.
8B	The first screen message has been displayed. The <wait> message is</wait>
	displayed. Performaing the PS/2 mouse check and extended BIOS data
	area allocation check next.
8C	Programming the Setup options next.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	The floppy drive controller has been configured. Configuring the hard disk
	drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has completed.
	The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST.
	Performing any required processing after the option ROM returned control.
99	Any initialization required after the option ROM test has completed.
	Configuring the timer data area and printer base address next.
9A	Return after setting timer and printer base address. Going to set the RS-232
	base address.
9B	Returned after setting the RS-232 base address. Performing any required
	Initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the
	Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after the Coprocessor test is complete. Checking the extended
	Keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID
	command next.
A2	Displaying any soft errors next.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait state programming is over. Clearing the screen and enabling
	parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before
	passing control to the adaptor ROM at E000 next.

Code	Description
A8	Initialization before passing control to the adaptor ROM at E000h
	completed. Passing control to the adaptor ROM at E000h next.
A9	Returned from adaptor ROM at E000h control. Performing any initialization
	required after the E000 option ROM had control next.
AA	Initialization after E000 option ROM control has completed. Displaying the
	system configuration next.
AB	Building the multiprocessor table, if necessary.
AC	Uncompressing the DMI data and initializing DMI POST next.
B0	The system configuration is displayed.
B1	Copying any code to specific areas.
00	Code copying to specific areas is done. Passing control to INT 19 h boot
	loader next.

4.10 Flash BIOS Utility

Utilize AMI Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact your technical window to get this utility if necessary.

NOTE : Remark or delete any installed Memory Management Utility (such as HIMEM.SYS, EMM386.EXE, QEMM.EXE, ..., etc.) in the CONFIG.SYS files before running Flash programming utility.