

# TB-6S-LX25-FANET Hardware User Manual

# Rev.1.02

Rev.1.02 TOKYO ELECTRON DEVICE LIMITED



#### **Revision History**

Version	Date	Description	Publisher
Rev.1.00	2011/09/29	Release version	Kiguchi
			Dan
Rev.1.01	2011/12/12	Redesigned for mass production (Rev.3)	Kiguchi
Rev.1.02	2012/03/27	Part is changed from s/n xxxxx-1.02.	Kiguchi
		OSC 25MHz(U10): EPSON to Abracom.	Odajima
		Modified following tables and figures	
		Figure 4-1, Table 1, Figure 7-1, Figure 7-2, Figure7-4	
		Figure 7-7, Table 6, Table 7, Table 9, Table 10, Table 11	
		P17 and P18: Added comment.	
		P19: modified pin name of DDR3	
		P36: modified comment.	



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# Introduction

Thank you for purchasing the **TB-6S-LX25-FANET** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

# SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- Before using the product, read these safety precautions carefully to assure correct use.
- These precautions contain serious safety instructions that must be observed.
- After reading through this manual, be sure to always keep it handy.

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
	Indicates the possibility of serious injury or death if the product is handled incorrectly.
	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual. (Examples)

	Turn off the power switch.	
	Do not disassemble the product.	
$\bigcirc$	Do not attempt this.	



Warning					
	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.				
	<b>If an unpleasant smell or smoking occurs, disconnect the power supply.</b> If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.				
X	<b>Do not disassemble, repair or modify the product.</b> Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.				
$\bigcirc$	<b>Do not touch a cooling fan.</b> As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.				
$\bigcirc$	<b>Do not place the product on unstable locations.</b> Otherwise, it may drop or fall, resulting in injury to persons or failure.				
$\bigcirc$	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.				
$\bigcirc$	<b>Do not touch the product with a metallic object.</b> Otherwise, a fire or electric shock may occur.				
$\bigcirc$	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.				
$\bigcirc$	<b>Do not get the product wet or touch it with a wet hand.</b> Otherwise, the product may break down or it may cause a fire, smoking or electric shock.				
$\oslash$	<b>Do not touch a connector on the product (gold-plated portion).</b> Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.				



Caution					
$\bigcirc$	<ul> <li>Do not use or place the product in the following locations.</li> <li>Humid and dusty locations</li> <li>Airless locations such as closet or bookshelf</li> <li>Locations which receive oily smoke or steam</li> <li>Locations exposed to direct sunlight</li> <li>Locations close to heating equipment</li> <li>Closed inside of a car where the temperature becomes high</li> <li>Staticky locations</li> <li>Locations close to water or chemicals</li> <li>Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.</li> </ul>				
$\bigcirc$	<b>Do not place heavy things on the product.</b> Otherwise, the product may be damaged.				

# Disclaimer

This product is the Xilinx's FPGA Spartan-6 evaluation board. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

- (1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
- (2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
- (3) Use of this product against the instructions given in this manual.
- (4) Malfunctions due to connection to other devices.Tokyo Electron Device Limited assumes no responsibility or liability for:
- (1) Erasure or corruption of data arising from use of this product.
- (2) Any consequences or other abnormalities arising from use of this product, or
- (3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.



# **1. Related Documents and Accessories**

#### **Related documents**

All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

#### Board mounting kit

- None

#### **Board accessories**

- AC adaptor: (1)

AC adaptor (Akizuki Denshi: GF12-US03320 or equivalents, with a modified connector)

# 2. Overview

This board is an embedded network evaluation platform module with Xilinx's FPGA Spartan-6 Series **LX25**.

### 3. Feature

- Xilinx's XC6SLX25-2CSG324
- 10/100Mbps Ethernet PHY and 2-port RJ45 connector
- 76-pin user GPIO on the soldered side of the board

(2.54mm-pitch, 44-pin stack connector x 2)

- DDR2 SDRAM (Chip) x 1: ESMT's M14D5121632A (or equivalents) (512Mbits x 1)
- 25MHz clock source. A 50MHz OSC can also be added.
- Control switch: Push SW/DIP SW/Rotary SW
- Monitor: LED



# 4. Block Diagram

The board block diagram is shown in Figure 4-1.



Figure 4-1 Board Block Diagram



# 5. External View of the Board

Figure 5-1 and 5-2 show the component side and the solder side of the board.



Figure 5-2 Solder Side



# 6. Board Specifications

Table 1 shows the TB-6S-LX25-FANET Board Specifications.

Table 1 TB-6S-LA25-FANET Board Specifications						
ltem#	Category 1	Category 2	Description	Remarks		
1		Number of layers	8 layers			
2	Doord	External dimensions	100mm x 70mm			
3	Board	Board thickness	1.6mm			
4	Composition	Board color	Red			
5		Material	FR-4			
6	Component	Component side	Not specified			
7	Height	Solder side	2mm	Without connectors		
8	Impedance	Single signal	50Ω±10%			
9	Control	Differential signal	100Ω±10%			
10	RoHS/Pbfree	RoHS/Pbfree	RoHS / lead-free solder			
11	Surface finishing	_	Gold flash			

#### Table 1 TB-6S-I X25-EANET Board Specifications



#### 6.1. TB-6S-LX25-FANET Board Dimensions

Figure 6-1 shows the TB-6S-LX25-FANET board dimensions.



Figure 6-1 TB-6S-LX25-FANET Board Dimensions



# 7. Description of Components

#### 7.1. Power Supply

Figure 7-1 shows the power supply block diagram.



Figure 7-1 Power Supply Block Diagram

#### 7.2. Power Supply Selector

The power supply can be configured by setting J1 to switch the input pin to the Power Connector (CN1) or Stack Connectors (CN2 and CN3) as shown in Figure 7-2. J2 is selection for 3.3V or 2.5V.



Figure 7-2 Power Supply Selector



#### 7.3. Power Connector (CN1)

Figure 7-3 shows the power connector (CN1), JST's B2P-VH (or JST's VHR-2N compatible connector).



Figure 7-3 Power Connector (CN1)

#### 7.4. Clock Structure

Figure 7-4 shows the board clock structure.



Figure 7-4 Clock Structure

Note: If mounting OSC 50MHz, please use CB3LV-3C-50M0000(CTS-Frequency Controls) or compatible device.



#### 7.5. Ethernet PHY (U4, U5) & RJ45 (CN7, CN8)

The board has two Micrel's Ethernet PHY (KSZ8721BL).

The RJ45 connector with pulse transformer has HanRun's HR911105A. The Ethernet PHY TXER is fixed to "L" setting on the board.



Figure 7-5 Ethernet PHY & RJ45

Ethernet PHY(U4)				Ethernet PHY(U5)	
Pin Name	FPGA Pin No.	Level		Pin Name	FPGA Pin No.
TXD0	G18			TXD0	L18
TXD1	G16			TXD1	K14
TXD2	F15			TXD2	N18
TXD3	G14			TXD3	M18
TXEN	F18			TXEN	K18
TXC	K15			TXC	L16
RXD0	F14			RXD0	K12
RXD1	E18			RXD1	J18
RXD2	E16			RXD2	J16
RXD3	D18			RXD3	H16
RXER	F17	3.3V		RXER	K17
RXDV	F16			RXDV	K13
RXC	H17			RXC	L15
COL	H14			COL	N17
CRS	G13			CRS	L17
XINT	H12			XINT	M16
MDIO	D17			MDIO	J13
MDC	C18			MDC	H15
XRST	C17			XRST	H13
LED1	P18			LED1	N15
XI	H18			XI	÷

#### Table 2 Ethernet PHY Pin Assignments

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Level

3.3V



#### 7.6. External IO Connector (CN2, CN3)

The board has two external I/O stack connectors, Samtec SSM-122-L-DV-K-TR (or compatible Samtec TSM-122-01-L-DV).

Table 3 shows the CN2 pin assignments.

Table 3   CN2 Pin Assignments							
Pin No.	FPGA Pin No.	Pin Name	Pin Name	FPGA Pin No.	Pin No.		
1		3.3V	uC_DAT_ENA	R3	2		
3	Т3	uC_ADR0	GND		4		
5	Τ4	uC_ADR1	uC_nBUSY	R5	6		
7	Т5	uC_ADR2	uC_nIRQ	V5	8		
9	U5	uC_ADR3	uC_nCS	N6	10		
11	V6	uC_ADR4	uC_DATA0	T7	12		
13	V7	uC_ADR5	uC_DATA1	U7	14		
15	P6	uC_ADR6	uC_DATA2	N7	16		
17	P7	uC_ADR7	uC_DATA3	V4	18		
19	T6	uC_ADR8	uC_DATA4	M8	20		
21	R7	uC_ADR9	uC_DATA5	V8	22		
23	U8	uC_ADR10	uC_DATA6	N8	24		
25	Т8	uC_ADR11	uC_DATA7	Т9	26		
27	P8	uC_ADR12	uC_DATA8	N9	28		
29	V9	uC_ADR13	uC_DATA9	N11	30		
31	M10	uC_ADR14	uC_DATA10	V12	32		
33	U10	uC_ADR15	uC_DATA11	V11	34		
35	R8	uC_EMULATIO	uC_DATA12	U11	36		
37	N10	uC_nBHE	uC_DATA13	R10	38		
39	P11	uC_nRD	uC_DATA14	V10	40		
41	T10	uC_nWR	GND		42		
43		3.3V	uC_DATA15	V13	44		

#### \*Power Supply

3.3V pin on CN2 is connected to USER\_3P3V on TB-6S-LX25-FANET. CN1 is available if setting J1.

#### \*IO Pin

IO pin on CN2 is connected to Bank 2 on FPGA. Voltage can be selected by J2.



Table 4 shows the CN3 pin assignments.

Pin No.	FPGA Pin No.	Pin Name	Pin Name	FPGA Pin No.	Pin No.
1	B2	USR_IOP0	3.3V		2
3		GND	USR_IOP10	B3	4
5	A2	USR_ION0	USR_ION10	A3	6
7	B4	USR_IOP1	USR_IOP11	C5	8
9	A4	USR_ION1	USR_ION11	A5	10
11	B6	USR_IOP2	USR_IOP12	D6	12
13	A6	USR_ION2	USR_ION12	C6	14
15	B8	USR_IOP3	USR_IOP13	C7	16
17	A8	USR_ION3	USR_ION13	A7	18
19	B9	USR_IOP4	USR_IOP14	D8	20
21	A9	USR_ION4	USR_ION14	C8	22
23	C10	USR_IOP5	USR_IOP15	G9	24
25	A10	USR_ION5	USR_ION15	F9	26
27	B12	USR_IOP6	USR_IOP16	B11	28
29	A12	USR_ION6	USR_ION16	A11	30
31	D11	USR_IOP7	USR_CLKP	D9	32
33	C11	USR_ION7	USR_CLKN	C9	34
35	F13	SYNC_OUT0	MOTH_MOSI		36
37	E13	SYNC_OUT1	MOTH_DIN		38
39	C13	LATCH_IN0	MOTH_XCS		40
41		GND	MOTH_CCLK		42
43	A13	LATCH_IN1	3.3V		44

#### Table 4 CN3 Pin Assignments

#### \*Power Supply

3.3V pin on CN3 is connected to USER\_3P3V on TB-6S-LX25-FANET. CN1 is available if setting J1.

#### \*IO Pin

IO pin on CN3 is connected to Bank3 on FPGA. Voltage can be selected by J2

#### \*MOTH\_MOSI(36), MOTH\_DIN(38), MOTH\_XCS(40) and MOTH\_CCLK(42)

These pins are connected to SPI Flash (J3 setting: 1-2).



#### 7.7. DDR2 SDRAM (U12)

The board has one ESMT DDR2 SDRAM (M14D5121632A) .

#### Pin

A[12:0], DQ[15:0], ODT, UDQS, /UDQS, LDQS, /LDQS, LDM, UDM, CK, /CK, CKE, /RAS, /CAS, /WE and BA[1:0] are connected.

CSN is fixed to "L" setting on the board.

#### Specifications

512Mbit (8Mword x 16bit x 4bank) DDR2-800

#### Address structure

Bank = 2bit Address = 13bit(Row address = 13bit / Column address = 10bit)

#### **Data Bus Structure**

Data strobe (DQS) during a read/write operation: byte-by-byte control Data Mask (DM): byte-by-byte control



Figure 7-6 DDR2SDRAM



DDR2	FPGA Pin
Pin Name	No.
A0	J7
A1	J6
A2	H5
A3	L7
A4	F3
A5	H4
A6	H3
A7	H6
A8	D2
A9	D1
A10	F4
A11	D3
A12	G6
BA0	F2
BA1	F1
CLK	G3
CLKN	G1
RASN	L5
CASN	K5
CKE	H7
WE	E3

# Table 5 DDR2SDRAM Pin Assignments

DDR2	FPGA Pin
Pin Name	No.
ODT	K6
DQ0	L2
DQ1	L1
DQ2	K2
DQ3	K1
DQ4	H2
DQ5	H1
DQ6	J3
DQ7	J1
DQ8	M3
DQ9	M1
DQ10	N2
DQ11	N1
DQ12	T2
DQ13	T1
DQ14	U2
DQ15	U1
LDQS	L4
LDQSN	L3
UDQS	P2
UDQSN	P1
UDM	K4
LDM	K3



#### 7.8. Configuration

Figure 7-7 shows the configuration block diagram. J3 setting (1-2) allows access to SPI Flash from CN3.



Figure 7-7 Configuration Block Diagram



#### 7.9. SPI Flash (U17)

The board has a Numonyx SPI Flash 128Mbit (M25P128) as FPGA configuration memory. After an FPGA is configured, it can be used as user area.



Figure 7-8 SPI Flash

SPI Flash		FPGA				
Pin No.	Signal Name	Pin No. Level				
7	XS	V3				
8	Q	R13				
15	D	T13	VCC_ADJ			
16	С	R15				

#### Table 6 SPI Flash Pin Assignments

#### 7.10. I2C EEPROM (U11)

The board has a Microchip I2C EEPROM 32Kbit (24LC32A) which can be used to store board specific configuration data and others.



#### Figure 7-9 I2C EEPROM

120	EEPROM	PGA	
Pin No.	Signal Name	Level	
5	SDA	U18	
6	SDL	U17	3.3V
7	WP	T18	

#### Table 7 I2C EEPROM Pin Assignments



#### 7.11. LED

Table 8 shows the onboard LEDs.

Table 8 LED Functions

BD Silk	Function	Connect to	Connect to: Pin No.	Connect to: Bank	Act	Level
D6	FPGA debugging		M14	1		2 2)/
D7	FPGA debugging		N14	1	L	3.3V
DE	This LED will light when FPGA					
50	Config is complete	EDCA				
D8	FPGA debugging	FFGA	P16	1		
D9			P15	1		2 2\/
D10			M13	1	L	3.3V
D11			L14	1		

#### 7.12. SW

Table 9 shows the onboard switches.

BD Silk	Function	SW Pin	Connect	Connect to:	Connect to:	Act	Level
		Sequence	to	Pin No.	Bank		
		8		C15	0		
0.4/4		4		B14	0		
5001		2		A15	0		
		1		A14	0		
		8		P12	2		
0.4/0		4		M11	2		
5002		2		B16	0		
	FPGA Config Rotary	1		A16	0		VCC
Switch	Switch	8		T14	2		
<b>C</b> \\/2		4	EPCA	T12	2	-   L	_ADJ
5003		2		T11	2		
		1	FPGA	R11	2		
		8		V14	2		
C) A / A		4		V15	2		
5004		2		U16	2		
		1		U15	2		
SWE	FPGA ReConfig	1		V2	2		
3005	Push SW	I					
SW6	EDCA Config Duch SM	2		F5	3		
SW7	Fron Coning Fush SW	3		F6	3		1 0\/
C///0		1		P3	3		1.0V
3000	FFGA CONING DIP SW	2		L6	3		

#### Table 9 Switch Functions



#### 7.13. Jumper

Table 10 shows the onboard jumpers.

Table 10 Jumper Functions

BD Silk	Function	Remarks
J1	Selection of 3.3V power supply to the	1-2: 3.3V is supplied from CN1
	board	2-3: 3.3V is supplied from CN2, CN3
J2	Selection of external IO pin Vcco	1-2: Connecting VCC_ADJ to 2.5V
		2-3: Connecting VCC_ADJ to 3.3V
10	Selection of SDI Flech connection	1-2: Connecting to CN3
13	Selection of SFI Flash connection	2-3: Connecting to JTAG



# 8. Default Settings

Figure 8-1 shows the default jumper and SW settings. Check jumpers and switches in the area enclosed by a blue line.



Figure 8-1 Default Settings on Component Side

Table 11 shows the default jumper and switch settings.

Table 11	Default Jumpe	r and Switch	Settings
----------	---------------	--------------	----------

No.	BD Silk	Default Setting	Function
1	J1	1-2	VCC_3P3V is supplied from CN1.
2	J2	2-3	VCC_ADJ is supplied from VCC_3P3V.
3	J3	2-3	FPGA Config SPI Flash is connected in JTAG mode.
4	SW8	Undefined	This switch is not used in default FPGA data.
5	SW1-4	Undefined	These switches are not used in default FPGA data.



# 9. Appendix

#### 9.1. Generating a configuration file

This section describes how to generate a configuration file using the Tool version **ISE 13.3**. First generate a configuration file to store the configuration in flash memory.

#### 1. Double click Generate Target PROM/ACE File.

Processes	: KOUN_TOP - RTL	<u>^</u>
	Design Summary/Reports Design Utilities User Constraints Synthesize - XST Implement Design Translate Map Place & Route Generate Programming File Configure Target Device	E
	Manage Configuration Project (iMPACT) Analyze Design Using ChipScope	

#### Figure 9-1 Generating a configuration file on ISE

#### 2. Double click Create PROM File.

ISE IMPACT (0.76xd)		
File Edit View Operations Output Debug Window Help		
iMPACT Flows ↔ □ S ×		
Boundary Scan		
Create PROM File (PROM File For-		
🕀 🖹 WebTalk Data	R	
IMPACT Processes ↔ □ 5 X		
Console		⇔⊡∄×
		*
		-
Courte Courte A Marian		•
🔄 Console 🥪 Errors 🔝 warnings		FFFFF

Figure 9-2 iMPACT Window - 1



3. Select SPI Flash - Configure Single FPGA and click Arrow.

Step 1.       Select Storage Target       Step 2.       Add Storage Device(s)       Step 3.         Storage Device Type :       Image: Storage Device (bits)       Spartan 3E       Image: Storage Device (bits)       Image: Storage Device (bits) </th <th></th>	
Storage Device Type :	Enter Data
<ul> <li>Ninx Flash/PROM</li> <li>Non-Volatile FPGA</li> <li>Spartan SAN</li> <li>SPI Flash</li> <li>Gonfigure Single FPGA</li> <li>Configure MultiBoot FPGA</li> <li>Configure MultiBoot FPGA</li> <li>Configure Single FPGA</li> <li>Configure MultiBoot FPGA</li> <li>Storage Device</li> <li>Remove Storage Device</li> <li>Fe Fmove Storage</li></ul>	Value
SPI Flash Configure MultiBoot FPGA Configure M	
Configure MultiBoot FPGA Configure MultiBoo	
Configure MultiBoot FPGA Configure form Paralleled PROMs Generic Parallel PROM	sp605_jtagcheck\
Configure from Paralleled PROMs Generic Parallel PROM Generic Parallel PROM Historean	Value
Use Power-of-2 for Start Addr Number of Bitstream Bitstream 0 Start Address Bitstream 1 Start Address Add Non-Configuration Data Files Number of Data File	BIN
Auto Select PROM       Number of Data File         Image: Auto Select PROM       Image: Auto Select PROM	No
Bitstream 0 Start Address Bitstream 1 Start Address Bitstream 1 Start Address Add Non-Configuration Data Files Number of Data File	2
Auto Select PROM     Auto Select PROM	0
Add Non-Configuration Data Files Number of Data File	675840
Auto Select PROM	Yes
Auto Select PRUM	
	•
Jescription:	
If you are targeting any 3rd party supplied SPI PROM, select this storage device type	
OK Can	cel Help



4. In the Storage Device (bits) selection pane select 128M and click Add Storage Device.

Step 1.	Select Storage Target		Step 2. A	dd Storag	ge Device(s)		Step 3.		Enter Da	ita
Storage Device T	ype :		Storage Device (bits)	128M	]		eneral File Deta		Value	
Xilinx Flash/P	ROM PGA		Add Storage Device	128K 256K	torage Device		Checksum Fill Value	FF		
Spartan3	AN			512K			Output File Name	Untitled		
Configure Configure	e Single FPGA MultiBoot FPGA			2M 4M 8M 1.6M			Output File Location	20110329_pn_	_sp605_jtagcheck\	B
Configure	e Single FPGA e MultiBoot FPGA			32M 64M			Flash/PROM F	ile Property	Value	
Configure Generic Paral	e from Paralleled PROMs lel PROM			128M 256M			File Format		BIN	T
				-			Use Power-of-2 for	r Start Addr	No	
							Number of Bitstrea	m	2	
							Bitstream 0 Start A	Address	0	
							Bitstream 1 Start A	Address	675840	
							Add Non-Configura	ation Data Files	Yes	Τ
							Number of Data Fil	e		
			Auto Select PRUM				×			Þ.
escription:										
1 this step, you w • Storage • Add Sto • Remove • Auto Se	Ill select the appropriate target device. <b>Device:</b> This selection allows you to of <b>rage Device:</b> After selecting the mem- <b>Storage Device:</b> Use this button to <b>lect PROM:</b> If you select this option, il	noose the ory target lelete the MPACT w	: specific device memory d , use this button to add th target device from the lis ill choose a device density	ensity you are e device to th t below. Selec large enough	targeting. e target Storage De t the device and clic to hold your specifie	ivice list ok this b ed data.	below. utton to remove it fr	om the list.		
							ОК	Gan	cel Heln	2

Figure 9-4 iMPACT Window - 3

5. Clock Arrow and enter any name (directory) you want in the Output File Name and Output File Location fields, and click OK.

**MIVSIN** 

Step 1.	Select Storage Targe	t	Step 2. Ad	ld Storage Device(s)		Step 3.		Enter	Data
Storage Device 1	ype :		Storage Device (bits)	128M 💌		eneral File Deta		Value	
Xilinx Flash/F	ROM PGA		Add Storage Device	Remove Storage Device		Checksum Fill Value	FF		
SPI Flash			128M			Output File Name	sample		
Configur Configur BPI Flash	e Single FPGA e MultiBoot FPGA					Output File Location	C:/work		P
- Configur	e Single FPGA e MultiBoot FPGA					Flash/PROM File Property		Value	
Configur Generic Para	e from Paralleled PROMs llel PROM					File Format		MCS	
						Add Non-Configura	ation Data Files	No	
			Auto Select PROM			Add Non-Configura	ation Data Files	No	
escription:			Auto Select PROM			Add Non-Configura	ation Data Files	No	
scription: this step, you ( Checks Output office for	vill enter information to assist in setting um Fill Value: When data is insufficier File Name: This allows you to spe file Location: This allows you to spe mat: PROM files can be generated in a	up and gen t to fill the the base n cify the dire	Auto Select PROM herating a PROM file for the entire memory of a PROM ame of the file to which you ectory in which the file nam of industry standard format	targeted storage device and moo the value specified here is used r PROM data will be written ed above will be created . Depending on the PROM file fc	de . to calcu prmat you	Add Non-Configura	of the unused po	Dortions.	UFP.

Figure 9-5 iMPACT Window - 4

6. Click OK.



Figure 9-6 iMPACT Window - 5

7. In the file selection dialog, select a bit file for generating a configuration file.

#### 8. Click No.



Figure 9-7 iMPACT Window - 7





inrevim

Figure 9-8 iMPACT Window - 8

10. Double click Generate File....

ISE IMPACT (0.76xd) - [PROM File Formatt	atter: SPI Flash Single FPGA]	
iMPACT Flows       ↔ □ ♂ ×         impact Flows       ↔ □ ♂ ×	Bownloadbit       0x0000_0000         PROM       PROM         PROM       PROM         PROM       PROM         0x00FF_FFFF	
	PROM File Formatter: SPI Flash Single FPGA	
Console		⇔⊓a×
		*
Console 🙆 Errors 📣 Warnings		
Select everything in the active file	PROM File Generation Target SPI Flash 6,411,696 Bits used File: sample in Location:	C:¥work/

Figure 9-9 iMPACT Window - 9



11. If the configuration file is successfully generated, a **Generate Succeeded** message will appear.



Figure 9-10 iMPACT Window - 10



#### 9.2. Writing a configuration file to Flash Memory

Connect a Platform USB cable to the JTAG connector (CN6) as shown in Figure 9-11. Turn on the power switch of the board, run **iMPACT**, and write the configuration to Flash Memory in accordance with the following procedure.



Figure 9-11 Onboard JTAG Connector

1. Double click Boundary Scan and click Initialize Chain (indicated by an arrow).



Figure 9-12 Writing to Device - 1



2. A bit/jed file configuration window will appear. Cancel it.

After selecting FPGA, right click Add SPI/BPI Flash.... to select it.

😼 ISE IMPACT (0.76xd) - [Boundary Scan]	]	
🛞 File Edit View Operations Outpu	ut Debug Window Help	- 8 ×
	BI PR	
iMPACT Flows ↔ □		
Boundary Scan     SystemACE     Greate PROM File (PROM File For     WebTalk Data	TDI Get Device ID Get Device Signature/Usercode Read Device DNA Add SPI/BPI Flash Assign New Configuration File Set Programming Properties Set Erase Properties	
iMPACT Processes ↔	Launch File Assignment Wizard	
Available Operations are: Get Device ID Get Device Signature/Usercode Read Device Status Read Device DNA		
	Boundary Scan	
Console		↔ 🗆 🗗 ×
done. PROGRESS_END - End Operation. Elapsed time = 0 sec. // *** BATCH CMD : identifyMP * III Console Errors & Warnings	M	* *
	Configuration Digilent JTAG-HS1 1000	000

Figure 9-13 Write to Device - 2

- 3. In the file selection dialog, select a configuration file (xxx.mcs) to write it to Flash Memory.
- 4. Select the onboard Flash M25P128 and click OK.

lect the PROM attache	d to FPGA:	
SPI PROM	M25P128	
Data Width:	1	
		2

Figure 9-14 Write to Device - 3



5. I	Double c	click F	Program	in th	e iMPACT	Processes	window.
------	----------	---------	---------	-------	----------	-----------	---------

Boundary Scan]		
🎲 File Edit View Operations Outpu	ut Debug Window Help	_ 8 ×
	# @ R I / N	
IMPACT Flows ↔ □ 🗗 ×		
Boundary Scan     SystemACE     A Create PROM File (PROM File For     B Create PROM File (PROM File For     B WebTalk Data	TDI xo6sb/25 bypass	
MELAT 5		
Available Operations are:		
Program		
i Verify		
📫 Erase		
Blank Check		
Readback		
Get Device Checksum     Road Davice Status		
Redu Device Status		
	Boundary Scan	
Console		↔ 🗆 🗗 ×
// *** BATCH CMD : identifyMP	M	
Selected part: M25P128		
<pre>// -** BATCH CMD : attachflas Unprotect sectors: FALSE</pre>	n -position 1 -spi "m25P128"	
<pre>// *** BATCH CMD : assignfile</pre>	toattachedflash -position 1 -file "C:/work/sample.mcs"	
		*
٠ m		E E
📃 Console 🥝 Errors 🤬 Warnings		
	Configuration Digilent JTAG-HS1 10000	0000

Figure 9-15 Write to Device - 4



#### 6. Click **OK**.

Boundary-Scan	<b>—</b>	
Device 1 (FPGA xc6slx25 )	Property Name	Value
Device 1 ( Attached FLASH, I	25 Verify	
0.7	General CPLD And PROM Properti	es
	Design-Specific Erase Before Prog	ramming 🔽
	FPGA Device Specific Programmir	ng Properties
	After programming Flash	automatically load i

Figure 9-16 Write to Device - 5

7. Writing to Flash Memory will start.

BISE IMPACT (0.76xd) - [Boundary Scan]	
🚱 File Edit View Operations Outpu	t Debug Window Help
	K?
IMPACT Flows ↔ □ 문 ×	The second secon
Boundary Scan     BystemACE     Create PROM File (PROM File For     B WebTalk Data	TDI
iMPACT Processes ↔	N
Available Operations are:	42
Program     Verify	
🔿 Erase	So Configuration Operation Status
Blank Check	Executing command
Readback	0%
Read Device Status	Abort
	Downlaw Coan
Canaala	
'1': ID Check passed.	+ L D X
'1': IDCODE is '202018' (in	hex).
'1': ID Check passed.	
'1': Using Sector Erase.	
	*
	R. I.
Unsole Urrors 1 Warnings	
	Connguration Diglient JTAG-HS1 10000000

#### Figure 9-17 Write to Device - 6



8. Select the onboard Flash M25P128 and click OK.

If writing to Flash Memory is successfully completed, a Program Succeeded message will appear.

Bundary Scan]			<b>X</b>
🛞 File Edit View Operations Outpu	it Debug Window Help		e ×
IMPACT Flows ↔ □ 중 ×			
Boundary Scan     Boundary Scan     Boundary Scan     Create PROM File (PROM File For     WebTalk Data	Right click device to select operations		
iMPACT Processes ↔ □			
Available Operations are:			
A Program			
i Verify			
📫 Erase			
Blank Check			
Readback			
<ul> <li>Get Device Checksum</li> <li>Read Device Status</li> </ul>		Program Succeeded	
	Boundary Scan		
Console		++1	3 & X
LCK cycle: NoWait INFO:IMPACT - '1': Checking d '1': Programmed successfully. PROGRESS_END - End Operation. Elapsed time = 41 sec.	one pindone.		• 0.
< _ m			F.
📃 Console 🙆 Errors 🔔 Warnings			
		Configuration Digilent JTAG-HS1 10000000	

Figure 9-18 Write to Device - 7



9. The configuration data written to Flash Memory is loaded into the FPGA device in Master-SPI mode. The configuration can be enabled by turning on the power switch of the board or pressing and holding the reconfiguration switch (see Figure 9-19) for more than 2 seconds.



#### Figure 9-19 Reconfiguration Switch

10. The board provides the status of FPGA configuration at location D5 (see Figure 9-20). If the configuration is successfully completed, the D5 green light will flash.



Figure 9-20 Configuration Status





Rev.1.02

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