

Hardware User Manual for iMX53 Carrier Card
iW-PRDTL-UM-02-R1.0-REL1.1
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1 Introduction

1.1 Purpose

The purpose of this document is to explain the procedure about the user interface, Power ON procedure and ATK tool kit usage for iMX53-Carrier Card.

1.2 Scope

This document describes the Hardware details, Power-on procedure and setting up Serial communication with PC/Laptop. This document also explains usage procedure for ATK tool kit.

1.3 Glossary

Table 1: Glossary

Acronyms	Description.
ATK	Advanced Tool Kit
CAN	Controller Area Network
LCD	Liquid Crystal Display
DDR	Double Data Rate
FAQ	Frequently Asked Question
HT	Hyper Terminal
MMC	Multi Media Card
PC	Personal computer
RS232	Recommended Standard 232
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VGA	Video graphic Array

2 Hardware Details

2.1 iMX53 – Carrier Card Connector details

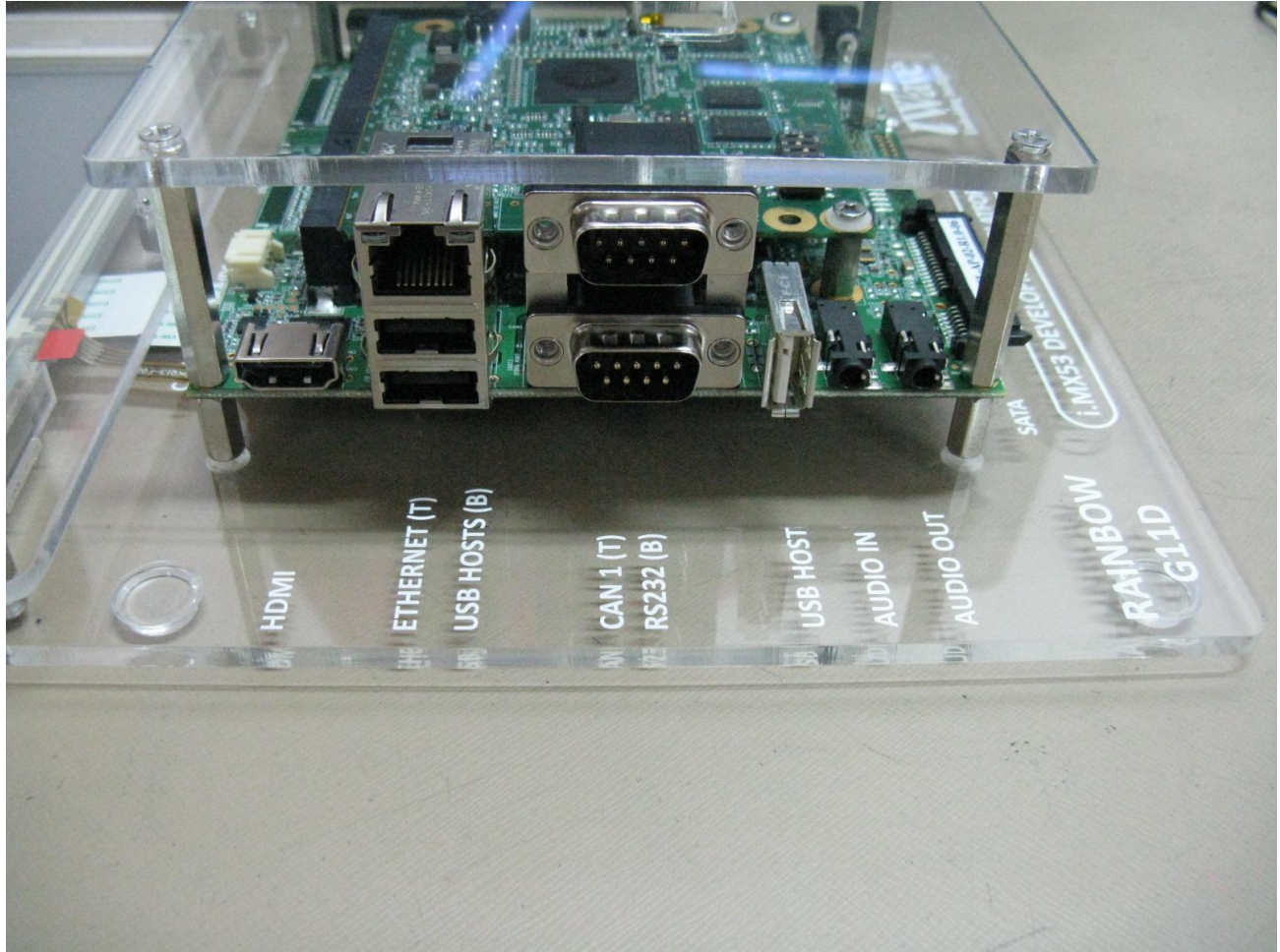


Figure 1:iMX53-Carrier Card Connector Details-1



Figure 2:iMX53-Carrier Card Connector Details-2

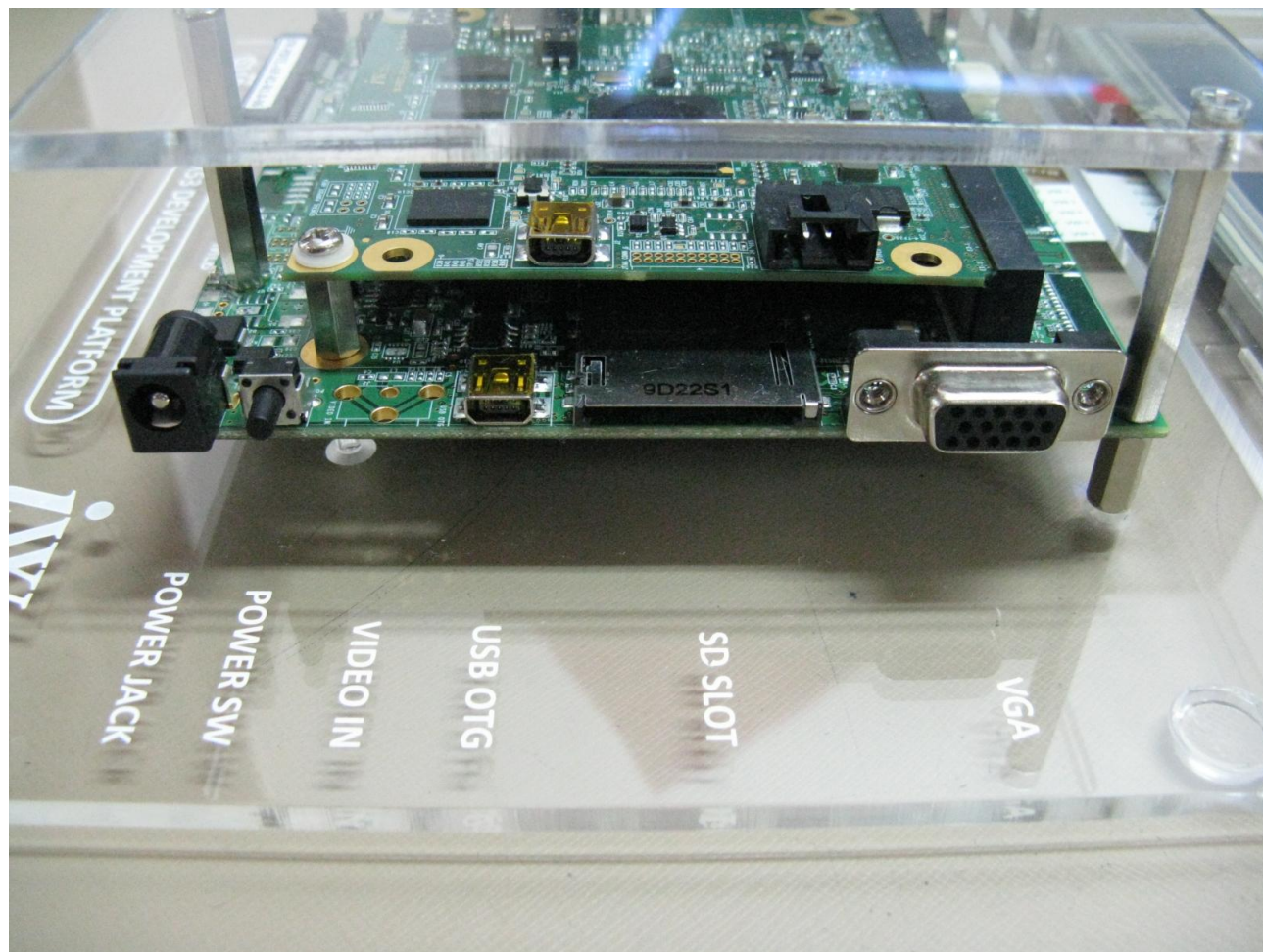


Figure 3: iMX53-Carrier Card Connector Details-3

2.2 Hardware Setup Details

2.2.1 Power Supply Connection Procedure

Insert the power plug of the power supply provided into the power jack of the iMX53-Carrier Card as shown below.

Power Rating: 5V input with 2.5A.

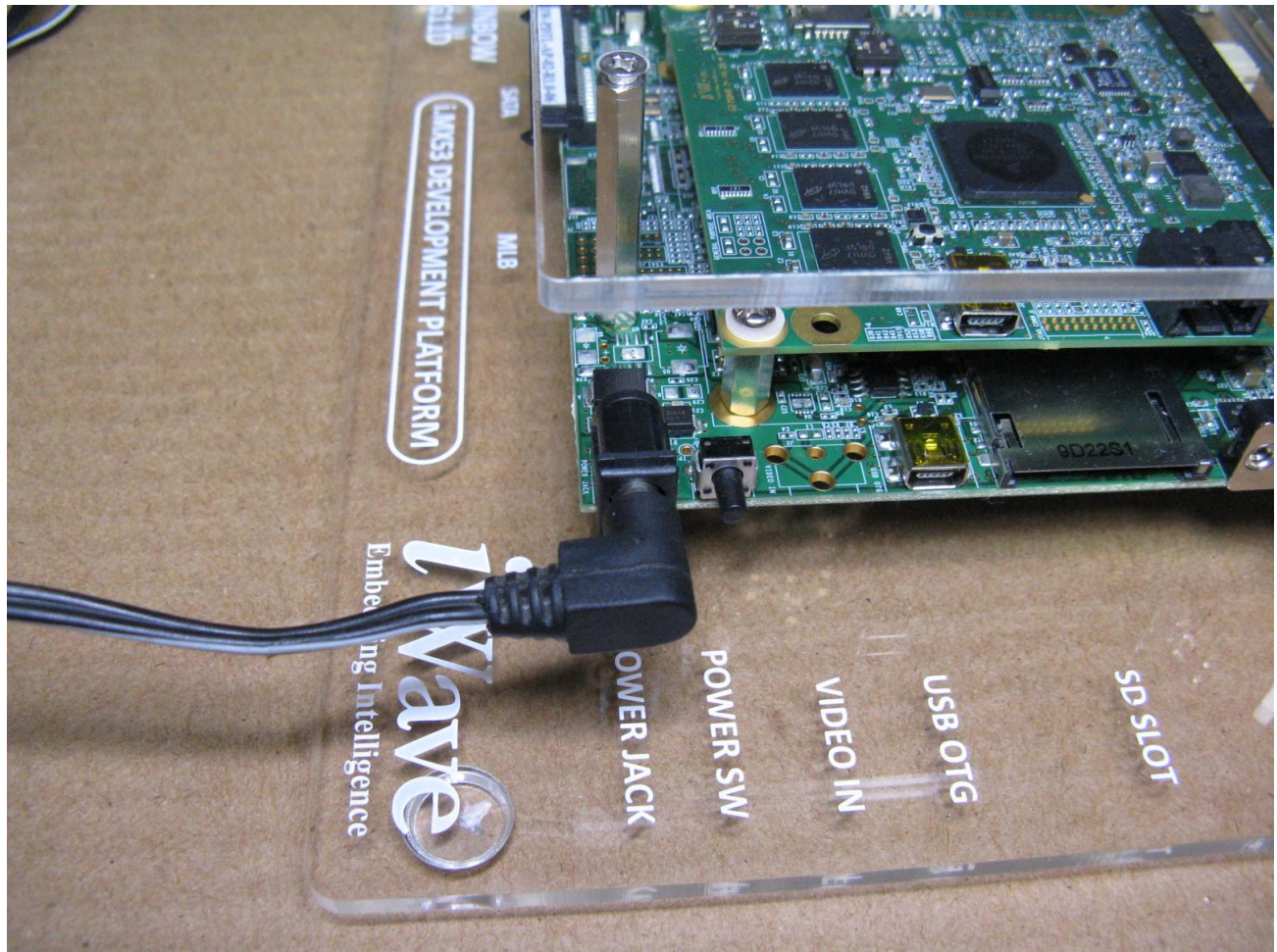


Figure 4: iMX53-Carrier Card Power Connection

2.2.2 Serial Cable Connection Procedure

1. Serial cable provided has DB9 connector (Female type) at both end.
2. Insert DB9 of the serial cable to PC/Laptop COM port.
3. Connect other end of the serial cable to iMX53 carrier board serial port connector (Bottom) as shown below.

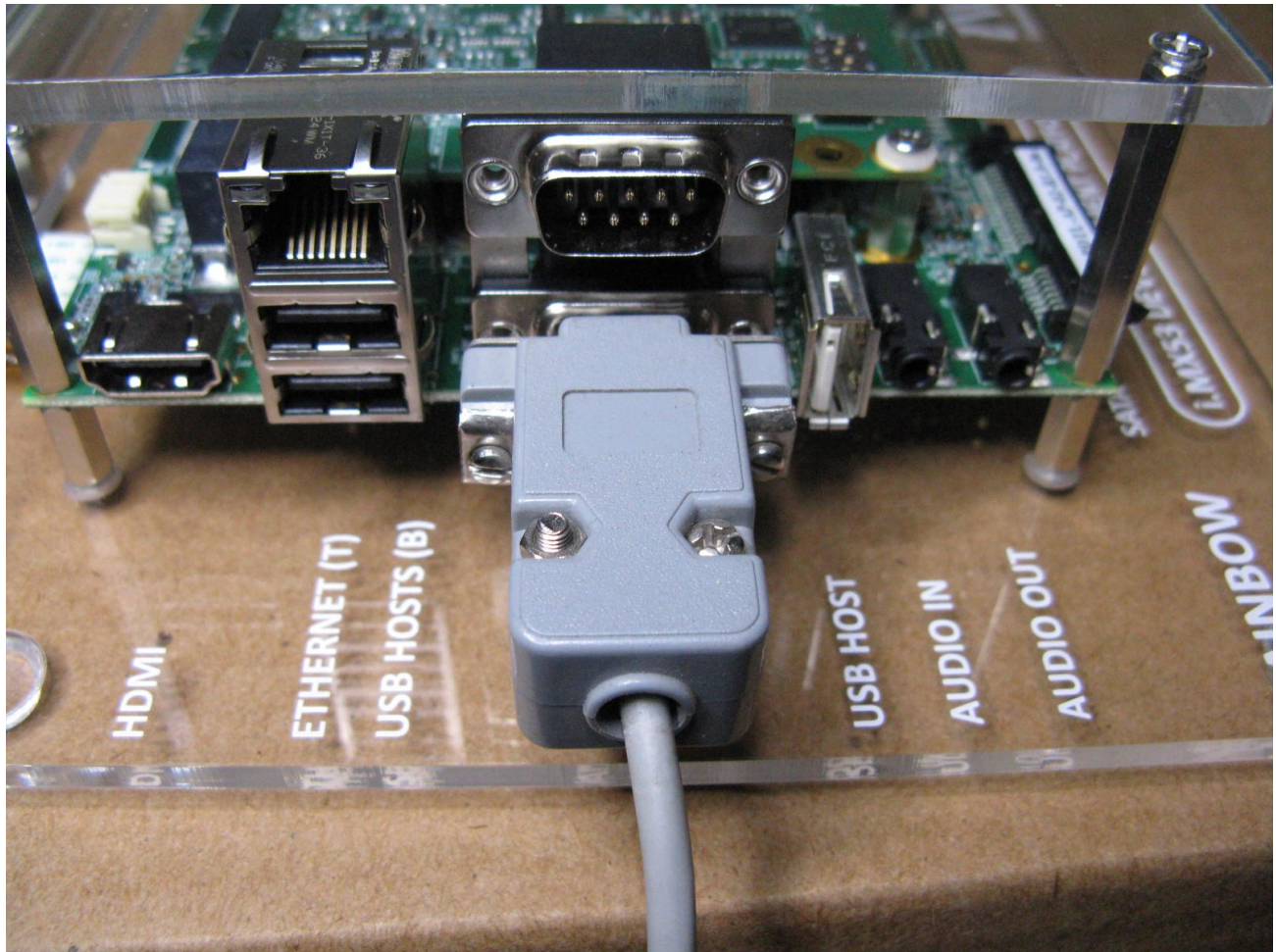


Figure 5: Serial Port Connection

The RS232 port pin outs are as in below table.

Table 2: RS232 port pin assignment

Pin No	Signal Name	Description
2	RXD	Receive Data(Input)
3	TXD	Transmit Data (Output)
5	GND	Ground
1,4,6,7,8,9	NC	No connection

2.2.3 USB OTG Connection Procedure

Insert the USB Device Mini B cable to the USB OTG connector as shown below & other end to HOST PC/Laptop.

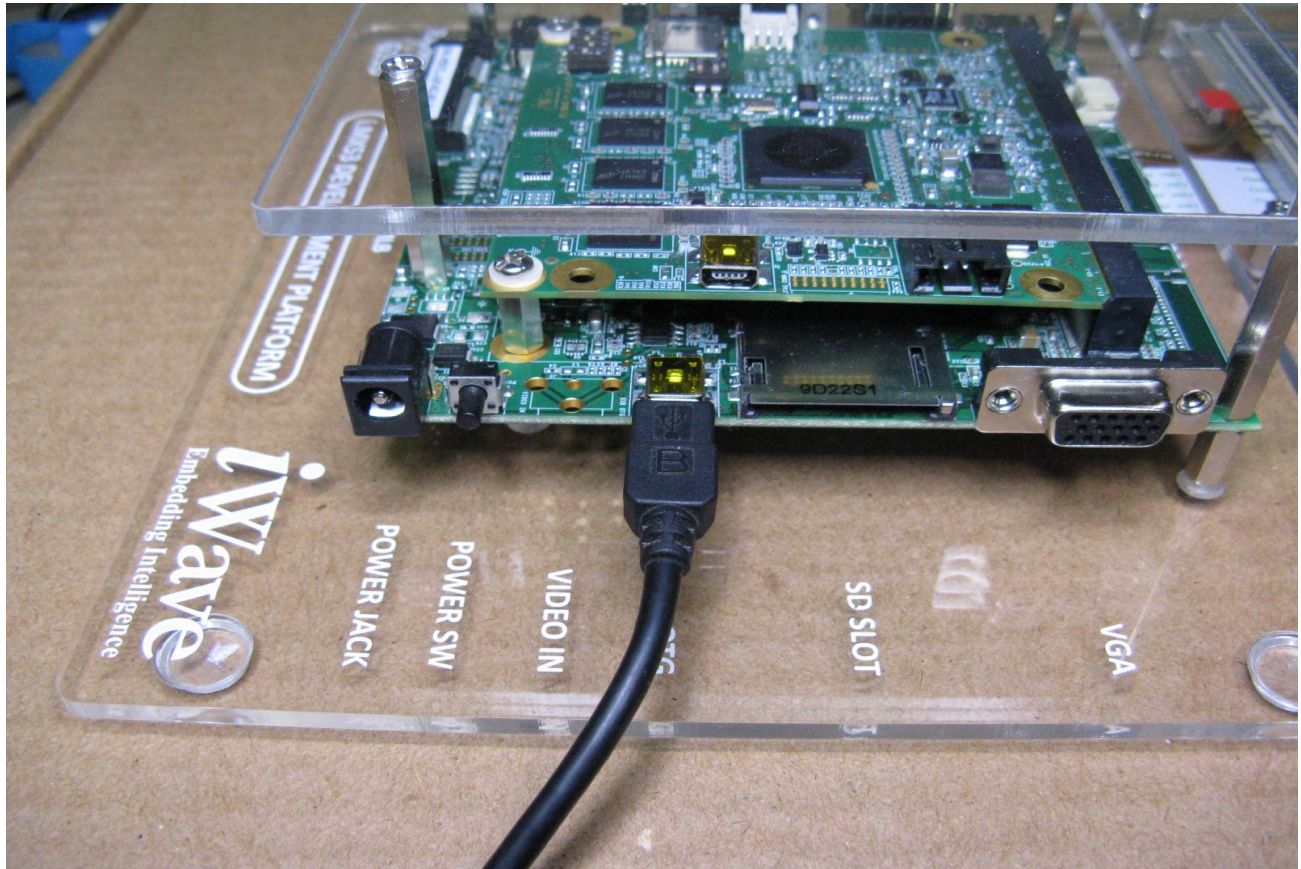


Figure 6: USB Device Connection

The USB OTG connector pin outs are as in below table.

Table 3: USB OTG connector pin assignment

Pin No	Signal Name	Description
1	VBUS_OTG	VBUS Supply
2	USB_OTG_DATA-	Data pair (IO)
3	USB_OTG_DATA+	
4	USB_ID	USB ID pin Float to act as a Device GND to act as a Host
5	GND	Ground

2.2.4 SD2/MMC Connection Procedure

Insert the SD Memory card in the 4 bit SD slot as shown below.

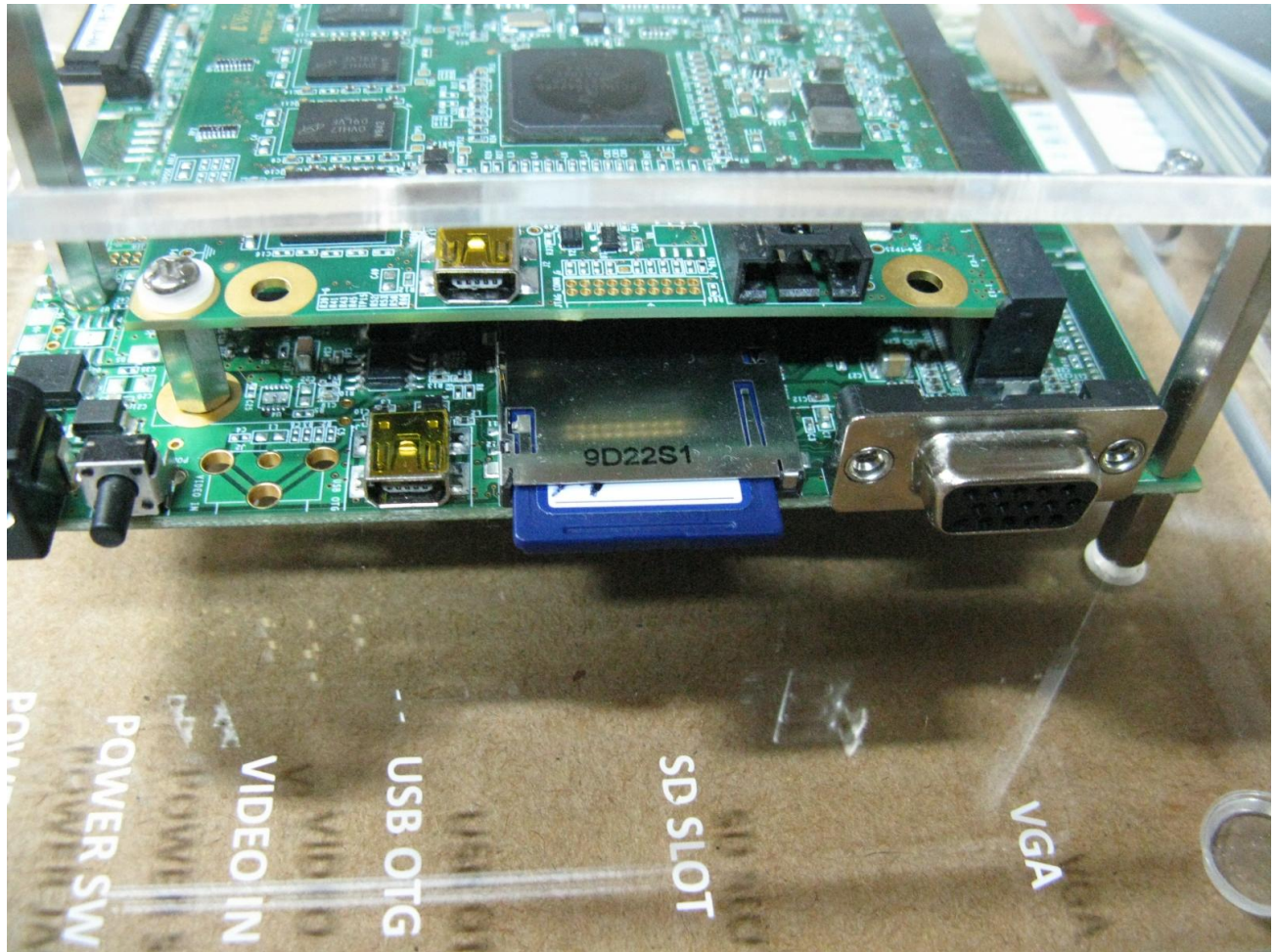


Figure 7: SD Connection

2.2.5 Audio In Cable Connection Procedure

Insert the Audio IN jack into the Audio in connector as shown below.

Note: Here the **RED color** cable is used to denote the audio input.

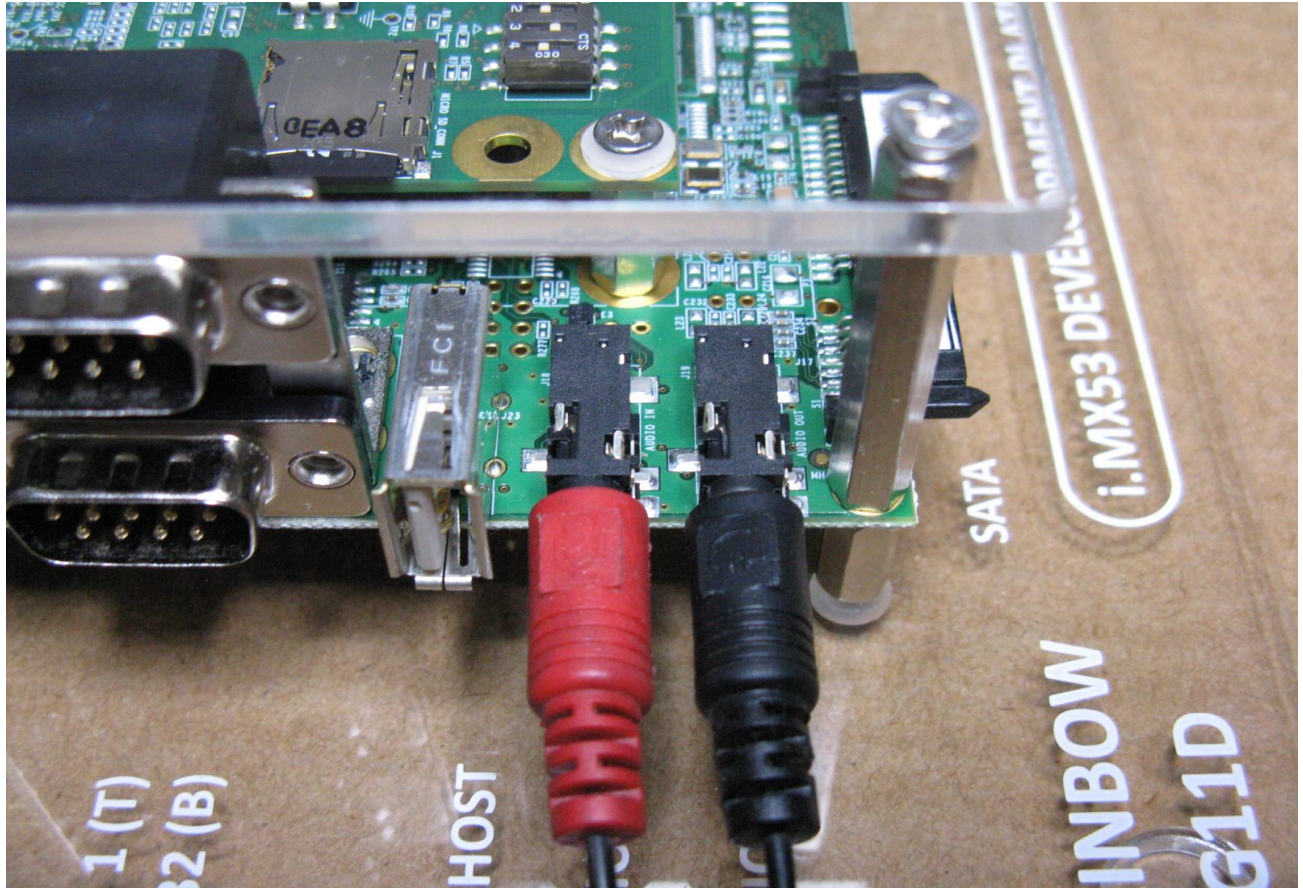


Figure 8: Audio In Connection

2.2.6 Audio Out Cable Connection Procedure

Insert the Audio OUT jack into the Audio out connector as shown below.

Note: Here the **Black color** cable is used to denote the audio output.

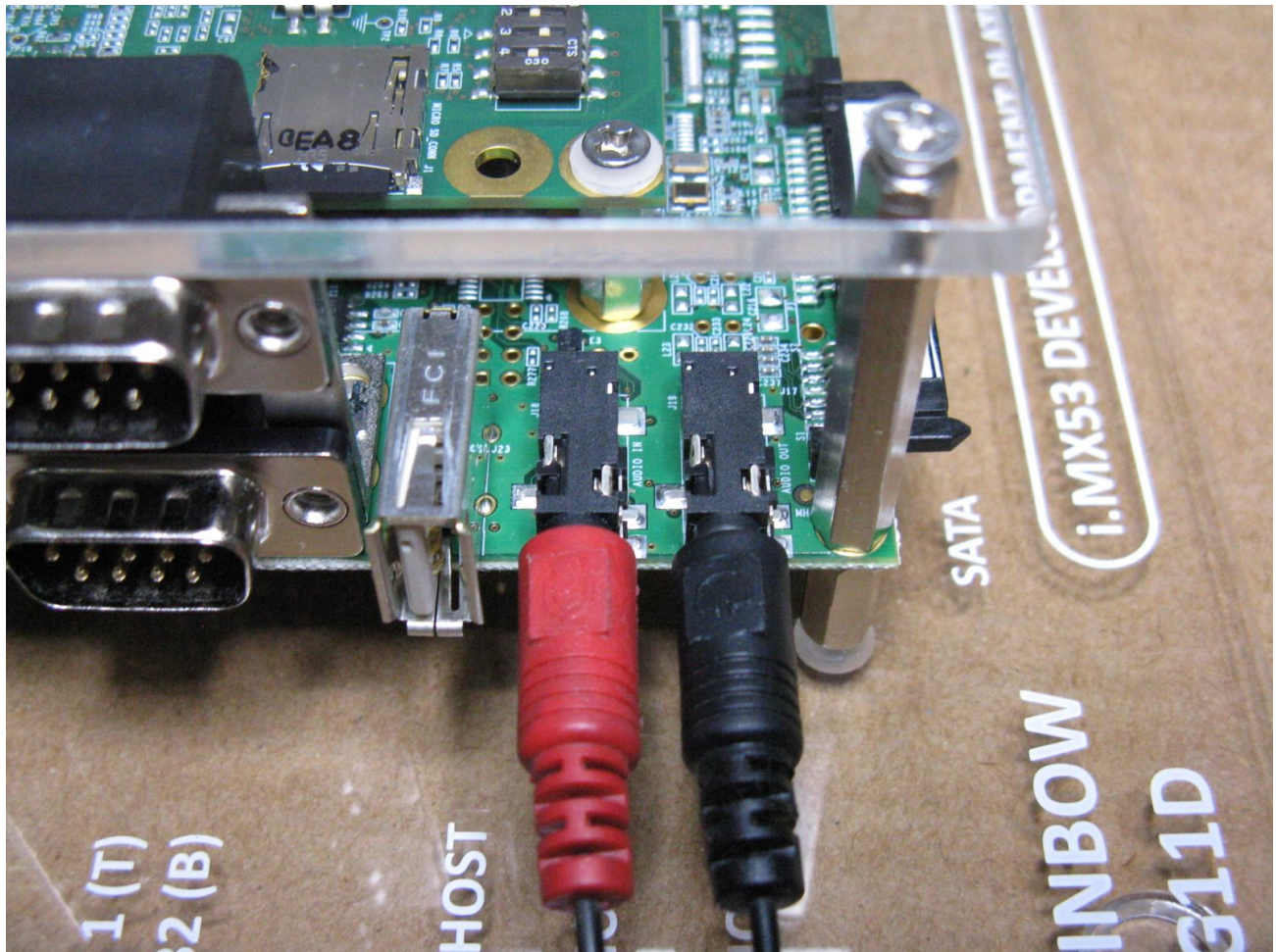


Figure 9: Audio Out Connection

2.2.7 VGA Cable Connection Procedure

Insert the VGA cable **carefully** into the into the VGA (DB15) connector. While removing the cable hold the VGA connector & then pull out the cable **carefully**.

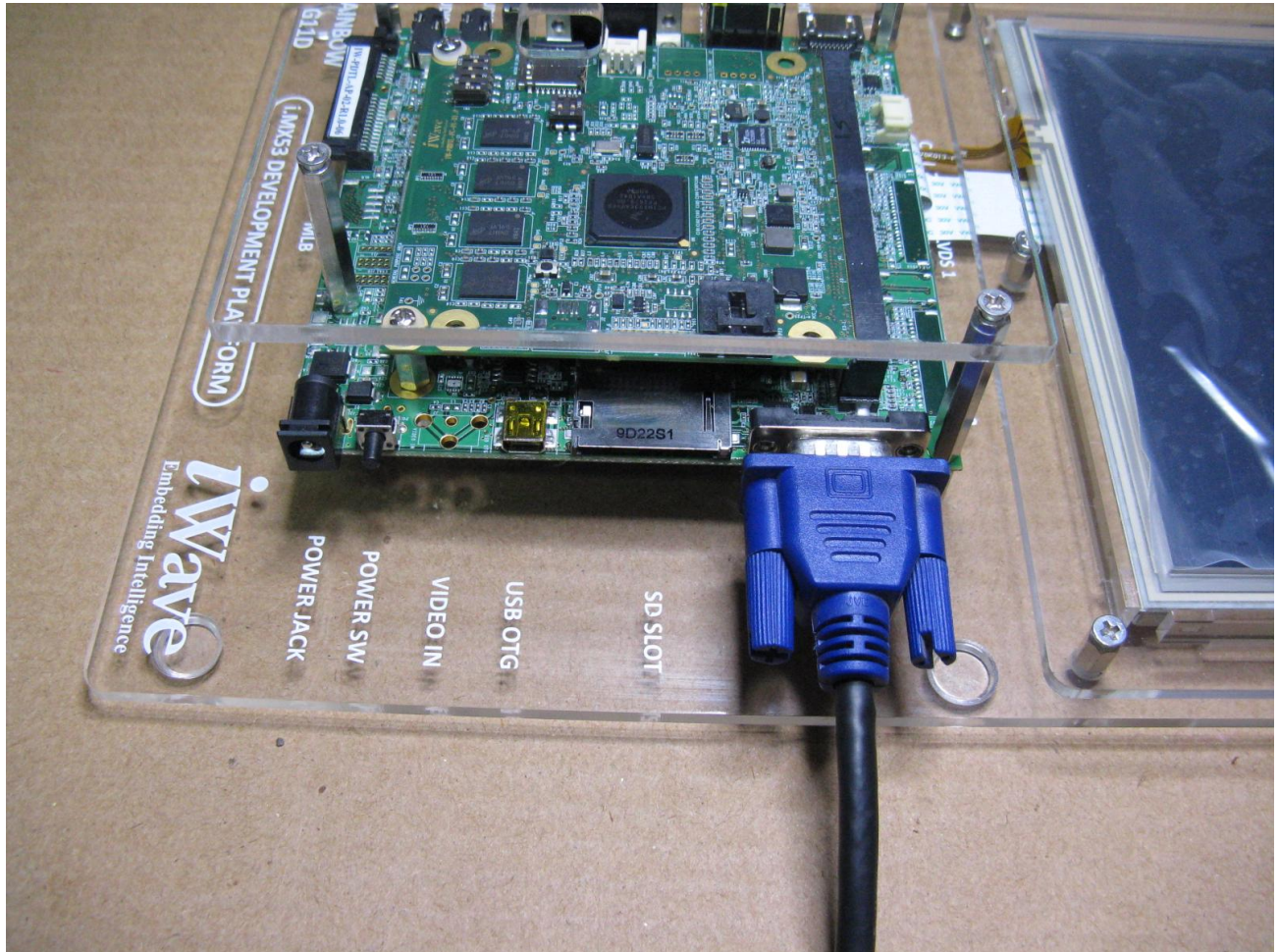


Figure 10: VGA Cable Connection

2.2.8 Ethernet Cable Connection Procedure

Insert the Ethernet cable into the RJ-45 Magjack connector as shown below.

Ignore the Green color LED glowing on the connector before inserting the cable.

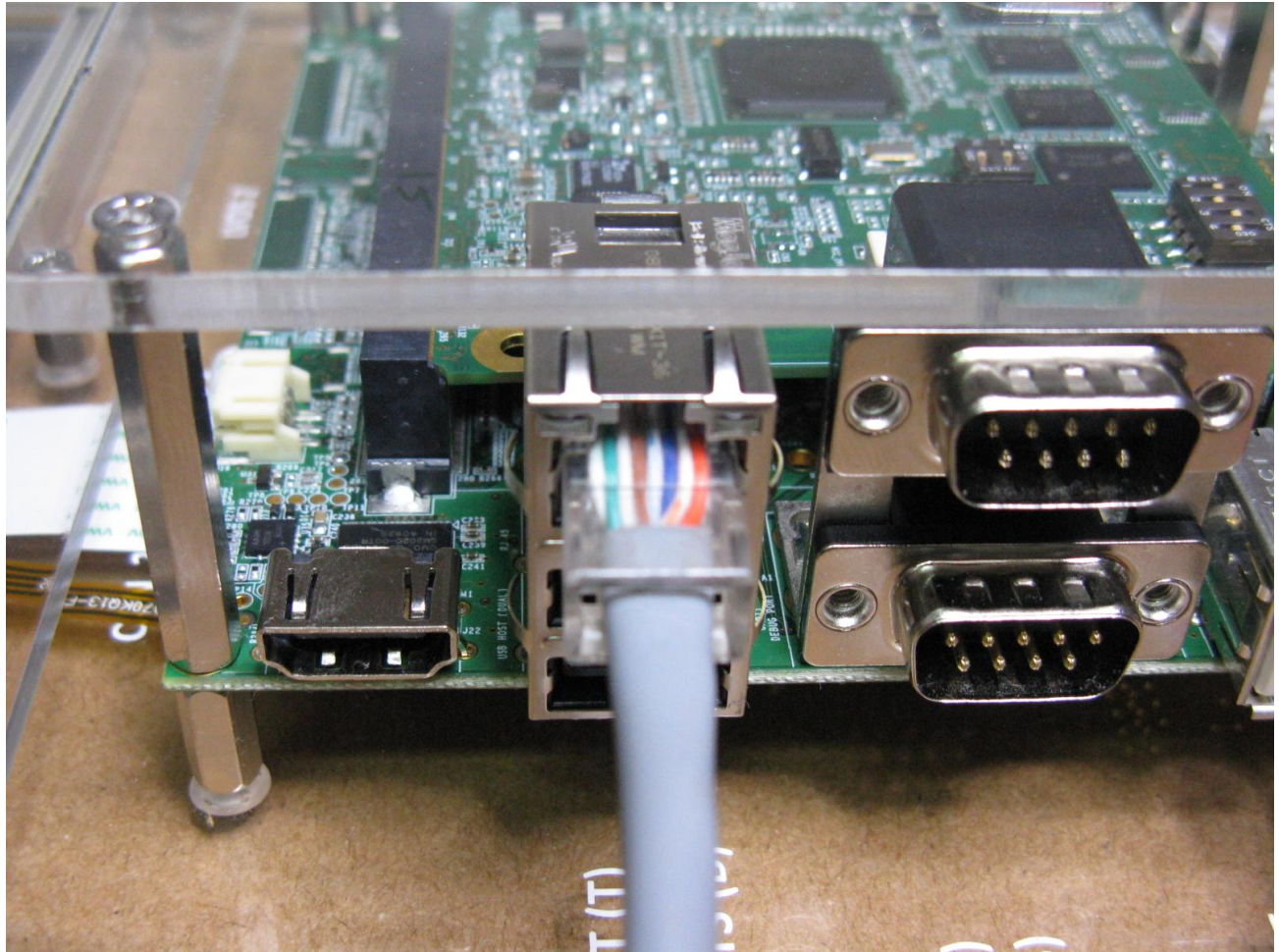


Figure 11: Ethernet Connection

2.2.9 USB Host 1 Connection Procedure

Insert the USB device (ex : USB cable) to the USB Host1 connector (Standard Type A) as shown below.

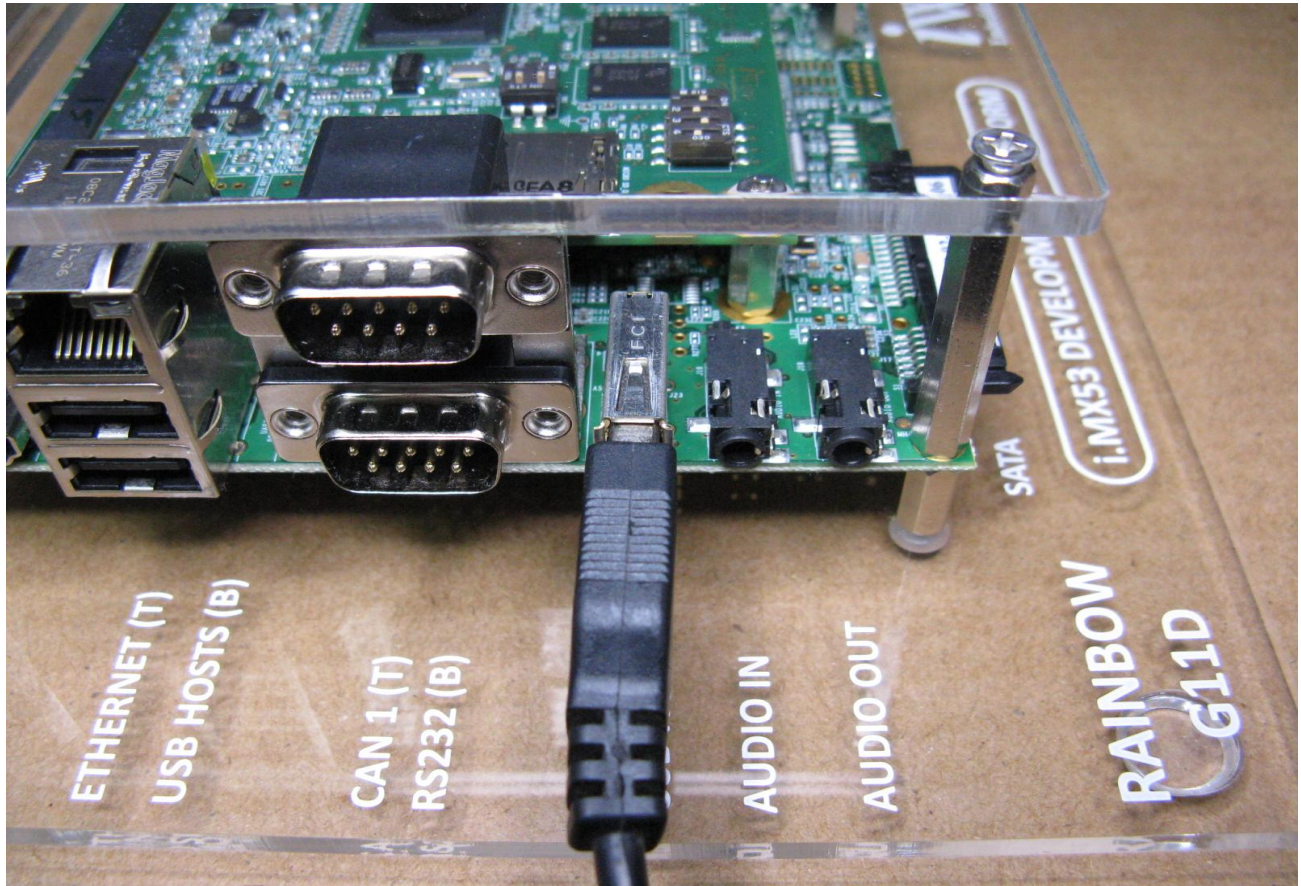


Figure 12: USB Host1 Connection

2.2.10 USB Host 2 Connection Procedure

Insert the USB device (ex : USB cable) to the USB Host 2 connector (Standard Type A) as shown below.

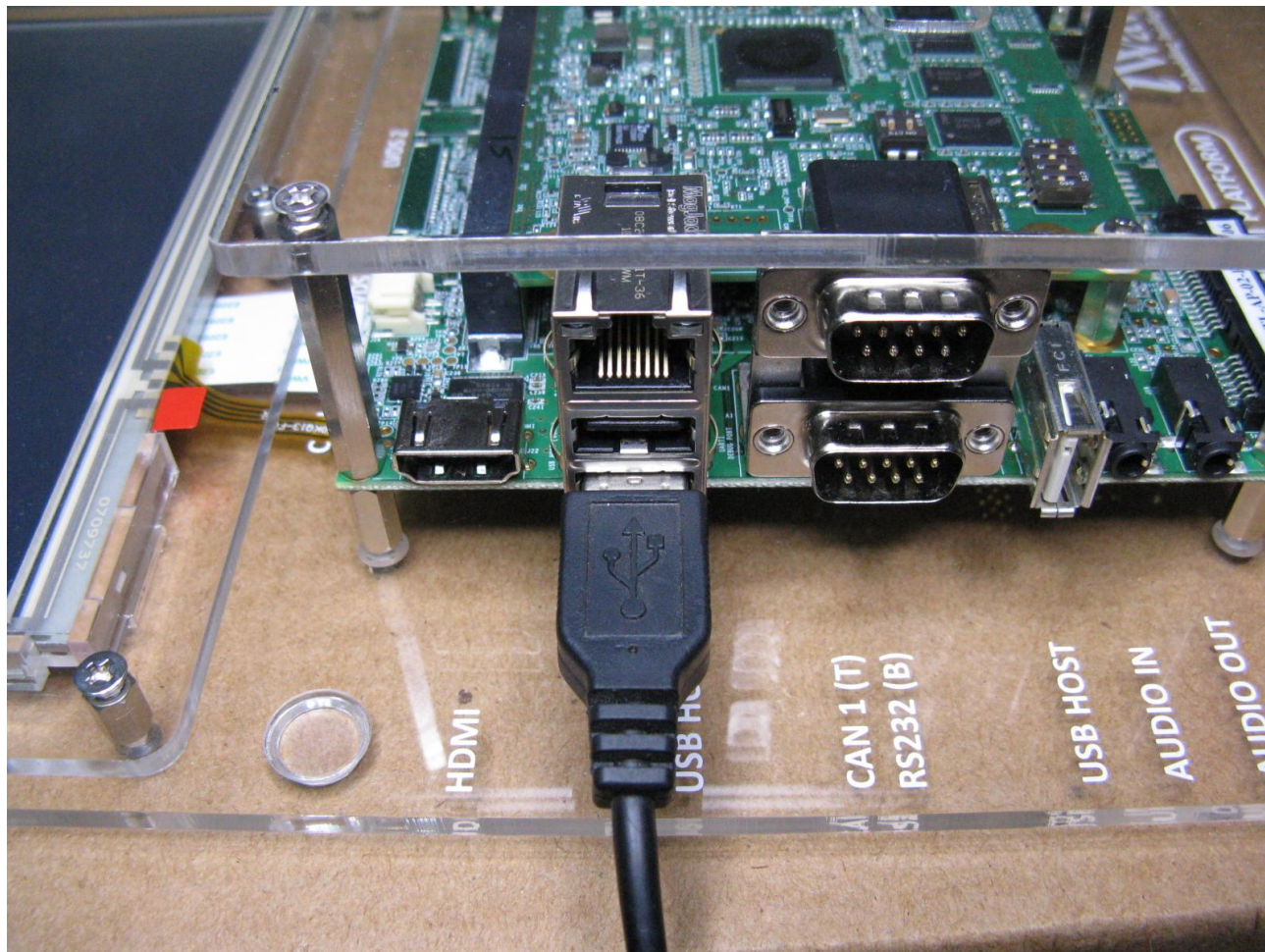


Figure 13: USB Host 2 Connection

2.2.11 USB Host 3 Connection Procedure

Insert the USB device (ex : USB cable) to the USB Host 3 connector (Standard Type A) as shown below.

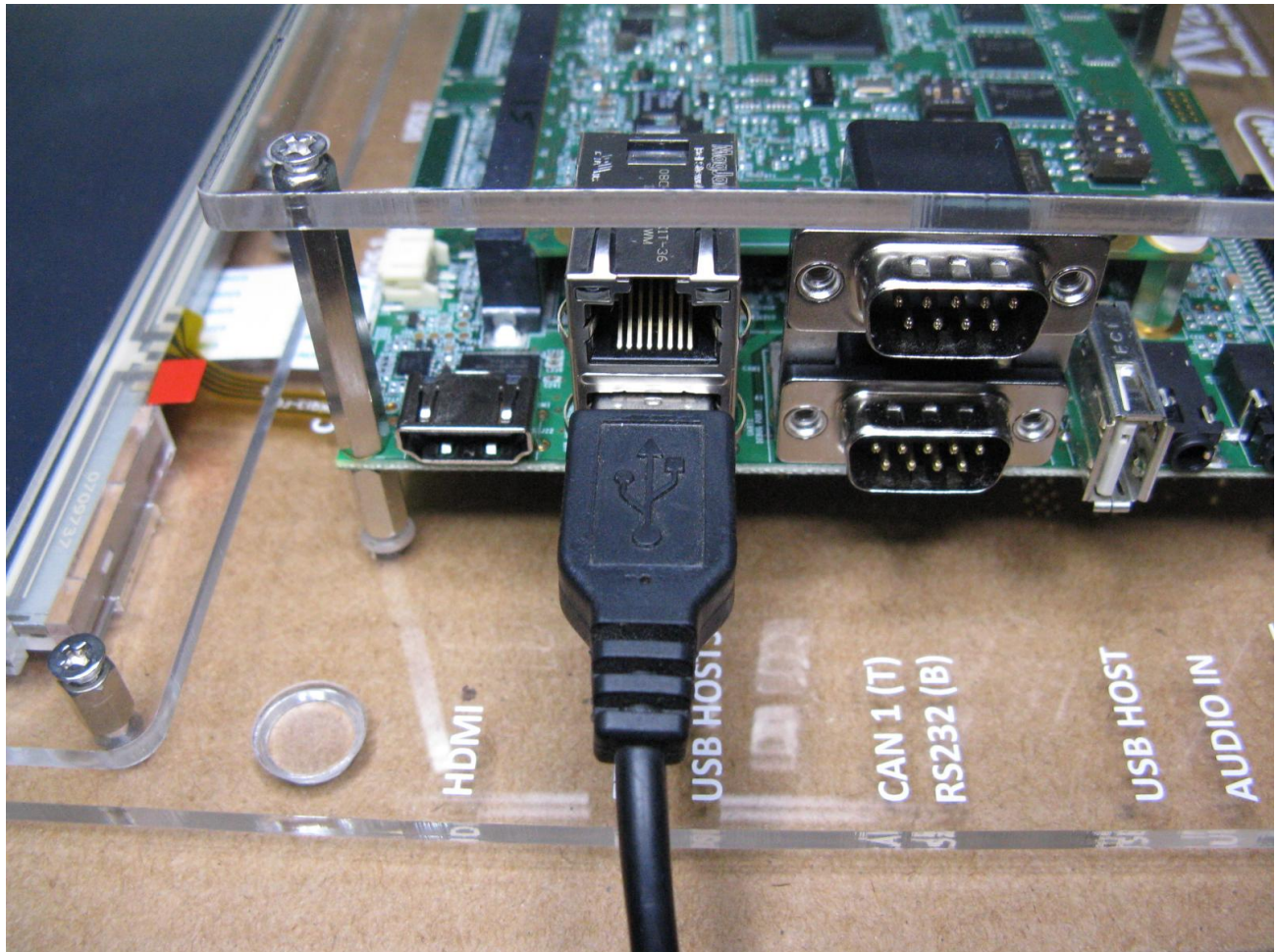


Figure 14: USB Host 3 Connection

2.2.12 CAN Connection Procedure

CAN Devices can be connected to the CAN port (TOP) provided as shown below.

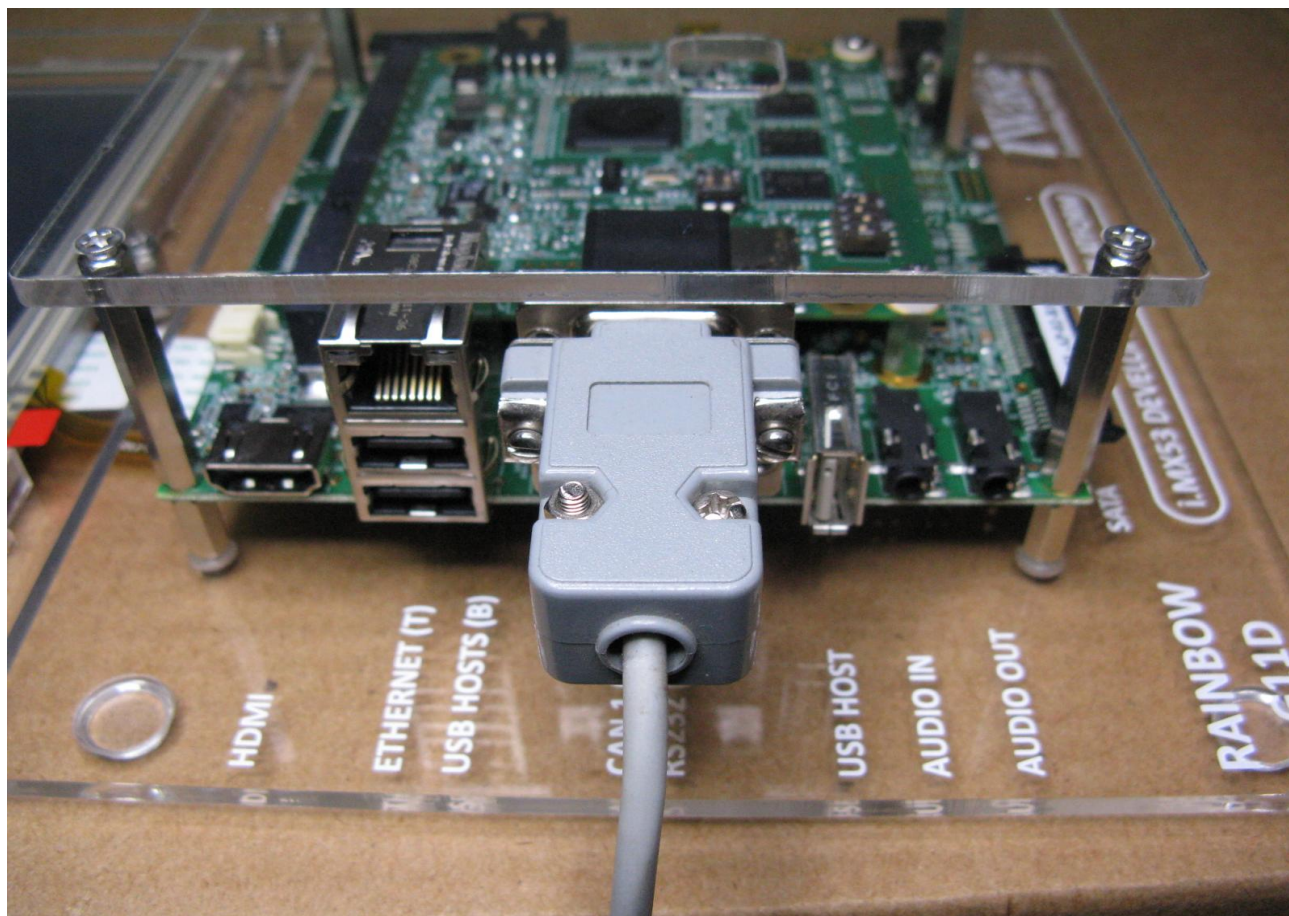


Figure 15: CAN Connection

The connector pin outs are shown in below table.

Table 4: CAN port pin assignment

Pin No	Signal Name	Description
2	CAN1H	Dominant High
7	CAN1L	Dominant Low
3,6	GND	Ground
1,4,5,8,9	NC	No connection

2.2.13 SATA Connection Procedure

Insert the 2.5" SATA HDD to the 22 pin SATA connector as shown below. Presently only 5V @1A supply is provided through the connector, since almost all the 2.5" SATA HDD requires only 5V.



Figure 16: SATA Connection

3 iMX53 – Carrier Card Connector Pin Assignments

3.1 iMX53 – Carrier Card Top

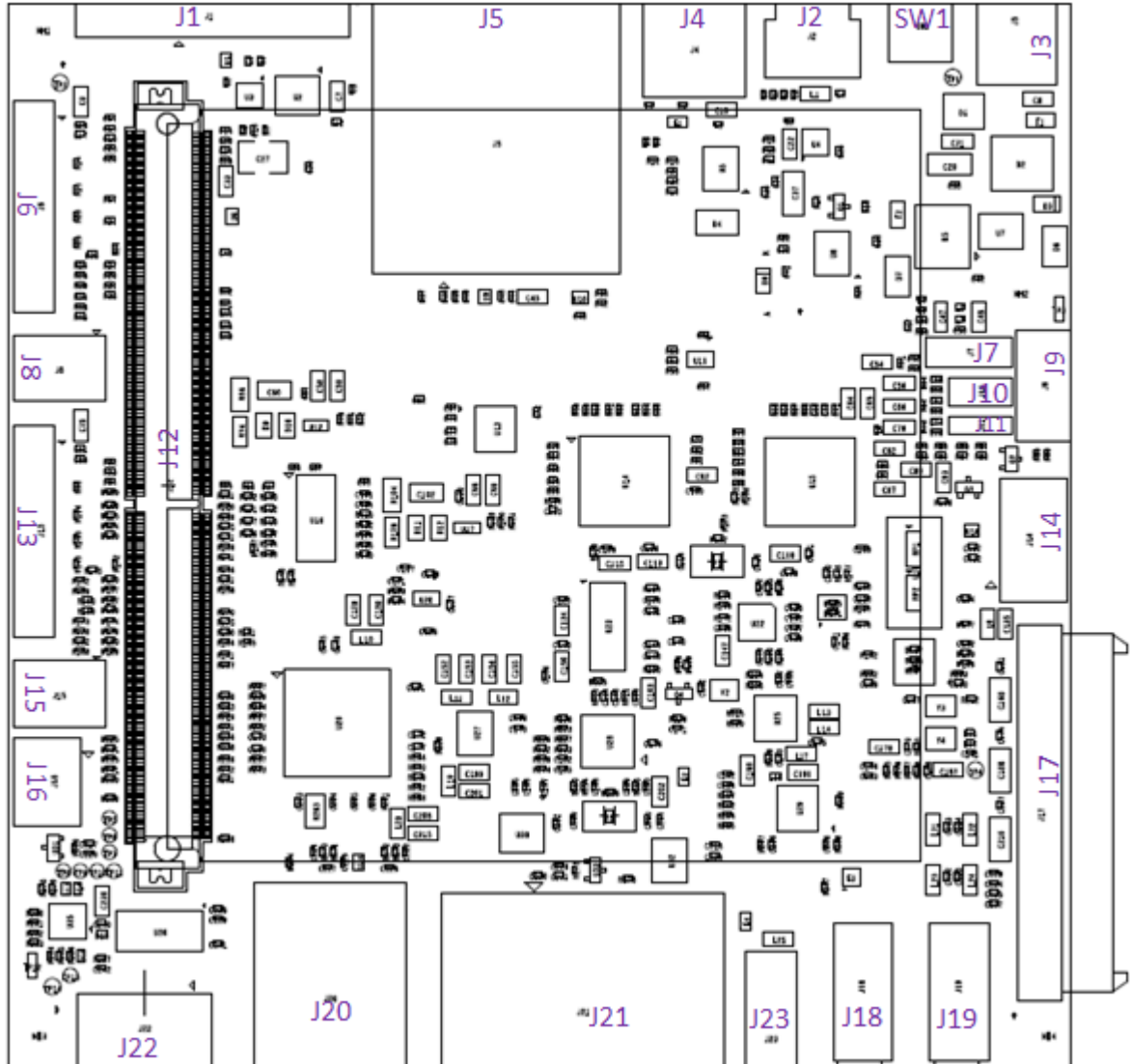


Figure 17: iMX53 – Carrier Card Top

Above Figure Shows the Carrier card connector reference numbers on top side.
Following are the list of Connectors on Top.side

- VGA Connector(J1)
- RCA Jack for Video In(J2)
- Power Jack(J3)
- USB OTG Mini AB Connector(J4)
- SD Connector(J5)
- LVDS Connector-1(J6)

- MOST JTAG Header(J7)
- MOST Connector(J9)
- 10pin_50mil header for ESAI Audio out(J10)
- 5pin_50mil header for ESAI Audio In(J11)
- 314 Pin MXM 3 RVS Connector(J12)
- LVDS Connector-0(J13)
- MLB Header(J14)
- CAN2 Header(J16)
- 22 Pin SATA Connector(J17)
- Audio In Jack(J18)
- Audio Out Jack(J19)
- RJ45/MagJack(J20)
- Dual DB9 Connector(J21)
- HDMI Connector(J22)
- USB Type A Connector(J23)

3.2 iMX53 – Carrier Card Bottom

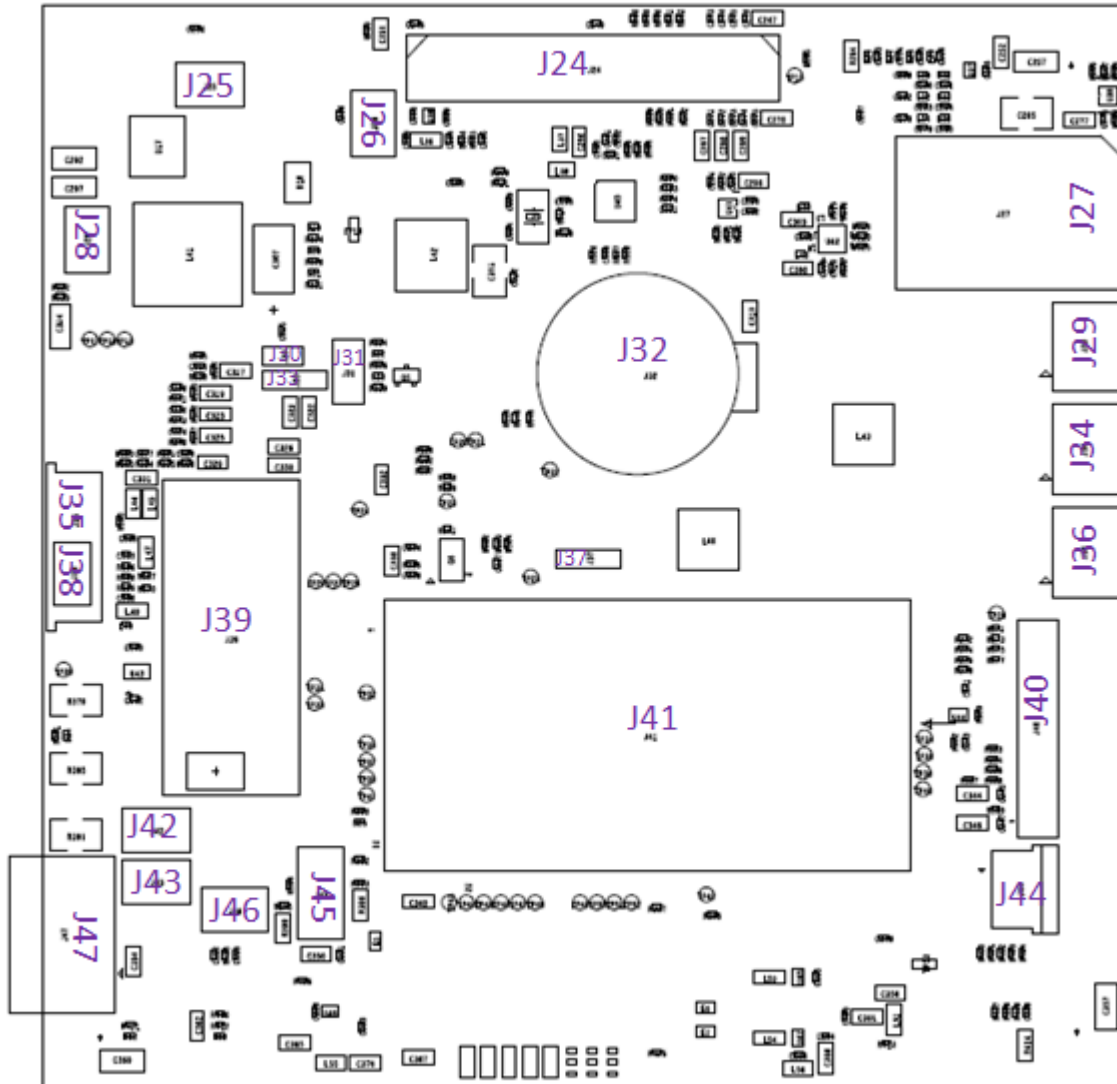


Figure 18: iMX53 – Carrier Card Bottom

Above Figure Shows the Carrier card connector reference numbers on bottom side.
Following are the list of Connectors on Bottom.side

- Expansion Connector(J24)
- Battery Charging Header(J25)
- 2 Pin Header For Video In(J26)
- SIM Connector(J27)

- FAN Circuit Header(J28)
- 3 Pin Header for UART5 interface(J29)
- 3 Pin_50mil Header for SPDIF Interface(J30)
- 10pin_50mil Header for ESAI Audio out(J31)
- 2 Pin Header for RTC Battery(J32)
- 5pin_50mil Header For ESAI Audio In(J33)
- 3 Pin Header for UART4 interface(J34)
- Camera Connector(J35)
- 3 Pin Header for UART3 interface(J36)
- 5 Pin_50mil Header for UART2 Interface(J37)
- Camera Connector(J38)
- WIFI Module Connector(J39)
- LCD Connector(J40)
- PCIe Connector(J41)
- 2 Pin Header for Speaker Out Left(J42)
- 2 Pin Header for Speaker Out Right(J43)
- Touch Connector(J44)
- 2G Module Connector(J45)
- MIC Connector(J46)
- 7-Pin SATA Connector(J47)

3.2.1 VGA Connector Pin Assignment (J1)

Pin	Signal Name	Direction	Description
1	TV_IOR	Output	Red Signal
2	TV_IOG	Output	Green Signal
3	TV_IOB	Output	Blue Signal
4	NC		No Connection
5	GND		Ground
6	GND		Ground
7	GND		Ground
8	GND		Ground
9	VCC_5V	Power	5V Power
10	GND		Ground
11	NC		No Connection
12	I2C2_DATA	IO	I2C2 Data
13	HSYNC	Output	Horizontal Synchronization
14	VSYNC	Output	Vertical Synchronization
15	I2C2_CLK	IO	I2C2 Clock
16	SHLD1		Shielding1
17	SHLD2		Shielding2

Table 5: VGA Connector pin assignment

3.2.2 RCA Jack for Video In Pin Assignment (J2)

Note: Not Mounted

Pin	Signal Name	Description
1	GND	Ground
2	VIDEO_IN_A	TV Input
3	GND	Ground
4	GND	Ground

Table 6: RCA Jack pin assignment

3.2.3 Power Jack Pin Assignment (J3)

Pin	Signal Name	Description
1	VCC_IN	Input Power (5V)
2	GND	Ground
3	GND	Ground

Table 7: Power Jack pin assignment

3.2.4 USB OTG Mini AB Connector Pin Assignment (J4)

Pin No	Signal Name	Direction	Description
1	VBUS_OTG		OTG Power
2	USB_OTG_DATA-	IO	Data Port -
3	USB_OTG_DATA+	IO	Data Port +
4	USB_ID	Input	Identification
5	GND		Ground

Table 8: USB Mini AB Connector pin assignment

3.2.5 SD Connector Pin Assignment (J5)

Pin	Signal Name	Direction	Description
1	SD1_DATA3	IO	Data3 Signal
2	SD1_CMD	IO	Command Signal
3	GND		Ground

4	VCC_3V3	Power	3.3V power
5	SD1_CLK	Output	Clock signal
6	GND		Ground
7	SD1_DATA0	IO	Data0
8	SD1_DATA1	IO	Data1
9	SD1_DATA2	IO	Data2
10	SD1_CD	Input	Card Detect
11	GND		Ground
12	SD_WP	Input	Write Protect

Table 9: SD Connector pin assignment

3.2.6 LVDS Connector Pin Assignment (J6)

Note: Not Mounted

Pin	Signal Name	Direction	Pin	Signal Name	Direction
1	VCC_3V3	Power	11	LVDS1_2-	Output
2	VCC_3V3	Power	12	LVDS1_2+	Output
3	GND		13	GND	
4	GND		14	LVDS1_CLK-	Output
5	LVDS1_0-	Output	15	LVDS1_CLK+	Output
6	LVDS1_0+	Output	16	GND	
7	GND		17	LVDS1_3-	Output
8	LVDS1_1-	Output	18	LVDS1_3+	Output
9	LVDS1_1+	Output	19	MODE_LVDS1	Pull up/down option
10	GND		20	SC_LVDS1	Pull up/down option

Table 10: LVDS Connector1 pin assignment

3.2.7 MOST JTAG Header Pin Assignment (J7)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	NC		No Connection
2	GND		Ground
3	NC		No Connection
4	GPIO3_20	IO	GPIO
5	GND		Ground
6	VCC_3V3	Power	3.3V Supply
7	JTAG_TDI	Input	Test data input
8	JTAG_TCK	Input	Test clock
9	VCC_3V3	Power	3.3V Supply
10	GND		Ground
11	JTAG_TDO	Output	Test data output
12	B_RESET_OUTn	Output	Reset signal
13	NC		No Connection
14	JTAG_TMS	Input	Test mode select

Table 11: MOST JTAG Header pin assignment

3.2.8 MOST Connctor Pin Assignment (J9)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	TX	Output	Transmit signal
2	FOT_TXVCC	Power	Transmit Power
3	NC		NC
4	FOT_RXVCC	Power	Receive Power
5	GND		Ground
6	GND		Ground
7	FOT_STATn	Input	Status input

8	GND		Ground
9	RX	Input	Receive signal
10	GND		Ground

Table 12: MOST Connector pin assignment

3.2.9 ESAI Audio Out Connector Pin Assignment (J10)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	AOUT_1	Output	Audio output signal
2	AOUT_2	Output	Audio output signal
3	AOUT_3	Output	Audio output signal
4	AOUT_4	Output	Audio output signal
5	AOUT_5	Output	Audio output signal
6	AOUT_6	Output	Audio output signal
7	AOUT_7	Output	Audio output signal
8	AOUT_8	Output	Audio output signal
9	GND		GND
10	GND		GND

Table 13: ESAI Audio Out Connector pin assignment

3.2.10 ESAI Audio In Connector Pin Assignment (J11)

Pin	Signal Name	Direction	Description
1	AIN_1	Input	Audio input signal
2	AIN_2	Input	Audio input signal
3	AIN_3	Input	Audio input signal
4	AIN_4	Input	Audio input signal
5	GND		Ground

Table 14: ESAI Audio In Connector pin assignment

3.2.11 314 Pin MXM 3 Connector Top Pin Assignments (J12)

Pin No	Signal Name	IO Level	Direction w.r.t SOM	Out of Reset Condition-Block IO	Description/ i.MX53 Ball name
E1-1	VCC (5V)	5V	Input		Main Input to the Board
E1-2	VCC (5V)				
E1-3	VCC (5V)				
E1-4	VCC (5V)				
E1-5	VCC (5V)				
E1-6	NC				
E1-7	NC				
E1-8	NC				
E1-9	GND	GND			
E1-10	LVDS1_TX1_P	2.5V	Output	gpio6_GPI[28]	Ball: AB13
E3-1	LVDS1_TX1_N	2.5V	Output	gpio6_GPI[29]	Ball: AC13
E3-2	GND	GND			
E3-3	LVDS1_TX0_P	2.5V	Output	gpio6_GPI[30]	Ball: AB14
E3-4	LVDS1_TX0_N	2.5V	Output	gpio6_GPI[31]	Ball: AC14
E3-5	GND	GND			
E3-6	LVDS1_CLK_P	2.5V	Output	gpio6_GPI[26]	Ball: Y13
E3-7	LVDS1_CLK_N	2.5V	Output	gpio6_GPI[27]	Ball: AA13
E3-8	GND	GND			
E3-9	LVDS1_TX2_N	2.5V	Output	gpio6_GPI[25]	Ball: AC12
E3-10	LVDS1_TX2_P	2.5V	Output	gpio6_GPI[24]	Ball: AB12
1	GND	GND			

3	LVDS1_TX3_P	2.5V	Output	gpio6_GPI[22]	Ball: Y12
5	LVDS1_TX3_N	2.5V	Output	gpio6_GPI[23]	Ball: AA12
7	GND	GND			
9	NANDE_WE_B	3.3V	IO	gpio6_GPIO[12]	Ball : AB8
11	NANDE_RE_B	3.3V	IO	gpio6_GPIO[13]	Ball : AC8
13	EIM_WAIT	3.3V	IO	emi_EIM_WAIT	Ball: AB9
15	CSIO_PIXCLK	3.3V	IO	gpio5_GPIO[18]	Ball: P1
17	CSIO_MCLK	3.3V	IO	gpio5_GPIO[19]	Ball: P2
19	CSIO_DATA_EN	3.3V	IO	gpio5_GPIO[20]	Ball: P3
21	DI0_PIN4	2.8V	IO	gpio4_GPIO[20]	Ball:D2
23	EIM_D26	3.3V	IO	gpio3_GPIO[26]	Ball: V5
25	EIM_D27	3.3V	IO	gpio3_GPIO[27]	Ball: V4
27	S5_OFF(WAKE Signal from PMIC)	5V	Output		Low when CPU module power is off High during normal working (5V level signal)
29	EIM_D31	3.3V	IO	gpio3_GPIO[31]	Ball: W5
31	CSIO_VSYNC	3.3V	IO	gpio5_GPIO[21]	Ball: P4
33	NANDE_CLE	3.3V	IO	gpio6_GPIO[7]	Ball: AA10
35	NANDE_ALE	3.3V	IO	gpio6_GPIO[8]	Ball: Y11
37	NANDE_WP_B	3.3V	IO	gpio6_GPIO[9]	Ball: AC9
39	NANDE_RB0	3.3V	IO	gpio6_GPIO[10]	Ball: U11
41	PATA_DMARQ	3.3V	IO	gpio7_GPIO[0]	Ball: J1
43	PATA_BUFFER_EN	3.3V	IO	gpio7_GPIO[1]	Ball: K4
45	NC				
47	TVDAC_IOR	2.8V	IO	TVDAC_IOR	Ball:AC21
49	TVDAC_IQG	2.8V	IO	TVDAC_IQG	Ball:AB20
51	TVDAC_IQB	2.8V	IO	TVDAC_IQB	Ball:AC19
53	NC				
55	NANDE_CS0	3.3V	GPIO	gpio6_GPIO[11]	Ball: W12
57	GND	GND			
59	LVDS0_CLK_P	2.5V	Output	gpio7_GPI[24]	Ball: AC16
61	LVDS0_CLK_N	2.5V	Output	gpio7_GPI[25]	Ball: AB16
63	LVDS0_TX0_P	2.5V	Output	gpio7_GPI[30]	Ball: AA17
65	LVDS0_TX0_N	2.5V	Output	gpio7_GPI[31]	Ball: Y17
67	LVDS0_TX1_P	2.5V	Output	gpio7_GPI[28]	Ball: AC17

69	LVDS0_TX1_N	2.5V	Output	gpio7_GPI[29]	Ball: AB17
71	GND	GND			
73	LVDS0_TX2_P	2.5V	Output	gpio7_GPI[26]	Ball: AA16
75	LVDS0_TX2_N	2.5V		gpio7_GPI[27]	Ball: Y16
77	LVDS0_TX3_P	2.5V	Output	gpio7_GPI[22]	Ball: AC15
79	LVDS0_TX3_N	2.5V	Output	gpio7_GPI[23]	Ball: AB15
81	GND	GND			
83	PATA_INTRQ	3.3V	IO	gpio7_GPIO[2]	Ball:K5
85	PATA_DIOR	3.3V	IO	gpio7_GPIO[3]	Ball:K3
87	GND	GND			
89	NC				
91	KEY_COL4	3.3V	IO	gpio4_GPIO[14]	Ball:E5
93	EIM_D30	3.3V	IO	gpio3_GPIO[30]	Ball:W4
95	NC				
97	GND	GND			
99	KEY_ROW2	3.3V	IO	gpio4_GPIO[11]	Ball: D5
101	KEY_COL2	3.3V	IO	gpio4_GPIO[10]	Ball: C4
103	EIM_DA9	3.3V	IO	emi_NAND_EIM _DA[9]	Ball: W10
105	EIM_DA10	3.3V	IO	emi_NAND_EIM _DA[10]	Ball:AB7
107	NC				
109	NC				
111	PATA_CS_0	3.3V	IO	gpio7_GPIO[9]	Ball: L5
113	PATA_CS_1	3.3V	IO	gpio7_GPIO[10]	Ball: L2
115	CSI0_DAT12	3.3V	IO	gpio5_GPIO[30]	Ball: T3
117	CSI0_DAT13	3.3V	IO	gpio5_GPIO[31]	Ball: T6
119	CSI0_DAT16	3.3V	IO	gpio6_GPIO[2]	Ball: T4
121	CSI0_DAT17	3.3V	IO	gpio6_GPIO[3]	Ball: T5
123	GND	GND			
125	CSI0_DAT18	3.3V	IO	gpio6_GPIO[4]	Ball: U3
133	CSI0_DAT19	3.3V	IO	gpio6_GPIO[5]	Ball: U4
135	CSI0_DAT15	3.3V	IO	gpio6_GPIO[1]	Ball: U2
137	CSI0_DAT14	3.3V	IO	gpio6_GPIO[0]	Ball: U1
139	GND	GND			
141	CSI0_DAT4	3.3V	IO	gpio5_GPIO[22]	Ball: R1
143	CSI0_DAT11	3.3V	IO	gpio5_GPIO[29]	Ball: T2
145	CSI0_DAT5	3.3V	IO	gpio5_GPIO[23]	Ball: R2

147	CSI0_DAT10	3.3V	IO	gpio5_GPIO[28]	Ball: R5
149	CSI0_DAT6	3.3V	IO	gpio5_GPIO[24]	Ball: R6
151	GPIO_0/GPIO_1*	3.3V	IO	gpio1_GPIO[0]	GPIO_0 connected by default
153	CSI0_DAT7	3.3V	IO	gpio5_GPIO[25]	Ball: R3
155	GND	GND			
157	GPIO_6	3.3V	IO	gpio1_GPIO[6]	Ball: B6
159	GPIO_2	3.3V	IO	gpio1_GPIO[2]	Ball: C7
161	GPIO_8	3.3V	IO	gpio1_GPIO[8]	Ball: B5
163	GPIO_17	3.3V	IO	gpio7_GPIO[12]	Ball: A3
165	GPIO_1	3.3V	IO	gpio1_GPIO[1]	Ball: B7
167	GPIO_18	3.3V	IO	gpio7_GPIO[13]	Ball: D7
169	GPIO_7	3.3V	IO	gpio1_GPIO[7]	Ball: A4
171	GPIO_9	3.3V	IO	gpio1_GPIO[9]	Ball: E8
173	GPIO_5*	3.3V	IO	gpio1_GPIO[5]	Not Connected (Ball:A5) Muxed with Pin 248
175	GPIO_16*	3.3V	IO	gpio7_GPIO[11]	Not Connected Ball: C6) Muxed with Pin 246
177	GPIO_4/DISP0_DAT22*	3.3V/ 2.8V	IO	gpio5_GPIO[16]	By default DISP0_DAT22 is connected
179	GPIO_3/DISP0_DAT20*	3.3V/ 2.8V	IO	gpio5_GPIO[14]	By default DISP0_DAT20 is connected
181	GND	GND			
183	KEY_COL0	3.3V	IO	gpio4_GPIO[6]	Ball: C5
185	KEY_COL1	3.3V	IO	gpio4_GPIO[8]	Ball: E7
187	GND	GND			
189	USB_H1_DN	2.5V, 3.3V	IO	USB_H1_DN	USB Host DATA- (Ball: B17)
191	USB_H1_DP	2.5V, 3.3V	IO	USB_H1_DP	USB Host DATA+ (Ball: A17)
193	GND	GND			
195	USB_OTG_VBUS	2.5V, 3.3V	Input	USB_OTG_VBUS	USB OTG VBUS (Ball: E15)

197	USB_OTG_ID	2.5V, 3.3V	Input	USB_OTG_ID	USB OTG ID (Ball: C16)
199	KEY_ROW4	2.5V, 3.3V	Output	gpio4_GPIO[15]	Ball: E6
201	USB_OTG_DP	2.5V, 3.3V	IO	USB_OTG_DP	USB OTG DATA+ (Ball: B19)
203	USB_OTG_DN	2.5V, 3.3V	IO	USB_OTG_DN	USB OTG DATA- (Ball: A19)
205	GND	GND			
207	NC				
209	GPIO_10	2.8V	IO	gpio4_GPIO[0]	Ball:W16
211	GND	GND			
213	GPIO_12	2.8V	IO	gpio4_GPIO[2]	Ball:W17
215	DISP0_DAT2	2.8V	IO	gpio4_GPIO[23]	Ball:H2
217	GPIO_13	2.8V	IO	gpio4_GPIO[3]	Ball:AA18
219	DISP0_DAT5	2.8V	IO	gpio4_GPIO[26]	Ball: H3
221	DISP0_DAT1	2.8V	IO	gpio4_GPIO[22]	Ball: J4
223	DI0_PIN3	2.8V	IO	gpio4_GPIO[19]	Ball: C2
225	DI0_PIN2	2.8V	IO	gpio4_GPIO[18]	Ball: D3
227	DISP0_DAT3	2.8V	IO	gpio4_GPIO[24]	Ball: F1
229	DISP0_DAT4	2.8V	IO	gpio4_GPIO[25]	Ball: G2
231	DISP0_DAT0	2.8V	IO	gpio4_GPIO[21]	Ball: J5
233	GND	GND			
235	DISP0_DAT11	2.8V	IO	gpio5_GPIO[5]	Ball: H5
237	DISP0_DAT9	2.8V	IO	gpio4_GPIO[30]	Ball: E2
239	DISP0_DAT10	2.8V	IO	gpio4_GPIO[31]	Ball: G3
241	DISP0_DAT7	2.8V	IO	gpio4_GPIO[28]	Ball: H6
243	EIM_OE*	3.3V	IO	emi_EIM_OE	Ball:V8 Optionally connected to PMIC IRQ pin
245	DISP0_DAT6	2.8V	IO	gpio4_GPIO[27]	Ball: G1
247	EIM_RW*	3.3V	IO	emi_EIM_RW	Ball:AB4 Optionally connected to PMIC PBSTAT pin
249	DISP0_DAT8	2.8V	IO	gpio4_GPIO[29]	Ball: G6

251	GND	GND			
253	SATA_TXM	2.5V	Output	SATA_TXM	SATA0 Transmit- (Ball: B10)
255	SATA_TXP	2.5V	Output	SATA_TXP	SATA0 Transmit+ (Ball: A10)
257	GND	GND			
259	SATA_RXP	2.5V	Input	SATA_RXP	SATA0 Receive+ (Ball: B12)
261	SATA_RXM	2.5V	Input	SATA_RXM	SATA0 Receive- (Ball: A12)
263	GND	GND			
265	NC				
267	EIM_CS1 *	3.3V	IO	emi_EIM_CS[1]	Ball:Y7 Optionally connected to ETH PHY INTn pin
269	GND	GND			
271	NC				
273	EIM_CS0 *	3.3V	IO	emi_EIM_CS[0]	By default not connected. Ball:W8 Connected to on module SPI Flash WP pin
275	GND	GND			
277	POWER_ON	5V	Input		Connected to ON pin of PMIC. Can be used to connect a pushbutton to power on the SOM module
279	RST_IN# (Optional)	3.3V	Input		Connected to RESET_IN_B pin of i.MX53. Can be used to connect a reset

					switch on the carrier card to reset the SOM module
281	SLEEP (Optional)	3.3V/5V	Output		PMIC_VSTBY_REQ signal of i.MX53 is inverted to 3.3V level. So at the MXM connector side: SLEEP=low means standby request SLEEP=high means normal operation

Table 15: MXM3 Connector Top Side pin assignment
3.2.12 314 Pin MXM 3 Connector Bottom Pin Assignments (J12)

Pin No	Signal Name	IO Level	Direction w.r.t SOM	Out of Reset Condition-Block IO	Description
E2-1	VCC (5V)	5V	Input		Main Input to the Board
E2-2	VCC (5V)				
E2-3	VCC (5V)				
E2-4	VCC (5V)				
E2-5	VCC (5V)				
E2-6	NC				
E2-7	VCC_3V3_MEM	3.3V RTC Backup	Input		Used as RTC backup voltage, when there is no main supply
E2-8	NC				
E2-9	GND	GND			
E2-10	NC				
E4-1	NC				
E4-2	GND	GND			
E4-3	NC				

E4-4	NC				
E4-5	GND	GND			
E4-6	NC				
E4-7	NC				
E4-8	GND	GND			
E4-9	NC				
E4-10	NC				
2	GND	GND			
4	EIM_DA0	3.3V	IO	emi_NAND_EIM_DA[0]	Ball:Y8
6	EIM_DA1	3.3V	IO	emi_NAND_EIM_DA[1]	Ball:AC4
8	GND	GND			
10	EIM_DA2	3.3V	IO	emi_NAND_EIM_DA[2]	Ball:AA7
12	EIM_DA3	3.3V	IO	emi_NAND_EIM_DA[3]	Ball:W9
14	GND	GND			
16	EIM_DA4	3.3V	IO	emi_NAND_EIM_DA[4]	Ball:AB6
18	EIM_DA5	3.3V	IO	emi_NAND_EIM_DA[5]	Ball:V9
20	GND	GND			
22	EIM_DA6	3.3V	IO	emi_NAND_EIM_DA[6]	Ball:Y9
24	EIM_DA7	3.3V	IO	emi_NAND_EIM_DA[7]	Ball:AC5
26	EIM_DA8	3.3V	IO	emi_NAND_EIM_DA[8]	Ball:AA8
28	PATA_DIOW *	3.3V	IO	gpio6_GPIO[17]	Default not connected Used ad UART1 Transmit Pin on the module(Ball:J3)
30	GND	GND			
32	USB_H1_VBUS	5V	IO	USB_H1_VBUS	Ball:D15
34	PATA_DMACK *	3.3V	IO	gpio6_GPIO[18]	Default not connected Used ad UART1 Receive Pin on the module

					(Ball:J2)
36	EIM_D23	3.3V	IO	gpio3_GPIO[23]	Ball: Y1
38	EIM_D29	3.3V	IO	gpio3_GPIO[29]	Ball: AA2
40	EIM_A20	3.3V	IO	emi_EIM_A[20]	Ball: Y6
42	EIM_A16	3.3V	IO	emi_EIM_A[16]	Ball: AA5
44	EIM_A24	3.3V	IO	emi_EIM_A[24]	Ball: Y5
46	EIM_A23	3.3V	IO	emi_EIM_A[23]	Ball: V6
48	EIM_EB3	3.3V	IO	gpio2_GPIO[31]	Ball: Y4
50	GND	GND			
52	EIM_BCLK	3.3V	Output	emi_EIM_BCLK	Ball:W11
54	NC				
56	NC				
58	EIM_A21	3.3V	IO	emi_EIM_A[21]	Ball: AA4
60	NC				
62	EIM_A22	3.3V	IO	emi_EIM_A[22]	Ball: AA3
64	EIM_A19	3.3V	IO	emi_EIM_A[19]	Ball: W7
66	EIM_A17	3.3V	IO	emi_EIM_A[17]	Ball: V7
68	EIM_A18	3.3V	IO	emi_EIM_A[18]	Ball: AB3
70	GND	GND			
72	KEY_ROW3/I2C0 Data	3.3V	IO	gpio4_GPIO[13]	I2C0 Data Signal (Ball: D4) Connected to PMIC with address 0x69 R/W
74	KEY_COL3/ I2C0 clock *	3.3V	IO	gpio4_GPIO[12]	I2C0 clock Signal(Ball: F6) Shared with pin162 Connected to PMIC with address 0x69 R/W
76	SD2_DATA2	3.3V	IO	gpio1_GPIO[13]	Ball: D14
78	SD2_DATA1	3.3V	IO	gpio1_GPIO[14]	Ball: C14
80	SD2_DATA3	3.3V	IO	gpio1_GPIO[12]	Ball: E13
82	PATA_DATA6	3.3V	IO	gpio2_GPIO[6]	Ball: N1
84	EIM_A25	3.3V	IO	emi_EIM_A[25]	Ball: W6
86	SD2_CMD	3.3V	IO	gpio1_GPIO[11]	Ball: C15
88	SD2_DATA0	3.3V	IO	gpio1_GPIO[15]	Ball: D13

90	SD2_CLK	3.3V	IO	gpio1_GPIO[10]	Ball: E14)
92	PATA_DATA4	3.3V	IO	gpio2_GPIO[4]	Ball: M3
94	PATA_DATA5	3.3V	IO	gpio2_GPIO[5]	Ball: M4
96	GND	GND			
98	NC				
100	NC				
102	NC				
104	GND	GND			
106	SD1_DATA2	3.3V	IO	gpio1_GPIO[19]	Ball: F17
108	SD1_DATA3	3.3V	IO	gpio1_GPIO[21]	Ball: F16
110	EIM_DA11	3.3V	IO	emi_NAND_EIM_DA[11]	Ball: AC6
112	SD1_DATA1	3.3V	IO	gpio1_GPIO[17]	Ball: C17
114	SD1_DATA0	3.3V	IO	gpio1_GPIO[16]	Ball: A20
116	SD1_CMD	3.3V	IO	gpio1_GPIO[18]	Ball: F18
118	PATA_DATA7	3.3V	IO	gpio2_GPIO[7]	Ball: M5
120	EIM_EB1	3.3V	IO	emi_EIM_EB[1]	Ball: AB5
122	EIM_DA12	3.3V	IO	emi_NAND_EIM_DA[12]	Ball: V10
124	SD1_CLK	3.3V	IO	gpio1_GPIO[20]	Ball: E16
134	GND	GND			
136	EIM_EB0	3.3V	IO	emi_EIM_EB[0]	Ball: AC3
138	PATA_DATA12	3.3V	IO	gpio2_GPIO[12]	Ball: N5
140	PATA_DATA14	3.3V	IO	gpio2_GPIO[14]	Ball: P6
142	EIM_DA13	3.3V	IO	emi_NAND_EIM_DA[13]	Ball: AC7
144	EIM_DA15	3.3V	IO	emi_NAND_EIM_DA[15]	Ball: AA9
146	PATA_DATA15	3.3V	IO	gpio2_GPIO[15]	Ball: P5
148	PATA_DA_2	3.3V	IO	gpio7_GPIO[8]	Ball: L4
150	PATA_DA_1	3.3V	IO	gpio7_GPIO[7]	Ball: L3
152	EIM_DA14	3.3V	IO	emi_NAND_EIM_DA[14]	Ball: Y10
154	PATA_DATA13	3.3V	IO	gpio2_GPIO[13]	Ball: N6
156	GND	GND			
158	NC				
160	NANDE_CS3	3.3V	IO	gpio6_GPIO[16]	Ball: W13
162	KEY_COL3 *	3.3V	IO	gpio4_GPIO[12]	Default not

					connected. Ball:F6 Shared with pin 74
164	NANDE_CS2	3.3V	IO	gpio6_GPIO[15]	Ball: V14
166	GPIO_19	3.3V	IO	gpio4_GPIO[5]	Ball: B4
168	NANDE_CS1	3.3V	IO	gpio6_GPIO[14]	Ball: V13
170	GND	GND			
172	DISP0_DAT23	2.8V	IO	gpio5_GPIO[17]	Ball: C3
174	DISP0_DAT21	2.8V	IO	gpio5_GPIO[15]	Ball: C1
176	DISP0_DAT19	2.8V	IO	gpio5_GPIO[13]	Ball: G5
178	DISP0_DAT18	2.8V	IO	gpio5_GPIO[12]	Ball: G4
180	EIM_D25	3.3V	IO	gpio3_GPIO[25]	Ball: W3
182	KEY_ROW1	3.3V	IO	gpio4_GPIO[9]	Ball: D6
184	KEY_ROW0	3.3V	IO	gpio4_GPIO[7]	Ball: B3
186	EIM_D24	3.3V	IO	gpio3_GPIO[24]	Ball: Y2
188	GND	GND			
190	EIM_D22	3.3V	IO	gpio3_GPIO[22]	Ball: W2
192	EIM_D20	3.3V	IO	gpio3_GPIO[20]	Ball: W1
194	EIM_D21	3.3V	IO	gpio3_GPIO[21]	Ball: V3
196	EIM_D28	3.3V	IO	gpio3_GPIO[28]	Ball: AA1
198	EIM_EB2	3.3V	IO	gpio2_GPIO[30]	Ball: Y3
200	EIM_D17	3.3V	IO	gpio3_GPIO[17]	Ball: U5 Used as eCSPI1_MISO
202	EIM_D18	3.3V	IO	gpio3_GPIO[18]	Ball: V1 Used as eCSPI1_MOSI
204	EIM_D16	3.3V	IO	gpio3_GPIO[16]	Ball: U6 Used as eCSPI1_CLK
206	NC				
208	NC				
210	NC				
212	NC				
214	GND	GND			
216	DI0_PIN15	2.8V	IO	gpio4_GPIO[17]	Ball: E4
218	NC				
220	DISP0_DAT12	2.8V	IO	gpio5_GPIO[6]	Ball: H1
222	DISP0_DAT14	2.8V	IO	gpio5_GPIO[8]	Ball: F2

224	DISP0_DAT13	2.8V	IO	gpio5_GPIO[7]	Ball: E1
226	DISP0_DAT15	2.8V	IO	gpio5_GPIO[9]	Ball: F3
228	DISP0_DAT16	2.8V	IO	gpio5_GPIO[10]	Ball: D1
230	GPIO_14	2.8V	IO	gpio4_GPIO[4]	Can be used as Main reset out from SOM Ball:W18
232	DI0_DISP_CLK	2.8V	IO	gpio4_GPIO[16]	Ball: H4
234	DISP0_DAT17	2.8V	IO	gpio5_GPIO[11]	Ball: F5
236	GND	GND			
238	NC				
240	NC				
242	CSIO_DAT8	3.3V	IO	gpio5_GPIO[26]	Ball: T1
244	CSIO_DAT9	3.3V	IO	gpio5_GPIO[27]	Ball: R4
246	GPIO_16*	3.3V	IO	gpio7_GPIO[11]	I2C3 Data signal (Ball: C6) Shared with Pin175
248	GPIO_5*	3.3V	IO	gpio1_GPIO[5]	I2C3 Clock signal (Ball: A5) Shared with Pin173
250	GND	GND			
252	NC				
254	EIM_D19*	3.3V	IO	gpio3_GPIO[19]	Default not connected Connected to SPI flash Chip select Ball:V2
256	NC				
258	LED1	3.3V	Output		Link activity LED Indication. This pin is driven active when a valid link is detected and blinks when activity is detected.

260	LED2	3.3V	Output		Link Speed LED Indication. This pin is driven active when the operating speed is 100Mbps. It is inactive when the operating speed is 10Mbps or during line isolation.
262	NC				
264	NC				
266	GND	GND			
268	ETH_RXP	3.3V	Input		Ethernet PHY signal Recieve +
270	ETH_RXN	3.3V	Input		Ethernet PHY signal Recieve -
272	ETH_TXP	3.3V	Output		Ethernet PHY signal Transmit +
274	ETH_TXN	3.3V	Output		Ethernet PHY signal Transmit -
276	GND	GND			
278	EIM_LBA	3.3V	IO	emi_EIM_LBA	Ball: AA6
280	PWR_RDY	3.3V	Output		Power Ready signal of SOM. Used for power on sequencing of carrier board

Table 16: MXM3 Connector Bottom Side pin assignment

3.2.13 LVDS Connector Pin Assignment (J13)

Note: Not Mounted

Pin	Signal Name	Direction	Pin	Signal Name	Direction
1	VCC_3V3	Power	11	LVDS0_2-	Output
2	VCC_3V3	Power	12	LVDS0_2+	Output
3	GND		13	GND	
4	GND		14	LVDS0_CLK-	Output
5	LVDS0_0-	Output	15	LVDS0_CLK+	Output

6	LVDS0_0+	Output	16	GND	
7	GND		17	LVDS0_3-	Output
8	LVDS0_1-	Output	18	LVDS0_3+	Output
9	LVDS0_1+	Output	19	MODE_LVDS0	Pull up/down option
10	GND		20	SC_LVDS0	Pull up/down option

Table 17: LVDS Connector2 pin assignment

3.2.14 MLB Header Pin Assignment (J14)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	GND		Ground
2	MLBDAT	IO	Media Local Bus Data
3	MLBSIG	IO	Media Local Bus Signal
4	MLBCLK	Output	Media Local Bus Clock
5	VCC_3V3	Power	3.3V Power Supply

Table 18: MLB Header pin assignment

3.2.15 CAN2 Header Pin Assignment (J16)

Pin	Signal Name	Direction	Description
1	GND		Ground
2	CAN2H	IO	High Bus Output
3	CAN2L	IO	Low Bus Output

Table 19: CAN2 Header pin assignment

3.2.16 22 Pin SATA Connector Pin Assignment (J17)

Pin	Signal Name	Direction	Description
1	GND		Ground
2	SATA_TXP_CON	Output	Transmit Signal
3	SATA_TXN_CON	Output	Transmit Signal
4	GND		Ground

5	SATA_RXN_CON	Input	Receive Signal
6	SATA_RXP_CON	Input	Receive Signal
7	GND		Ground
8	3V3_SATA	Power	3.3V Power
9	3V3_SATA	Power	3.3V Power
10	3V3_SATA	Power	3.3V Power
11	GND		Ground
12	GND		Ground
13	GND		Ground
14	5V_SATA	Power	5V Power
15	5V_SATA	Power	5V Power
16	5V_SATA	Power	5V Power
17	GND		Ground
18	GND		Ground
19	GND		Ground
20	12V_SATA	Power	12V Power
21	12V_SATA	Power	12V Power
22	12V_SATA	Power	12V Power

Table 20: 22 Pin SATA Connector pin assignment

3.2.17 Audio In Connector Pin Assignment (J18)

Pin	Signal Name	Direction	Description
1	GND		Ground
2	MIC	Input	Microphone Signals
3	NC		No Connection
4	MIC_DET_B	Input	MIC Signal detection
5	MIC_INT	Input	Microphone interrupt Signals

Table 21: Audio In pin assignment

3.2.18 Audio Out Connector Pin Assignment (J19)

Pin	Signal Name	Direction	Description
1	GND		Ground
2	HP_L	Output	Left Head phone Output
3	HP_R	Output	Right Head phone Output
4	HEADPHONE_DET_B	Input	Head phone detection signal
5	NC		No Connection

Table 22: Audio Out Connector pin assignment

3.2.19 RJ45 MAGJACK Pin Assignment (J20)

Pin	Signal	Direction	Description
1	TCT		Ref Voltage
2	ETH_TXP	Output	Transmit data+
3	ETH_TXN	Output	Transmit data-
4	ETH_RXP	Input	Receive data+
5	ETH_RXN	Input	Receive data-
6	RCT		Ref Voltage
7	LED1_K		LED Signal
8	LED1		LED Signal
9	LED2_K		LED signal
10	LED2		3.3V Power
11	SHIELD		Shielding
12	SHIELD		Shielding
13	SHIELD		Shielding
14	SHIELD		Shielding

Table 23: RJ45 MAGJACK Pin assignment

3.2.20 Dual DB9 Connector Pin Assignment (J21)

Pin No	Signal Name	Direction	Description
A2	RXD1	Input	Receive Data
A3	TXD1	Output	Transmit Data
A5	GND		Ground
B2	CAN1H	IO	High bus output
B7	CAN1L	IO	Low bus output
B6,B3	GND		Ground
A1,A4,A6,A7,A8,A9	NC		No Connection
B1,B4,B8, B5,B9	NC		No Connection

Table 24: Dual DB9 Connector Pin assignment

Note: B → TOP DB9 Connector (Not Tested)

A → BOTTOM DB9 Connector

3.2.21 HDMI Connector Pin Assignment (J22)

Note: Not Tested

Pin	Signal Name	Direction	Description
1	TX2+	Output	Data 2+
2	GND		Ground
3	TX2-	Output	Data 2-
4	TX1+	Output	Data 1 +
5	GND		Ground
6	TX1-	Output	Data 1-
7	TX0+	Output	Data 0+
8	GND		Ground
9	TX0-	Output	Data 0-
10	TXC+	Output	Clock +
11	GND		Ground
12	TXC-	Output	Clock-
13	CEC_O	Output	Referenced Logic Out
14	NC		No Connection
15	HDMI_SCK_O	Input	Clock

16	HDMI_SDA_O	IO	Data DVI Signals
17	GND		Ground
18	5V		5V Power
19	HPD_CON	Input	Hot Plug Detect

Table 25: HDMI Connector Pin assignment

3.2.22 USB Type A Connector Pin Assignment (J23)

Pin No	Pin Detail	Direction	Description
1	VBUS2_H2	Power	5V power
2	H1_DM2 (USB_HOST1-)	IO	USB Hub1 Port 2 Data -
3	H1_DP2 (USB_HOST1+)	IO	USB Hub1 Port 2 Data +
4	GND		Ground Power
5	CHASI_GND		Chassis Ground
6	CHASI_GND		Chassis Ground

Table 26: USB Type A Connector Pin assignment

3.2.23 Expansion Connector Pin Assignment (J24)

Note: Not Mounted

Pin	Signal Name	Direction	Pin	Signal Name	
1	GND		2	GND	
3	EIM_DA0	IO	4	EIM_DA1	IO
5	EIM_DA2	IO	6	EIM_DA3	IO
7	EIM_DA4	IO	8	EIM_DA5	IO
9	EIM_DA6	IO	10	EIM_DA7	IO
11	EIM_DA8	IO	12	EIM_DA9	IO
13	EIM_DA10	IO	14	EIM_DA11	IO
15	EIM_DA12	IO	16	EIM_DA13	IO
17	EIM_DA14	IO	18	EIM_DA15	IO
19	GND		20	GND	
21	EIM_D16	IO	22	EIM_D17	IO
23	EIM_D18	IO	24	EIM_D19	IO
25	EIM_D20	IO	26	EIM_D21	IO
27	EIM_D22	IO	28	EIM_D23	IO

29	EIM_D24	IO	30	EIM_D25	IO
31	EIM_D26	IO	32	EIM_D27	IO
33	EIM_D28	IO	34	EIM_D29	IO
35	EIM_D30	IO	36	EIM_D31	IO
37	GND		38	GND	
39	EIM_A16	Output	40	EIM_A17	Output
41	EIM_A18	Output	42	EIM_A19	Output
43	EIM_A20	Output	44	EIM_A21	Output
45	EIM_A22	Output	46	EIM_A23	Output
47	EIM_A24	Output	48	EIM_A25	Output
49	NC		50	NC	
51	EIM_EB0	IO	52	EIM_EB1	IO
53	EIM_EB2	IO	54	EIM_EB3	IO
55	GND		56	GND	
57	EIM_OE	Input	58	EIM_CS0	Input
59	EIM_CS1	Input	60	NC	
61	NC		62	NC	
63	NC		64	NC	
65	EIM_WAIT	Output	66	EIM_LBA	Input
67	EIM_BCLK	Input	68	EIM_RW	Input
69	NC		70	AUD4_TXD	Output
71	GND		72	GND	
73	UART2_RTS	Output	74	UART2_CTS	Input
75	UART2_RXD	Input	76	UART2_TXD	Output
77	OWIRE	IO	78	AUD3_TXFS	Input
79	AUD4_RXFS	Input	80	CSI0_DAT7	Output
81	AUD4_RXC	Input	82	AUD3_TXD	Output
83	AUD4_SYNC	Input	84	AUD3_TXC	Output
85	DISP0_D7	Input	86	I2C1_SDA	Output
87	AUD4_RXD	Input	88	I2C1_SCL	Output

89	GND		90	GND	
91	eCOMPASS_INT	IO	92	GPIO2_29	IO
93	ACCL_INT2	IO	94	B_RESET_OUTn	IO
95	I2C3_SCL	IO	96	I2C2_SCL	IO
97	I2C3_SDA	IO	98	I2C2_SDA	IO
99	ACCL_INT1	IO	100	KPP_COL2	IO
101	VCC_1V8		102	VCC_1V8	
103	VCC_1V8		104	VCC_1V8	
105	VCC_3V3		106	VCC_3V3	
107	VCC_3V3		108	VCC_3V3	
109	VCC_5V		110	VCC_5V	
111	VCC_5V		112	VCC_5V	
113	VCC_5V		114	VCC_5V	
115	VCC_IN		116	VCC_IN	
117	VCC_IN		118	VCC_IN	
119	VCC_IN		120	VCC_IN	

Table 27: Expansion Connector Pin assignment

NOTE: The Signal Namings are given as per Schematics. Signals can be used as per requirement based on IO Mux Configuration

3.2.24 Video Input Header Pin Assignment (J26)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	GND		Ground
2	VIDEO_IN_B	Input	Video Input

Table 28: Video Input Header Pin assignment

3.2.25 SIM Connector Pin Assignment (J27)

Pin	Signal Name	Direction	Description
1	VSIM_3V	Power	3V Supply
2	UICC_RESET	Output	Reset signal

3	UICC_CLK	Output	Clock signal
4	GND		Ground
5	SIM_VPP	Power	Peak to peak power
6	VSIM_3V	Power	3V Supply
7	NC		No connection
8	NC		No connection

Table 29: SIM Connector Pin assignment

3.2.26 UART5 Connector Pin Assignment (J29)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	GND		Ground
2	TXD5	Output	Transmit signal
3	RXD5	Input	Receive signal

Table 30: UART5 Connector Pin assignment

3.2.27 SPDIF IN Connector Pin Assignment (J30)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	MUTEC	Output	Mute Signal
2	GND		Ground
3	SPDIF_IN	Input	Audio Input

Table 31: SPDIF IN Connector Pin assignment

3.2.28 ESAI Audio Out Connector Pin ASSIGNMENT (J31)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	AOUT_1N	Output	Audio output signal
2	AOUT_2N	Output	Audio output signal
3	AOUT_3N	Output	Audio output signal
4	AOUT_4N	Output	Audio output signal
5	AOUT_5N	Output	Audio output signal
6	AOUT_6N	Output	Audio output signal
7	AOUT_7N	Output	Audio output signal
8	AOUT_8N	Output	Audio output signal
9	GND		GND
10	GND		GND

Table 32: ESAI Audio Out Connector Pin assignment

3.2.29 RTC Battery Header Pin Assignment (J32)

Pin	Signal Name	Direction	Description
1	VCC_RTC	Input	RTC Power (3V to 3.3V)
2	GND		Ground

Table 33: RTC Header Pin assignment

3.2.30 ESAI Audio In Connector Pin Assignment (J33)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	AIN_1N	Input	Audio input signal
2	AIN_2N	Input	Audio input signal
3	AIN_3N	Input	Audio input signal
4	AIN_4N	Input	Audio input signal
5	GND		Ground

Table 34: ESAI Audio In Connector Pin assignment

3.2.31 UART4 Connector Pin Assignment (J34)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	GND		Ground
2	TXD4	Output	Transmit signal
3	RXD4	Input	Receive signal

Table 35: UART4 Connector Pin assignment

3.2.32 UART3 Connector Pin Assignment (J36)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	GND		Ground
2	TXD3	Output	Transmit signal
3	RXD3	Input	Receive signal

Table 36: UART3 Connector Pin assignment

3.2.33 UART2 Connector Pin Assignment (J37)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	GND		Ground
2	RTS2	IO	Request to send data
3	RXD2	Input	Receive data
4	CTS2	IO	Clear to send data
5	TXD2	Output	Transmit data

Table 37: UART2 Connector Pin assignment

3.2.34 Camera Connector Pin Assignment (J38)

Note: Not Tested

Pin	Signal Name	Direction	Description
1	NC		No Connection
2	GND		Ground
3	B_B_I2C1_SDA	IO	I2C1 Data
4	VCC_2V8_CAM	Power	2.8V
5	B_B_I2C1_SCL	Input	I2C1 Clock
6	B_B_RESET_OUTn	Output	Reset Signal
7	B_CSI0_VSYNC	Input	Camera VSYNC
8	B_CAM_PWDN1	Output	Camera Power Down
9	B_CSI0_HSYNC	Input	Camera HSYNC
10	VCC_1V8	Power	VCC 1.8V
11	VCC_2V8_CAM	Power	VCC 2.8V
12	B_CSI0_D19	Input	Camera0 Data 19
13	B_CSI0_MCLK	Input	Camera0 Master Clock
14	B_CSI0_D18	Input	Camera0 Data 18
15	GND		Ground
16	B_CSI0_D17	Input	Camera0 Data 17

17	B_CSI0_PIXCLK	Input	Camera0 Pixel Clock
18	B_CSI0_D16	Input	Camera0 Data 16
19	B_CSI0_D12	Input	Camera0 Data 12
20	B_CSI0_D15	Input	Camera0 Data 15
21	B_CSI0_D13	Input	Camera0 Data 13
22	B_CSI0_D14	Input	Camera0 Data 14
23	B_CSI0_D11	Input	Camera0 Data 11
24	B_CSI0_D10	Input	Camera0 Data 10

Table 38: Camera Connector Pin assignment

3.2.35 WIFI Module Connector Pin Assignment (J39)

Note: Not Tested

Pin	Signal Name	Direction	Pin	Signal Name	Direction
1	GND		11	GND	
2	eSDHC4_DAT1	IO	12	SLP_CLK	Input
3	eSDHC4_DAT0	IO	13	GND	
4	GND		14	GPIO2_29	IO
5	eSDHC4_CLK	IO	15	B_RESET_OUTn	Output
6	VCC_3V3		16	KPP_ROW2	IO
7	eSDHC4_CMD	IO	17	KPP_COL2	IO
8	eSDHC4_DAT3	IO	18	GND	
9	eSDHC4_DAT2	IO	19	VCC_5V	Power
10	GND		20	VCC_5V	Power

Table 39: WIFI Module Connector Pin assignment

3.2.36 LCD Connector Pin Assignment (J40)

Pin	Signal Name	Direction	Description
1	VLED	Power	Power Voltage for LED Driver
2	VLED	Power	Power Voltage for LED Driver
3	DISP0_BRIGHTNESS_CTL	Output	Adjust the LED Brightness with PWM Pulse
4	GND		Ground
5	GND		Ground
6	VCC_3V3	Power	Power voltage for digital circuit
7	VCC_3V3	Power	Power voltage for digital circuit
8	MODE1	Output	DE or HV mode control
9	DISP0_DE	Output	Data Enable
10	DISP0_VSYNC	Output	VSYNC signal input
11	DISP0_HSYNC	Output	HSYNC signal input
12	GND		Ground
13	DISP0_D7	Output	Blue Data Input 7
14	DISP0_D6	Output	Blue Data Input 6
15	DISP0_D5	Output	Blue Data Input 5
16	GND		Ground
17	DISP0_D4	Output	Blue Data Input 4
18	DISP0_D3	Output	Blue Data Input 3
19	DISP0_D2	Output	Blue Data Input 2
20	GND		Ground
21	DISP0_D15	Output	Green Data Input 15
22	DISP0_D14	Output	Green Data Input 14
23	DISP0_D13	Output	Green Data Input 13
24	GND		Ground

25	DISP0_D12	Output	Green Data Input 12
26	DISP0_D11	Output	Green Data Input 11
27	DISP0_D10	Output	Green Data Input 10
28	GND		Ground
29	DISP0_D23	Output	Red Data Input 23
30	DISP0_D22	Output	Red Data Input 22
31	DISP0_D21	Output	Red Data Input 21
32	GND		Ground
33	DISP0_D20	Output	Red Data Input 20
34	DISP0_D19	Output	Red Data Input 19
35	DISP0_D18	Output	Red Data Input 18
36	GND		Ground
37	DISP0_PCLK	Output	Sample Clock
38	GND		Ground
39	L/R1	Input	Select Left or Right Scanning Direction
40	U/D1	Input	Select Up or Down Scanning Direction

Table 40: 7" Formike LCD Connector Pin assignment

3.2.37 Mini PCIe Connector Pin Assignment (J41)

Pin	Pin Detail	Description
1	MODEM_WKUP	Modem Wake up signal
2	VCC_3V3	3.3 V power
3	NC	No connection
4	GND	Ground Power
5	NC	No connection
6	3G_1_5V	3G_1_5V Test point
7	NC	No connection
8	VSIM_3V	VCC 3V supply output to SIM
9	GND	Ground Power
10	UICC_DATA	SIM data
11	NC	No connection
12	UICC_CLK	SIM clock
13	NC	No connection
14	UICC_RESET	SIM Reset
15	GND	Ground Power
16	SIM_VPP	SIM Power
17	NC	No connection
18	GND	Ground Power
19	NC	No connection
20	W_DISABLE	Wireless Disable
21	GND	Ground Power
22	B_RESET_OUTn	Reset Signal
23	NC	No connection
24	VCC_3V	3.3 V power
25	NC	No connection
26	GND	Ground Power
27	GND	Ground Power
28	3G_1_5V_1	3G_1_5V_1 Test Point
29	GND	Ground Power
30	3G_SMB_CLK	3G_SMB_CLK Test Point
31	NC	No connection
32	3G_SMB_DATA	3G_SMB_DATA Test point
33	NC	No connection
34	GND	Ground Power
35	GND	Ground Power
36	H1_DM1	USB Hub1 Port1 Data-

37	GND	Ground Power
38	H1_DP1	USB Hub1 Port1 Data-
39	VCC_3V3	3.3 V power
40	GND	Ground Power
41	VCC_3V3	3.3 V power
42	LED	LED Signal
43	GND	Ground Power
44	LED_WLAN#	LED Driver signal out
45	AUD4_CLK	Audio clock
46	LED_WPAN#	LED Driver signal out
47	AUD4_TXD	Audio Transmit Signal
48	3G_1_5V_2	3G_1_5V_2 Test Point
49	AUD4_RXD	Audio Receive Signal
50	GND	Ground Power
51	AUD4_SYNC	Audio Synchronous Signal
52	VCC_3V3	3.3 V power

Table 41: Mini PCIe Connector Pin assignment

3.2.38 Left Speaker Connector Pin Assignment (J42)

Note: Not Mounted

Pin	Signal	Direction	Description
1	OUT L+	Output	Left Speaker Signals
2	OUT L-	Output	Left Speaker Signals

Table 42: Left Speaker Output Connector Pin assignment

3.2.39 Right Speaker Connector Pin Assignment (J43)

Note: Not Mounted

Pin	Signal	Direction	Description
1	OUT R+	Output	Right Speaker Signals
2	OUT R-	Output	Right Speaker Signals

Table 43: Left Speaker Output Connector Pin assignment

3.2.40 Resistive Touch Connector Pin Assignment (J44)

Pin	Signal	Direction	Description
1	TS_Y+	Input	Touch Left Signals
2	TS_X+	Input	Touch Up Signals
3	TS_Y-	Input	Touch Right Signals
4	TS_X-	Input	Touch Down Signals

Table 44: Resistive Touch Connector Pin assignment

3.2.41 2G Module Connector Pin Assignment (J45)

Note: Not Mounted

Pin	Signal Name	Direction	Pin	Signal Name	Direction
1	VCC_5V	Power	5	UART2_CTS	IO
2	UART2_TXD	Output	6	GPIO	IO
3	UART2_RXD	Input	7	GPIO	IO
4	UART2_RTS	IO	8	GND	

Table 45: 2G Module Connector Pin assignment

3.2.42 MIC Connector Pin Assignment (J46)

Note: Not Mounted

Pin	Signal	Direction	Description
1	MIC_INT	Input	Onboard MIC Signal
2	GND		Ground

Table 46: MIC Connector Pin assignment

3.2.43 7 Pin SATA Connector Assignment (J47)

Note: Not Mounted

Pin	Signal Name	Direction	Description
1	GND		Ground
2	SATA_TXP	Output	Transmit Signal
3	SATA_TXN	Output	Transmit Signal
4	GND		Ground
5	SATA_RXN	Input	Receive Signal
6	SATA_RXP	Input	Receive Signal
7	GND		Ground

Table 47: 7 Pin SATA Connector Pin assignment

4 Power On

Connect the 5V supply provided & power on the board.

4.1 HyperTerminal Setup

1. Insert one end of the serial cable to PC/Laptop COM port (DB9 Male Connector.)
2. Connect the other end of the serial cable to serial connector in the Board as shown in Figure 5.
3. Open the HyperTerminal on the PC/Laptop as mentioned below
4. Go to Start -> Programs -> Accessories -> Communication -> HyperTerminal on the host PC/Laptop.
5. In hyperterminal,Go to Files ->Properties
6. Select COM1 or COM2 port depending on which port you have connected the serial cable as shown below.

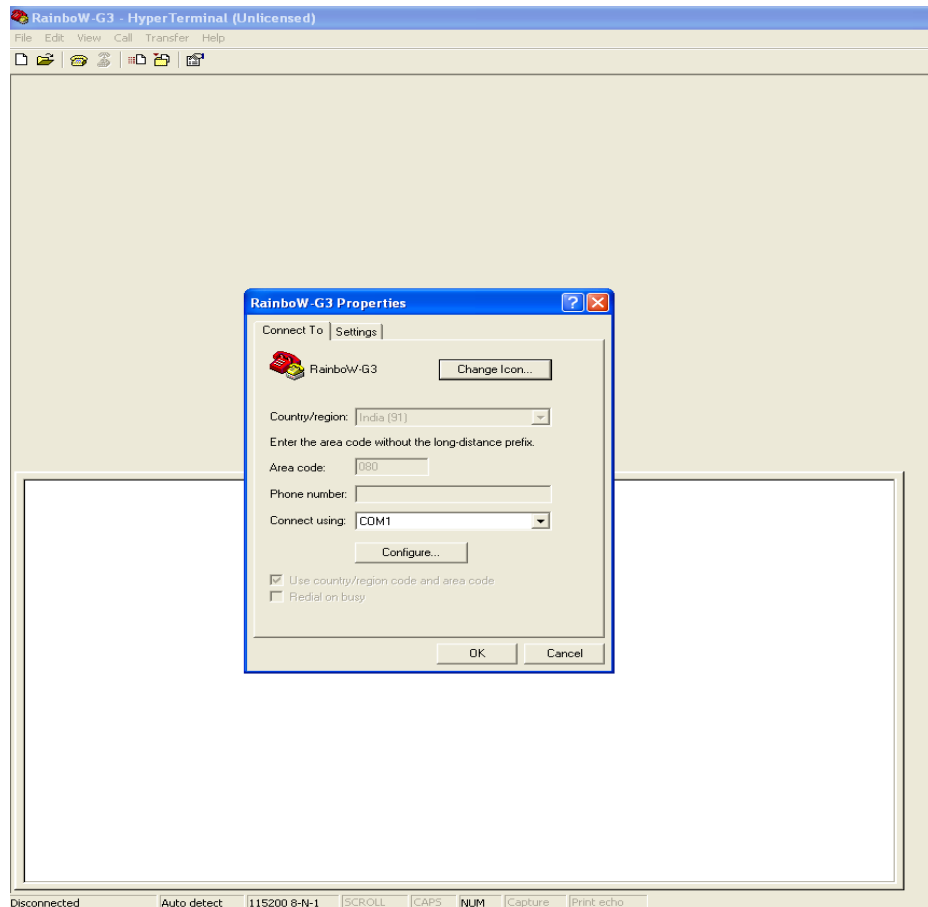


Figure 19: Hyperterminal settings-1

7. Now Click Configure button and do Port Settings as below..

Bits per Second (Baud Rate) :**115200**
Data bits :**8**
Parity :**None**
Stop Bits :**1**
Flow Control :**None**

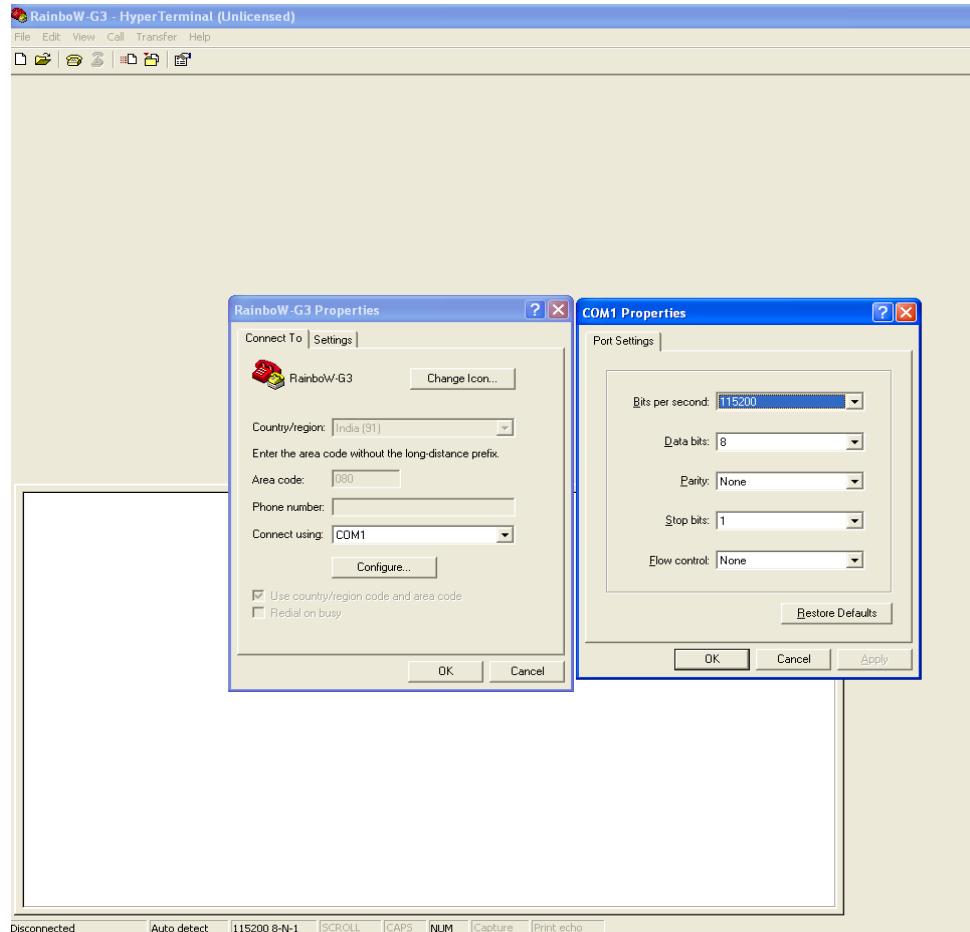


Figure 20: Hyperterminal settings-2

8. Go to File -> Properties -> Settings -> ASCII Setup.
9. Now Select 'Echo typed characters locally' has to be enabled as shown in Figure 23.
10. Go to Call -> Call to connect.
11. If you want to disconnect, Go to Call -> Disconnect.

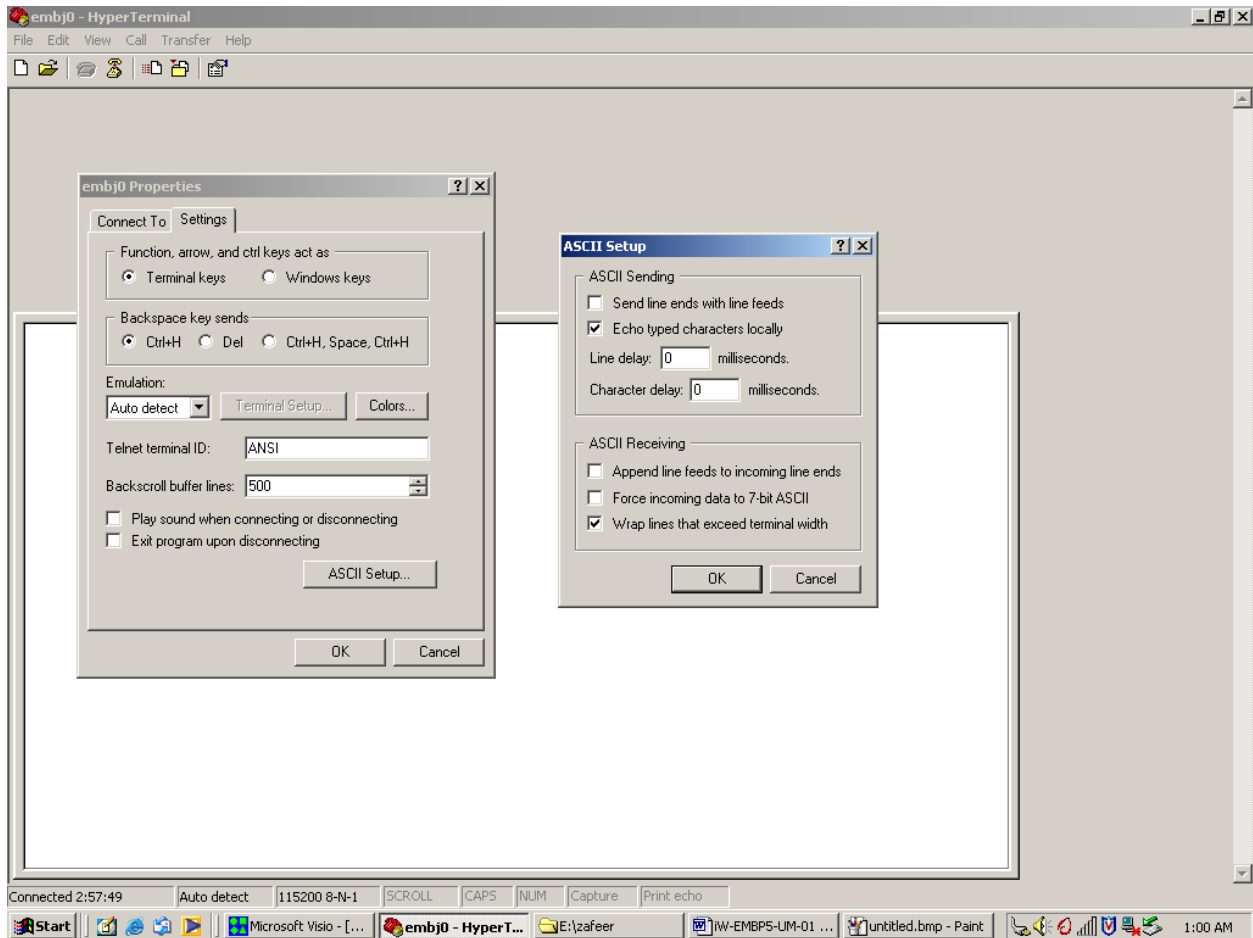
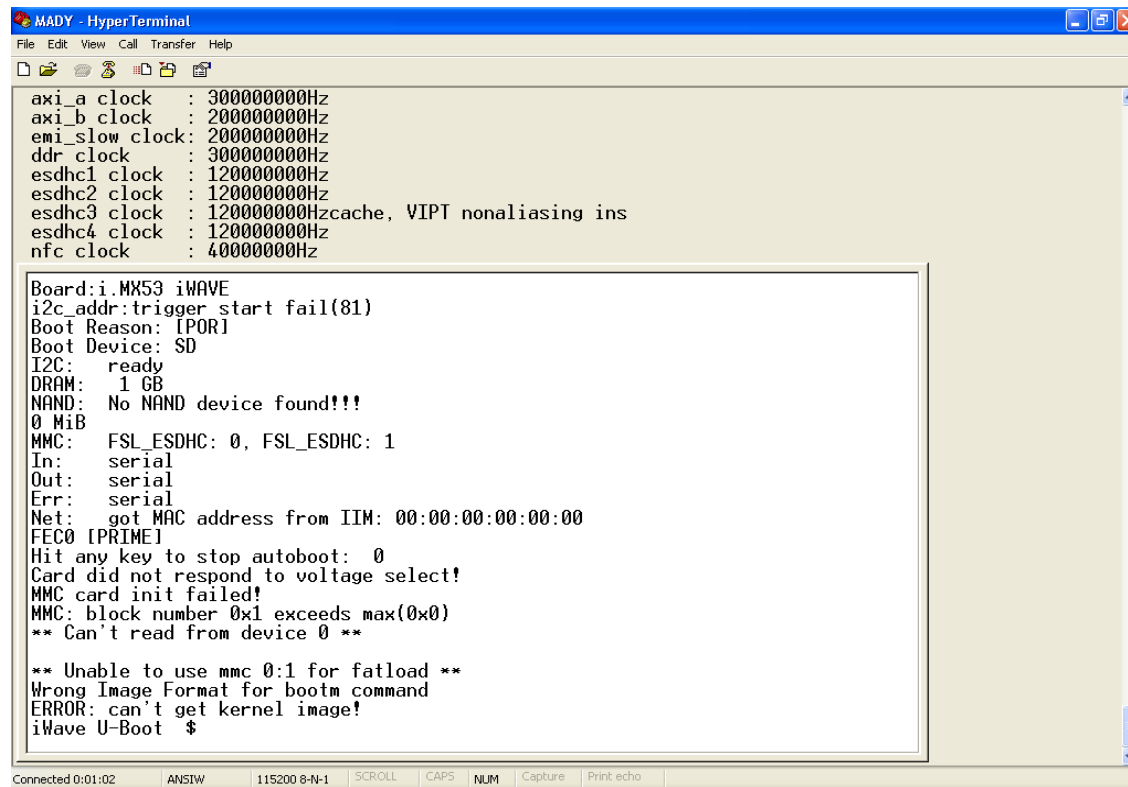


Figure 21: Enable Echo typed characters

The UART console messages will appear on the HT as shown below.



```
MADDY - HyperTerminal
File Edit View Call Transfer Help

axi_a clock : 300000000Hz
axi_b clock : 200000000Hz
emi_slow clock: 200000000Hz
ddr clock : 300000000Hz
esdhc1 clock : 120000000Hz
esdhc2 clock : 120000000Hz
esdhc3 clock : 120000000Hzcache, VIPT nonaliasing ins
esdhc4 clock : 120000000Hz
nfc clock : 400000000Hz

Board:i.MX53 iWAVE
i2c_addr:trigger start fail(81)
Boot Reason: [POR]
Boot Device: SD
I2C: ready
DRAM: 1 GB
NAND: No NAND device found!!!
0 MiB
MMC: FSL_ESDHC: 0, FSL_ESDHC: 1
In: serial
Out: serial
Err: serial
Net: got MAC address from IIM: 00:00:00:00:00:00
FEC0 [PRIME]
Hit any key to stop autoboot: 0
Card did not respond to voltage select!
MMC card init failed!
MMC: block number 0x1 exceeds max(0x0)
** Can't read from device 0 **

** Unable to use mmc 0:1 for fatload **
Wrong Image Format for bootm command
ERROR: can't get kernel image!
iWave U-Boot $
```

Connected 0:01:02 ANS1W 115200 8-N-1 SCROLL CAPS NUM Capture Print echo

Figure 22: UART Console Window

5 ATK User Manual

5.1 Installing Advanced Tool Kit

1. Install “FSL_ATK_TOOL_WINS_STD_INSTALL_1_71.exe” setup in Windows PC (PC must have COM port or USB to serial convertor).

5.2 Initial Setup of Advanced Tool Kit

1. Connect serial port from PC to i.MX 53 Processor board debug serial port.
2. Set the Bootstrap mode switch on the CPU Module (push both switches to ON position for bootstrap) to program the board.

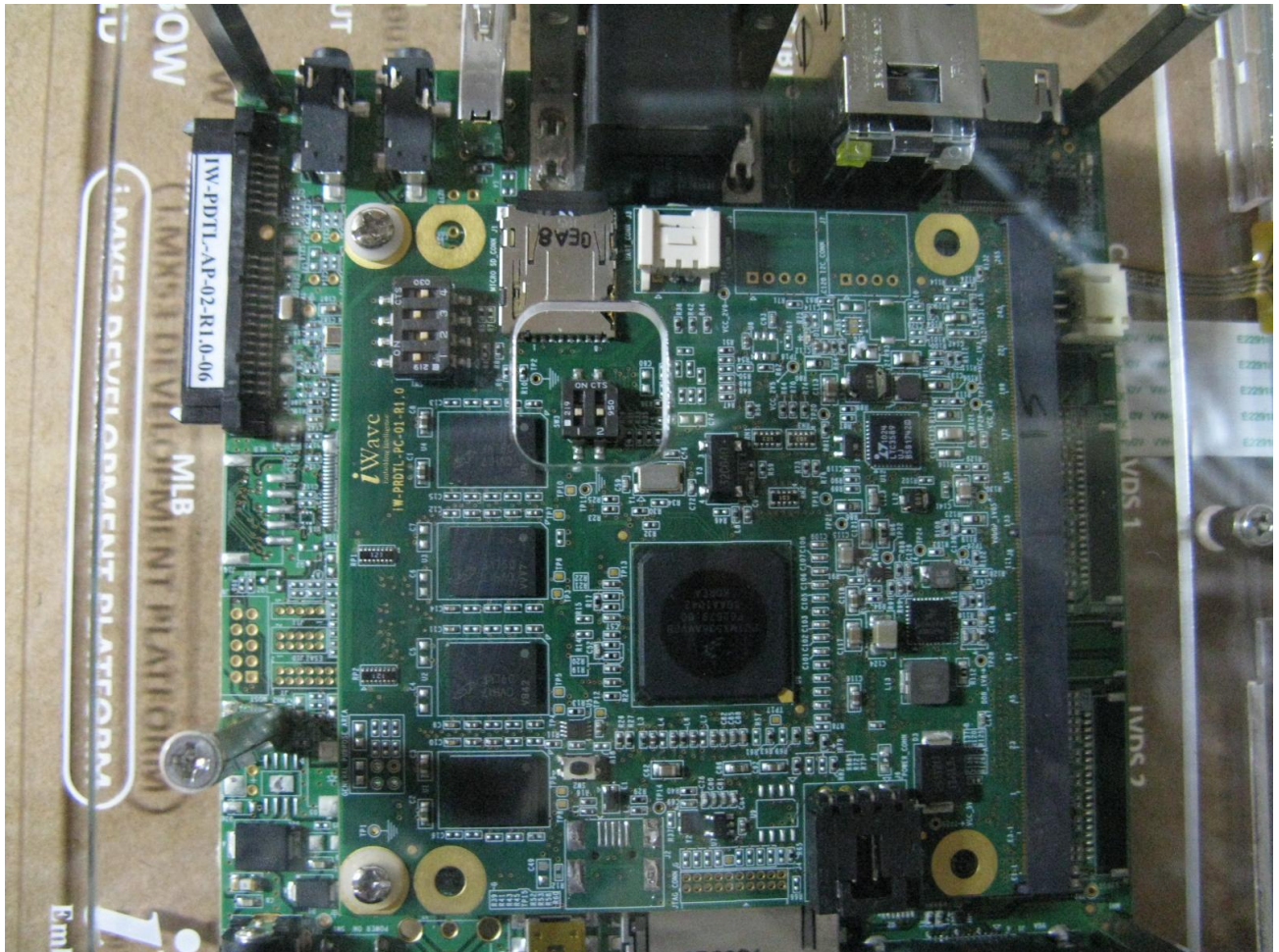


Figure 23: Bootstrap Switch

3. Open Advanced Toolkit application by double clicking the “Advanced Tool Kit V1.71” located in Desktop.
4. In Device Setting select the i.MX CPU as iMX53.
5. In Host Setting, select Communication channel as “Serial Port” and select the COM port. For example, select COM1 Port.
6. Click Next to Continue

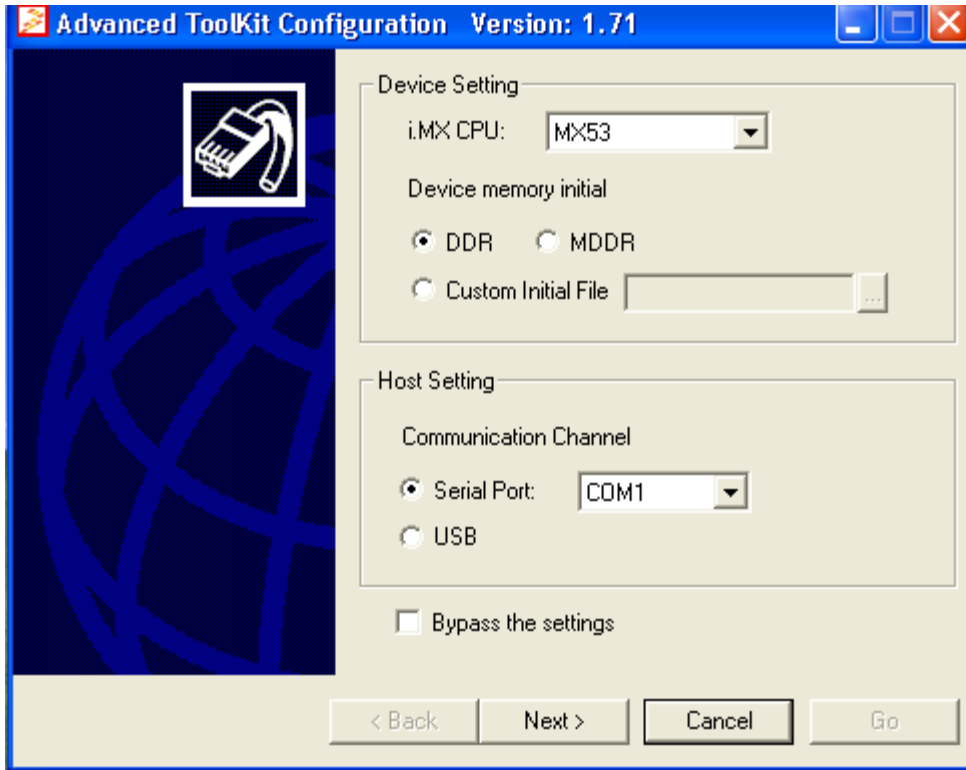


Figure 24: ATK Toolkit Settings

7. Select Flash Tool and Click Go button.

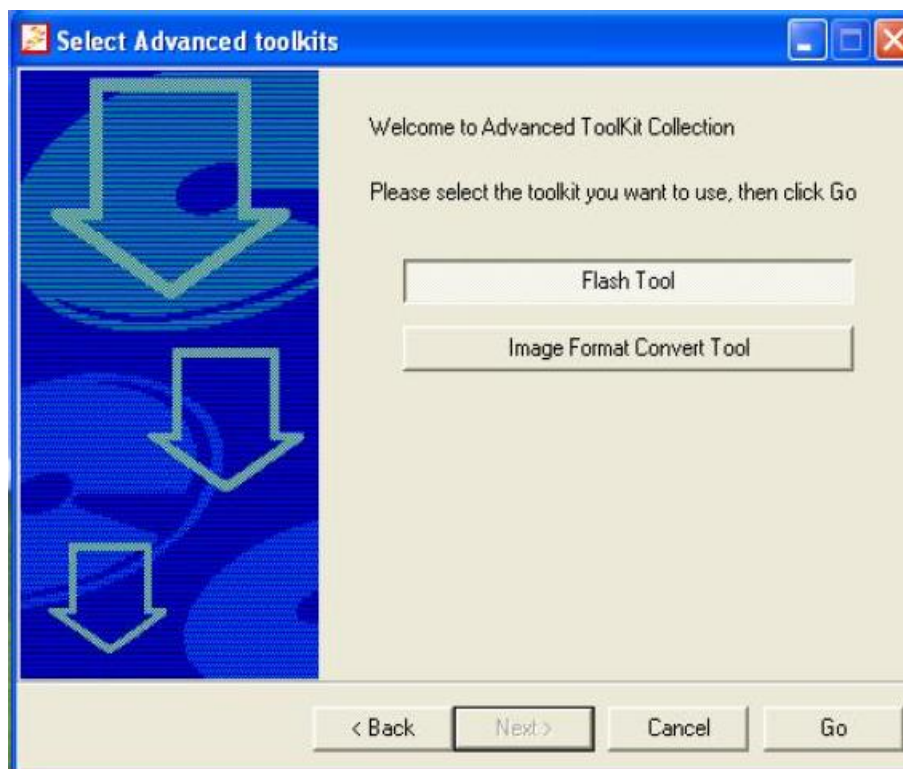


Figure 25: Flash Tool Selection

5.3 MMC/SD Programming

1. Select the option as shown in below figure & select the appropriate bin file for programming.

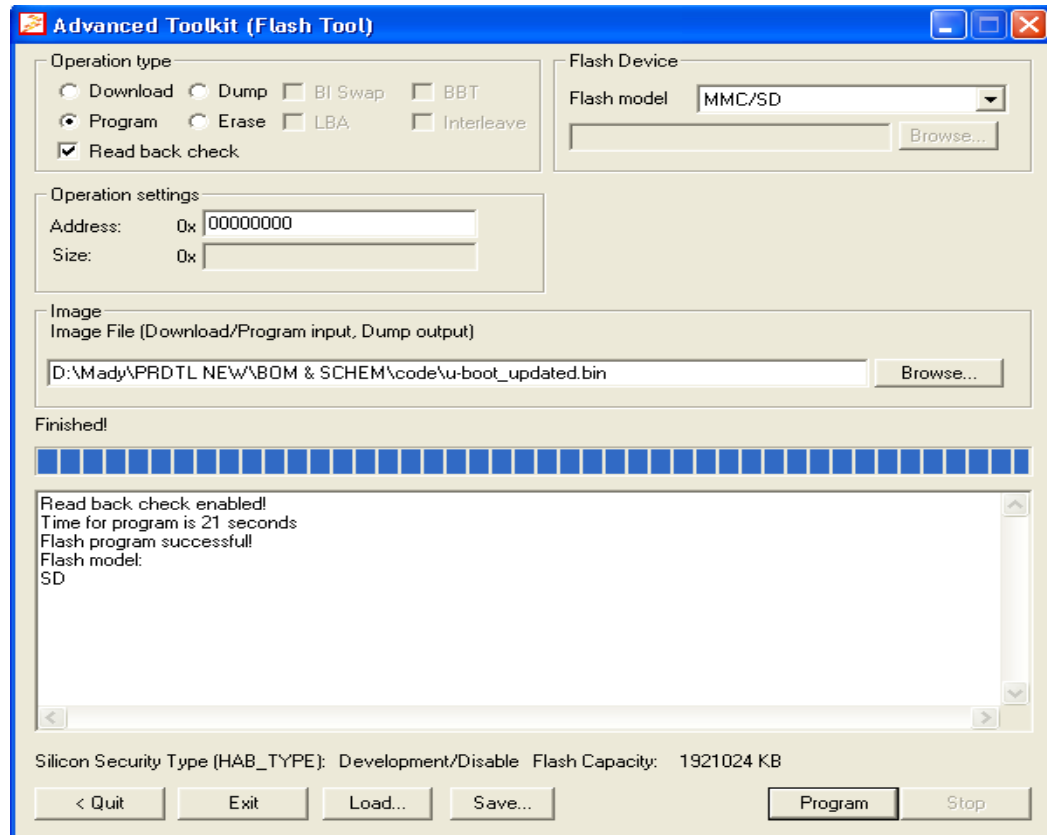


Figure 26: MMC/SD programming

2. Click Program button & wait till the Flash program successful message on text box.
3. Power off the Board & Set the Bootstrap mode switches on the CPU Module (push both switches to OFF position for booting).
4. Power ON the Board for Booting.

5.4 ATK-FAQs:

1. What can be done if bootstrap mode is not detected message displayed in ATK toolkit ?
<Answer> There may be three of reasons
 - a. Check whether COM port is selected properly?
 - b. Check whether board is set in bootstrap mode
 - c. If both options are not helping, power off board and power on again.
2. What can be done If flash programming is getting failed (for any reason) half the way?

<Answer> Repeat the flash programming procedure for particular image once again.

3. What should I do “COM port is already in use message is displayed” ?

<Answer> Check any program is using COM port (e.g Hyperterminal). Close the that application(which is using COM port) and try again.

6 TECHNICAL SUPPORT

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