High-Definition Multimedia Interface Version 1.4b Quantum Data MOI v1.0

Test: DDC Sink

October 7, 2015

Preface

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Introduction

This document provides a set of test methods for tests described in High-Definition Multimedia Interface Compliance Test Specification DDC Clarification.

Scope

This document provides testing procedures for HDMI CTS 1.4b Sink DDC tests: 1) I2C Bus LOWlevel Output Voltage, 2) Pull-Up Resistance, 3) Bus Timing (driving SDA) and 4) Bus Timing (reading SDA).

References

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011. HDMI Compliance Test Specification Version 1.4b, October 11, 2011. High-Definition Multimedia Interface Compliance Test Specification DDC Clarification, Version 1.04 – May 1, 2014.

Informative Reference

No additional informative references.

Test: Sink - I²C Bus LOW-Level Output Voltage

Objective

Confirm that the LOW-level output voltage of the I²C Bus, formed when connecting the Sink DUT to a compliant Source configured so that a LOW-level output current of 3mA results in $V_{OL} = 0.4V$, is less than or equal to the required maximum V_{OL} for the DDC SDA signal.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This
	Specification, the Display Data Channel (DDC) I/Os and
	wires (SDA, SCL, DDC/CEC Ground), shall meet the
	requirements specified in the I2C-bus specification and
	user manual UM10204, Rev. 5 ("I2C Specification"),
	Section 6.1 for "Standard-mode" devices
I2C-bus specification and user manual	Maximum LOW-level output voltage, V _{OL} = 0.4V (at 3mA
UM10204, Rev.5, Section 6.1	sink current)

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Master	980 Advanced Test Platform series:	1
	EDID Analyzer	980 HDMI Phy & Protocol Aux Channel Analyzer	
		module.	

Generic Procedure

- 1. Connect TPA to Sink DUT.
- 2. Configure DDC Master with 1.5K pull-up resistance to +4.7V supply on both SCL and SDA wires.
- 3. Connect EDID Analyzer to DDC Master.
- 4. Connect DDC Master to TPA.
- 5. Apply +5.0V between +5V Power and DDC/CEC Ground.
- 6. Power on the Sink DUT.
- 7. Test LOW-level output voltage of SDA:

- 7.1. Use the DDC Master to read block 0 of the Sink's EDID.
- 7.2. If the Sink DUT does not respond to the DDC transaction, then FAIL.
- 7.3. Use the DDC Master (if capable) or the General Oscilloscope to measure the LOWlevel output voltage of SDA (VOL-SDA) during the DDC read transaction.
- 7.4. If VOL-SDA > 0.4V, then FAIL.

Test: Sink - Pull-Up Resistance

Objective

Confirm that the Sink pull-up resistance meets the minimum requirements for DDC signals SCL and SDA.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the
	Sink pull-up resistance on SDA shall be greater than, or equal
	to, 42.3kΩ (which is 47kΩ minus 10%).
HDMI 1.4b, Section 4.2.8	Sink pull-up resistors for SCL signal – $47k\Omega + -10\%$

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1		980 Advanced Test Platform series:	1
		980 HDMI Phy & Protocol Aux Channel Analyzer	
		module.	

Generic Procedure

- 1. Connect TPA to Sink DUT HDMI input connector.
- 2. Drive +5.0V between +5V Power and DDC/CEC Ground on the TPA.
- 3. Power on the Sink DUT.
- 4. Test the resistance of SDA:
 - 4.1. Measure, then connect a 10K, 1% resistor (RSDA-T) between the SDA pin and DDC/CEC Ground on the TPA.
 - 4.2. Measure the voltage of the SDA pin on the TPA (VSDA-A) referenced to DDC/CEC Ground on the TPA.
 - 4.3. If $OV \leq VSDA \cdot A \leq 0.1V$, then skip to step 5.
 - 4.4 Leave the 10K, 1% resistor (RSDA-T) connected (as it was in step 4.1). Measure, then connect an additional 51.7K 1% resistor (RSDA-S) to the SDA pin on the TPA. Connect the other end the 51.7K 1% resistor (RSDA-S) to the positive terminal of a DC Power Supply set to +3.58V 1% and measured (VSDA-B). Connect the negative

terminal of the (VSDA-B) supply to DDC/CEC Ground on the TPA. The Thevenin equivalent of this test circuit is calculated as VSDA-TH = VSDA-B (1/(1+(RSDA-S/RSDA-T))) and RSDA-TH = (RSDA-S*RSDA-T)/(RSDA-S+RSDA-T).

- 4.5. Measure the voltage of the SDA pin on the TPA (VSDA-C) referenced to DDC/CEC Ground on the TPA.
- 4.6. Remove the 10K, 1% resistor, leaving the 51.7K 1% resistor and +3.58V DC Power Supply (that were added in step 4.4).
- 4.7. Measure the voltage of the SDA pin on the TPA (VSDA-D) referenced to DDC/CEC Ground on the TPA.
- 4.8. If 42300 ohms ≤ (VSDA-D VSDA-C)/(((VSDA-C VSDA-TH)*(1/RSDA-TH))-((VSDA-D VSDA-B)*(1/RSDA-S))), then continue; otherwise FAIL.
- 5. Test the resistance of SCL:
 - 5.1 Measure, then connect a 51.7K 1% resistor (RSCL-S) to the SCL pin on the TPA. Connect the other end the 51.7K 1% resistor (RSCL-S) to the positive terminal of a DC Power Supply set to +3.58V 1% and measured (VSCL-A). Connect the negative terminal of the (VSCL-A) supply to DDC/CEC Ground on the TPA.
 - 5.2. Measure the voltage of the SCL pin on the TPA (VSCL-B) referenced to DDC/CEC Ground on the TPA.
 - 5.3. Measure, then connect an additional 10K, 1% resistor (RSCL-T) between the SCL pin and DDC/CEC Ground on the TPA, leaving the 51.7K 1% resistor (RSCL-S) and +3.58V DC Power Supply (VSCL-A) that were added in step 5.1. The Thevenin equivalent of this test circuit is calculated as VSCL-TH = VSCL-A (1/(1+(RSCL-S/RSCL-T))) and RSCL-TH = (RSCL-S*RSCL-T)/(RSCL-S+RSCL-T).
 - 5.4. Measure the voltage of the SCL pin on the TPA (VSCL-C) referenced to DDC/CEC Ground on the TPA.
 - 5.5. If 42300 ohms \leq (VSCL-B VSCL-C)/(((VSCL-C VSCL-TH)*(1/RSCL-TH))-((VSCL-B VSCL-A)*(1/RSCL-S))) \leq 51700 ohms, then PASS; otherwise FAIL.

Test: Sink - Bus Timing (driving the SDA signal)

Objective

Confirm that the Sink meets the setup and hold bus timing parameters specified in the I2C bus specification when driving the SDA signal.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Display Data Channel (DDC) I/Os and wires (SDA, SCL, DDC/CEC Ground), shall meet the requirements specified in the I2C-bus specification and user manual UM10204, Rev. 5 ("I2C Specification"), Section 6.1 for "Standard-mode" devices
I2C-bus specification and user manual UM10204, Rev.5, Section 6.1	1) Data hold time (t _{HD;DAT}) ≥ 0 μs 2) Data setup time (t _{SU;DAT}) ≥ 250 ns

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Master	980 Advanced Test Platform series:	1
	EDID Analyzer	980 HDMI Phy & Protocol Aux Channel Analyzer	
		module.	

Generic Procedure

- 1. Connect TPA to Sink DUT.
- 2. Configure DDC Master with 2.0K pull-up resistance to +5.5V supply on both SCL and SDA wires.
- 3. Configure DDC Master to achieve 750pF total capacitance on SCL and SDA wires.
- 4. Configure DDC Master so that $f_{SCL} = 100$ kHz.
- 5. Connect EDID Analyzer to DDC Master.
- 6. Connect DDC Master to TPA.
- 7. Apply +5.0V between +5V Power and DDC/CEC Ground.
- 8. Power on the Sink DUT.

- 9. Use the EDID Analyzer to read block 0 of the Sink's EDID.
- 10. If the Sink DUT does not appropriately ACK each I2C transaction, then FAIL.
- 11. Use the DDC Master (if capable) or the General Oscilloscope to measure the specified timing parameters for each occurrence during the EDID read.
 - 11.1. If any occurrence of $t_{HD;DAT} < 0\mu s$, then FAIL.
 - 11.2. If any occurrence of $t_{SU;DAT}$ < 250ns, then FAIL.

Test: Sink - Bus Timing (reading the SDA signal)

Objective

Confirm that the Sink does not require more setup or hold time than specified in the I2C bus specification when reading the SDA signal.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Display Data Channel (DDC) I/Os and wires (SDA, SCL, DDC/CEC Ground), shall meet the requirements specified in the I2C-bus specification and user manual UM10204, Rev. 5 ("I2C Specification"), Section 6.1 for "Standard-mode" devices
I2C-bus specification and user manual UM10204, Rev.5, Section 6.1	1) Data hold time (t _{HD;DAT}) ≥ 0 μs 2) Data setup time (t _{SU;DAT}) ≥ 250 ns

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Master	980 Advanced Test Platform series:	1
	EDID Analyzer	980 HDMI Phy & Protocol Aux Channel Analyzer	
		module.	

Generic Procedure

- 1. Connect TPA to Sink DUT.
- 2. Configure DDC Master with 2.0K pull-up resistance to +5.5V supply on both SCL and SDA wires.
- 3. Configure DDC Master to achieve 750pF total capacitance on SCL and SDA wires.
- 4. Configure DDC Master so that $f_{SCL} = 100$ kHz.
- 5. Test the hold time sensitivity of the Sink DUT:
 - 5.1. Configure DDC Master so that when the DDC Master is writing to SDA, the hold time of SDA is equal to 0 μs.
 - 5.2. Connect EDID Analyzer to DDC Master.
 - 5.3. Connect DDC Master to TPA.

- 5.4. Apply +5.0V between +5V Power and DDC/CEC Ground.
- 5.5. Power on the Sink DUT.
- 5.6. Use the EDID Analyzer to read block 0 of the Sink's EDID.
- 5.7. If the Sink DUT does not appropriately ACK each I2C transaction, then FAIL.
- 5.8. If the bytes read from offsets 0-7 do not constitute a valid EDID header, then FAIL.
- 5.9. If the EDID checksum byte read from the Sink DUT does not match the checksum calculated by the EDID analyzer, then FAIL.
- 6. Test the setup time sensitivity of the Sink DUT:
 - 6.1. Configure DDC Master so that when the DDC Master is writing to SDA, the setup time of SDA is equal to 250ns.
 - 6.2. Connect EDID Analyzer to DDC Master.
 - 6.3. Connect DDC Master to TPA.
 - 6.4. Apply +5.0V between +5V Power and DDC/CEC Ground.
 - 6.5. Power on the Sink DUT.
 - 6.6. Use the EDID Analyzer to read block 0 of the Sink's EDID.
 - 6.7. If the Sink DUT does not appropriately ACK each I2C transaction, then FAIL.
 - 6.8. If the bytes read from offsets 0-7 do not constitute a valid EDID header, then FAIL.
 - 6.9. If the EDID checksum byte read from the Sink DUT does not match the checksum calculated by the EDID analyzer, then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI Phy & Protocol Aux Channel Analyzer Module

The Quantum Data 980 HDMI Phy & Protocol Aux Channel Analyzer module can be installed in the 980B or 980R series Advanced Test Platforms. This 980 HDMI Phy & Protocol Aux Channel Analyzer module serves the generic test functions called out in the HDMI CTS DDC Clarification. Refer to the table below:

Item	Quantum Data Equ	ipment		
1	980 Advanced Tes	980 Advanced Test Platform series:		
	Equipped with:	980 HDMI Phy & Protocol Aux Channel Analyzer module		

980 HDMI Phy & Protocol Aux Channel Analyzer with 980B Series Platform Configuration

The figure below shows a depiction of the 980 Phy & Protocol Aux Channel Analyzer module equipped in various 980B platform. **Note**: Card positioning may vary depending on configuration.



Tests: Sink DDC Tests

1. Objectives

I2C Bus LOW-level Output Voltage - Confirm that the LOW-level output voltage of the I2C Bus, formed when connecting the Sink DUT to a compliant Source configured so that a LOW-level output current of 3mA results in VOL = 0.4V, is less than or equal to the required maximum VOL for the DDC SDA signal.

Pull-Up Resistance - Confirm that the Sink pull-up resistance meets the minimum requirements for DDC signals SCL and SDA.

Bus Timing (driving SDA) - Confirm that the Sink meets the setup and hold bus timing parameters specified in the I2C bus specification when driving the SDA signal.

Bus Timing (reading SDA) - Confirm that the Sink does not require more setup or hold time than specified in the I2C bus specification when reading the SDA signal.

2. Test Overview

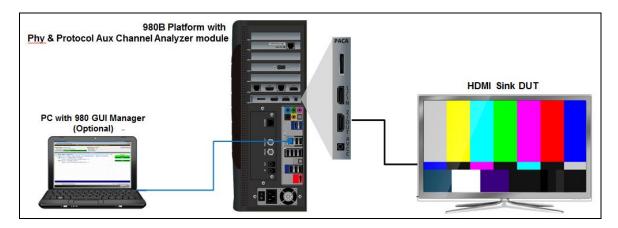
The Pass/Fail criteria is assessed by the application with no human examination required.

3. Procedure

Use the following procedure to conduct this test.

1 Connect Sink DUT to the Quantum Data 980 HDMI Phy & Protocol Aux Channel Analyzer at the module's port labeled IN. Use a High Speed HDMI cable. The figure below shows a depiction of connections to the 980 HDMI Phy & Protocol Aux Channel Analyzer module residing in the 980 series chassis.

Note: Be sure to use the supplied HDMI cable. Part No. 30-00218 Description: CBL, HDMI, 7ft High Speed Heac, Calibrated-Sink.



2 Operate the Sink DUT in a normal mode.

3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Phy & Protocol Aux Channel Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

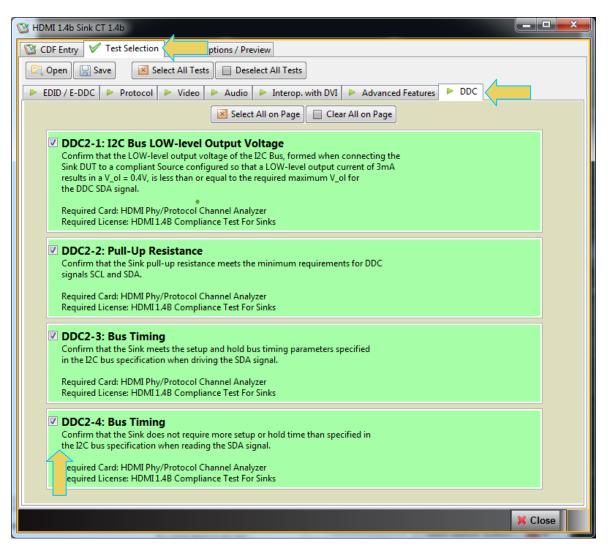
- 4 Complete the following steps:
 - 4.1 Click on the HDMI Source CTS 1.4b icon in the Compliance Tests page of the Apps panel.

💮 Apps								
		C, quantur	πdata					
	Compliance Tests							
	HDMI EDID CTS 1.4b	HDMI Sourc CTS 1.4b	æ	HDMI Source CTS 2.0				
	HDMI Sink CTS 1.4b	HDMI Sink CTS 2.0	: ł	IDMI HDCP Transmitter CTS 1.2				
<								
Ť					•			
	MHL Source CTS 1.2 - 2.1	MHL Sink CTS 1.2 - 2.		MHL Dongle CTS 1.2 - 2.1				
	0131.2-2.1	CT3 1.2 - 2.	1	0131.2-2.1				
		\checkmark		\checkmark				
	CBUS Source	CBUS Sink		CBUS Dongle				
	CTS 1.2 - 2.1	CTS 1.2 - 2.	1	CTS 1.2 - 2.1				
		Page 2 of	4					
	Card Control	Compliance Tests	Editors	Other				

4.2 Navigate to the CDF tab if not already there. There are no CDF requirements to be entered. Simply fill in the name and model number of the device and click OK and optionally save the file. Be sure to indicate the number of HDMI outputs.

🕑 HDMI 1.4b Sink CT 1.4b		x
CDF Entry	lection 🕨 Test Options / Preview	
C Open New	Save CDF File: < not saved>	
Product	s • Formats • Audio	
Manufacturer	What is the product manufacturer's name?	
	ACME	_
Model	What is the model name/number of the product? XYZ	
Call UDMI Order & Carrie	How many HDMI output ports are on the product?	
Sink_HDMI_Output_Count	$\bigcirc 0 \ \bigcirc 1 \ \bigcirc 2 \ \oslash 3 \ \oslash 4 \ \oslash 5 \ \oslash 6 \ \oslash 7 \ \oslash 8 \ \oslash 9$	
Sink_P	The number of the HDMI Input Port being tested.	
Sink_P	$\textcircled{O}1 \ \bigcirc 2 \ \bigcirc 3 \ \bigcirc 4 \ \bigcirc 5 \ \bigcirc 6 \ \bigcirc 7 \ \oslash 8 \ \oslash 9 \ \bigcirc 10 \ \oslash 11 \ \oslash 12 \ \oslash 13 \ \oslash 14 \ \oslash 15$	
Sink_Image_Size	Does the DUT indicate correct size at Image Size area in the EDID?	
	Ves No x cm	
Sink May TMDS Clock	What is the maximum TMDS clock frequency (in MHz) supported by the product? (Any value, e.g. 74.25, 148.5, 222.75, etc.	
Sink_Max_1Mb5_clock	148.5	
	X Close	

4.3 Click on the Test Selection tab and the DDC sub tab and select the DDC1-1: I2C Bus Low-Level Output Voltage test, the DDC1-2 Pull-Up Resistance test; DDC1-3: Bus Timing (driving the SDA); and the DDC1-4: Bus Timing (reading the SDA). Refer to the sample screen below.



4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.

🖄 HDMI 1.4b Sink CT 1.4b	_ _ _X
CDF Entry 🖌 Test Selection 🕨 Test Options / Preview	
Test List	
☑ All ✓ ✓ Instrument: My980B [192.168.254.185] ▼	Execute Tests
Category / Test Name	V
▲ ► DDC	
DDC2-1: I2C Bus LOW-level Output Voltage	\checkmark
• Iter 01:	\checkmark
DDC2-2: Pull-Up Resistance	\checkmark
• Iter 01:	\checkmark
🖌 📃 DDC2-3: Bus Timing	\checkmark
• Iter 01:	\checkmark
a 🔄 DDC2-4: Bus Timing	\checkmark
• Iter 01:	
	X Close

4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.

12 HDMI 1.4b Sink CT 1.4b	
CDF Entry 🗹 Test Selection 🕨 Test Options / Preview	
Test List	
Image: All	► Execute Tests
Category / Test Name	V
▲ ► DDC	
🛛 🖉 DDC2-1: I2C Bus LOW-level Output Voltage	\checkmark
• Iter 01:	\checkmark

Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:

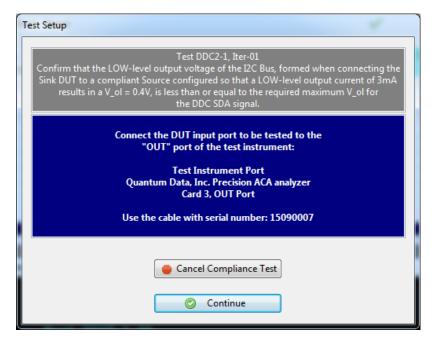
ŀ	HDMI 1.4b Sink (1.4b) CT Results	
	Test Results Name	
	Execute HDMI 1.4b Sink (1.4b) Compliance Tests on Instrument: My980B @ 192.168.254.185	
	Enter a name for the Test Results.	
	My_ACA_Sink_Test_1	
	06_17_2015_10_21_06	
	Cancel Ok	

Enter a name, click OK and the test will begin.

A Test Window will appear (below) indicating the progress of the test.

IDMI 1.4b Sink Compliance Test (1.4b): "My_ACA_Sink_Test_1"		
Test List		
Reset Status		
Category / Test Name	V	Status
A > DDC		
DDC2-1: I2C Bus LOW-level Output Voltage	\checkmark	In Progress
📦 Iter 01:	\checkmark	In Progress
DDC2-2: Pull-Up Resistance	\checkmark	Not Tested
DDC2-3: Bus Timing	\checkmark	Not Tested
DDC2-4: Bus Timing	\checkmark	Not Tested
Test Log		
Line Message		*
• 0003 Assembling the test list.		
• 0004 Transferring the CDF to the Test Instrument.		
• 0005 Test DDC2-1-01		
<pre></pre>		
·		•
Cancel the Compliance Test	ion	

A dialog box will appear (below) indicating the test setup.



Note: Be sure to use the supplied HDMI cable. Part No. 30-00218.

When the tests are complete the results are shown in the test window.

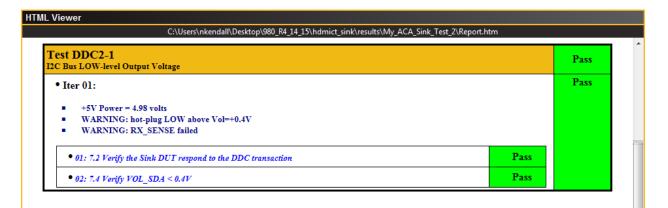
IDMI 1.4b Sink Com	pliance Test (1.4b): "My_ACA_Sink_Test_2"		1000
	Test List		
	Reset Status		
	8		
	/ Test Name	V	Status
	1. TOO Due TOW lovel output Welters	V	Pass
	2-1: I2C Bus LOW-level Output Voltage	× ✓	Pass
	2-2: Pull-Up Resistance	V V	Pass
⊳ ⊖ It		¥	Pass
	2-3: Bus Timing	¥	Pass
⊳ ⊖ It		×	Pass
	2-4: Bus Timing	V	Pass
b 📄 It		1	Pass
	* .1		
	Test Log		
Line	Message		
• 0016	Test DDC2-3 Iter 01 -> Pass		
• 0017	Test DDC2-4-01		
• 0018	Executing the test.		
• 0019	Processing test results.		
• 0020	Test DDC2-4 Iter 01 -> Pass		=
• 0021	Tests completed		Ŧ
	Close Window	esting	
		county	

The test will run and the test application will assess pass or fail. The test results screens appears as shown below. If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS. If the 980 HDMI Phy & Protocol Aux Channel Analyzer compliance test application reports FAIL, then FAIL.

HDM1 1.4b Sink Compliance Test Results sults Name: My_ACA_Sink_Test_2 Manufacturer: Date Tested: October 7, 2015 8:31 AM Model Name: rerall Status: GIS 1.4b - Pass Port Tested: 1 Test Results Test Name / Details DDC2-1: I2C Bus LOW-level Output Voltage I ter 01:	0	Time HTML Rep
Date Tested: October 7, 2015 8:31 AM Model Name: rerall Status: CTS 1.4b - Pass Port Tested: 1 Test Results Test Name / Details DDC2-1: I2C Bus LOW-level Output Voltage I ter 01:	Q 	
Verall Status: CTS 1.4b - Pass Port Tested: 1 Test Results Test Results DDC2-1: I2C Bus LOW-level Output Voltage Image: Comparison of the compariso	0	Status
Test Results Test Results Test Results DDC2-1: I2C Bus LOW-level Output Voltage Iter 01:	Q	Status
Test Name / Details DDC2-1: I2C Bus LOW-level Output Voltage Iter 01:	(2)	Status
DDC2-1: I2C Bus LOW-level Output Voltage	0	Status
▲		
•		Pass
		Pass
• +5V Power = 4.98 volts		
WARNING: hot-plug LOW above Vol=+0.4V		
WARNING: RX SENSE failed		
⊖ 01: 7.2 Verify the Sink DUT respond to the DDC transaction		Pass
		Pass
DDC2-2: Pull-Up Resistance		Pass
• Iter 01:		Pass
• +5V Power = 4.97 volts		
▲		Pass
• VSDA A = 0.797340V		
• Calculated resistance of SDA is 48342.3 ohms		
$4 \oplus 02$: 5.4 Verify the resistance of SCL is in valid Range		Pass
 Calculated resistance of SCL is 47778.9 ohms 		1000
DDC2-3: Bus Timing		Pass
A liter 01:		Pass
• +5V Power = 4.98 volts		
• WARNING: hot-plug LOW above Vol=+0.4V		
• WARNING: RX SENSE failed		
○ 01: 10 Verify the Sink DUT appropriately ACK each I2C transaction		Pass
01: 10 Verify the Sink bor appropriately Ken each 12c transaction		Pass
○ 02: 11.1 Verify NO t ND,DAT is less than ous ○ 03: 11.2 Verify NO t SU;DAT is less than 250ns		Pass
DDC2-4: Bus Timing		Pass
▲ Diter 01:		Pass
<pre> • +5V Power = 4.98 volts </pre>		1035
 WARNING: hot-plug LOW above Vol=+0.4V 		
• WARNING: NOC-pilly low above voi-to.4v		
-		Pass
○ 01: 5.7 Verify the Sink DUT appropriately ACK each I2C transaction	~	Pass
02: 5.8 Vefity the bytes read from offsets 0-7 constitute a valid EDII 03: 5.8 Velidete the EDID shockers bute mod from the Sick DUM		
03: 5.9 Validate the EDID checksum byte read from the Sink DUT		Pass
04: 6.7 Verify the Sink DUT appropriately ACK each I2C transaction	_	Pass
05: 6.8 Vefity the bytes read from offsets 0-7 constitute a valid EDII 0.000 C.0. Whidete the UDID sharks but much from the Cick DUM	,	Pass
\bigcirc 06: 6.9 Validate the EDID checksum byte read from the Sink DUT		Pass
DC2-1: 12C Bus LOW-level Output Voltage		
strument: [My980B [192.168.254.185]	- I	Continue Test Executi
		X Close

You can also obtain an HTML report. The report can be a summary or include the details of the test results. These are shown below.

Results Name: My_ACA_Sink_Test_3 Date Tested: October 7, 2015 8:38 AM Overall Status: Pass Test DDC2-1 I2C Bus LOW-level Output Voltage Test DDC2-2 Pull-Up Resistance		ifacturer: ACME el Name: XYZ	
I2C Bus LOW-level Output Voltage Test DDC2-2	Por	t Tested: 1	:
		Pass Pass	
Test DDC2-3 Bus Timing Test DDC2-4 Bus Timing		Pass Pass	



Test DDC2-2 Pass Pull-Up Resistance Pass • Iter 01: +5V Power = 4.97 volts • 01: 4.4 Verify the resistance of SDA is in valid Range Pass VSDA_A = 0.797340V Calculated resistance of SDA is 48342.3 ohms Pass • 02: 5.4 Verify the resistance of SCL is in valid Range Calculated resistance of SCL is 47778.9 ohms

Iter 01:		Pass
+5V Power = 4.98 volts		
 WARNING: hot-plug LOW above Vol=+0.4V WARNING: RX_SENSE failed 		
• 01: 10 Verify the Sink DUT appropriately ACK each I2C transaction	Pass	
• 02: 11.1 Verify NO t_HD;DAT is less than Ous	Pass	
• 03: 11.2 Verify NO t_SU;DAT is less than 250ns	Pass	