High-Definition Multimedia Interface

Version 1.4b

Quantum Data MOI v1.0

Test: DDC Sink

October 7, 2015

Preface

Notice

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Document Revision History

1.0 October 7, 2015 – Initial Release.

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Contact Information

The URL for the HDMI Forum web site is: **http://www.hdmiforum.org/**

The URL for the Quantum Data website is: **http://www.quantumdata.com**.

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Introduction

This document provides a set of test methods for tests described in High-Definition Multimedia Interface Compliance Test Specification DDC Clarification.

Scope

This document provides testing procedures for HDMI CTS 1.4b Sink DDC tests: 1) I2C Bus LOW-level Output Voltage, 2) Pull-Up Resistance, 3) Bus Timing (driving SDA) and 4) Bus Timing (reading SDA).

References

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Compliance Test Specification DDC Clarification, Version 1.04 – May 1, 2014.

Informative Reference

No additional informative references.

Test: Sink - I^2C Bus LOW-Level Output Voltage

Objective

Confirm that the LOW-level output voltage of the I^2C Bus, formed when connecting the Sink DUT to a compliant Source configured so that a LOW-level output current of 3mA results in V_{OL} = 0.4V, is less than or equal to the required maximum V_{OL} for the DDC SDA signal.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Display Data Channel (DDC) I/Os and wires (SDA, SCL, DDC/CEC Ground), shall meet the requirements specified in the I2C-bus specification and user manual UM10204, Rev. 5 ("I2C Specification"), Section 6.1 for “Standard-mode” devices...
I2C-bus specification and user manual UM10204, Rev.5, Section 6.1	Maximum LOW-level output voltage, V_{OL} = 0.4V (at 3mA sink current)

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Master EDID Analyzer	980 Advanced Test Platform series: 980 HDMI Phy & Protocol Aux Channel Analyzer module.	1

Generic Procedure

Setup:

1. Connect TPA to Sink DUT.
2. Configure DDC Master with 1.5K pull-up resistance to +4.7V supply on both SCL and SDA wires.
3. Connect EDID Analyzer to DDC Master.
4. Connect DDC Master to TPA.
5. Apply +5.0V between +5V Power and DDC/CEC Ground.
6. Power on the Sink DUT.
7. Test LOW-level output voltage of SDA:

7.1. Use the DDC Master to read block 0 of the Sink's EDID.

7.2. If the Sink DUT does not respond to the DDC transaction, then FAIL.

7.3. Use the DDC Master (if capable) or the General Oscilloscope to measure the LOW-level output voltage of SDA (VOL-SDA) during the DDC read transaction.

7.4. If VOL-SDA > 0.4V, then FAIL.

Test: Sink - Pull-Up Resistance

Objective

Confirm that the Sink pull-up resistance meets the minimum requirements for DDC signals SCL and SDA.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Sink pull-up resistance on SDA shall be greater than, or equal to, 42.3kΩ (which is 47kΩ minus 10%).
HDMI 1.4b, Section 4.2.8	Sink pull-up resistors for SCL signal – 47kΩ +/-10%

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1		980 Advanced Test Platform series: 980 HDMI Phy & Protocol Aux Channel Analyzer module.	1

Generic Procedure

Setup:

1. Connect TPA to Sink DUT HDMI input connector.
2. Drive +5.0V between +5V Power and DDC/CEC Ground on the TPA.
3. Power on the Sink DUT.
4. Test the resistance of SDA:
    - 4.1. Measure, then connect a 10K, 1% resistor (RSDA-T) between the SDA pin and DDC/CEC Ground on the TPA.
    - 4.2. Measure the voltage of the SDA pin on the TPA (VSDA-A) referenced to DDC/CEC Ground on the TPA.
    - 4.3. If 0V ≤ VSDA-A ≤ 0.1V, then skip to step 5.
    - 4.4 Leave the 10K, 1% resistor (RSDA-T) connected (as it was in step 4.1). Measure, then connect an additional 51.7K 1% resistor (RSDA-S) to the SDA pin on the TPA. Connect the other end the 51.7K 1% resistor (RSDA-S) to the positive terminal of a DC Power Supply set to +3.58V 1% and measured (VSDA-B). Connect the negative

terminal of the (VSDA-B) supply to DDC/CEC Ground on the TPA. The Thevenin equivalent of this test circuit is calculated as VSDA-TH = VSDA-B (1/(1+(RSDA-S/RSDA-T))) and RSDA-TH = (RSDA-S*RSDA-T)/(RSDA-S+RSDA-T).

4.5. Measure the voltage of the SDA pin on the TPA (VSDA-C) referenced to DDC/CEC Ground on the TPA.

4.6. Remove the 10K, 1% resistor, leaving the 51.7K 1% resistor and +3.58V DC Power Supply (that were added in step 4.4).

4.7. Measure the voltage of the SDA pin on the TPA (VSDA-D) referenced to DDC/CEC Ground on the TPA.

4.8. If 42300 ohms ≤ (VSDA-D - VSDA-C)/(((VSDA-C - VSDA-TH)*(1/RSDA-TH))-((VSDA-D - VSDA-B)*(1/RSDA-S))), then continue; otherwise FAIL.

5. Test the resistance of SCL:

5.1 Measure, then connect a 51.7K 1% resistor (RSCL-S) to the SCL pin on the TPA. Connect the other end the 51.7K 1% resistor (RSCL-S) to the positive terminal of a DC Power Supply set to +3.58V 1% and measured (VSCL-A). Connect the negative terminal of the (VSCL-A) supply to DDC/CEC Ground on the TPA.

5.2. Measure the voltage of the SCL pin on the TPA (VSCL-B) referenced to DDC/CEC Ground on the TPA.

5.3. Measure, then connect an additional 10K, 1% resistor (RSCL-T) between the SCL pin and DDC/CEC Ground on the TPA, leaving the 51.7K 1% resistor (RSCL-S) and +3.58V DC Power Supply (VSCL-A) that were added in step 5.1. The Thevenin equivalent of this test circuit is calculated as VSCL-TH = VSCL-A (1/(1+(RSCL-S/RSCL-T))) and RSCL-TH = (RSCL-S*RSCL-T)/(RSCL-S+RSCL-T).

5.4. Measure the voltage of the SCL pin on the TPA (VSCL-C) referenced to DDC/CEC Ground on the TPA.

5.5. If 42300 ohms ≤ (VSCL-B - VSCL-C)/(((VSCL-C - VSCL-TH)*(1/RSCL-TH))-((VSCL-B - VSCL-A)*(1/RSCL-S))) ≤ 51700 ohms, then PASS; otherwise FAIL.

Test: Sink - Bus Timing (driving the SDA signal)

Objective

Confirm that the Sink meets the setup and hold bus timing parameters specified in the I2C bus specification when driving the SDA signal.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Display Data Channel (DDC) I/Os and wires (SDA, SCL, DDC/CEC Ground), shall meet the requirements specified in the I2C-bus specification and user manual UM10204, Rev. 5 ("I2C Specification"), Section 6.1 for “Standard-mode” devices….
I2C-bus specification and user manual UM10204, Rev.5, Section 6.1	1) Data hold time ($t_{HD;DAT}$) ≥ 0 µs 2) Data setup time ($t_{SU;DAT}$) ≥ 250 ns

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Master EDID Analyzer	980 Advanced Test Platform series: 980 HDMI Phy & Protocol Aux Channel Analyzer module.	1

Generic Procedure

Setup:

1. Connect TPA to Sink DUT.
2. Configure DDC Master with 2.0K pull-up resistance to +5.5V supply on both SCL and SDA wires.
3. Configure DDC Master to achieve 750pF total capacitance on SCL and SDA wires.
4. Configure DDC Master so that f_{SCL} = 100kHz.
5. Connect EDID Analyzer to DDC Master.
6. Connect DDC Master to TPA.
7. Apply +5.0V between +5V Power and DDC/CEC Ground.
8. Power on the Sink DUT.

9. Use the EDID Analyzer to read block 0 of the Sink's EDID.

10. If the Sink DUT does not appropriately ACK each I2C transaction, then FAIL.

11. Use the DDC Master (if capable) or the General Oscilloscope to measure the specified timing parameters for each occurrence during the EDID read.

    11.1. If any occurrence of $t_{HD;DAT} < 0\mu s$, then FAIL.

    11.2. If any occurrence of $t_{SU;DAT} < 250ns$, then FAIL.

Test: Sink - Bus Timing (reading the SDA signal)

Objective

Confirm that the Sink does not require more setup or hold time than specified in the I2C bus specification when reading the SDA signal.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Display Data Channel (DDC) I/Os and wires (SDA, SCL, DDC/CEC Ground), shall meet the requirements specified in the I2C-bus specification and user manual UM10204, Rev. 5 ("I2C Specification"), Section 6.1 for “Standard-mode” devices….
I2C-bus specification and user manual UM10204, Rev.5, Section 6.1	1) Data hold time ($t_{HD;DAT}$) ≥ 0 µs 2) Data setup time ($t_{SU;DAT}$) ≥ 250 ns

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Master EDID Analyzer	980 Advanced Test Platform series: 980 HDMI Phy & Protocol Aux Channel Analyzer module.	1

Generic Procedure

Setup:

1. Connect TPA to Sink DUT.
2. Configure DDC Master with 2.0K pull-up resistance to +5.5V supply on both SCL and SDA wires.
3. Configure DDC Master to achieve 750pF total capacitance on SCL and SDA wires.
4. Configure DDC Master so that f_{SCL} = 100kHz.
5. Test the hold time sensitivity of the Sink DUT:
    - 5.1. Configure DDC Master so that when the DDC Master is writing to SDA, the hold time of SDA is equal to 0 µs.
    - 5.2. Connect EDID Analyzer to DDC Master.
    - 5.3. Connect DDC Master to TPA.

5.4. Apply +5.0V between +5V Power and DDC/CEC Ground.

5.5. Power on the Sink DUT.

5.6. Use the EDID Analyzer to read block 0 of the Sink's EDID.

5.7. If the Sink DUT does not appropriately ACK each I2C transaction, then FAIL.

5.8. If the bytes read from offsets 0-7 do not constitute a valid EDID header, then FAIL.

5.9. If the EDID checksum byte read from the Sink DUT does not match the checksum calculated by the EDID analyzer, then FAIL.

6. Test the setup time sensitivity of the Sink DUT:

6.1. Configure DDC Master so that when the DDC Master is writing to SDA, the setup time of SDA is equal to 250ns.

6.2. Connect EDID Analyzer to DDC Master.

6.3. Connect DDC Master to TPA.

6.4. Apply +5.0V between +5V Power and DDC/CEC Ground.

6.5. Power on the Sink DUT.

6.6. Use the EDID Analyzer to read block 0 of the Sink's EDID.

6.7. If the Sink DUT does not appropriately ACK each I2C transaction, then FAIL.

6.8. If the bytes read from offsets 0-7 do not constitute a valid EDID header, then FAIL.

6.9. If the EDID checksum byte read from the Sink DUT does not match the checksum calculated by the EDID analyzer, then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

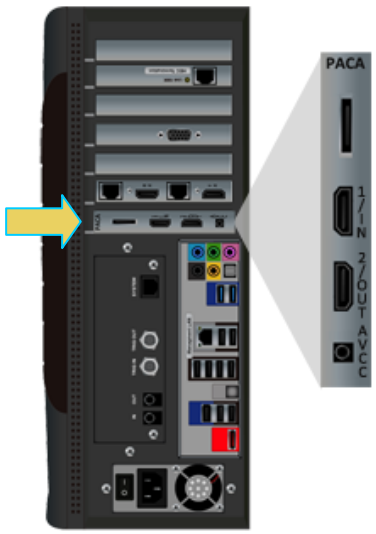
HDMI Phy & Protocol Aux Channel Analyzer Module

The Quantum Data 980 HDMI Phy & Protocol Aux Channel Analyzer module can be installed in the 980B or 980R series Advanced Test Platforms. This 980 HDMI Phy & Protocol Aux Channel Analyzer module serves the generic test functions called out in the HDMI CTS DDC Clarification. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI Phy & Protocol Aux Channel Analyzer module

980 HDMI Phy & Protocol Aux Channel Analyzer with 980B Series Platform Configuration

The figure below shows a depiction of the 980 Phy & Protocol Aux Channel Analyzer module equipped in various 980B platform. **Note**: Card positioning may vary depending on configuration.



Tests: Sink DDC Tests

1. Objectives

I2C Bus LOW-level Output Voltage - Confirm that the LOW-level output voltage of the I2C Bus, formed when connecting the Sink DUT to a compliant Source configured so that a LOW-level output current of 3mA results in VOL = 0.4V, is less than or equal to the required maximum VOL for the DDC SDA signal.

Pull-Up Resistance - Confirm that the Sink pull-up resistance meets the minimum requirements for DDC signals SCL and SDA.

Bus Timing (driving SDA) - Confirm that the Sink meets the setup and hold bus timing parameters specified in the I2C bus specification when driving the SDA signal.

Bus Timing (reading SDA) - Confirm that the Sink does not require more setup or hold time than specified in the I2C bus specification when reading the SDA signal.

2. Test Overview

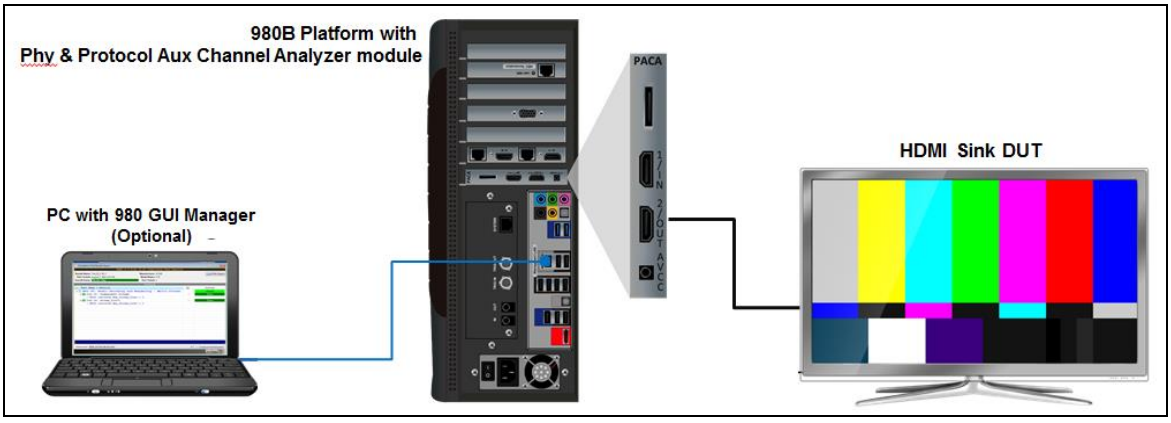
The Pass/Fail criteria is assessed by the application with no human examination required.

3. Procedure

Use the following procedure to conduct this test.

1 Connect Sink DUT to the Quantum Data 980 HDMI Phy & Protocol Aux Channel Analyzer at the module's port labeled IN. Use a High Speed HDMI cable. The figure below shows a depiction of connections to the 980 HDMI Phy & Protocol Aux Channel Analyzer module residing in the 980 series chassis.

Note: Be sure to use the supplied HDMI cable. Part No. 30-00218 Description: CBL, HDMI, 7ft High Speed Heac, Calibrated-Sink.



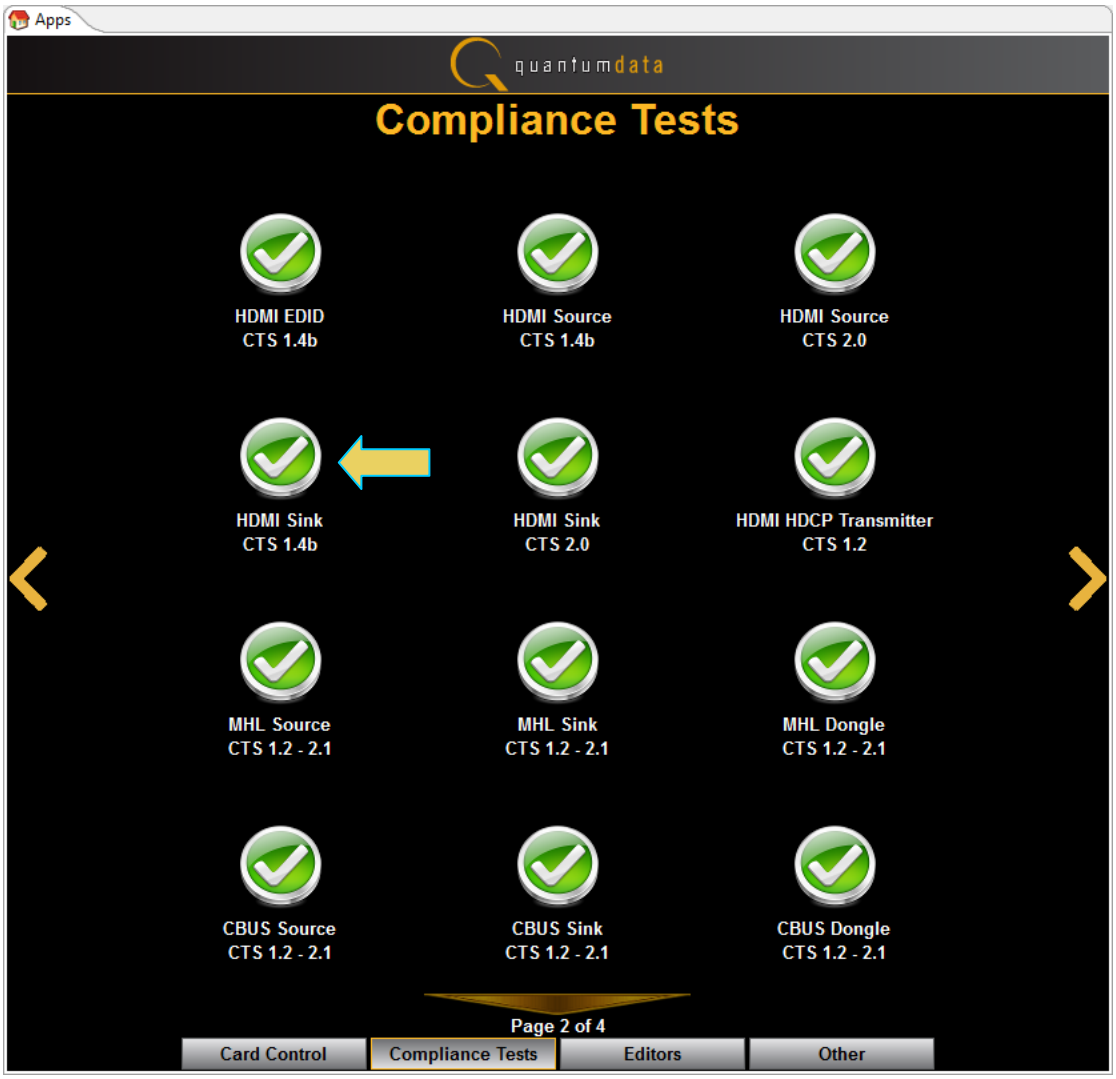
2 Operate the Sink DUT in a normal mode.

3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

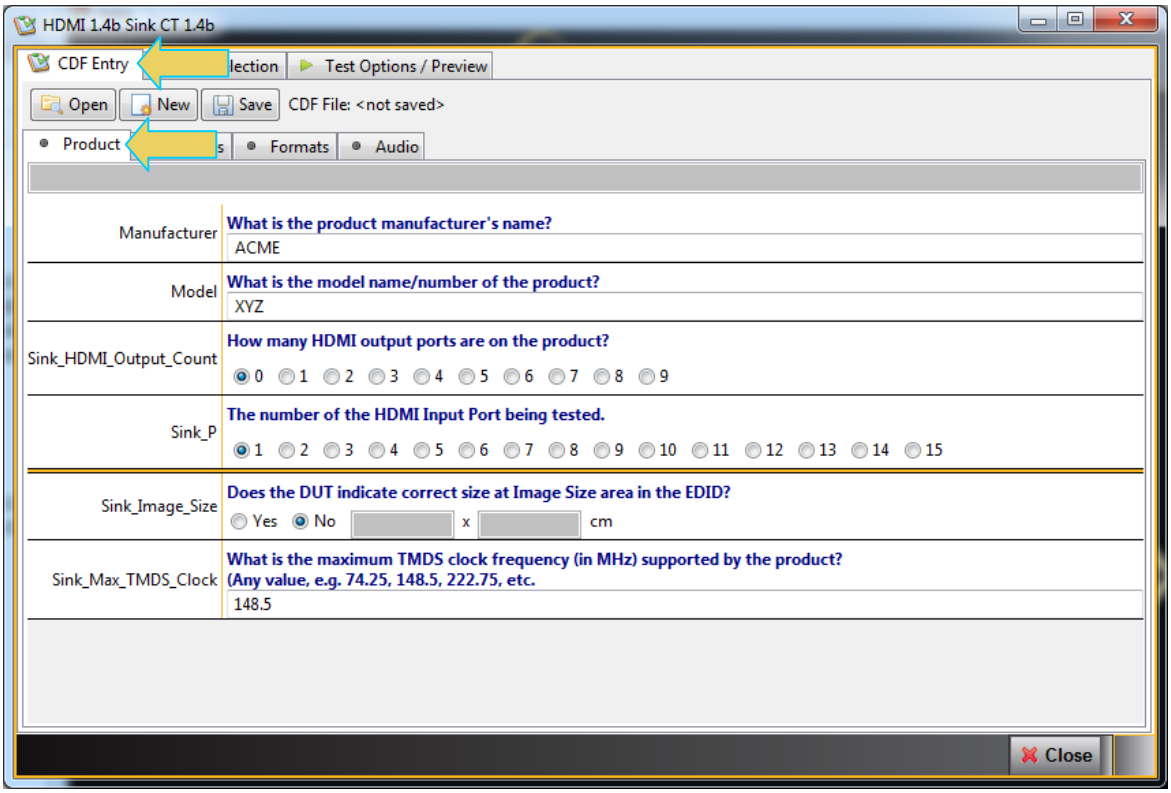
Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Phy & Protocol Aux Channel Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

4 Complete the following steps:

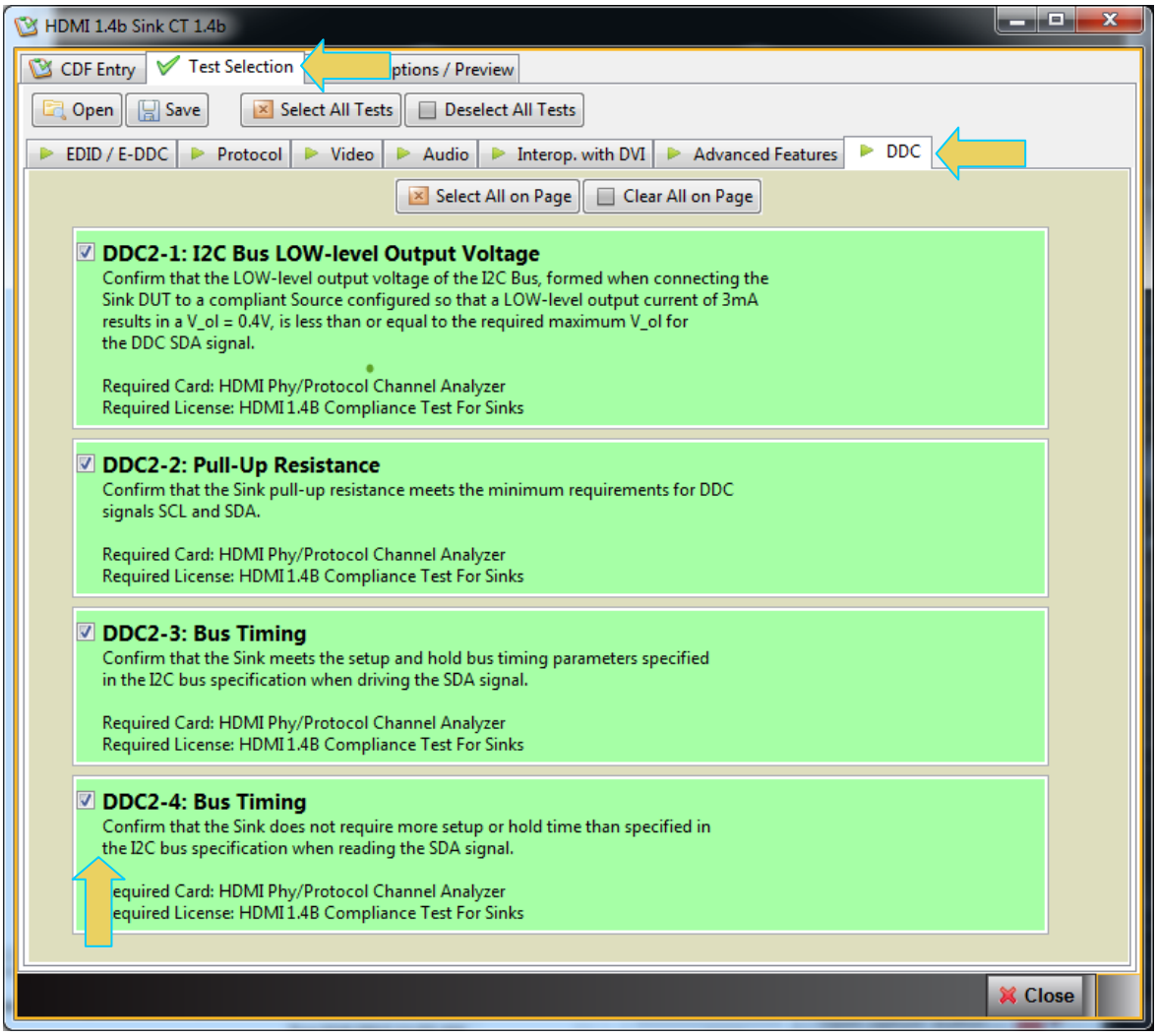
4.1 Click on the HDMI Source CTS 1.4b icon in the Compliance Tests page of the Apps panel.



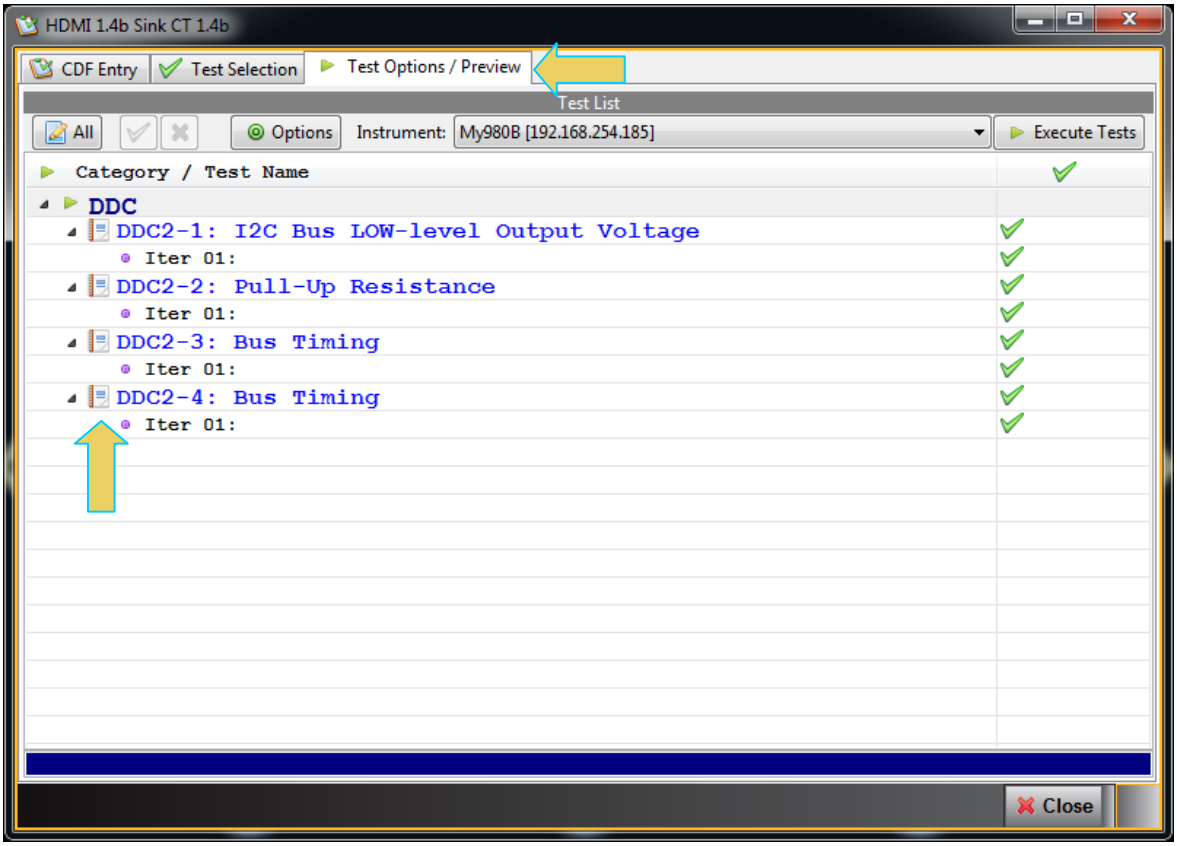
4.2 Navigate to the CDF tab if not already there. There are no CDF requirements to be entered. Simply fill in the name and model number of the device and click OK and optionally save the file. Be sure to indicate the number of HDMI outputs.



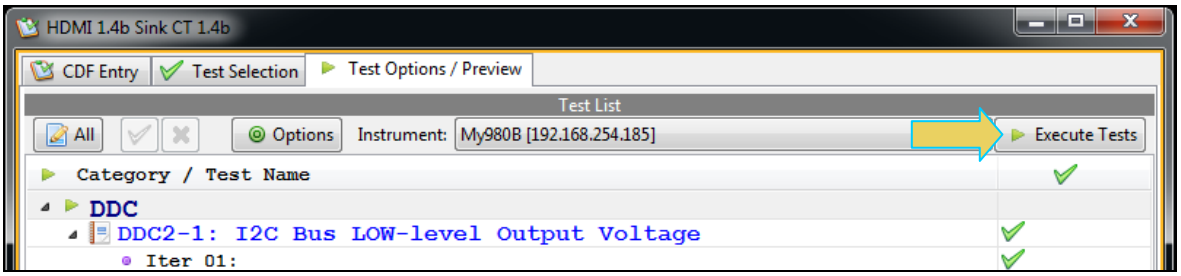
4.3 Click on the Test Selection tab and the DDC sub tab and select the DDC1-1: I2C Bus Low-Level Output Voltage test, the DDC1-2 Pull-Up Resistance test; DDC1-3: Bus Timing (driving the SDA); and the DDC1-4: Bus Timing (reading the SDA). Refer to the sample screen below.



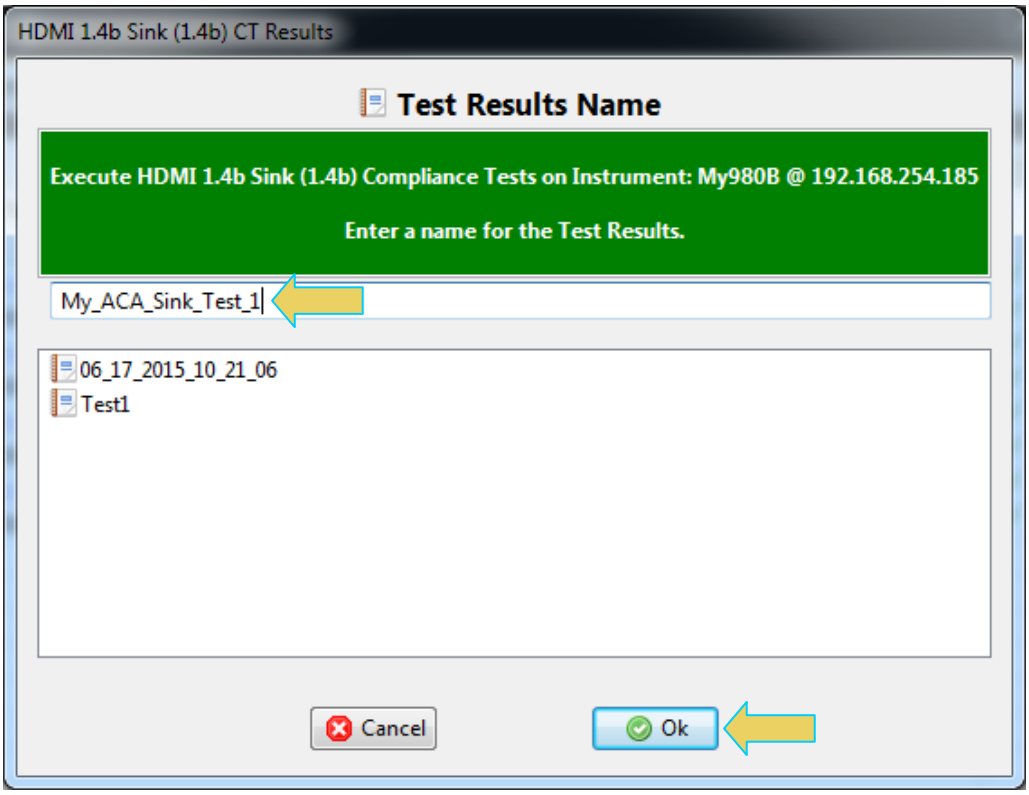
4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.

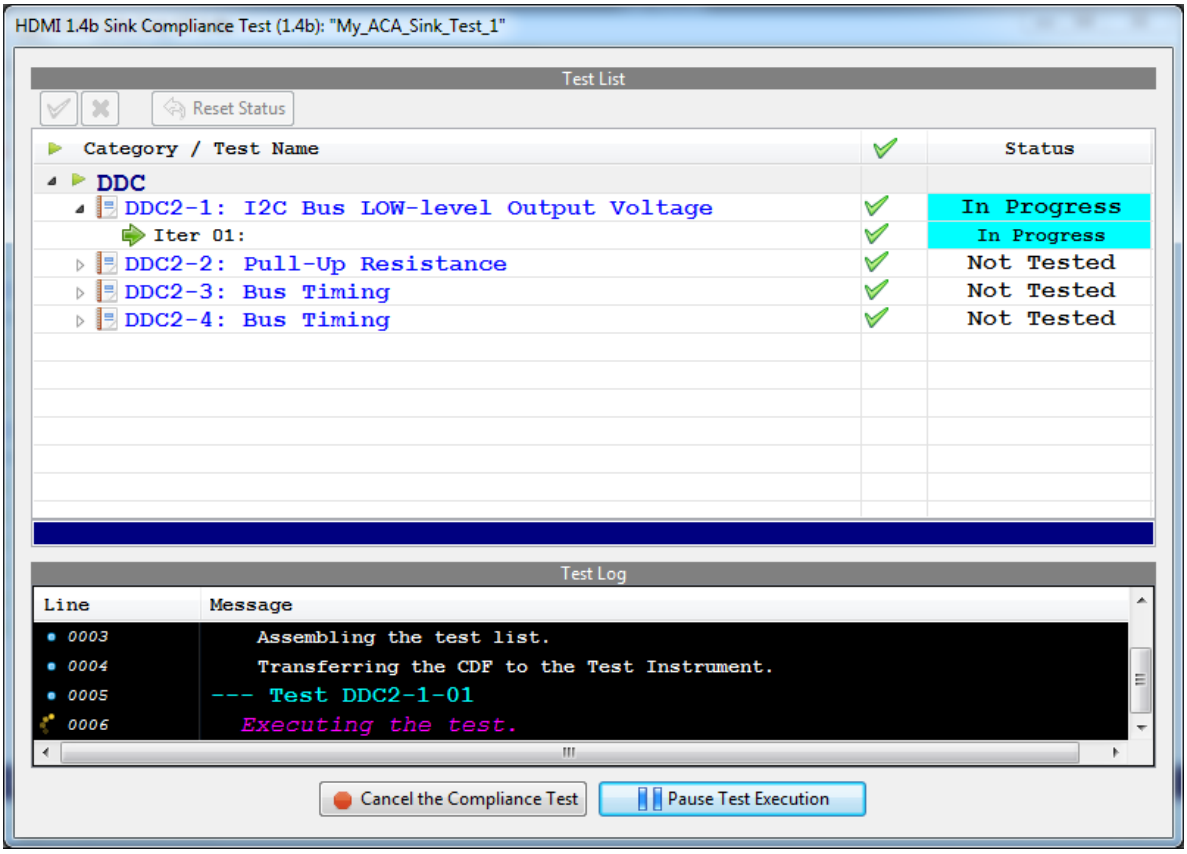


Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:

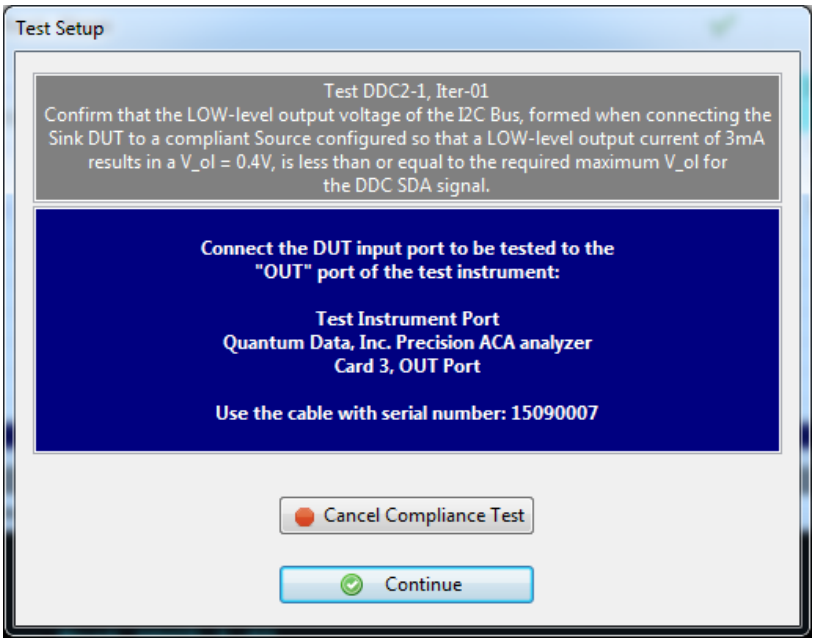


Enter a name, click OK and the test will begin.

A Test Window will appear (below) indicating the progress of the test.

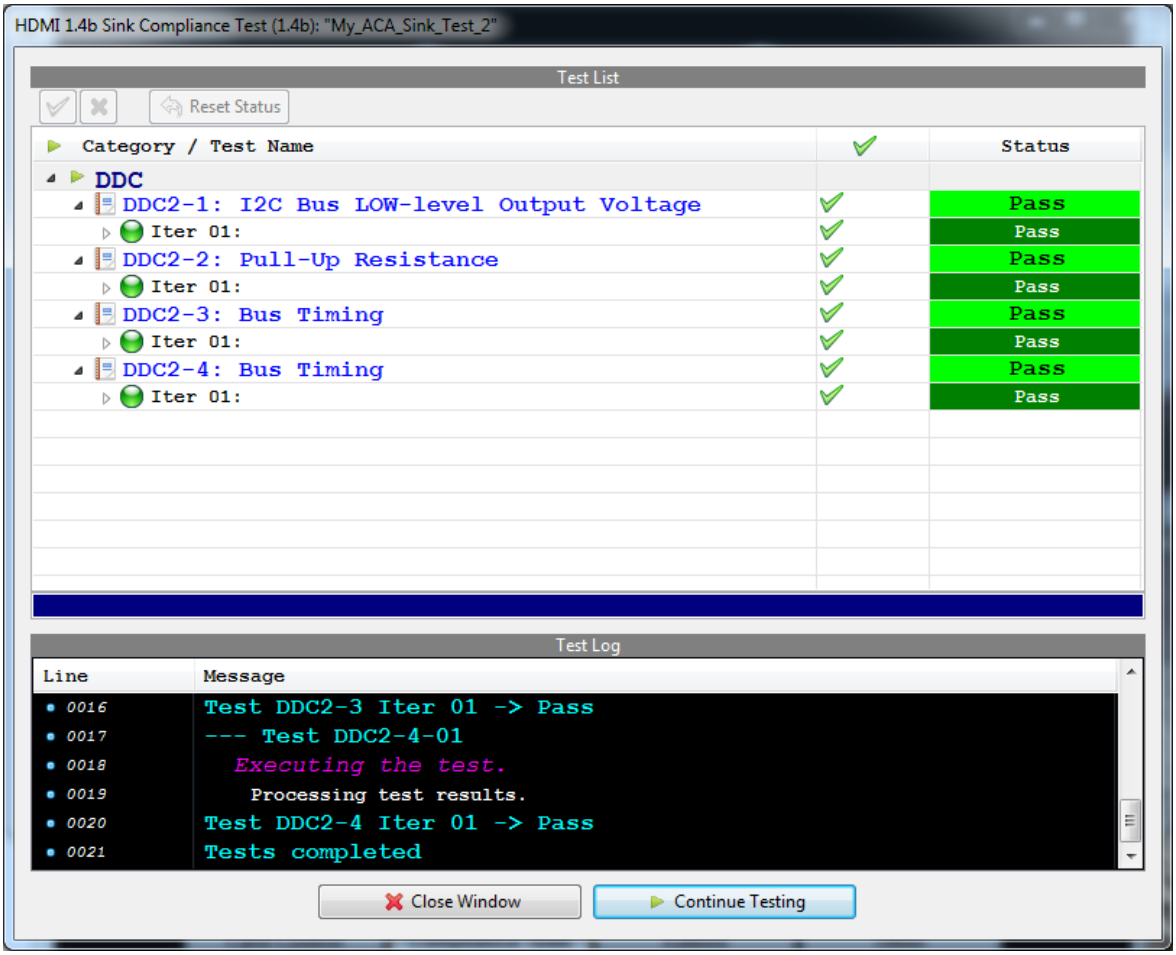


A dialog box will appear (below) indicating the test setup.

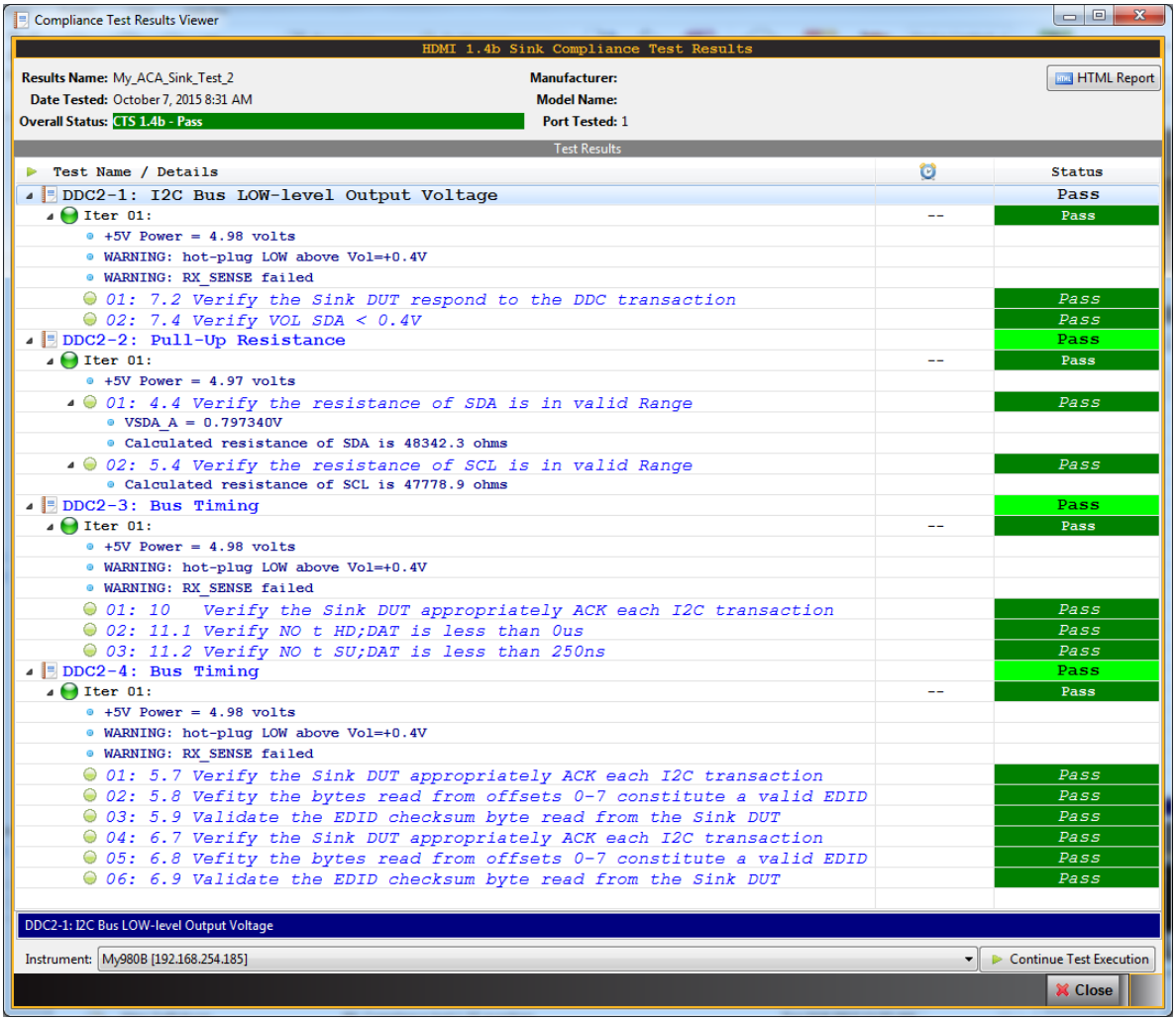


Note: Be sure to use the supplied HDMI cable. Part No. 30-00218.

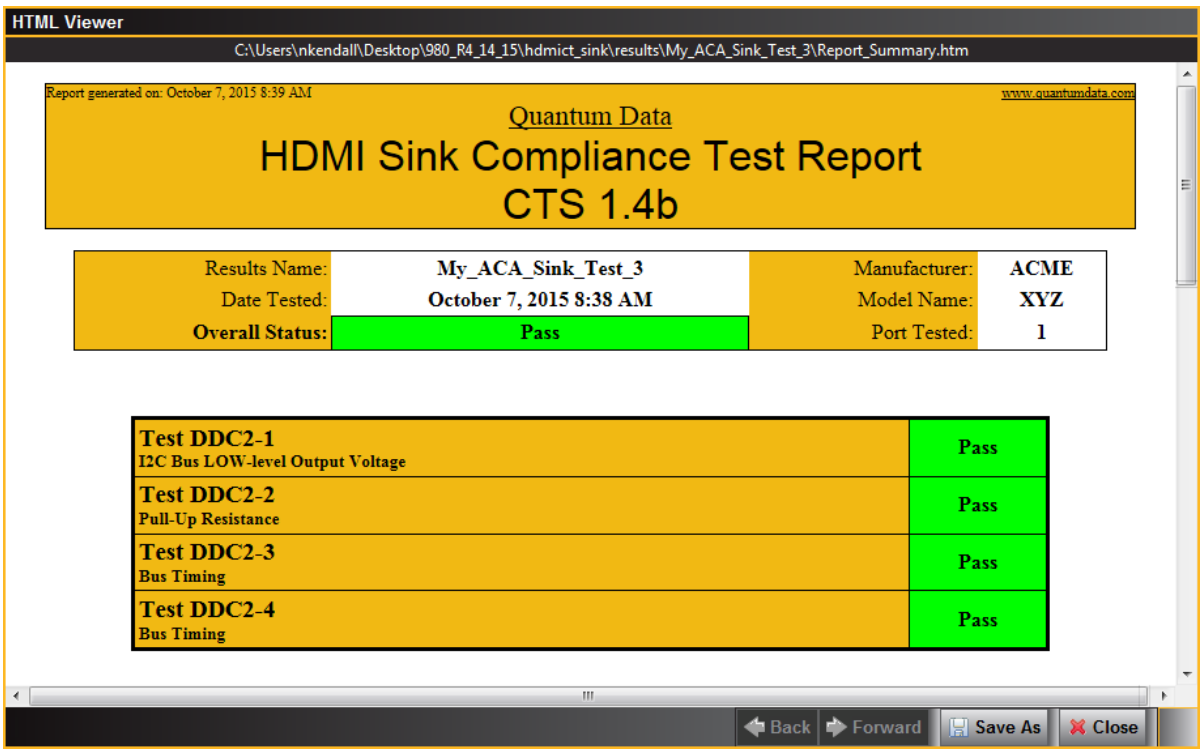
When the tests are complete the results are shown in the test window.

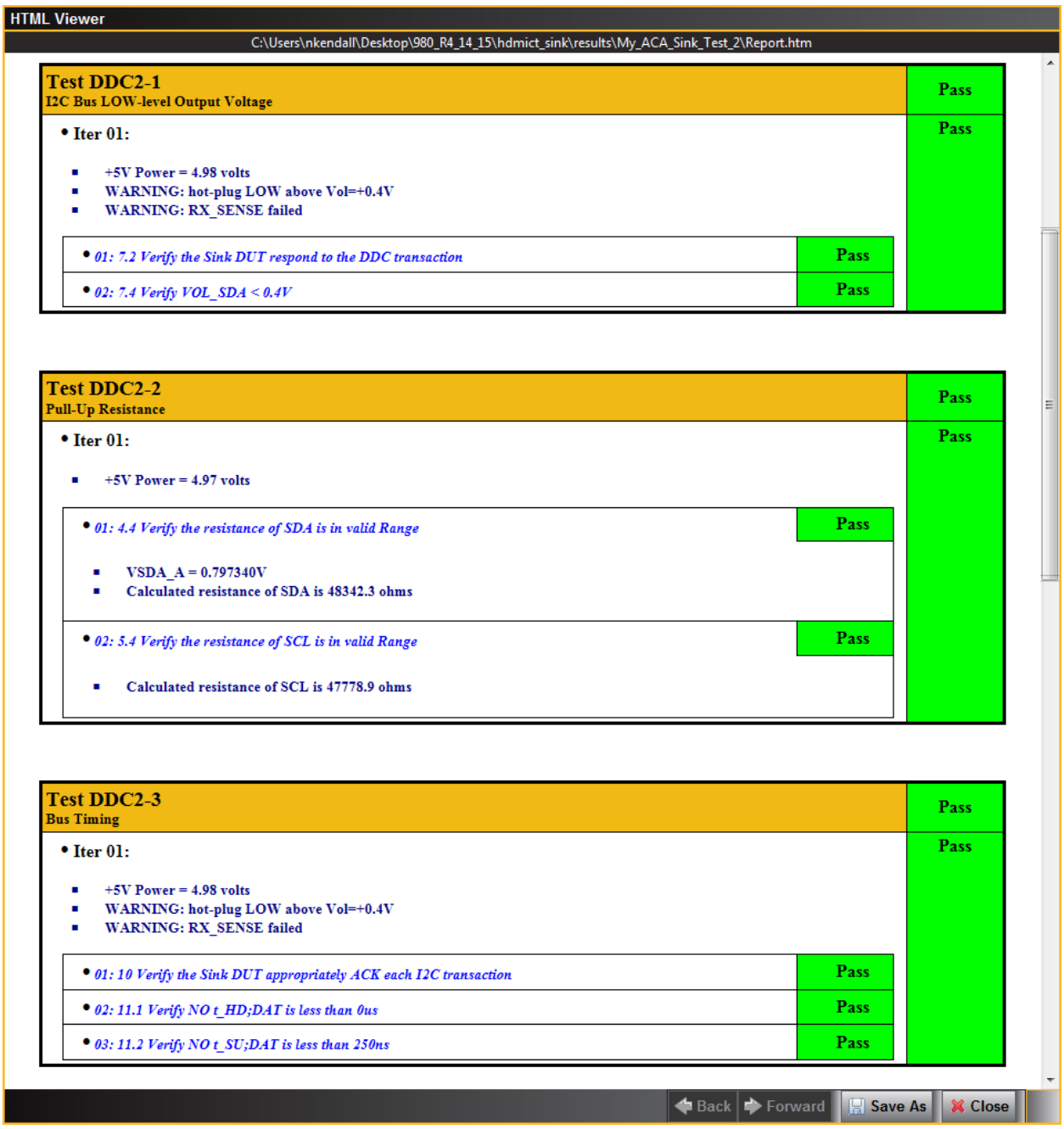


The test will run and the test application will assess pass or fail. The test results screens appears as shown below. If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS. If the 980 HDMI Phy & Protocol Aux Channel Analyzer compliance test application reports FAIL, then FAIL.



You can also obtain an HTML report. The report can be a summary or include the details of the test results. These are shown below.


HTML Viewer
C:\Users\nkendall\Desktop\980_R4_14_15\hdmict_sink\results\My_ACA_Sink_Test_3\Report_Summary.htm
Report generated on: October 7, 2015 8:39 AM
www.quantumdata.com
Quantum Data
HDMI Sink Compliance Test Report
CTS 1.4b
Results Name: My_ACA_Sink_Test_3
Date Tested: October 7, 2015 8:38 AM
Overall Status: Pass
Manufacturer: ACME
Model Name: XYZ
Port Tested: 1
Test DDC2-1
I2C Bus LOW-level Output Voltage
Pass
Test DDC2-2
Pull-Up Resistance
Pass
Test DDC2-3
Bus Timing
Pass
Test DDC2-4
Bus Timing
Pass
Back
Forward
Save As
Close


HTML Viewer
C:\Users\nkendall\Desktop\980_R4_14_15\hdmict_sink\results\My_ACA_Sink_Test_2\Report.htm
Test DDC2-1
I2C Bus LOW-level Output Voltage
Pass
Pass
• Iter 01:
▪ +5V Power = 4.98 volts
▪ WARNING: hot-plug LOW above Vol=+0.4V
▪ WARNING: RX_SENSE failed
• 01: 7.2 Verify the Sink DUT respond to the DDC transaction
Pass
• 02: 7.4 Verify VOL_SDA < 0.4V
Pass
Test DDC2-2
Pull-Up Resistance
Pass
Pass
• Iter 01:
▪ +5V Power = 4.97 volts
• 01: 4.4 Verify the resistance of SDA is in valid Range
Pass
▪ VSDA_A = 0.797340V
▪ Calculated resistance of SDA is 48342.3 ohms
• 02: 5.4 Verify the resistance of SCL is in valid Range
Pass
▪ Calculated resistance of SCL is 47778.9 ohms
Test DDC2-3
Bus Timing
Pass
Pass
• Iter 01:
▪ +5V Power = 4.98 volts
▪ WARNING: hot-plug LOW above Vol=+0.4V
▪ WARNING: RX_SENSE failed
• 01: 10 Verify the Sink DUT appropriately ACK each I2C transaction
Pass
• 02: 11.1 Verify NO t_HD;DAT is less than 0us
Pass
• 03: 11.2 Verify NO t_SU;DAT is less than 250ns
Pass
Back
Forward
Save As
Close