Acromag®

Series 935X-I
VME Isolated Analog I/O Card

Series 9450-I
VME General Purpose Isolated Digital I/O Card

Series 9510-X
VME Multi-Function Card

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ redundancy, and comprehensive failure analysis to insure a safe and satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

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1.1 INTRODUCTION

The AVME935X-I/9450-I/9510-X Series of VME cards offer a variety of features which make them an ideal choice for a broad spectrum of Data Aquisition and Control Applications. The following table highlights these features.

	ANALOG INPUTS	ANALOG OUTPUTS	DIGITAL I/O
AVME9350-I	xx		
AVME9351-I	xx	xx	
AVME9450-I			xx
AVME9510 AVME9510-I	xx xx	xx xx	xx xx

General Features

- All Analog Inputs, Analog Outputs and Digital Inputs and Outputs are Isolated as a group from the VMEbus (except model AVME9510).
- BYTE or WORD data transfers.
- PASS/FAIL status indicator LEDs on the front panel.

1.2 ANALOG INPUT FEATURES (935X-I & 9510-X)

- High level inputs - 16 differential/32 single-ended (jumper selectable).
- High speed successive approximation 12 bit A/D converter for a maximum throughput time of 32 microseconds per conversion.
- Jumper selectable input ranges of ±10V, 0-10V and ±5V.
- Software programmable gains of 1, 2, 4, and 8.
- Resistor programmable gains of 1 to 1000 (special order).
- External trigger input capability for synchronization of the conversion sequence to external events.
- Hardware Timed Periodic Conversion capability for precise sampling intervals.

- Field connections accessible through the P2 connector.

- User calibration for "live end-points" of spans.

- Scan Mode for efficient scanning of sequential channels.

1.3 ANALOG OUTPUT FEATURES (9351-I & 9510-X)

-High level voltage outputs - 2 channels.

-12 bit D/A conversion with settling time of 6 microseconds.

-Field connections accessible through the P2 connector.

-Jumper selectable output ranges of ±10V, ±5V, ±2.5V, 0 to +5V, 0 to +10V.

1.4 DIGITAL I/O FEATURES (9450-I & 9510-X)

-32 programmable I/O points (lines) configured as four - 8 bit ports.

-Ability to read back output states.

-Outputs sink up to 100 mA, from up to a 30 V source.

-Built-in protection diodes for driving relay coils.

-Input filtering (by installing capacitor networks, see Section 2.7.1).

-Input range of 0 to 30 v.

-Input hysteresis (0.3 Volts).

-Input threshold adjustable (by installing Resistor Networks, see Section 2.7.2).

-Compatible with industry standard solid state relays and termination panels, PB16A.

-Field connections accessible through connectors mounted on the Front Panel.

-TTL and CMOS compatible.

1.5 VMEbus INTERFACE FEATURES

-Slave module A24, A16, D16, D08 (EO).

-Short I/O Address Modifiers 29H, 2DH (a capital H suffix indicates a hexadecimal number).

-Standard Address Modifiers 39H, 3DH.

-I(1-7) interrupter (w/analog inputs only) - jumper programmable interrupt level, software programmable interrupt vector. Release On Register Access (RORA) type.

-Decode on 1K byte boundaries.

1.6 FIELD COMPATIBILITY

See specific instruction manuals for more information on compatible products.

1.6.1 Analog Inputs and Outputs

Directly compatible with Acromag termination panels via a ribbon cable connected to P2.

Cable:

Model 9940 -	Standard 50 pin analog cable.
Model 9941 -	Shielded 50 pin analog cable.

Termination Panel:

Model 6924-16D -	Sixteen differential high level inputs and two analog outputs.
Model 6924-32S -	Thirty-two single-ended high level inputs and two analog outputs.
Model 6925-16D -	Sixteen filtered differential inputs and two analog outputs.

1.6.2 Digital Inputs and Outputs

Directly compatible with Acromag universal termination panels and the industry standard type PB16A solid state relay termination panels.

Cable:

Model 9943 -	Standard 50 pin cable for connecting the digital I/O to termination panels with edge connectors.

Termination Panel:

Model 6980-16U -	Sixteen channel universal digital termination panel.
Model 6980-16 -	PB16A type solid state relay termination panel.

This chapter provides information about preparing your board for system operation.

2.1 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

The board is adequately protected with foam during shipment. It is advisable though to visually inspect the board for evidence of severe handling prior to applying power.

2.2 CARD CAGE CONSIDERATIONS

Refer to the specifications for bus loading and power requirements. Be sure that the system power supplies are able to accommodate the additional requirements within the voltage tolerances specified.

Adequate circulation of air must be provided to prevent a temperature rise above the maximum operating temperature. Large and continuing fluctuations in ambient air temperature should be avoided. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air filtering.

2.3 BOARD CONFIGURATION

The Board may be configured in a variety of ways for many different applications. Each possible jumper setting will be discussed in the following sections. The jumper locations are shown in Figure 2.1.

2.3.1 Default Jumper Configuration

VMEbus INTERFACE CONFIGURATION

When a board is shipped from the factory, it is configured as follows:

- VMEbus Short I/O Address of 0000H.

- Set to respond to both Address Modifiers 29H and 2DH.

- Interrupt Level: none. Therefore, even if interrupts are enabled through the Board Status Register, no interrupts will be caused. Interrupts are available with analog inputs only.

2.3.1.1 Analog Input Default Configuration

- 16 Differential Input Channels numbered 0 through 15.

- -10V to +10V Input Range calibrated for Binary 2's complement data as follows:

Analog Input Voltage	A/D Data (12 Bits Left Justified)
+9.9951 V	7FF0 H
+9.9902 V	7FE0 H
.	.
.	.
.	.
+0.0049 V	0010 H
0.0000 V	0000 H
-0.0049 V	FFF0 H
.	.
.	.
.	.
-9.9951 V	8010 H
-10.0000 V	8000 H

2.3.1.2 Analog Output Default Configuration

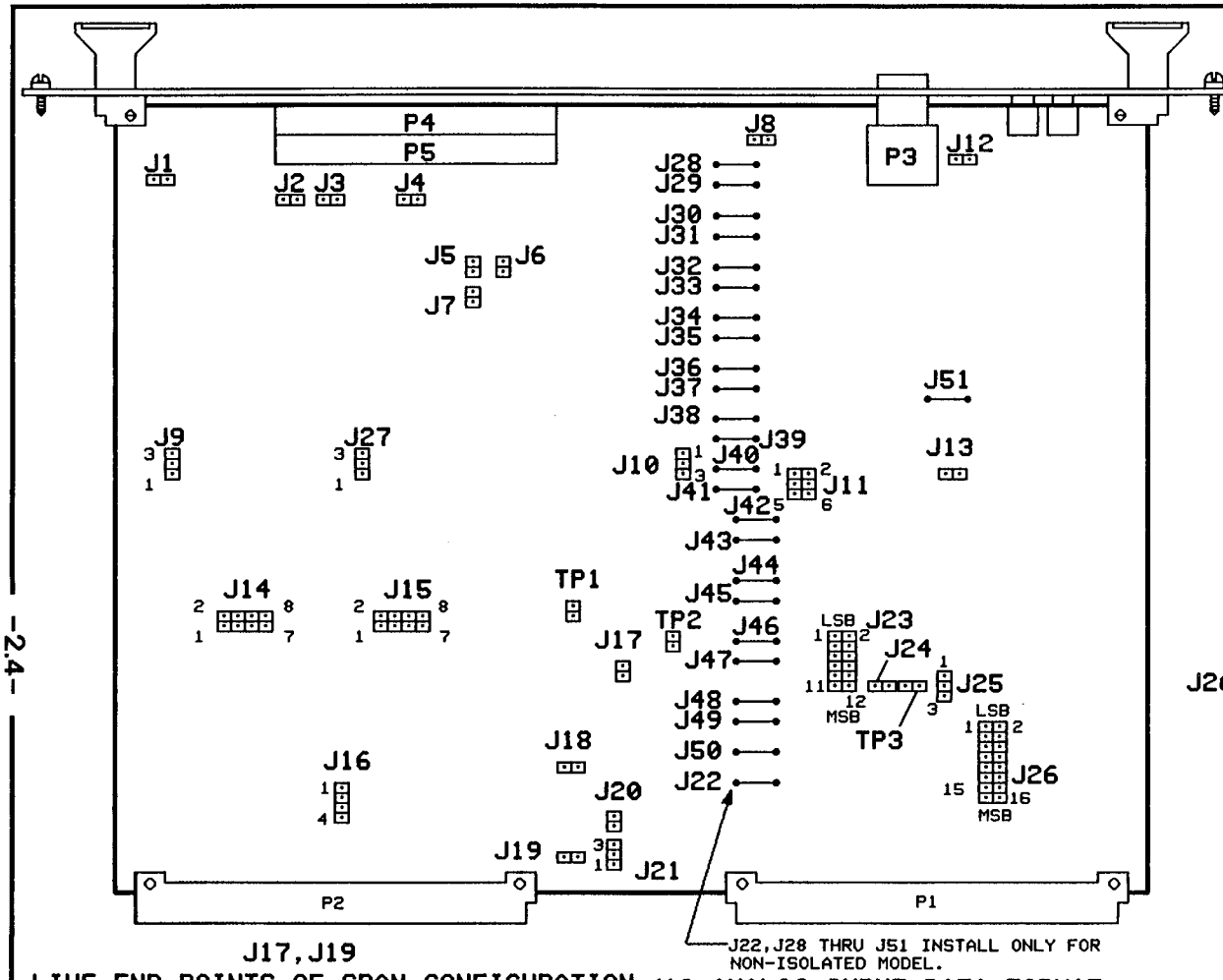
- 2 Analog Output Channels numbered 0 and 1.

- -10V to +10V Output Range calibrated for Binary 2's complement data as follows:

D/A Data (12 Bits Left Justified)	Analog Output Voltage
7FF0 H	+9.9951 V
7FE0 H	+9.9902 V
.	.
.	.
.	.
0010 H	+0.0049 V
0000 H	0.0000 V
FFF0 H	-0.0049 V
.	.
.	.
.	.
8010 H	-9.9951 V
8000 H	-10.0000 V

2.3.1.3 Digital I/O Default Configuration

- 32 Programmable Digital Input/Output points.
- All configured as inputs.
- 0-5V Range (All lines jumpered to be pulled up by the internal 5V supply).
- Digital filtering (capacitor network not installed, see Section 2.7.1).
- Hystersis threshold set at 1 volt to 1.3 volts (resistor networks not installed, see Section 2.7.2).



J17,J19

J22,J28 THRU J51 INSTALL ONLY FOR NON-ISOLATED MODEL.

DIGITAL I/O PULL-UP VOLTAGE JUMPERS J3,J1

PORTS N+0,N+1	J3
PORTS N+2,N+3	J1

VS+ & VS- (J8 & J12)

SUPPLY	SUPPLY ON	SUPPLY OFF
VS+	J8 (IN)	J8 (OUT)
VS-	J12 (IN)	J12 (OUT)

J23 BASE ADDRESS DECODE

OPEN=0 CLOSED=1

A15 A10	BASE ADDRESS
000000	00000000H
000001	00000400H
000010	00000800H
000011	00000C00H
000100	00001000H
•	•
•	•
•	•
111011	0000EC00H
111100	0000F000H
111101	0000F400H
111110	0000F800H
111111	0000FC00H

J11 INTERRUPT LEVEL SELECTION

OPEN=0 CLOSED=1

INTERRUPT LEVEL	PINS OF J11 5 & 6	3 & 4	1 & 2
NONE	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

J25,J24,J13 ADDRESS MODIFIER SELECTION

PINS OF J25,J24,J13 J25 1&2	J25 2&3	J24 1&2	J13 1&2	
OUT	IN	OUT	IN	2DH ONLY SHORT SUPERVISORY
OUT	IN	IN	IN	29H + 2DH SHORT SUPERVISORY AND NON - PRIVILEGED ACCESS
IN	OUT	OUT	OUT	3DH STANDARD SUPERVISORY - ACCESS
IN	OUT	IN	OUT	39H + 3DH STANDARD SUPERVISORY DATA ACCESS AND STANDARD NON - PRIVILEGED DATA ACCESS

J26 BASE ADDRESS DECODE

OPEN=0 CLOSED=1

A23 A16	BASE ADDRESS
00000000	00000000H
00000001	00010000H
00000010	00020000H
00000011	00030000H
00000100	00040000H
•	•
•	•
•	•
11111011	00FB0000H
11111100	00FC0000H
11111101	00FD0000H
11111110	00FE0000H
11111111	00FF0000H

J2,J4,J5,J7 ENABLE OR DISABLE DIGITAL I/O OUTPUTS*

PORTS	OUTPUT ENABLE	OUTPUT DISABLE
PORT N+0	J5 (IN)	J5 (OUT)
PORT N+1	J2 (IN)	J2 (OUT)
PORT N+2	J7 (IN)	J7 (OUT)
PORT N+3	J4 (IN)	J4 (OUT)

*THESE JUMPERS ARE SHORTED ON THE SOLDER SIDE OF P.C.B.

LIVE END POINTS OF SPAN CONFIGURATION

DESIRED SPAN CONFIGURATION	CONNECT PINS OF J17	CONNECT PINS OF J19
NON-LIVE END POINT	1 AND 2	NONE
LIVE END POINT UNIPOLAR	1 AND 2	1 AND 2
LIVE END POINT BIPOLAR	NONE	NONE

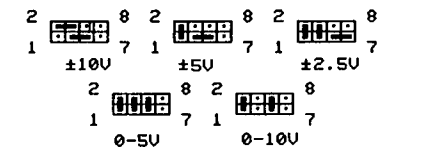
J10 ANALOG INPUT DATA FORMAT

DATA FORMAT	ANALOG INPUT RANGE	CONNECT PINS OF J10
USB	UNIPOLAR	2 AND 3
BOB	BIPOLAR	2 AND 3
BTC	BIPOLAR	1 AND 2

J9(J27) ANALOG OUTPUT DATA FORMAT

DESIRED DATA FORMAT	ANALOG OUTPUT RANGE	CONNECT PINS OF J9 (J27)
USB	UNIPOLAR	1 AND 2
BOB	BIPOLAR	1 AND 2
BTC	BIPOLAR	2 AND 3

J14 OR J15 ANALOG OUTPUT VOLTAGE RANGE SELECTION



J18,J20,J21 ANALOG INPUT RANGES

CONFIGURATION (AT GAIN = X1)	CONNECT PINS OF J18	CONNECT PINS OF J20	CONNECT PINS OF J21
±10V BIPOLAR	1 AND 2	NONE	1 AND 2
0 TO 10V UNIPOLAR	NONE	1 AND 2	2 AND 3
±5V BIPOLAR	1 AND 2	NONE	2 AND 3

J6,J16 ANALOG INPUT TYPE

CONFIGURATION	CONNECT PINS OF J16	CONNECT PINS OF J6	CHANNEL ADDRESS
16 CHANNEL DIFFERENTIAL	2 AND 3	NONE	0 THRU 15
32 CHANNEL SINGLE-ENDED	1 AND 2, 3 AND 4	1 AND 2	0 THRU 31

AcroMag® MIXOR, PACIFIC

5 JAN 94	B	94A004	TAV	JGV	BC	
31 JAN 94	A	9006	TAV	BP	TH	
18 AUG 88	-	——	SJK	DW	—	
DATE	REV	ECO	DR	ENG	ELP	

TITLE: MULTI-FUNCTION JUMPER CONFIGURATION

SIZE	SERIES	SHEET	DRAWING	REV
D	935X-I/ 9450-I/9510-X	1 OF 1	4500-957	B

2.4 VMEbus CONFIGURATION

2.4.1 Address Decode Jumper Configuration

The board interfaces with the VMEbus as a 1K block of address locations in the VMEbus Short I/O Address Space or Standard Address Space. J23 and J26 decode the fourteen most significant address lines A10 through A23 to provide segments of 1K address space. The configuration of the jumpers for different base address locations are shown below. ("In" means that the pins are shorted together with a shorting clip. "Out" indicates that the clip has been removed.) J23 decodes Address lines A10 through A15 and J26 decodes Address lines A16 through A23. Therefore when configured for the Short I/O Address space, only J23 needs to be configured.

Pins of J23						
Base Address	A15 11 & 12	A14 9 & 10	A13 7 & 8	A12 5 & 6	A11 3 & 4	A10 1 & 2
00000000H	out	out	out	out	out	out
00000400H	out	out	out	out	out	in
00000800H	out	out	out	out	in	out
00000C00H	out	out	out	out	in	in
00001000H	out	out	out	in	out	out
.	.	.	.	.	.	.
.	.	.	.	.	.	.
0000EC00H	in	in	in	out	in	in
0000F000H	in	in	in	in	out	out
0000F400H	in	in	in	in	out	in
0000F800H	in	in	in	in	in	out
0000FC00H	in	in	in	in	in	in

Pins of J26								
Base Address	A23 15 & 16	A22 13 & 14	A21 11 & 12	A20 9 & 10	A19 7 & 8	A18 5 & 6	A17 3 & 4	A16 1 & 2
00000000	out	out	out	out	out	out	out	out
00010000	out	out	out	out	out	out	out	in
00020000	out	out	out	out	out	out	in	out
00030000	out	out	out	out	out	out	in	in
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
00FC0000	in	in	in	in	in	in	out	out
00FD0000	in	in	in	in	in	in	out	in
00FE0000	in	in	in	in	in	in	in	out
00FF0000	in	in	in	in	in	in	in	in

2.4.2 Address Modifier Jumper Configuration

The VMEbus Address Modifier jumper, J25, J24 and J13 permits the board to respond to the various Address Modifier Codes.

Pins of J25, J24, J13				
J25 1&2	J25 2&3	J24 1&2	J13 1&2	
OUT	IN	OUT	IN	2DH Only Short Supervisory
OUT	IN	IN	IN	29H + 2DH Short Supervisory and Non-privileged Access
IN	OUT	OUT	OUT	3DH Standard Supervisory - Data Access
IN	OUT	IN	OUT	39H + 3DH Standard Supervisory Data Access and Standard Non-privileged Data Access

2.4.3 Interrupt Level Select Jumper Configuration (w/Analog Inputs Only)

The Interrupt Level is selected by configuring Jumper J11 as follows:

	Pins of J11		
Interrupt Level	5 and 6	3 and 4	1 and 2
None	out	out	out
1	out	out	in
2	out	in	out
3	out	in	in
4	in	out	out
5	in	out	in
6	in	in	out
7	in	in	in

Note: "In" means that the pins are shorted together with a shorting clip.
"Out" indicates that the clip has been removed.

2.5 ANALOG INPUT CONFIGURATION (935X-I & 9510-X)

2.5.1 Analog Input Type Jumper Configuration

The board can accept either 16 channels of differential input or 32 channels of single-ended input. The selection is made by configuring J6 and J16 as follows (see Figure 2.2):

Configuration	Connect Pins of J16	Connect Pins of J6	Channel Address
16 Channel Differential	2 and 3	None	0 thru 15
32 Channel Single-Ended	1 and 2, 3 and 4	1 and 2	0 thru 31

2.5.2 Analog Input Ranges Jumper Configuration

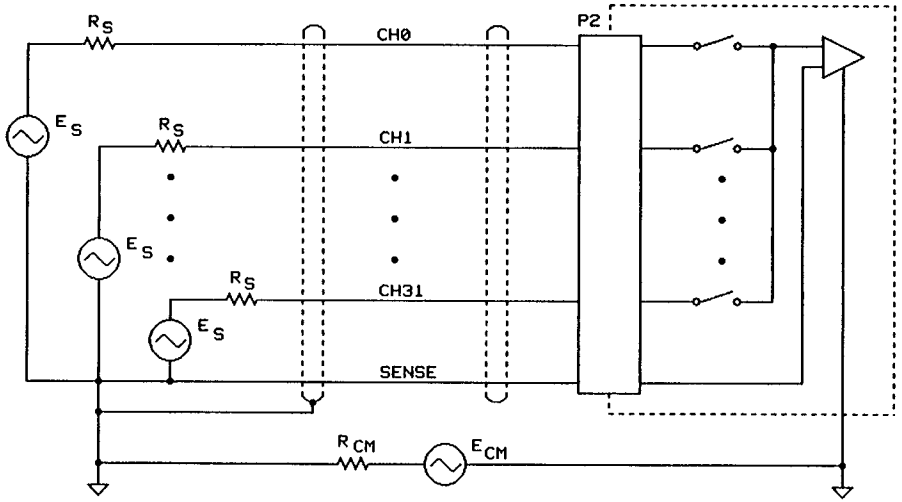
The Analog Input ranges may be selected through J18, J20 and J21. The basic Analog Input Ranges are ±10V Bipolar, ±5V Bipolar and 0V to +10V Unipolar. Other ranges may be obtained by changing the Software Programmable Gain (See Board Control Register Description, Section 3.1.4) from X1 to X2, X4, or X8. Input ranges may be selected as follows:

Configuration (at Gain = x1)	Connect Pins of J18	Connect Pins of J20	Connect Pins of J21
+/-10V Bipolar	1 and 2	None	1 and 2
0 to +10V Unipolar	None	1 and 2	2 and 3
+/-5V Bipolar	1 and 2	None	2 and 3

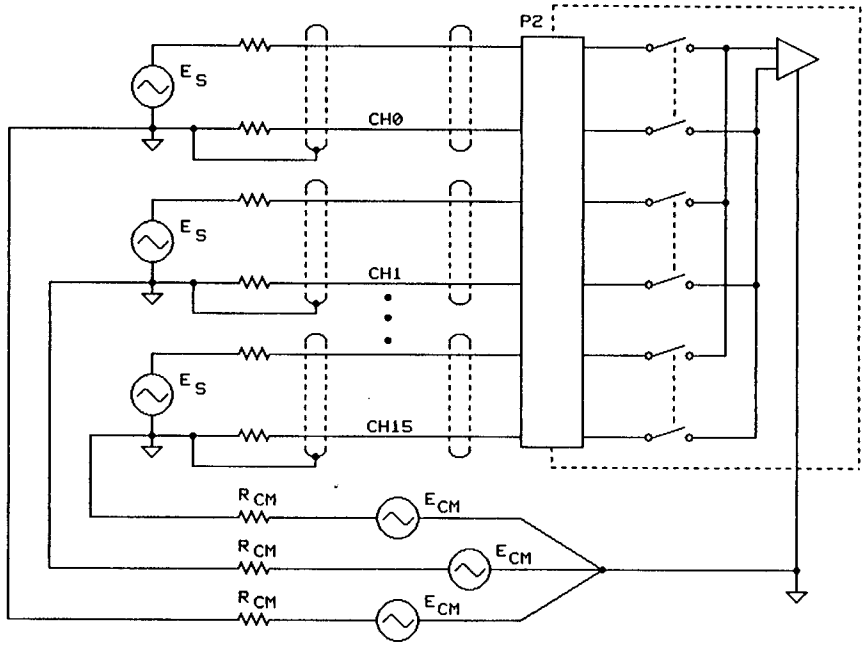
Note: When changing from Bipolar to Unipolar and vice versa it will be necessary to recalibrate the gain. See Service Information in Chapter 5 for details.

Available input ranges:

Software Programmable Gain	Hardware Configurable Ranges		
X1	+/- 10V	+/- 5V	0-10V
X2	+/- 5V	+/- 2.5V	0-5V
X4	+/- 2.5V	+/- 1.25V	0-2.5V
X8	+/- 1.25V	+/- 0.625V	0-1.25V



SINGLE ENDED VOLTAGE INPUT CONNECTION DIAGRAM



DIFFERENTIAL VOLTAGE INPUT CONNECTION DIAGRAM

ANALOG INPUT FIELD CONFIGURATION

AcroMag® WIXOM, MICH.							
31 JAN 91	A	9806	TAV	BP	TH		
8 DEC 88	–	———	TAV	DW	—		
DATE	REV	EO	DR	ENG	ELP		
TITLE: ANALOG INPUT FIELD CONFIGURATION							
SIZE D DWG	SERIES 935X-I/9510-X	SHEET 1 OF 1	DRAWING 4500-963	REV A			

FIGURE 2.2

2.5.3 Analog Input Data Format Jumper Configuration

The analog input data can appear as Unipolar Straight Binary (USB), Bipolar Offset Binary (BOB), or Bipolar Two's Complement (BTC). The data format is determined by the Analog Input Range (Paragraph 2.5.2) that is chosen and by the configuration of J10.

Desired Data Format	Analog Input Range	Connect Pins of J10
USB	Unipolar	2 and 3
BOB	Bipolar	2 and 3
BTC	Bipolar	1 and 2

Assuming standard calibration, the following tables indicate the relationship between Data Format and actual Analog Input Voltage.

2.5.3.1 Unipolar Straight Binary (USB) Analog Input Data Format

USB is used for the Unipolar 0V to +10V range:

Analog Input Voltage	USB Data
9.9976 V	FFF0H
9.9951 V	FFE0H
.	.
.	.
0.0024 V	0010H
0.0000 V	0000H

2.5.3.2 Bipolar Offset Binary (BOB) and Bipolar Two's Complement (BTC) Analog Input Data Format

BOB and BTC are used for the Bipolar -10V to +10V range:

Analog Input Voltage	BOB Data	BTC Data
+9.9951 V	FFF0H	7FF0H
+9.9902 V	FFE0H	7FE0H
.	.	.
+0.0049 V	8010H	0010H
0.0000 V	8000H	0000H
-0.0049 V	7FF0H	FFF0H
.	.	.
-9.9951 V	0010H	8010H
-10.0000 V	0000H	8000H

2.5.4 Analog Input "Live" End Points Of Span Configuration

It is possible for the user to calibrate for "live" end points of the input span. This means that for a given input range, such as -10V to +10V for example, the actual input range will be expanded slightly. Therefore, input voltages of -10V and +10V will actually be within the A/D's input range, instead of at the very ends of the input range. This "live" end point calibration can be useful if the user expects to be converting signals as large as those at the end points of the selected span.

Jumpers J17 and J19 are used to facilitate "live" end point span adjustment for the Bipolar range and "live" end point offset adjustment for the Unipolar range respectively.

Desired Span Configuration	Connect Pins of J17	Connect Pins of J19
Non-Live End Point	1 and 2	None
Live End Point Unipolar	1 and 2	1 and 2
Live End Point Bipolar	None	None

See Paragraph 5.3 for Calibration Procedure.

2.5.4.1 "Live" End Point Range Analog Input for Unipolar Straight Binary Data

Analog Input Voltage	USB Data
10.0769 V	FFF0H
10.0744 V	FFE0H
.	.
.	.
10.0025 V	FE10H
10.0000 V	FE00H
9.9975 V	FDF0H
.	.
.	.
0.0025 V	0210H
0.0000 V	0200H
-0.0025 V	01F0H
.	.
.	.
-0.0769	0010H
-0.0794	0000H

2.5.4.2 "Live" End Point Range for Analog Input Bipolar Offset Binary and Bipolar Two's Complement Data

Analog Input Voltage	BOB Data	BTC Data
10.1538V	FFFOH	7FFOH
10.1488V	FFEOH	7FEOH
.	.	.
.	.	.
.	.	.
10.0050V	FE1OH	7E1OH
10.0000V	FEOOH	7EOOH
9.9950V	FDFOH	7DFOH
.	.	.
.	.	.
.	.	.
0.0050V	801OH	001OH
0.0000V	8000H	0000H
-0.0050V	7FFOH	FFFOH
.	.	.
.	.	.
.	.	.
-9.9950V	021OH	821OH
-10.0000V	0200H	8200H
-10.0050V	01FOH	81FOH
.	.	.
.	.	.
.	.	.
-10.1538V	001OH	801OH
-10.1587V	0000H	8000H

2.5.5 Analog Input Resistor Programmable Gain

It is possible for the gain to be custom programmed through resistors R44 and R42, which are not present on the standard product. The gain at the instrumentation amplifier can be programmed for values of 1 to 1000. Usage of resistor programmable gain may, however, degrade other performance specifications of the Board. See Paragraph 4.5.2.

NOTE: The customer is advised to order modified Boards from Acromag rather than try to install these parts himself. This will avoid the possibility of damaging the Board and voiding the warranty.

2.6 ANALOG OUTPUT CONFIGURATION (9351-I & 9510-X)

2.6.1 Analog Output Range Jumper Configuration

Jumpers J14 and J15 are used to select the output voltage range for Analog Output Channels 0 and 1 respectively.

The available analog output voltage ranges are ±10V, ±5V, ±2.5V, 0 to +5V, and 0 to +10V. The following table shows the jumper connections necessary to select the desired voltage range ("In" means that the pins are shorted together with a shorting clip. "Out" indicates that the clip is not present).

Pins of J14 or J15						Output Voltage Range
1&2	2&4	3&4	3&5	5&6	5&7	
OUT	IN	OUT	IN	OUT	OUT	±10V
IN	OUT	OUT	IN	OUT	OUT	±5V
IN	OUT	IN	OUT	OUT	IN	±2.5V
IN	OUT	IN	OUT	IN	OUT	0 to +5V
IN	OUT	OUT	OUT	IN	OUT	0 to +10V

NOTE: The analog output channels are calibrated for the bipolar ±10V range. Without recalibration, the other ranges may have an offset error of as much as 0.15% and span error of as much as 0.3%. If greater accuracy is desired on a specific range it will be necessary to recalibrate on the particular range.

2.6.2 Analog Output Data Format Jumper Configuration

The analog output data can appear as Unipolar Straight Binary (USB), Bipolar Offset Binary (BOB), or Bipolar Two's Complement (BTC). The data format is determined by the Analog Output Range (Paragraph 2.6.1) that is chosen and by the configuration of J9 and J27 for channels 0 and 1 respectively.

Desired Data Format	Analog Output Range	Connect Pins of J9 or J27
USB	Unipolar	1 and 2
BOB	Bipolar	1 and 2
BTC	Bipolar	2 and 3

The following two tables indicate the relationship between Data Format and actual Analog Output Voltage.

USB - Used for the Unipolar OV to +10V range.

Analog Output Voltage	USB Data
9.9976 V	FFFOH
9.9951 V	FFEOH
.	.
.	.
.	.
0.0024 V	0010H
0.0000 V	0000H*

BOB and BTC - Used for the Bipolar -10V to +10V range

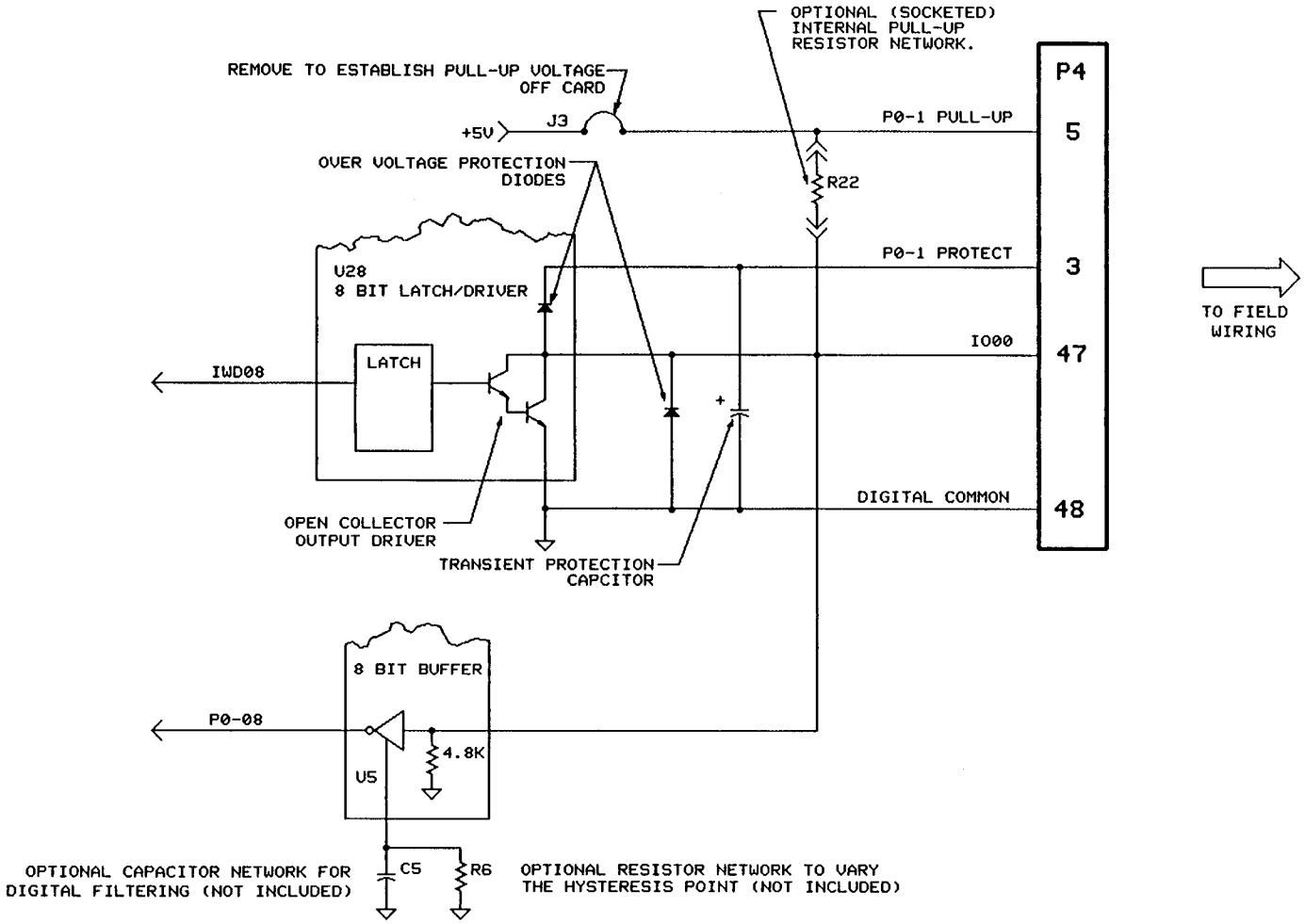
Analog Output Voltage	BOB Data	BTC Data
+9.9951 V	FFFOH	7FFOH
+9.9902 V	FFEOH	7FEOH
.	.	.
.	.	.
.	.	.
+0.0049 V	8010H	0010H
0.0000 V	8000H	0000H*
-0.0049 V	7FFOH	FFFOH
.	.	.
.	.	.
.	.	.
-9.9951 V	0010H	8010H
-10.0000 V	0000H*	8000H

*Reset Condition

2.7 DIGITAL I/O CONFIGURATION (9450-I & 9510-X)

The Digital Inputs and Outputs are configurable to interface to many different types of devices, such as relays, contact closures, indicators, and switches. Some features such as adjustable hysteresis levels and input noise filtering makes the digital outputs adaptable to most applications. See Figure 2.3 for simplified schematic of a digital I/O point.

SIMPLIFIED DIGITAL I/O POINT SCHEMATIC



AcroMag® WIXOM, MICH.	31 JAN 91	A	9806	TAV	BP	TH
	5 DEC 98	—	—	SK	DW	—
	DATE	REV	ECO	DR	ENG	CLP

TITLE: SIMPLIFIED I/O SCHEMATIC

SIZE	SERIES	SHEET	DRAWING	REV
D (24x36)	9450-I/9510-X	1 OF 1	4500-960	A

FIGURE 2.3

2.7.1 Digital I/O Input Filtering

The digital input receivers are equipped with input bandwidth control. By limiting the input bandwidth, false data readings caused by such things as switch contact "bounce", EMI interference, and ground loop distortion can be greatly reduced or eliminated. The bandwidth limiting is implemented by octal capacitor networks C5, C2, C7 and C4 which filter ports 0, 1, 2, and 3 respectively. Filtering must be added in groups of 8 points because of the use of octal capacitor networks.

It should be noted that when trying to write, then read back an output immediately, the receiver may not respond to a change in output level as fast as it is read back. Therefore, false readings could occur and consideration should be given to delaying a read back more than the minimum pulse width of the receiver (see Section 2.7.3). Consult factory for installation information.

SPRAGUE PART NUMBER	CAPACITANCE uF	PULSE WIDTH**
--	No Cap	Approx. 220ns
470C8Y5U103M5ET	0.01	3.2uS
470C8Y5U153M5ET	0.015	4.4uS
470C8Y5U223M5ET	0.022	6.0uS
470C8Y5U333M5ET	0.033	8.7uS
470C8Y5U473M5ET	0.047	12uS
470C8Y5U683M5ET	0.068	17uS
470C8Y5U104M5ET	0.1	24uS
470C8Y5U154M5ET	0.15	28uS
470C8Y5U224M5ET	0.22	33uS

**This is the minimum pulse width that can be read. These values are based on a 5 Volt transient level and a 0 to 5 Volt input range. Higher transient voltages reduce the minimum pulse width and higher capacitance suppresses wider pulse widths.

2.7.2 Digital I/O Adjustable Hysteresis Point

The input receivers have a fixed input hysteresis band of 0.3 Volts. The hysteresis band may be moved within the 0 to 30 Volt input range to change the level at which a logic 1 or logic 0 is read. Increasing the voltage of the input thresholds may be used to reject errors due to low voltage transients at the inputs. This is accomplished by installing resistor networks R6, R1, R7, R3 for ports 0, 1, 2, 3 respectively. The resistance value determines the input threshold voltage. The units are shipped with no resistors installed which aligns the hysteresis band for TTL logic level inputs. Consult factory for installation information.

ACROMAG PART NO.	BOURNS PART NO.	RESISTANCE	POSITIVE THRESHOLD	NEGATIVE THRESHOLD
--	--	No Resistor	1.3V	1.0V
1100-490	4310R-101-102	1000 ohm	3.4V	3.1V
1100-497	4310R-101-561	560 ohm	5.8V	5.5V
1100-498	4310R-101-391	390 ohm	7.8V	7.5V
1100-499	4310R-101-271	270 ohm	10.8V	10.5V
1100-500	4310R-101-221	220 ohm	13.3V	13.0V

2.7.3 Digital I/O Write and Read Back Timing

Each digital I/O point that is configured as an output may be written to and then read back immediately for verification purposes. Timing must be considered before data is read back. There are two sources of delay that must settle before accurate data can be read back.

-Digital Filtering Delay: If the receivers are set up for digital filtering (see Digital I/O Input Filtering), the pulse width delay must be provided before data is read back after a write.

-Field Wiring Delay: The output driver is an open collector transistor and its rise time depends on the pull up impedance and the stray capacitance on the field wiring. The pull up impedance is defined as the total impedance from the output driver to the voltage supply. Stray capacitance is measured from the output driver to ground. Time delay for the field wiring delay can be calculated as follows:

Wait Time = Rpullup * Cstray

(Time required for the output to be 66% of full scale.)

2.7.4 Disabling the Output Drivers

When a Digital I/O Point is configured as an input, the output latch driver should be disabled. The drivers may be software programmably disabled or enabled (see programming information). In the event that a port driver must be hardware disabled (off), a foil is provided on the solder side of the PC Board that may be cut to insure disabled outputs. Cut the foil under the following jumpers to disable the following ports output drivers:

JUMPER	PORT
J5	0
J2	1
J7	2
J4	3

2.7.5 Digital I/O Use With Solid State Relays

The digital I/O area may be used with most industry standard solid state relays. This is most easily accomplished by interfacing to an industry standard PB16A type (or equivalent) termination panel.

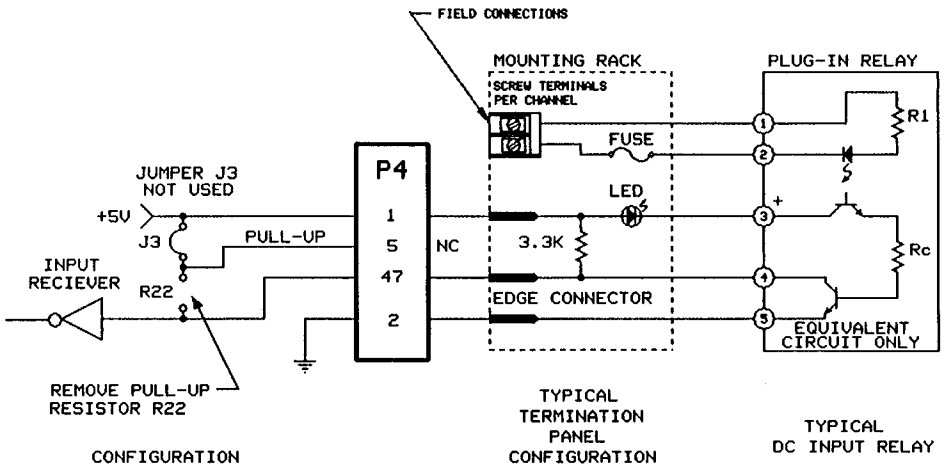
2.7.5.1 Configuring for Solid State Relays

The connectors P4 and P5 are directly compatible with a standard termination panel. The available pull-up line is not used by the relays and therefore J3, J1 and Pull-up resistor networks R2, R4, R22, and R23 may be removed. The inputs and outputs may be programmed on a bit by bit basis.

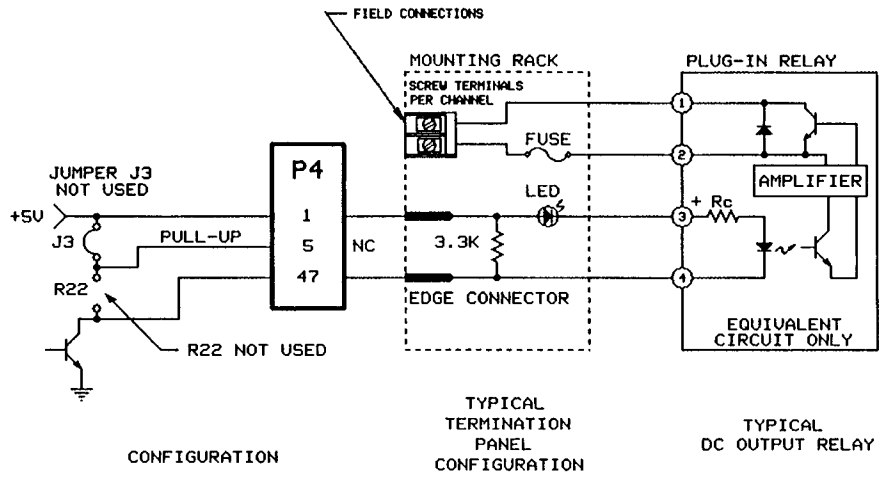
For bit positions corresponding to output modules, writing a Logic 1 will turn the I/O point on and the output latch will sink current. Writing a Logic 0 will turn the module off. For bit positions corresponding to input modules, writing a Logic 1 state indicates the presence of a low voltage for the "on" state of the module. Writing a Logic 0 state indicates a high voltage present.

2.7.5.2 Configuring the PB16A Termination Panel

If the PB16A is to get power from the board, install a jumper at pin 1 or pin 49 on the PB16A termination panel and do not connect power to the terminal block. Install appropriate solid state relay modules. Connect the 50 Pin ribbon cable between PB16A and the board observing the pin 1 index mark.



INPUT CELL CONFIGURATION



OUTPUT CELL CONFIGURATION

TYPICAL SOLID STATE RELAY CONFIGURATION

AcroMag® WIXOM, MICH.	31 JAN 91	A	9806	TAV	BP	TH
	5 DEC 88	–	———	SK	DW	—
	DATE	REV	ECO	DR	ENG	CLP

TITLE: RELAY CONFIGURATION

SIZE	SERIES	SHEET	DRAWING	REV
D PMS	9450-I/9510-X	1 OF 1	4500-962	A

FIGURE 2.4

2.7.6 Digital I/O Use With Other Devices

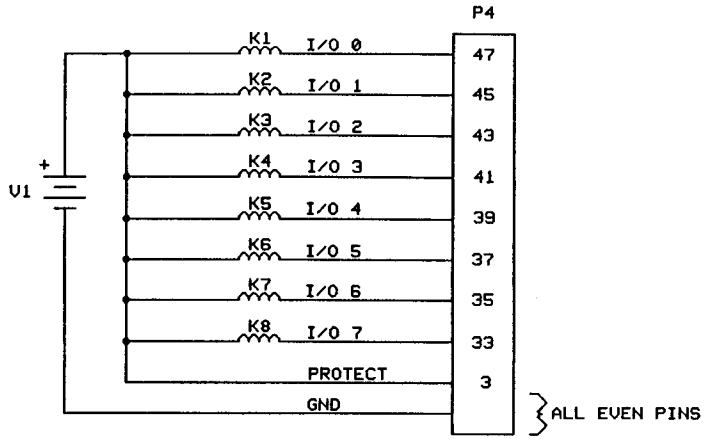
The digital I/O circuitry can interface with a variety of discrete devices such as relays, switches, contact closures, and indicators. Optional termination panel 6980-16U can be used to connect field wiring to the board. The following guidelines should be followed to insure proper interfacing.

2.7.6.1 Relay Coils and Other Inductive Loads

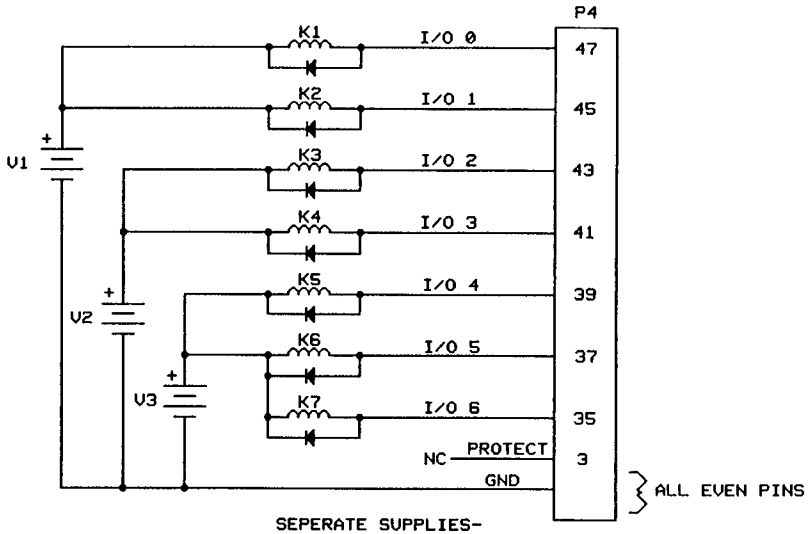
When driving relay coils or other inductive loads, the PROTECT line should be tied to the voltage supply of the loads. This puts a diode across each load to limit the voltage spike generated when an inductive load is switched off quickly. Since each PROTECT line is common to 16 outputs, the supply voltage for all loads must be the same. Otherwise, each load will have to have its own external diode. The pullup resistors should be removed from the digital I/O card also. See Figure 2.5 Relay Driver Configurations, for connection information.

2.7.6.2 Contact Closures and Switches

When sensing contact closures that already are connected to a voltage source, the pullup resistor networks should be removed. The input voltage should be within the range listed in Specifications, Section 6. For isolated or grounded contacts, the pull-ups and the +5 volt supply can be used to establish an input voltage. See Figure 2.6 Contact Closure Configurations for various input configurations.

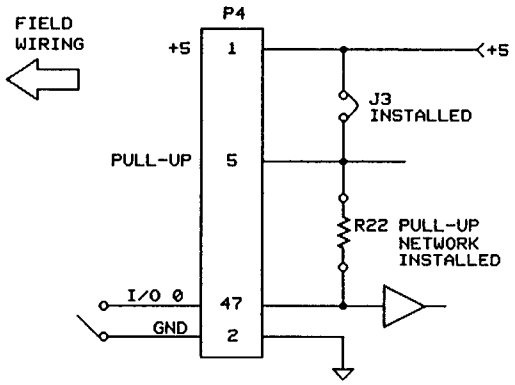


COMMON SUPPLY-
PROTECT LINE TIED TO V1,
PUTS A PROTECTION DIODE
ACROSS EACH RELAY.

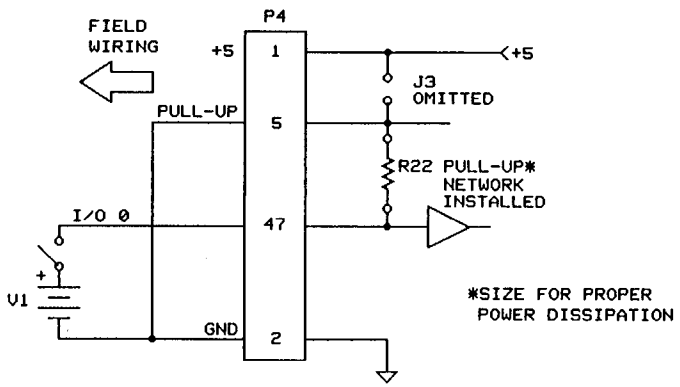


SEPERATE SUPPLIES-
EACH RELAY NEEDS ITS
OWN EXTERNAL DIODE

FIGURE 2.5: RELAY DRIVER CONFIGURATIONS
(SHOWN FOR PORT N + 0)



SIMPLE CONTACT CLOSURE SENSING



CONTACTS SWITCHING A VOLTAGE

FIGURE 2.6: CONTACT CLOSURE CONFIGURATIONS
(SHOWN FOR PORT N + 0, I/O POINT 0)

AcroMag®	5 JAN 94	B	94A001	TAV	JCV	BC
	31 JAN 91	A	9886	TAV	BP	TH
	5 DEC 88	–	———	TV	DW	—
	DATE	REV	ECO	DR	ENG	CLP

TITLE: RELAY DRIVER & CONTACT CLOSURE CONFIGURATION

SIZE	SERIES	SHEET	DRAWING	REV
D	9450-I/9510-X	1 OF 1	4500-961	B

2.7.7 Digital I/O Pull-Up Voltage Jumper Configuration

The digital outputs use open collector latch drivers and may be pulled up to operate at ranges as high as 0 to 30 volts. To configure the output latch for the 0 to +5 volt range internally, the output latch may be pulled up to the "on-board" +5 volt supply via a jumper and an "on-board" 1K ohm pull-up resistor pack. Jumper J3 selects the local +5 volt pull-up for ports 0 to 1, and jumper J1 for ports 2 and 3. One thousand ohm resistor packs R22, R2, R23, R4 pull-up ports 0, 1, 2, 3, respectively. To configure for other output ranges, the jumpers J1 and J3 must be removed along with the pull-up resistor packs (which are socketed) R22, R2, R23, R4. The user must provide externally both the pull-up resistor and the voltage supply.

When Jumper is in place, it pulls the Digital I/O Lines to the on board +5V through socketed 1K ohm resistor pull-up Networks. NOTE: One jumper selects two ports. Short the Jumper to select a pulled-up configuration.

Ports N+0, N+1	J3
Ports N+2, N+3	J1

2.8 CONNECTORS

2.8.1 Analog Input/Output Connector

Analog inputs and outputs are connected to the board via Connector P2. Table 2.1 defines the assignment. These connections can be easily accommodated through the use of Acromag Termination Panels and Ribbon Cable Assemblies or through the use of a user defined Termination Panel.

TABLE 2.1: P2 CONNECTOR

Single Ended Connection	Differential Connection	Pin	Pin	Differential Connection	Single Ended Connection
#	#	8A	8C	Shield	Shield
Analog Com.	Analog Com.	9A	9C	Analog Com.	Analog Com.
CH30 In	-CH14 In	10A	10C	-CH15 In	CH31 In
CH22 In	+CH14 In	11A	11C	+CH15 In	CH23 In
SENSE		12A	12C		SENSE
CH28 In	-CH12 In	13A	13C	-CH13 In	CH29 In
CH20 In	+CH12 In	14A	14C	+CH13 In	CH21 In
#	#	15A	15C	#	#
CH26 In	-CH10 In	16A	16C	-CH11 In	CH27 In
CH18 In	+CH10 In	17A	17C	+CH11 In	CH19 In
#	#	18A	18C	#	#
CH24 In	-CH8 In	19A	19C	-CH9 In	CH25 In
CH16 In	+CH8 In	20A	20C	+CH9 In	CH17 In
+CH1 Out		21A	21C	-CH1 Out	
CH14 In	-CH6 In	22A	22C	-CH7 In	CH15 In
CH6 In	+CH6 In	23A	23C	+CH7 In	CH7 In
#	#	24A	24C	#	#
CH12 In	-CH4 In	25A	25C	-CH5 In	CH13 In
CH4 In	+CH4 In	26A	26C	+CH5 In	CH5 In
+CH0 Out		27A	27C	-CH0 Out	
CH10 In	-CH2 In	28A	28C	-CH3 In	CH11 In
CH2 In	+CH2 In	29A	29C	+CH3 In	CH3 In
+BIAS	+BIAS	30A	30C	-BIAS	-BIAS
CH8 In	-CH0 In	31A	31C	-CH1 In	CH9 In
CH0 In	+CH0 In	32A	32C	+CH1 In	CH1 In

NOTE: # = No Connection

2.8.2 Digital Input/Output Connector

Digital I/O points are connected to the field wiring in groups of 16 channels via two 50-pin Connectors. Table 2.2 defines the assignment. P4 connects Ports N+0, N+1, and P5 connects N+2, N+3. The connector pin-out is defined such that they will directly interface to industry standard optical relay termination panels via a 50-pin ribbon cable.

TABLE 2.2: P4 (P5) CONNECTOR

CONNECTION P4 (P5)	PIN
Ports 0, 1 Protect (Ports 2,3 Protect)	3
Ports 0, 1 Pull-up (Ports 2,3 Pull-up)	5
Ports 0, Point 7 (Port 2, Point 7)	33
Ports 0, Point 6 (Port 2, Point 6)	35
Ports 0, Point 5 (Port 2, Point 5)	37
Ports 0, Point 4 (Port 2, Point 4)	39
Ports 0, Point 3 (Port 2, Point 3)	41
Ports 0, Point 2 (Port 2, Point 2)	43
Ports 0, Point 1 (Port 2, Point 1)	45
Ports 0, Point 0 (Port 2, Point 0)	47
+5V Supply	1
+5V Supply	49
GND	2
GND	50
Ports 1, Point 7 (Port 3, Point 7)	17
Ports 1, Point 6 (Port 3, Point 6)	19
Ports 1, Point 5 (Port 3, Point 5)	21
Ports 1, Point 4 (Port 3, Point 4)	23
Ports 1, Point 3 (Port 3, Point 3)	25
Ports 1, Point 2 (Port 3, Point 2)	27
Ports 1, Point 1 (Port 3, Point 1)	29
Ports 1, Point 0 (Port 3, Point 0)	31
Circuit Common	All Even Pins

2.8.3 External Trigger Connector

The External Trigger signal is connected to the board through P3, a BNC connector at the front panel.

Analog-to-Digital conversions can be synchronized to external events by using an external trigger source. The external trigger must be a TTL compatible, debounced signal. A conversion is triggered on the falling edge of a normally high signal.

The pulse must be low for a minimum of 100 nanoseconds. The signal must return high for a minimum of 100 nanoseconds before going low again. The external trigger signal should normally be in the high state and should be returned to the high state after causing the desired conversions and before changing the Trigger Type or Conversion Timer Enable bits of the board control register.

2.8.4 VMEbus Connections

Table 2.3 indicates pin assignments for the VMEbus signals at the P1 connector. The P1 connector is the upper connector on the board as viewed from the front. The connector consists of 32 rows of three pins labeled A, B, and C. Pin A1 is located at the upper left hand corner of the connector.

2.9 POWER-UP TIMING AND LOADING

The board uses two Logic Cell Arrays to handle the bus interface and control logic timing. Upon power-up, the Logic Cell Arrays automatically clock in configuration vectors from local serial PROMs to initialize the logic circuitry for normal operation. This time is measured as the first 145 mS (typ) after the +5 Volt supply raises to +2.5 Volts at power-up. If a data transfer is attempted during this time, it will simply be ignored and the board will not respond. This should not be a problem because the VME specification requires that the bus master drive the system reset for the first 200 mS after power-up, thus inhibiting any data transfers from taking place.

The Digital I/O output levels are undefined for the first 4.5 mS after the +5 Volt supply raises to +2.5 Volts. This means that any output or input bit may toggle low for this time period. After this time, all bits are reset, configured as inputs and therefore no further loading considerations are necessary. Most power supplies take much longer than this to power up and many circuits may not be at full power during this time.

The Analog Output channels are undefined for the time period when the 5 volt supply is raising between 0V and +2.0V. This means that the output may be at any value during this time. After the power is above 2.0V, all channels properly reset and no considerations are necessary.

TABLE 2.3: P1 BUS CONNECTIONS

PIN NUMBER	MNEMONIC	PIN NUMBER	MNEMONIC	PIN NUMBER	MNEMONIC
1A	D00	1B	BBSY*	1C	D08
2A	D01	2B	BCLR *	2C	D09
3A	D02	3B	ACFAIL*	3C	D10
4A	D03	4B	BGOIN*	4C	D11
5A	D04	5B	BGOOUT*	5C	D12
6A	D05	6B	BG1IN*	6C	D13
7A	D06	7B	BG1OUT*	7C	D14
8A	D07	8B	BG2IN*	8C	D15
9A	GND	9B	BG2OUT*	9C	GND
10A	SYSCLK	10B	BG3IN*	10C	SYSFAIL*
11A	GND	11B	BG3OUT*	11C	BERR*
12A	DS1*	12B	BRO*	12C	SYSRESET*
13A	DSO*	13B	BR1*	13C	LWORD*
14A	WRITE*	14B	BR2*	14C	AM5
15A	GND	15B	BR3*	15C	A23
16A	DTACK*	16B	AMO	16C	A22
17A	GND	17B	AM1	17C	A21
18A	AS*	18B	AM2	18C	A20
19A	GND	19B	AM3	19C	A19
20A	IACK*	20B	GND	20C	A18
21A	IACKIN*	21B	SERCLK (#)	21C	A17
22A	IACKOUT*	22B	SERDAT*(#)	22C	A16
23A	AM4	23B	GND	23C	A15
24A	A07	24B	IRQ7*	24C	A14
25A	A06	25B	IRQ6*	25C	A13
26A	A05	26B	IRQ5*	26C	A12
27A	A04	27B	IRQ4*	27C	A11
28A	A03	28B	IRQ3*	28C	A10
29A	A02	29B	IRQ2*	29C	A09
30A	A01	30B	IRQ1*	30C	A08
31A	-12V	31B	+5V STDBY	31C	+12V
32A	+5V	32B	+5V	32C	+5V

* Indicates that the signal is active low.
\# Indicates no connection.

Refer to the VMEbus specification for additional information on the VMEbus signals.

2.10 DATA TRANSFER TIMING

The board uses optical couplers to transmit digital information across the local on-board isolation barrier. On a VMEbus data transfer to a register across the local isolation barrier, the 16 bit VME data word is converted into two 8 bit serial data streams, then clocked across the isolation barrier.

Therefore, data transfers across the isolation take longer than data transfers to the non-isolated area. Data transfer time is measured from the falling edge of AS* to the falling edge of DTACK*.

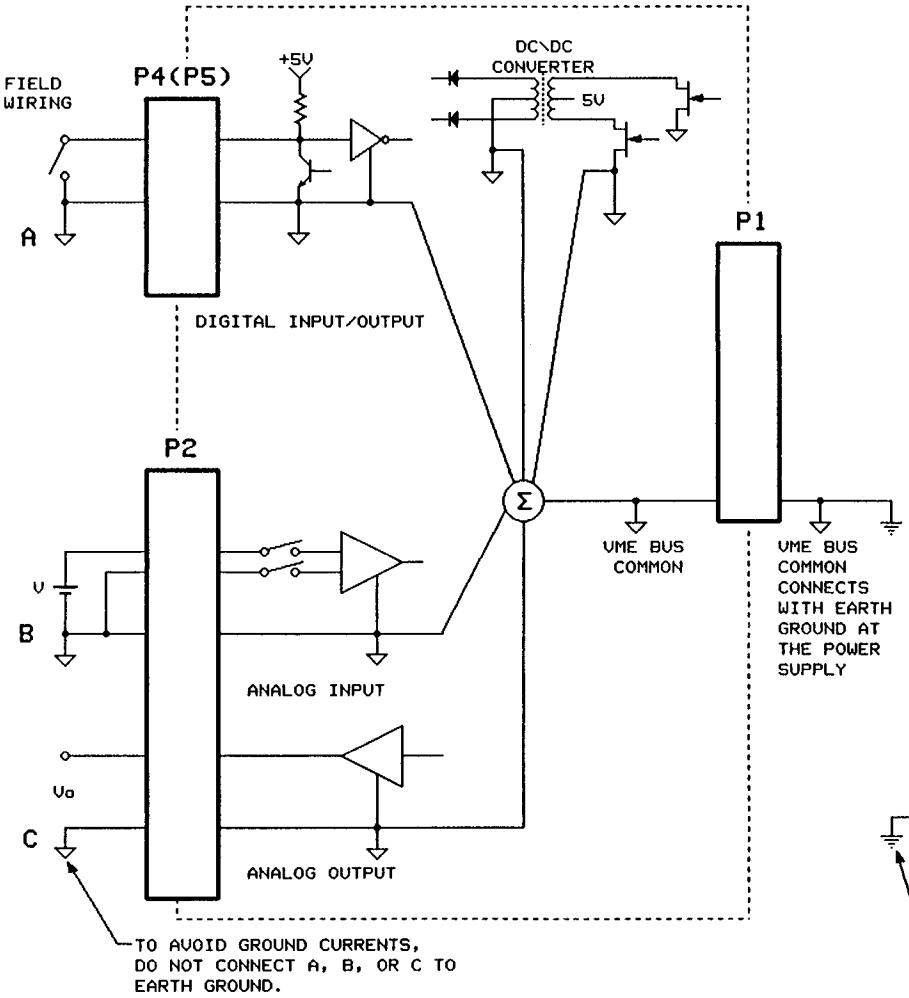
REGISTER	DATA TRANSFER TIME
Analog Input Register	5.8uS
Analog Output Register	5.8uS
Digital I/O Data Registers	5.8uS
All other Registers	940nS

2.11 FIELD GROUNDING CONSIDERATIONS

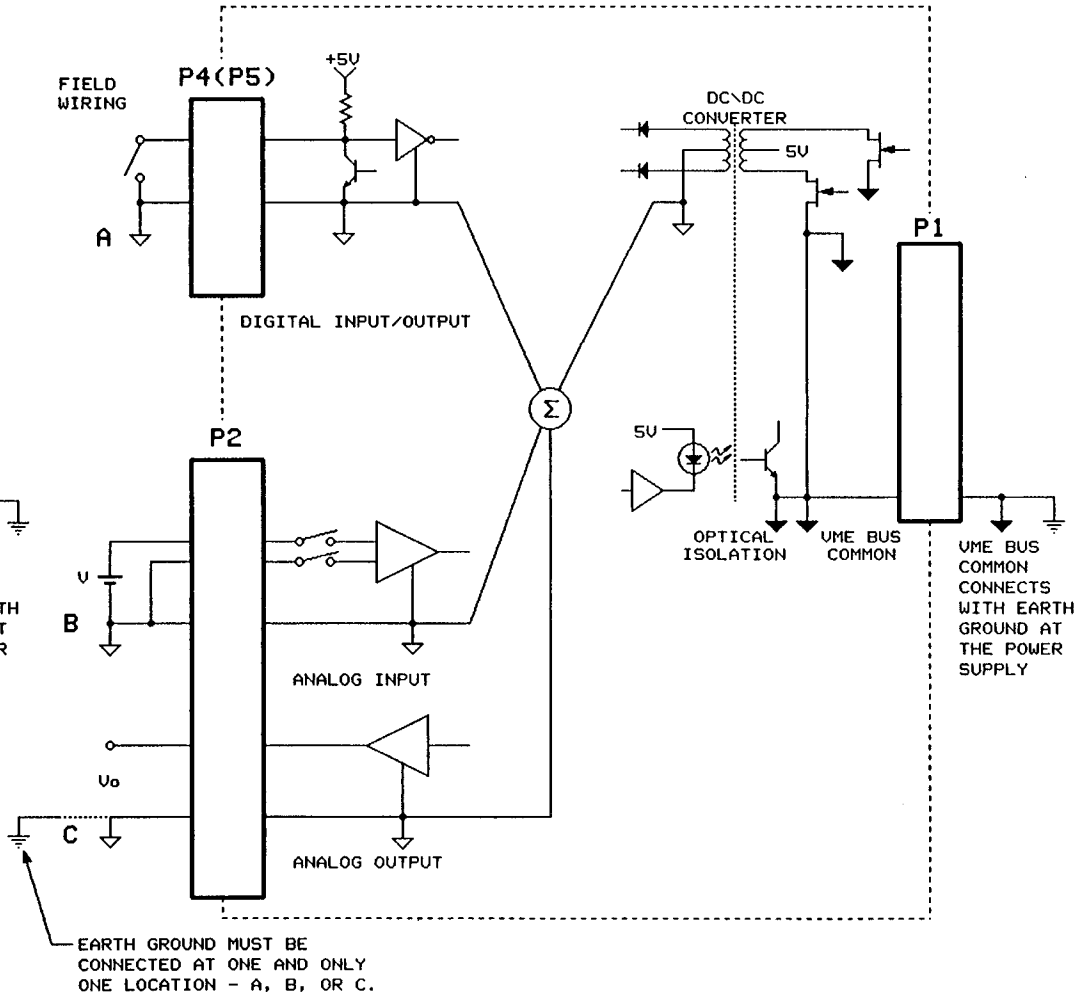
The board has certain field wiring requirements that should be considered to provide trouble-free operation (see Figure 2.7 for a typical setup).

The board is designed to isolate the Digital I/O and the Analog I/O as a group from the VMEbus. This is intended to protect the VMEbus from voltage spikes and transients such as those caused by ground currents and "pick-up". The isolation provides the ability to earth ground the field wiring without the concern of ground currents damaging the card cage. Because the digital I/O and Analog I/O circuits share the same common, only one point should be earth grounded to avoid ground currents through the field circuitry. However, the field circuitry is floating with respect to the earth ground, and one point must be earth grounded to prevent undesirable high voltages on the field wiring.

The AMVE9510 has all of the same functions as the AVME9510-I except that it is not isolated from the VMEbus. It is intended to be used when the ground currents between the field wiring and the VMEbus are low or when sensors are used that isolate the field wiring from earth ground. Special considerations should be given to avoid ground currents to the VMEbus.



AVME 9510 TYPICAL GROUNDING



AVME 9XXX-I TYPICAL GROUNDING

GROUNDING CONSIDERATIONS

AcroMag® WIXOM, MICH.	31 JAN 91	A	9806	TAV	BP	TH
	9 DEC 88	–	——	TAV	DW	——
	DATE	REV	CO	DR	ENG	CLP
TITLE: MULTIFUNCTION GROUNDING CONSIDERATIONS						
SIZE D DWG	SERIES 935X-I/ 9450-I/9510-X	SHEET 1 OF 1	DRAWING 4500-964	REV A		

FIGURE 2.7

3.1 MEMORY MAP

The board is addressable on 1K byte boundaries in the Short I/O Address Space or Standard Address Space (See Paragraph 2.4.1). All Acromag VMEbus non-intelligent slaves have a standard interface configuration which consists of a 32 byte board ID PROM and a Board Status register. The rest of the 1K byte address space contains registers or memory specific to the function of the board. The memory map is shown in Figure 3.1.

3.1.1 Board Identification PROM - (read only) - 01H thru 3FH (odd)

The board contains an identification section. This section of data describes the board model number and the manufacturer. The identification section starts at the board's base address plus 1 and is 32 bytes in length. Bytes are addressed using only the odd addresses between 1 and 63. The PROM contents are shown in Figure 3.2.

3.1.2 Board Status Register - (read/write) - 81H

The Board Status Register reflects and controls functions globally on the board.

MSB 7	6	5	4	3	2	1	LSB 0
<--- Reserved --->			Software Reset	Global Int. Enable	Global Int. Pending	Green LED	Red LED

Where:

Bits 7,6,5: Reserved for future use - equal "0" if read.

Bit 4: Software Reset (W) - writing a "1" to this bit causes a software reset. Writing "0" or reading the bit has no effect. The effect of a software reset on the various registers is described in the explanation of each register.

Reset Condition: Set to "0".

Bit 3: Global Interrupt Enable (R/W) - writing a "1" to this bit enables interrupts to occur from the board. A "0" prevents interrupts. Note that interrupt capability exists only on boards with analog inputs.

Reset Condition: Set to "0", interrupts disabled.

Bit 2: Global Interrupt Pending (R) - this bit will be a "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Note that interrupt capability exists only on boards with analog inputs.

Reset condition: Set to "0".

Bit 1: Green LED (R/W) - this bit when written will control the state of the green LED on the front panel. A "1" will turn it on, a "0" will turn it off. Reading it will reflect its current state.

Reset Condition: Set to "0", LED off.

Bit 0: Red LED (R/W) - this bit when written will control the state of the red LED on the front panel and the state of the VMEbus SYSFAIL* signal. A "1" will turn the LED off and set SYSFAIL* high, a "0" will turn the LED on and set SYSFAIL* low. Reading it will reflect its current state. (See Section 5.2 for additional information on using SYSFAIL*.)

Reset Condition: Set to "0", LED lit, and SYSFAIL* is set low.

3.1.2.1 Status Bits Usage

The status register bits 1 and 0 along with the green and red LEDs provide the user with a means of keeping track of a board's functionality in the system. Since there is no intelligence on the board, the host computer controls these bits. The following paragraphs are possible uses of the bits in the status register and the LEDs on the front panel.

On power-up the bits in the status register reads low, with the green LED off, the red LED lit, and SYSFAIL* low. This indicates that the board has failed or that it hasn't been tested yet.

The Status Register Bit 1 reads low and Bit 0 reads high. The LEDs will both be off and SYSFAIL* is high. This indicates an inactive board.

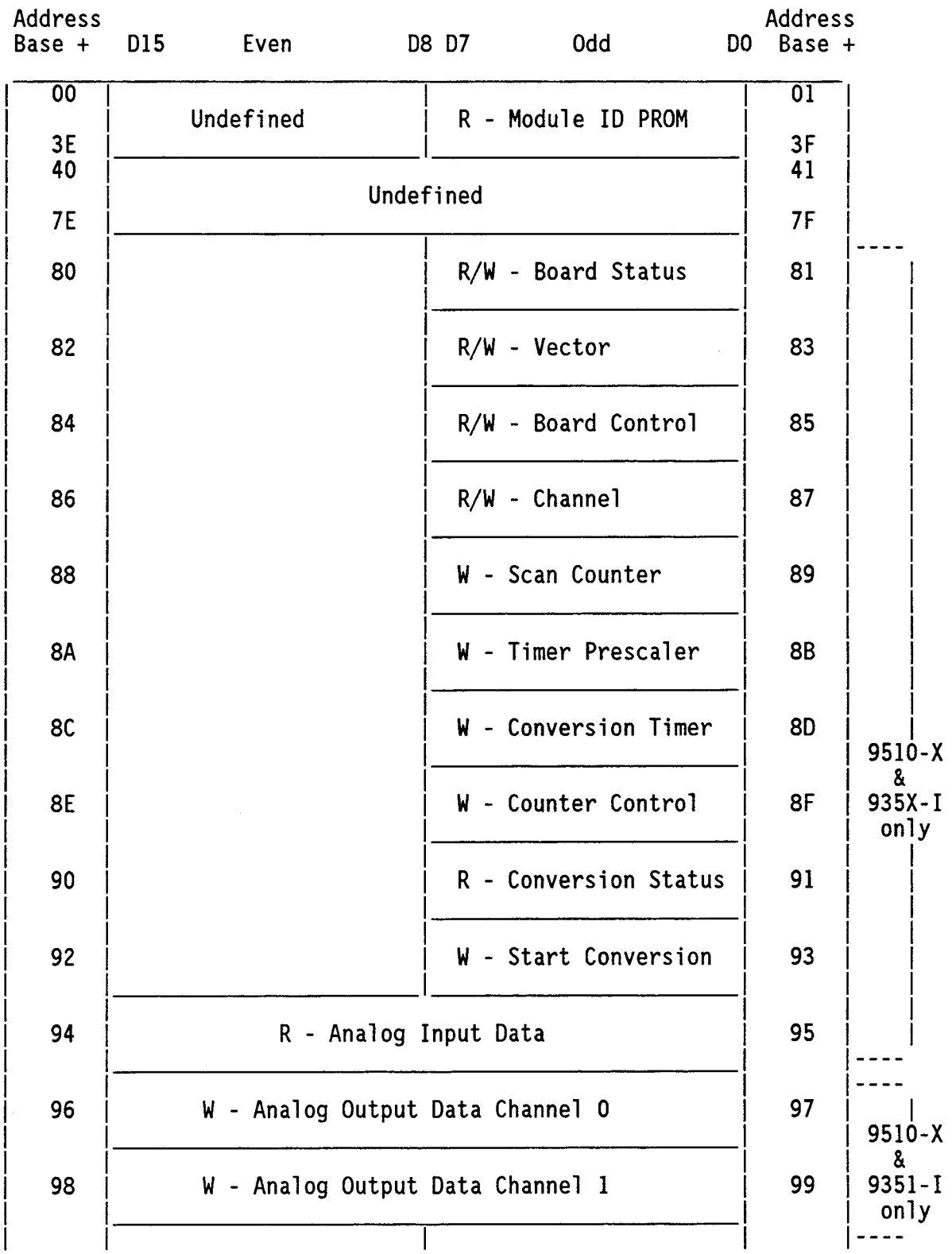
The Status Register Bit 1 reads high and Bit 0 reads low. The LEDs will both be lit and SYSFAIL* is low. This indicates the board is undergoing a diagnostic checkout.

The Status Register Bits 1 and 0 read high. The green LED will be lit with the red LED off and SYSFAIL* is high. This indicates the board is fully functional.

Status Bits Possible Usage

Bit 0 (Red LED)	Bit 1 (Green LED)	SYSFAIL*	Description
0, (on)	0, (off)	Low	Failed or reset condition
1, (off)	0, (off)	High	Inactive board
0, (on)	1, (on)	Low	Diagnostics are running
1, (off)	1, (on)	High	Normal operation

Figure 3.1: Board Memory Map



Board Memory Map - Continued

9A	R/W - Digital I/O Port N + 0	R/W - Digital I/O Port N + 1	9B	9510-X & 9450-I only
9C	R/W - Digital I/O Port N + 2	R/W - Digital I/O Port N + 3	9D	
3EF	Undefined		3FF	

Figure 3.2: Board Identification Prom

Offset From Board Base Address	Value ASCII Character	Value Numeric	Descriptions
01H	V	56H	Always VMEID for all boards
03H	M	4DH	
05H	E	45H	
07H	I	49H	
09H	D	44H	
0BH	A	41H	Manufacturers I. D., ACR for ACROMAG
0DH	C	43H	
0FH	R	52H	
11H	9	39H	Board Model Number (4 characters and 3 trailing blanks)*
13H	5	35H	
15H	1	31H	
17H	0	30H	
19H		20H	
1BH		20H	
1DH		20H	
1FH	1	31H	Number of KILOBYTES of address space used.
21H		20H	
23H	Undefined		Reserved
25H	Undefined		
27H	Undefined		
29H	Undefined		
2BH	Undefined		
2DH	Undefined		
2FH	Undefined		
31H	Undefined		
33H	Undefined		
35H	Undefined		
37H	Undefined		
39H	Undefined		
3BH	Undefined		
3DH	Undefined		
3FH	Undefined		

(*The model 9XXX-I would have six characters and one trailing blank.)

3.1.3 Vector Register - (read/write) - 83H

The Vector Register maintains the 8 bit interrupt vector number which is provided to the VMEbus Interrupt Handler when an interrupt is being serviced. The register content is undefined upon reset. Note that interrupt capability exists only on boards with analog inputs.

3.1.4 Board Control Register - (read/write) - 85H

The Control Register contains bits which are used to control how the analog inputs function.

7	6	5	4	3	2	1	0
<--Reserved-->		CNTEN	Trigger Type	MSB Mode	LSB Mode	MSB Gain	LSB Gain

Where:

Bits 7 and 6: Reserved - read as "0".

Bit 5: CNTEN - Conversion Timer Enable. A "0" disables the timer. Writing a "1" to this bit enables the conversion timer circuit. This Conversion Timer must be completely set up before enabling it through this bit. See Paragraph 3.3.3.

Bit 4: Trigger Type - A "0" selects "on Board" triggering via the start Conversion Register or the Conversion Timer circuit. A "1" selects external triggering.

Bits 3 and 2: Mode - these bits select the mode in which the board will operate. See Paragraph 3.2 for a detailed discussion of operating modes. The modes are selected as follows:

Bit 3	Bit 2	Mode
0	0	Channel
0	1	Scan
1	0	Resv'd
1	1	Resv'd

Bits 1 and 0: Gain - these bits select the gain at which the currently selected analog input channel will be read. The gains are selected as follows:

Bit 1	Bit 0	Gain
0	0	X1
0	1	X2
1	0	X4
1	1	X8

Reset condition: All bits set to "0" (gain = X1).

3.1.5 Channel Register - (read/write) - 87H

The Channel Register is used to select the analog input channel to be converted. The contents are undefined upon power-up.

7	6	5	4	3	2	1	0
0	0	0	MSB				LSB
			<-------- Channel Number -------->				

Reset condition: The register content is not affected by reset.

3.1.6 Counter Control Register - (write only) - 8FH

The Counter Control Register is used to set up the on board counter device for counting in the Scan Mode and for measuring time when timed periodic conversions are desired. A write to the counter control register should be followed by a write to the scan counter, timer prescaler, or conversion timer registers.

7	6	5	4	3	2	1	0
<---------- Counter Control Codes ---------->							

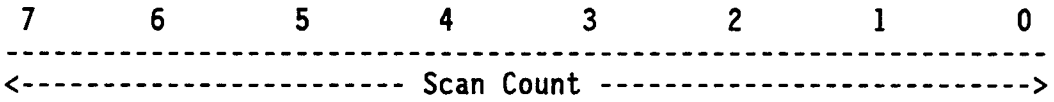
Three Counter Control Codes may be written into this register:

CODE	FUNCTION
14H	Sets up the "on Board" counter device to receive the one BYTE value of the number of channels to be scanned in the Scan Counter Register (89H).
54H	Sets up the "on Board" counter device to receive the one BYTE prescaler count in the Timer Prescaler Register (8BH).
B4H	Sets up the "on Board" counter device to receive the two BYTE timer count in the Conversion Timer Register (8DH). (Least significant Byte, then the most significant Byte.)

See Paragraph 3.3.3 for a detailed discussion on timed periodic conversions. See Paragraph 3.2.2 for a discussion of the Scan Mode. The register content is undefined upon reset.

3.1.7 Scan Counter Register - (write only) - 89H

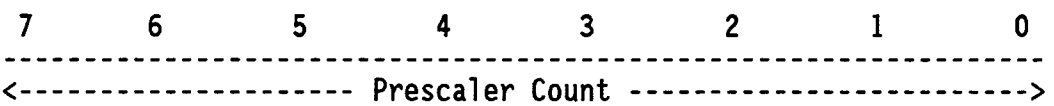
The Scan Counter Register is used to hold the one BYTE count of the number of channels in the scan.



For example, if channels 2, 3, 4 and 5 are to be in the scan, then the number 4 should be written into the Scan Counter Register and the first channel number 2 should be written into the Channel register. The Counter Control Register must be used to set up the counter device. The register content is undefined upon reset. If the board is set up for sixteen Differential channels and channels E, F, 0, 1, and 2 are to be in the scan, write an E to the Channel Register and write the number "five" to the Scan Counter Register.

3.1.8 Timer Prescaler Register - (write only) - 8BH

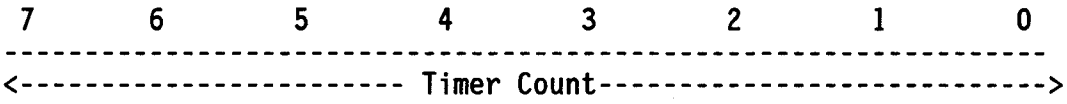
The Timer Prescaler Register is used to hold the Prescaler Count.



This 8-bit number divides a 2 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register and the resulting frequency is used to generate periodic triggers for precisely timed intervals between conversions. The register content is undefined upon reset.

3.1.9 Conversion Timer Register - (write only) - 8DH

The Conversion Timer Register is used to hold the Timer Count.



This number is the second divisor of a 2 MHz clock signal and is used together with the Timer Prescaler Register (Paragraph 3.1.8) to derive the frequency of periodic triggers for precisely timed intervals between conversions. The Timer Count is a 16 Bit number entered by consecutively writing the least significant byte and then the most significant byte. The register content is undefined upon reset.

3.1.10 Conversion Status Register - (read only) - 91H

This register reflects the status of A/D conversions.

7	6	5	4	3	2	1	0
EOCF	STRD	CREQ	MTI	0	0	0	0

Where:

Bit 7: End of Conversion Flag (EOCF): This bit is set to a "1" when a conversion sequence is completed. The bit is set to "0" when the Data Register is read.

Bit 6: Conversion Started (STRD): Set to a "1" when the A/D starts to digitize the analog input signal. At this point, since the sample and hold circuit is in the hold mode, the data in the Channel Select and Control Registers can be changed without affecting the conversion data. Reset to a "0" when the Data Register is read.

Bit 5: Conversion Requested (CREQ): Set to a "1" when a conversion sequence is requested provided that the data from the previous conversion has been read. Reset to a "0" when the A/D starts to digitize the analog input signal. The prime use of this signal is for diagnostics.

Bit 4: Missed Trigger Input (MTI): This Bit is set to "1" if a trigger occurs after a conversion has been started and before the digital data for the conversion has been read. The status of this bit can be critical in assuring that the A/D data is valid when there is a possibility of not reading it before another trigger occurs. The bit is reset to "0" when the Data Register is read.

Reset condition: All bits set to "0".

3.1.11 Start Conversion Register - (write only) - 93H

The Start Conversion Register is a write only register and is used to trigger a conversion when software triggering has been selected with Bit 4 of the Control Register.

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

NOTE: "X" means the bit value does not matter.

Reset condition: This Register is not affected by RESET.

3.1.12 Input Data Register - (read only) - 94H, 95H

The Input Data Register Contains the result of the most recent analog to digital conversion. The data is valid only after Bit 7 (EOCF) of the conversion status register goes to a "1" and only until Bit 6 (STRD) of the same register goes to a "1". See Paragraph 2.5.3 for a discussion on analog input data formats.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<---------- Analog Input Data ---------->												0	0	0	0

Reset condition: This register is not affected by RESET.

3.1.13 Output Data Registers 0 and 1 - (write only) - 96H, 97H, and 98H, 99H

These registers are used to control the voltage of the two optional analog output channels. Upon reset, channels set up for USB or BTC Data Formats reset to 0 volts. Channels set up for BOB reset to the most value (for example -10V). See Paragraph 2.6.2 for a discussion on analog output data formats.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<---------- Analog Output Data ---------->												X	X	X	X

NOTE: "X" means the bit value does not matter.

3.1.14 Digital I/O Port Registers - (read/write) - 9AH through 9DH

The I/O Port Registers reflect and/or control the state of the bidirectional I/O points. Points are grouped 8 to a Port. To use a point as an input, write a 0 to it first to cause the output driver to go into an off (hi-z) state. To use a point as an output, write the desired "1" or "0" to the point. If the point is read, it will reflect the state of the output as well.

Reset Condition: Will read a "0", I/O point off, configured as an input.

Example: Port N+0 (9AH)

7	6	5	4	3	2	1	0
Chan 7	Chan 6	Chan 5	Chan 4	Chan 3	Chan 2	Chan 1	Chan 0
<---------- Port N+0 I/O Channels ---------->							

3.2 MODES OF OPERATION FOR A/D CONVERSION (935X-I & 9510-X)

3.2.1 Channel Mode

The Channel Mode is used when a single channel is to be converted. Usage is:

- OPTIONAL: Interrupt on end of conversion.
  Write the Interrupt Vector number to the Interrupt Vector Register (83H).
  Write to Board Status Register (81H) to enable interrupts.
  Select the interrupt level using hardware jumper J11. At the end of the next A/D conversion, an interrupt request will be issued.

- OPTIONAL: Automatic Timed Periodic conversions after an initial software start or external trigger pulse.

  Write 54H to the Counter Control Register (8FH).

  Write prescale value in Timer Prescaler Register (8BH).

  Write B4H to the Counter Control Register (8FH).

  Write the Low BYTE of the Timer Count into the Conversion Timer Register (8DH).

  Write the High BYTE of the Timer Count into the Conversion Timer Register (8DH).

  Enable the conversion timer by writing a 1 into bit 5 (CTEN) of the board control register (85H).

  After the next external or software trigger, Timed Periodic Conversions will happen automatically.

- Write the correct code to the Control Register (85H) for the Channel Mode and for the desired gain and type of triggering.

- Write the desired channel number to the Channel Register (87H).

- Perform a write operation to the Start Conversion Register (93H) if software triggering has been selected or wait for an external or timed trigger.

- Poll the Conversion Status Register (91H) until the conversion is complete or wait for an interrupt if interrupts have been enabled.

- Read data from the data register (94H). Reading the data will also clear the interrupt if it has been enabled.

NOTE: The same channel may be converted by repeated triggering without need of writing to the Channel or Control Registers.

3.2.2 Scan Mode

The Scan Mode is used when a series of consecutive channels are to be scanned. Usage is almost the same as for Channel Mode except that the Counter Control Register and the Scan Counter Register must be used to configure the on board counter device and to hold the count of the number of channels to be scanned respectively. The following steps must be performed:

- Write 14H to the Counter Control Register (8FH).
- Write the value of the number of consecutive channels to be scanned into the Scan Counter Register (89H).
- Write 0 and 1 into bits 3 and 2 respectively of the Board Control Register (85H) to select the scan mode of operation.
- Write the initial channel into the Channel Register (87H).

After the beginning of each conversion, the Channel Register is incremented automatically by analog input circuitry in anticipation of repeated triggering. In this way sequential channels may be scanned very quickly without the overhead of incrementing the Channel Register through software and having the conversion delayed by the settling time of the analog input circuitry. The settling time delay can be eliminated since it occurs during the conversion time of the previous channel. This is the method which maximum throughput rate may be achieved.

3.3 INITIATING ANALOG-TO-DIGITAL CONVERSIONS (935X-I & 9510-X)

Analog-to-Digital conversions may be initiated or triggered in three different ways. Each way has advantages which will be discussed in the following subsections.

3.3.1 Software Triggering - Register Access

Conversions may be triggered by performing a byte write to the Start Conversion Register after having enabled software triggering via bit 4 of the Board Control Register. The value of the byte written does not matter. This method of starting a conversion is most useful for its simplicity, when the precise time of conversion is not critical. Be aware that writing a byte at a precise point in time may be difficult in a multi-tasking system or in a system with an arbitrated bus.

3.3.2 External Triggering - TTL Input

Conversions may be triggered by an external TTL compatible signal input through BNC connector P3 on the front panel. External triggering is enabled via bit 4 of the Board Control Register. The conversion is initiated on the falling edge of the External Trigger Signal. See Section 2.8.3 for additional specifications for this input. This type of conversion triggering is useful for synchronizing the A/D conversion of analog inputs to external events.

Precise intervals between conversions can be accomplished two ways. In the first method, the user would supply an external timing device and cause external triggers synchronous with external events. This method is most useful when the external event is non-linear with respect to time. The second method uses an initial trigger and then the Multi-function board automatically causes conversions at precise time intervals. This method is described in the following section.

3.3.3 Timed Periodic Triggering

Timed periodic triggering can be used to achieve precise time intervals between conversions. An on board conversion timer device must be configured for the desired time interval. The first trigger must be provided by a Software or External Trigger and thereafter the user must not cause anymore triggers by software or external sources. After the first trigger causes a conversion, subsequent conversions will be caused by the timer. Triggering will continue until the conversion timer is disabled.

The conversion timer is implemented by cascading two counters. The first counter, the prescaler, is clocked by a 2 MHz clock signal. The output of this counter is input to the second counter, the conversion timer, and the output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$T = \frac{(N1)x(N2)}{2}$$

Where:

T = time period between trigger pulses in microseconds.
N1 = prescaler count (8 bit)
N2 = conversion timer count (16 bit)

As can be seen, the maximum period of time which can be programmed to occur between conversions is 8.35 seconds.

$$\frac{(255)x(65535)}{2} = 8.35 \times 10^6 \text{ uS or } 8.35 \text{ S.}$$

The minimum period is not defined by the counters but is defined by the maximum conversion rate of the hardware. Conversions may occur as frequently as once every 32 microseconds. The value written into either counter must not be less than 2.

Following is the required order of steps necessary to set up and activate the Conversion Timer:

1. Write 54H into the Counter Control register.
2. Write the prescaler count (N1) into the Timer Prescaler Register.
3. Write B4H into the Counter Control Register.
4. Write the least significant byte of the timer count (N2) into the Conversion Timer Register.
5. Write the most significant byte of the timer count (N2) into the Conversion Timer Register.
6. Enable the conversion timer by writing a "1" into bit 5 (CNTEN) of the Board Control Register.
7. Start timed periodic conversions with a single Software or External Trigger.

3.4 GENERAL PROGRAMMING CONSIDERATIONS

3.4.1 Board Diagnostics

The board is a non-intelligent slave and does not perform self diagnostics. It does, however, provide a standard interface architecture which includes a Board Status Register useful in system diagnostics. Refer to Paragraph 3.1.2: Board Status Register.

Status bits, control of front panel LEDs, and control of the SYSFAIL* signal are provided through the Board Status Register. Bits 0 and 1 may be used as follows:

Board Status Register bit 1	bit 0	LEDs Green	Red	SYSFAIL* Signal	Condition
0	0	Off	On	On	Board failed test or has not been tested.
1	0	On	On	On	Board is being tested.
1	1	On	Off	Off	Board has passed test.
0	1	Off	Off	Off	Board is inactive.

At power up, the system diagnostic software can test each non-intelligent slave, sequencing the status bits to indicate "undergoing test" and then to "passed" or "failed".

After testing each board, the system software records which boards have failed and sets their status to indicate "inactive". By setting the boards status to inactive, the SYSFAIL* signal is released and may then be useful for an on-line indication of failure by other boards.

Alternatively the system software could simply set the bits and therefore front panel LEDs, to "passed test" as a visual indication that the presence of the board is recognized.

3.4.2 The Analog to Digital Conversion Sequence

Each time a conversion trigger occurs, the conversion control circuitry on the board goes through a sequence of steps to perform the conversion. This conversion sequence is indicated by the state of bits in the Conversion Status Register (See Paragraph 3.1.10).

Note that an A/D conversion will not actually start until there has been adequate front end settling time (approximately 15 microseconds) after writing to the Mode or Channel Registers. Nor will a conversion start until the sample and hold device has had time (approximately 3 microseconds) to re-acquire the input signal after a conversion.

Figure 3.3 shows the timing diagrams of the conversion sequence.

The highest conversion rate for consecutive conversions on the same channel can be realized by reading the data as quickly as possible after the end of conversion and triggering another conversion. The highest conversion rate for converting different channels consecutively requires that immediately after a conversion has been started, the channel register is changed. It is possible to do this because as soon as a conversion starts the sample and hold device goes into the hold mode which keeps the analog input signal constant at the A/D converter. After the end of conversion the data is read and another conversion is started immediately. This method takes advantage of letting the front end settling time for the next channel to be converted take place during the conversion of the present channel.

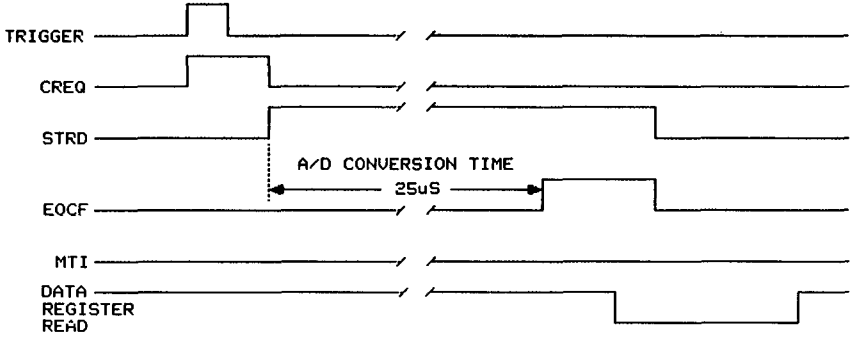
There are three ways to tell when an A/D conversion is complete:

1. Poll the End of Conversion Flag (EOCF) bit in the Conversion Status Register.
2. Set up and enable interrupts.
3. Wait long enough after triggering a conversion to insure that the conversion is complete.

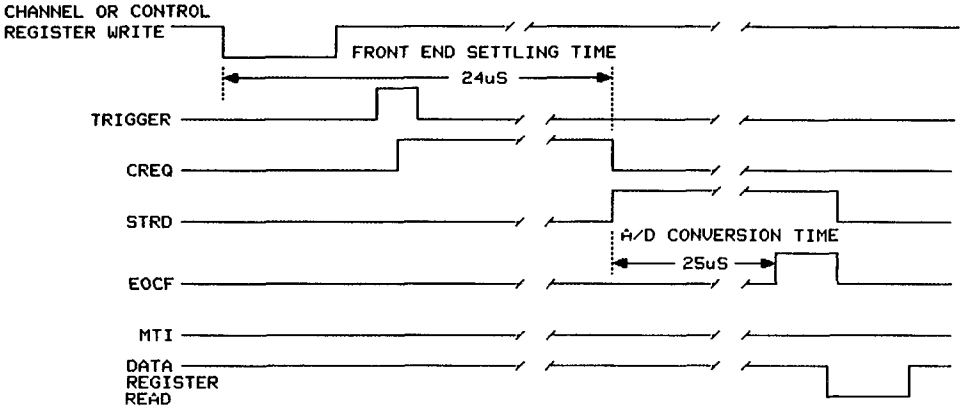
Each method has advantages and disadvantages. Generally it is advisable to somehow be sure that a conversion has completed and the data was read before causing another trigger. In cases where this may be difficult, such as with External or Timed Periodic Triggering, it may be useful to check the Missed Trigger Input (MTI) bit in the Conversion Status Register to be sure that data for the last conversion was read before another conversion was started. Figure 3.4 shows timing diagrams resulting from a missed Trigger.

3.4.3 Treatment of Data

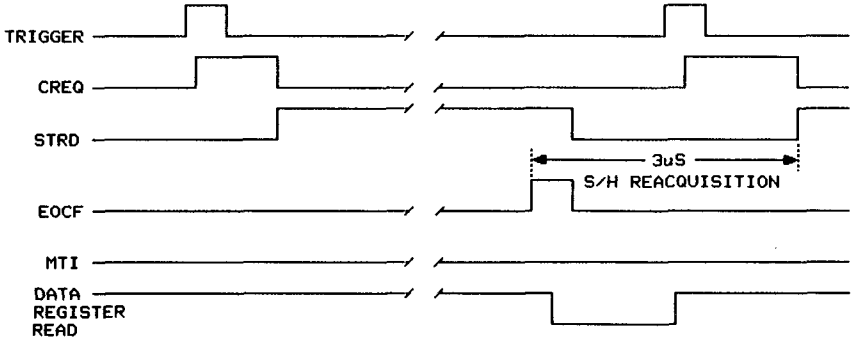
The input and output data is 12 bit left justified. When working with bipolar signals, the user may find it advantageous to treat the data as 16 bit two's complement numbers. In that way future products with higher resolution A/D and D/A converters may use the same software drivers. Similarly, unipolar data may best be treated as 16 bit unsigned numbers.



NORMAL OPERATION



CONVERSION DELAY DUE TO FRONT END SETTLING TIME



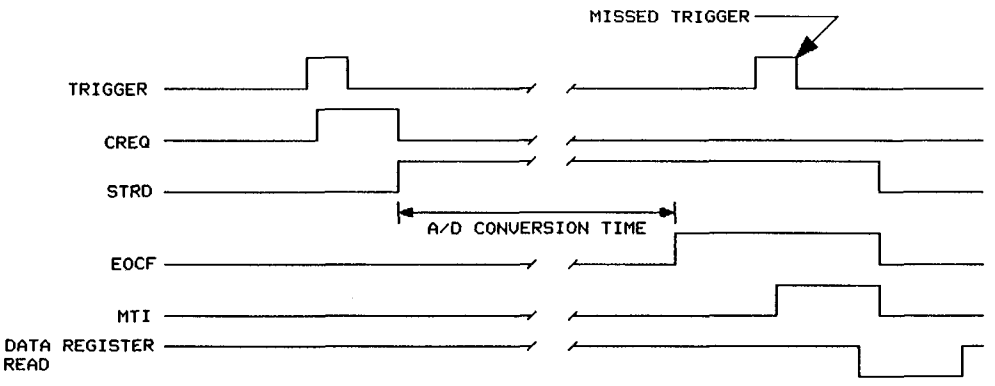
SAMPLE/HOLD REACQUISITION TIME

AcroMag® WIXOM, MICH.	22 SEP 93	B	93J015	TAV	JCV	BC
	31 JAN 91	A	9806	TAV	BP	TH
	14 DEC 88	–	———	TV	DW	—
	DATE	REV	ECO	DR	ENG	CLP

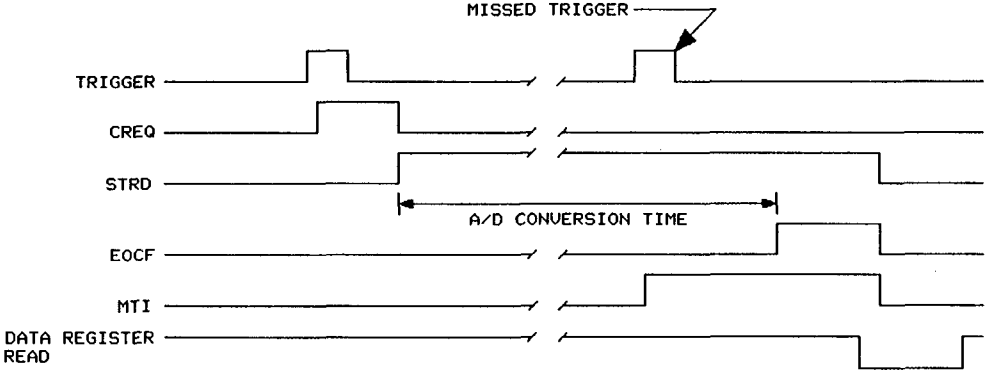
TITLE: CONVERSION TIMING DIAGRAM

SIZE	SERIES	SHEET	DRAWING	REV
D	935X-I/9510-X	1 OF 1	4500-965	B

FIGURE 3.3



MISSED TRIGGER OCCURRING BEFORE READING A/D DATA



MISSED TRIGGER OCCURRING DURING CONVERSION

AcroMag® WIXOM, MICH.	31 JAN 91	A	9806	TAV	BP	TH
	14 DEC 88	-	———	TV	DW	—
	DATE	REV	ECO	DR	ENG	CLP

TITLE: MISSED TRIGGER DIAGRAM

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	935X-I/9510-X	1 OF 1	4500-966	A

FIGURE 3.4

3.4.4 Analog Input Throughput Rate

The analog input total throughput rate depends on the technique used in sampling data. There are a few timing factors that contribute to the calculation of throughput rate and they are:

-A/D Conversion Time (time required for the A/D Converter to process all 12 bits of data) - - 25uS.

-Input Settling Time (time required for input circuitry to settle to 1LSB from a 20 volt step) - - 24uS.

-Reacquisition Time (time required for the Sample and Hold to reacquire the input at the end of conversion) - - 3uS.

-Data Transfer Time (read analog input data) - - 5.8uS.

-EOCF Polling Time (read conversion status register) - - 940nS.

Maximum throughput rate is achieved when the input channel is changed while the A/D converter is converting. This allows the next input to settle while the previous channel is converted, thus allowing us to neglect the settling time in the calculation. The channel scan mode does this automatically.

Also, the reacquisition time automatically times out while the previous channel is being read. It too may be neglected.

A/D Conversion Time	25.00 uS
Read Conversion Status Register	.94 uS
Read Analog Data	5.80 uS
Total Throughput	31.74 uS Max

4.1 INTRODUCTION

This chapter describes the circuitry that is used on the board. A block diagram is shown in Figure 4.1. Schematics and parts lists are shown in Chapter 7.

4.2 VMEbus INTERFACE

The VMEbus interface is composed of three functional circuit areas.

-Data buffers (U77, U78)
-Interrupter (U15, U72, U54)
-Address decode and bus control logic (U73, U74, U54)

4.3 REGISTER LOCATION

Local memory locations are implemented in various data registers on board. The registers are located in the following devices:

-I.D. PROM (U38)
-Board Status Register (U54)
-Interrupt Vector Register (U40)
-Board Control Register (U56, U39)
-Channel Register (U54)
-Scan Counter Register (U54)
-Timer Prescaler (U36)
-Conversion Timer (U36)
-Conversion Control (U36)
-Conversion Status (U54)
-Start Conversion (U54)
-Analog Input Data Register (U69)
-Analog Output Data Registers (U22 thru U27)
-Digital Input/Output Registers (U20, U21, U28, U29)

4.4 ISOLATION BARRIER (935X-I, 9450-I & 9510-I)

The isolation barrier is used to protect the VMEbus from transients caused by ground loops produced by field wiring connections. The isolation barrier is composed of three functional circuit areas.

-Optical Isolation
-Power Isolation
-Isolated Data Transfer Controller

4.4.1 Optical Isolation

The analog input control signals are transmitted from the conversion control circuits to the A/D Converter via optocouplers U50, U51, U49, U70 and U71. The Serial Data communication across the isolation barrier and handshaking lines are transmitted through optocouplers using U33, U34, U35, U11, U12, U13 and U14. The non-isolated version of the board jumpers out the optocouplers with hardware jumpers.

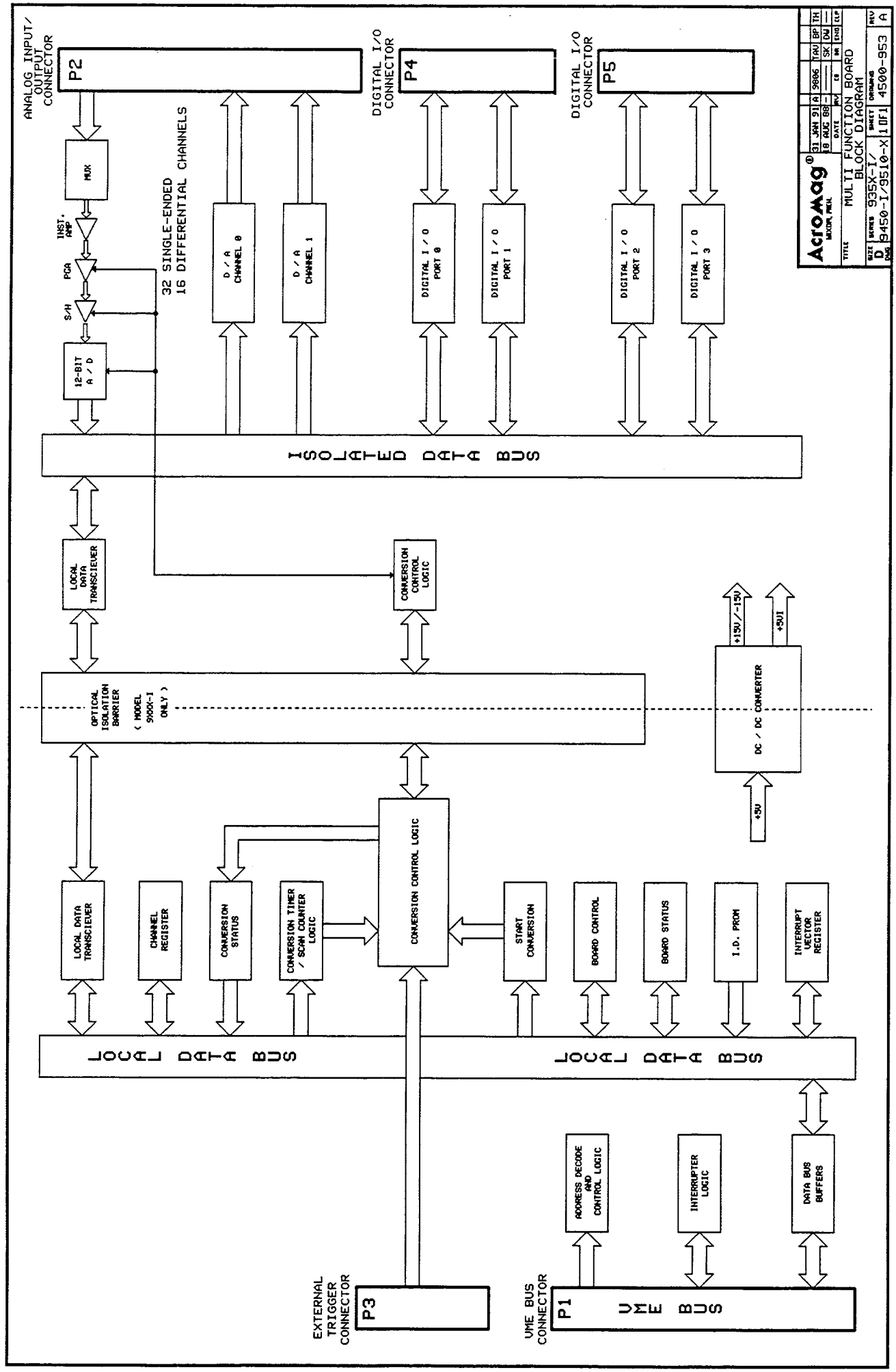


FIGURE 4.1

4.4.2 Isolated Data Transfer Controller

The isolated data transfer controller arbitrates the passing of data across the local isolation barrier. For example, a VME transfer may try to read the analog input register. Internally, the board will get the data from the analog input register and transfer it across the isolation barrier and provide it to the bus interface control logic for later transfer to the VMEbus.

On write cycles, the data transfer controller converts the 16 bit data bus into two 8 bit serial data streams using shift registers U41 and U42. Then the bit streams are clocked across the isolation barrier and reconverted to a 16 bit data bus using shift registers U30 and U32. The clock is a 2 MHz type derived from the 16 Mhz VMEbus SYSCLK in device U54.

On read cycles, the data transfer controller converts the 16 bit data bus on the isolated side to two 8 bit data streams using the shift registers in U9. The data streams are clocked across the isolation barrier and converted into a 16 bit data word using shift registers U57 and U58 for access from the VMEbus.

4.4.3 Power Isolation

Power to the isolated circuitry is provided by an on board triple output DC to DC converter. The voltage isolation is maintained by using power transformer T1. Astable multivibrator U17 drives the gates of mosfets Q1 and Q2 which in turn commutate the five volt supply for use as a power driver for the transformer. The isolated +/- 15 volts output is regulated using regulators U18 and U19. The five volt supply is unregulated.

4.5 ANALOG INPUT SECTION (935X-I & 9510-X)

The various functional areas comprising the analog input circuitry are described in the following subsections.

4.5.1 Analog Input Multiplexer

An input configuration consists of four 8-input, CMOS analog multiplexers and accepts 16 differential or 32 single-ended inputs via the Analog Input Connector, P2. The three least significant bits of the Channel Select Register are applied to each of the 8-input analog multiplexers to determine which one of the eight inputs will be activated. When configured for single-ended operation, only one of the analog multiplexers is enabled at a time. For differential operation, two analog multiplexers are enabled simultaneously.

A combinational logic decoder in U9 decodes the higher order bits from the Channel Select Register and is jumper programmed for either differential or single-ended operation. U45 decodes the programmable gain selection analog switch U46.

Jumper J16 is used to connect the outputs of the analog multiplexers to the instrumentation amplifier.

4.5.2 Instrumentation Amplifier

The instrumentation amplifier U67, is fast-settling and has FET inputs. The offset adjust R43 is used to correct for the offsets in both the instrumentation amplifier and the programmable gain amplifier U47.

It is possible for the gain to be custom programmed through R42 and R44. These resistors are not present on the standard product and the instrumentation amplifier has a gain of one in this configuration. If these resistors are to be selected, they should be chosen for minimum temperature drift and for as fine an adjustment capability as possible over the desired adjustment range. The gain equation is:

$$G = 1 + [40K / RG]$$

Where:

G is the gain of the instrumentation amplifier.
RG is the combined resistance of R42 and R44.

Note: High gains programmed through R42 and R44 at the instrumentation amplifier can increase the initial offset, the offset and gain drift with temperature and settling time.

4.5.3 Programmable Gain Circuit

The output of one-half of U47 is divided by a matched resistor set to form a feedback voltage for each of the four gains: X1, X2, X4 and X8. Analog switch U46 connects one of the voltages to the minus input of U47.

4.5.4 Sample and Hold Amplifier

The Sample and Hold Amplifier U68 follows the output of the Programmable Gain Amplifier until the signal to digitize the analog input is generated. Then it switches from the sample mode to the hold mode and maintains a constant voltage at the input to the A/D converter during the digitizing process.

4.5.5 Analog-to-Digital Converter

The Analog-to-Digital Converter U69 consists of a 12-bit analog to digital converter, a precision reference, a high speed comparator, successive approximation register converter control circuitry, a clock, and a digital interface. The output data is not valid during the time that the converter is digitizing the analog input signal.

4.5.6 Conversion Control Circuits

Refer to Figure 3.3 for the timing diagrams of the board. There are three timed functions that must be properly sequenced by the control logic: the amplifier settling timer, the A/D converter, and the sample and hold acquisition timer.

The amplifier settling timer, 1/2 of U75 is a retriggerable timer. Each time data is written into either the control or the channel select register, the 15uS timer delay is initiated. This timer allows the multiplexer, the instrumentation amplifier, programmable gain and offset circuits, and the sample and hold amplifier time to settle within the required accuracy before the A/D conversion takes place.

At the end of the amplifier settling time delay and if a conversion has been requested, the Sample and Hold, U68, is switched from the sample to the hold mode and the A/D converter, U69, starts the digitizing process. Once this process starts, it is permissible to change the control or channel select registers. Data is not valid during the digitizing process.

The Sample and Hold acquisition timer, 1/2 of U75, is triggered by the A/D converter at the end of the digitizing process, allowing sufficient time for the sample and hold circuit to again acquire its input signal before the next A/D conversion takes place.

Conversion status and control is provided by programmable logic device U54.

4.5.7 External Trigger

The External Trigger is input through P3 and buffered through U59. Programmable logic device U52 decodes which trigger source to provide to U54 for conversion control.

4.5.8 Timed Periodic Trigger Circuit

Timed Periodic Triggering is provided by two of the programmable counters within U36. These counters are cascaded to provide widely variable measured time periods. See Paragraph 3.3.3, Timed Periodic Triggering.

4.5.9 Scan Mode Counter Circuits

The Scan Mode is implemented with two counters. One of the counters is a 5-bit parallel load binary counter. In channel mode, this counter will only contain the channel number written into the Channel Register. In Scan Mode, this counter will be automatically incremented just after the beginning of each analog-to-digital conversion. This will cause scanning of the input channels.

The other counter used is the remaining programmable counter within U36. It is loaded with the count of the number of channels to be scanned. It is decremented every time the channel register counter is incremented. When all of the channels to be scanned have been converted, the scan counter outputs a load pulse which causes the channel register counter to be reloaded with the starting channel number. The starting channel number is always the last value written into the Channel Register.

4.6 ANALOG OUTPUT SECTION (9351-I & 9510-X)

Each analog output channel is composed of a 12 bit voltage output D/A converter (U43, U44) and a jumper (J14, J15) for selection of one of five output ranges. Input latches U22 thru U27 hold the data word for the D/A converters.

4.7 DIGITAL INPUT/OUTPUT SECTION (9450-I & 9510-X)

There are 32 digital input/output points available on the board. The hardware separates them into four ports of 8 points each. Each port has an 8 bit output latch (U20, U21, U28, U29) and two 4 bit input receivers (see schematic). With these receivers, Digital outputs may be read back. Diode protection and Resistor pull-up are also provided for each channel.

This section provides calibration procedures, service diagrams, and instructions on how to obtain service and repair assistance.

5.1 SERVICE AND REPAIR ASSISTANCE

It is highly recommended that a non-functioning board be returned to Acromag for repair. Acromag uses tested and burned-in parts, and in some cases, parts that have been selected for characteristics beyond that specified by the manufacturer. Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

5.2 PRELIMINARY SERVICE PROCEDURE

Before beginning calibration or repair, be sure that all of the procedures in Chapter 2, Preparation For Use, have been followed. The procedures are necessary since the board has jumpers that must be properly configured.

CAUTION POWER MUST BE OFF BEFORE REMOVING OR INSERTING BOARDS

Note: It has been observed that on occasion, a "boot" program for a disk operating system will "hang" waiting for the VMEbus SYSFAIL* signal to be released by an intelligent disk controller board. Acromag's non-intelligent slave boards assert the SYSFAIL* signal as described to the VMEbus Specification Rev. C.1 and therefore, the disk operating system will remain "hung". The best solution to this problem is to correct the boot program so that it is no longer dependent upon the SYSFAIL* signal. When this solution is not practical, it is possible to disconnect the SYSFAIL* from the circuitry on the Acromag board by cutting a PC board foil near the P1 connector on the solder side. Caution should be exercised so as not to cut any other foils nor damage the board in any other way. Call Acromag's Applications Engineering Department for assistance.

5.3 CALIBRATION OF ANALOG INPUT (935X-I & 9510-X)

The board is calibrated at the factory for standard ±10V bipolar analog input. Should unipolar or live endpoint calibration be desired or should recalibration ever become necessary, the Board may be calibrated in the field or may be returned to the factory. Care should be taken to insure the integrity of any adjustments being made.

The following equipment will be required in order to calibrate the board's analog input section:

1. A precision adjustable voltage source with 0 to 10V output range, 0.001% accuracy, and isolated output.

2. A precision Digital Voltmeter (DVM) with 0.001% accuracy and isolated input.

Note that any calibration of the analog input section first requires calibration of the programmable gain stage offset.

Proper grounding requires that each system have one and only one earth ground. Care should be used to insure this on all models. Failure to ground properly may result in noisy data.

5.3.1 Analog Input Offset Calibration for the Programmable Gain Stage

The offset calibration for the programmable gain stage must always be performed before calibration of the input range. The offset calibration is performed as follows:

1. Configure the Board for differential inputs.

2. Connect the DVM signal and ground input leads to test point 1 (TP-1 ground pin is farthest from P2.) See Figures 2.1 and the schematic on Page 9.

3. Apply zero volts to channel zero.

4. Setup the Board so that channel number zero and Channel Mode are selected.

5. Adjust R43 until the voltage at TP-1 is zero volts (within ±50uV).

5.3.2 Analog Input Standard Bipolar Calibration

Perform this calibration as follows:

1. Configure the Board for the standard bipolar configuration, differential inputs, and bipolar two's complement data format (See Chapter 2, Preparation for Use).

2. Connect the precision voltage source to input channel zero and connect the voltage source signal ground to analog ground on the board. These connections can be made at P2 or on a termination panel if one is available.

3. Set up the registers on the Board so that channel number zero, Channel Mode and a gain of x1 are selected.

4. Apply a DC input voltage equivalent to 1/2 LSB above 0 volts (i.e., +0.0024 volts). Assuming bipolar two's complement data format, adjust R53 until data read on analog input channel 0 toggles evenly between 0000H and 0010H (remember that the 12-bit data is left justified in the Input Data Register).

5. Apply a DC input voltage equivalent to 1 and 1/2 LSB less than +10 volts (i.e., +9.9927 volts). Assuming bipolar two's complement data format, adjust R24 until data read on analog input channel 0 toggles evenly between 7FE0H and 7FF0H (remember that the 12-bit data is left justified in the Input Data Register).

5.3.3 Analog Input Standard Unipolar Calibration

Perform this calibration as follows:

1. Configure the Board for the standard unipolar configuration, differential inputs, and unipolar straight binary data format (See Chapter 2, Preparation for Use).

2. Connect the precision voltage source to input channel zero and connect the voltage source signal ground to analog ground on the Board. These connections can be made at P2 or on a termination panel if one is available.

3. Set up the registers on the Board so that channel number zero, Channel Mode and a gain of x1 are selected.

4. Apply a DC input voltage equivalent to 1/2 LSB above 0 volts (i.e., +0.0012 volts). Assuming unipolar straight binary data format, adjust R54 until data read on analog input channel 0 toggles evenly between 0000H and 0010H (remember that the 12-bit data is left justified in the Input Data Register).

5. Apply a DC input voltage equivalent to 1 and 1/2 LSB less than 10 volts (i.e., +9.9963 volts). Assuming unipolar straight binary data format, adjust R24 until data read on analog input channel 0 toggles evenly between FFE0H and FFF0H (remember that the 12-bit data is left justified in the Input Data Register).

5.3.4 Analog Input Live End Point Bipolar Calibration

Perform this calibration as follows:

1. Configure the Board for the live end point bipolar configuration, differential inputs, and bipolar two's complement data format (See Chapter 2, Preparation for Use).

2. Connect the precision voltage source to input channel zero and connect the voltage source signal ground to analog ground on the board. These connections can be made at P2 or on a termination panel if one is available.

3. Set up the registers on the Board so that channel number zero, Channel Mode and a gain of x1 are selected.

4. Apply a DC input voltage equivalent to 1/2 LSB above 0 volts (i.e., +0.0025 volts). Assuming bipolar two's complement data format, adjust R53 until data read on analog input channel 0 toggles evenly between 0000H and 0010H (remember that the 12-bit data is left justified in the Input Data Register).

5. Apply a DC input voltage equivalent to 1/2 LSB less than 10 volts (i.e., +9.9975 volts). Assuming bipolar two's complement data format, adjust R24 until data read on analog input channel 0 toggles evenly between 7DF0H and 7E00H (remember that the 12-bit data is left justified in the Input Data Register and that the value 7E00H represents exactly 10 volts with this type of calibration).

5.3.5 Analog Input Live End Point Unipolar Calibration

Perform this calibration as follows:

1. Configure the Board for the live end point unipolar configuration, differential inputs, and unipolar straight binary data format (See Chapter 2, Preparation for Use).

2. Connect the precision voltage source to input channel zero and connect the voltage source signal ground to analog ground on the board. These connections can be made at P2 or on a termination panel if one is available.

3. Set up the registers on the board so that channel number zero, Channel Mode and a gain of x1 are selected.

4. Apply a DC input voltage equivalent to 1/2 LSB above 0 volts (i.e., +0.0012 volts). Assuming unipolar straight binary data format, adjust R54 until data read on analog input channel 0 toggles evenly between 0200H and 0210H (remember that the 12-bit data is left justified in the Input Data Register and that the value 0200H represents exactly 0 volts with this type of calibration).

5. Apply a DC input voltage equivalent to 1/2 LSB less than 10 volts (i.e., +9.9988 volts). Assuming unipolar straight binary data format, adjust R24 until data read on analog input channel 0 toggles evenly between FDF0H and FE00H (remember that the 12-bit data is left justified in the Input Data Register and that the value of FE00H represents exactly 10 volts with this type of calibration).

5.4 CALIBRATION OF ANALOG OUTPUTS (9351-I & 9510-X)

The board is calibrated at the factory for standard ±10 volt bipolar analog output. Should the use of another output range be desired or should recalibration become necessary, the Board may be calibrated in the field or may be returned to the factory. Care should be taken to insure the integrity of any adjustments being made.

The following equipment will be required in order to calibrate the board analog outputs: A precision DVM with 0.001% accuracy and isolated input.

5.4.1 Analog Output Bipolar Calibration

For each of the two analog output channels perform the following steps:

1. Configure the board for bipolar analog output configuration and bipolar two's complement data format (See Chapter 2, Preparation for Use).

2. Connect the DVM signal and ground input leads to channel 0 output terminals.

3. Offset Adjustment: Assuming bipolar two's complement data format, write the code 8000H into the Analog Output Channel 0 Data Register. Adjust R29 (R36 for channel 1) for the output voltage corresponding to the desired output voltage range:

Desired Analog Output Range	Adjust until Output Voltage is
± 10 Volts	-10.000 Volts
± 5 Volts	-5.0000 Volts
± 2.5 Volts	-2.5000 Volts

4. Span Adjustment: Assuming bipolar two's complement data format, write the code 7FF0H into the analog output channel 0 data register. Adjust R28 (R35 for channel 1) for the output voltage corresponding to the desired output voltage range:

Desired Analog Output Range	Adjust until Output Voltage is
± 10 Volts	+9.9951 Volts
± 5 Volts	+4.9976 Volts
± 2.5 Volts	+2.4988 Volts

5.4.2 Analog Output Unipolar Calibration

For each analog output channel perform the following steps:

1. Configure the board for unipolar analog output configuration and unipolar straight binary data format (See Chapter 2, Preparation for Use).

2. Connect the DVM signal and ground input leads to channel 0 output terminals.

3. Offset Adjustment: Assuming unipolar straight binary data format, write the code 0000H into the Analog Output Channel 0 Data Register. Adjust R29 (R36 for channel 1) for output voltage value of 0.0000 Volts.

4. Span Adjustment: Assuming unipolar straight binary data format, write the code FFF0H into the Analog Output Channel 0 Data Register. Adjust R28 (R35 for channel 1) for output voltage corresponding to the desired output voltage range:

Desired Analog Output Range	Adjust until Output Voltage is
0 to +10 Volts	+9.9976 Volts
0 to +5 Volts	+4.9988 Volts

5.5 PARTS LIST

The Parts List (Table 5.1) is provided as an aid to the user in troubleshooting the Board. Replacement parts and repair services are available from Acromag. If parts are replaced in the analog circuitry, recalibration may be required. If repair is deemed necessary in this circuitry, it is highly recommended that the Board be returned to Acromag for repair and recalibration.

Changes are sometimes made to improve the product, to facilitate delivery, or to control cost. It is therefore important to include the reference Number, the Acromag Part Number, the Board Model Number, and the Board Serial Number when providing information to order parts.

TABLE 5.1A
AVME9350-I PARTS LIST

LOCATION	ACROMAG #	DESCRIPTION
C12 14 77-80 87	1002-321	CAP 10UF
C16 42 91	1002-314	CAP 150UF
C17 19	1002-319	CAP 3.3UF
C38	1002-549	CAP 100PF
C39 96 97	1002-438	CAP .001UF
C41	1002-312	CAP 22UF
C43	1002-316	CAP .22UF
C8 9 13 15 18 20 31-36 40 44-46 C53-57 66-70 72-76 81-86 88-90 C92-95 98	1002-530	CAP .1UF
C65 100	1002-434	CAP 560PF
C71	1002-442	CAP .01UF
C99 101	1002-422	CAP 33PF
D10	1001-166	LED RED
D5 15 16	1001-113	DIODE 1N914B
D7 8 11-14	1001-167	DIODE FAST REC.
D9	1001-165	LED GREEN
F1	1030-471	FUSE, 10 AMP
J10 21 25	1004-333	HEADER 1R 3P
J11	1004-374	HEADER 2R 6P
J16	1004-365	HEADER 1R 4P
J23	1004-383	HEADER 2R 12P
J26	1004-379	HEADER 2R 16P
J6 8 12 13 17-20 24 TP1-TP3	1004-410	HEADER 1R 2P
L1-5	1016-005	INDUCTOR, 47UH
L6	1016-061	INDUCTOR, 1UH
P1	1004-505	CONN. EDGE 96 MALE
P2	1004-528	CONN. EDGE 64 MALE
P3	1004-529	CONNECTOR, BNC RIGHT
Q1 2	1023-117	TRANS. MTP50N06V
R10 11 13 25	1100-496	RES NETWORK 680 OHM
R14	1000-834	RES 1.8K
R16	1006-775	RES 7.15K
R17	1000-811	RES 22 OHM
R19	1000-822	RES 180 OHM

TABLE 5.1A
AVME9350-I PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
R21	1006-672	RES 604 OHM
R24	1000-713	POT 200 OHM
R30 31	1006-693	RES 1K
R43 54	1100-145	POT 10K
R45-48	1100-522	RES MATCHED SET
R49 50	1000-837	RES 3.3K
R5 27	1100-268	RES NETWORK 4.7K
R51	1006-568	RES 49.9 OHM
R52	1006-616	RES 158 OHM
R53	1100-139	POT 100 OHM
R55	1008-885	RES 100K
R56	1006-827	RES 24.9K
R57	1006-585	RES 75 OHM
R58	1006-643	RES 301 OHM
R59 60	1100-494	RES NETWORK 1K
R61	1006-867	RES 64.9K
R62	1006-780	RES 8.06K
R63 65	1000-825	RES 330 OHM
R64	1000-828	RES 560 OHM
R8 12 18 26	1100-495	RES NETWORK 470 OHM
R9	1000-817	RES 68 OHM
T1	1014-095	TRANS. PICO #10769
U10	9000-172	----------
U11 12 13 14 35 49-51 70 71	1033-720	IC HCPL-2631
U15	1033-719	IC 74ALS136
U16	1033-146	IC 4069
U17	1033-323	IC 4047
U18	1033-234	IC 79M15
U19	1033-222	IC 78M15
U31	1033-340	IC LM78L05
U36	1033-671	IC QP8254-5
U37	1033-259	IC 74LS14
U38	9000-178	----------
U39 53	1033-670	IC 74LS174N3
U40	1033-724	IC 74LS374
U45	1033-269	IC 74LS139
U46	1033-288	IC HI-201
U47	1033-321	IC LF-353
U48	1033-255	IC 74LS04ND
U52	9000-152	----------
U55	9000-175	----------

TABLE 5.1A
AVME9350-I PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
U56 60 61	1033-273	IC 74LS244
U57 58	1033-658	IC 74LS164N
U59	1033-623	IC N74F38N
U62-65	1033-292	IC HI1-0508A-7
U67	1033-582	IC AD524AD
U68	1033-677	IC SHC5320
U69	1033-290	IC HI1-574
U72	1033-048	IC 7445N
U73 74	1033-626	IC AM25LS2521PCB
U75	1033-276	IC 74LS423ND
U76	1033-284	IC 74LS393ND
U77 78	1033-627	IC 74LS645-1ND
U9 54	1033-715	IC 2018-84PLCC

TABLE 5.1B
AVME9351-I PARTS LIST

LOCATION	ACROMAG #	DESCRIPTION
C12 14 77-80 87	1002-321	CAP 10UF
C16 42 91	1002-314	CAP 150UF
C17 19	1002-319	CAP 3.3UF
C38	1002-549	CAP 100PF
C39 96 97	1002-438	CAP .001UF
C41	1002-312	CAP 22UF
C43	1002-316	CAP .22UF
C51 52 62 63	1002-320	CAP 1UF
C37 47 58 64	1002-428	CAP 100PF
C49 60 71	1002-442	CAP .01UF
C65 100	1002-434	CAP 560PF
C8 9 13 15 18 20 22 23 25 26 C31-36 40 44-46 48 50 53-57 59 61 C66-70 72-76 81-86 88-90 92-95 98	1002-530	CAP .1UF
C99 101	1002-422	CAP 33PF
D10	1001-166	LED RED
D5 15 16	1001-113	DIODE 1N914B
D7 8 11-14	1001-167	DIODE FAST REC.
D9	1001-165	LED GREEN
F1	1030-471	FUSE, 10 AMP
J11	1004-374	HEADER 2R 6P
J14 15	1004-377	HEADER 2R 8P
J16	1004-365	HEADER 1R 4P
J23	1004-383	HEADER 2R 12P
J26	1004-379	HEADER 2R 16P
J6 8 12 13 17-20 24 TP1-TP3	1004-410	HEADER 1R 2P
J9 10 21 25 27	1004-333	HEADER 1R 3P
L1-5	1016-005	INDUCTOR, 47UH
L6	1016-061	INDUCTOR, 1UH
P1	1004-505	CONN. EDGE 96 MALE
P2	1004-528	CONN. EDGE 64 MALE
P3	1004-529	CONNECTOR, BNC RIGHT
Q1 2	1023-117	TRANS. MTP50N06V

TABLE 5.1B
AVME9351-I PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
R10 11 13 25	1100-496	RES NETWORK 680 OHM
R14	1000-834	RES 1.8K
R16	1006-775	RES 7.15K
R17	1000-811	RES 22 OHM
R19	1000-822	RES 180 OHM
R21	1006-672	RES 604 OHM
R24	1000-713	POT 200 OHM
R28 29 35 36 43 54	1100-145	POT 10K
R30 31	1006-693	RES 1K
R32 39	1006-943	RES 402K
R33 40	1006-518	RES 15 OHM
R34 41	1000-872	RES 2.7M
R37	1100-492	RES NETWORK 33 OHM
R38	1100-493	RES NETWORK 68 OHM
R45-48	1100-522	RES MATCHED SET
R49 50	1000-837	RES 3.3K
R5 27	1100-268	RES NETWORK 4.7K
R51	1006-568	RES 49.9 OHM
R52	1006-616	RES 158 OHM
R53	1100-139	POT 100 OHM
R55	1008-885	RES 100K
R56	1006-827	RES 24.9K
R57	1006-585	RES 75 OHM
R58	1006-643	RES 300 OHM
R59 60	1100-494	RES NETWORK 1K
R61	1006-867	RES 64.9K
R62	1006-780	RES 8.06K
R63 65	1000-825	RES 330 OHM
R64	1000-828	RES 560 OHM
R8 12 18 26	1100-495	RES NETWORK 470 OHM
R9	1000-817	RES 68 OHM
T1	1014-095	TRANS. PICO #10769
U10	9000-173	----------
U11-14 33-35 49-51 70 71	1033-720	IC HCPL-2631
U15	1033-719	IC 74ALS136
U16	1033-146	IC 4069
U17	1033-323	IC 4047
U18	1033-234	IC 79M15
U19	1033-222	IC 78M15
U22-27	1033-657	IC 74LS175N
U30 32 57 58	1033-658	IC 74LS164N
U31	1033-340	IC LM78L05

TABLE 5.1B
AVME9351-I PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
U36	1033-671	IC QP8254-5
U37	1033-259	IC 74LS14
U38	9000-179	----------
U39 53	1033-670	IC 74LS174N3
U40	1033-724	IC 74LS374
U41 42	1033-712	IC 74LS165N
U43 44	1033-656	IC DAC80
U45	1033-269	IC 74LS139
U46	1033-288	IC HI-201
U47	1033-321	IC LF-353
U48	1033-255	IC 74LS04ND
U52	9000-152	----------
U55	9000-176	----------
U56 60 61	1033-273	IC 74LS244
U59	1033-623	IC N74F38N
U62-65	1033-292	IC HI1-0508A-7
U67	1033-582	IC AD524AD
U68	1033-677	IC SHC5320
U69	1033-290	IC HI1-574
U72	1033-048	IC 7445N
U73 74	1033-626	IC AM25LS2521PCB
U75	1033-276	IC 74LS423ND
U76	1033-284	IC 74LS393ND
U77 78	1033-627	IC 74LS645-1ND
U9 54	1033-715	IC 2018-84PLCC

TABLE 5.1C
AVME9450-I PARTS LIST

LOCATION	ACROMAG #	DESCRIPTION
C1 3 6 8 9 15 20 21 24 28-36 40 C72 89 90 92-95 98	1002-530	CAP .1UF
C10 11	1002-315	CAP 10UF 35V
C14 27	1002-321	CAP 10UF
C16 42 91	1002-314	CAP 150UF
C19	1002-319	CAP 3.3UF
C38	1002-549	CAP 100PF
C39	1002-438	CAP .001UF
C41	1002-312	CAP 22UF
C43	1002-316	CAP .22UF
D10	1001-166	LED RED
D1-4	1001-168	DIODE DAP801
D5	1001-113	DIODE 1N914B
D7 8 12 13	1001-167	DIODE FAST REC.
D9	1001-165	LED GREEN
F1	1030-471	FUSE, 10 AMP
J1 3 8 13 24 TP1	1004-410	HEADER 1R 2P
J23	1004-383	HEADER 2R 12P
J25	1004-333	HEADER 1R 3P
J26	1004-379	HEADER 2R 16P
L6	1016-061	INDUCTOR, 1UH
P1	1004-505	CONN. EDGE 96 MALE
P4 5	1004-592	CONNECTOR, BNC RIGHT
Q1 2	1023-117	TRANS. MTP50N06V
R10 11 13	1100-496	RES NETWORK 680 OHM
R16	1006-775	RES 7.15K
R17	1000-811	RES 22 OHM
R19	1000-822	RES 180 OHM
R2 4 22 23	1100-490	RES NETWORK 1K
R21	1006-672	RES 604 OHM
R5 27	1100-268	RES NETWORK 4.7K
R59 60	1100-494	RES NETWORK 1K
R65	1000-825	RES 330 OHM
R8 12 18	1100-495	RES NETWORK 470 OHM
R9	1000-817	RES 68 OHM
T1	1014-095	TRANS. PICO #10769

TABLE 5.1C
AVME9450-I PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
U10	9000-174	----------
U11-14 33-35	1033-720	IC HCPL-2631
U15	1033-719	IC 74ALS136
U16	1033-146	IC 4069
U17	1033-323	IC 4047
U19	1033-222	IC 78M15
U1-8	1033-346	IC 1489PD
U20 21 28 29	1033-515	IC 5801ABU
U30 32 57 58	1033-658	IC 74LS164N
U31	1033-340	IC LM78L05
U37	1033-259	IC 74LS14
U38	9000-180	----------
U41 42	1033-712	IC 74LS165N
U48	1033-255	IC 74LS04ND
U53	1033-670	IC 74LS174N3
U55	9000-177	----------
U59	1033-623	IC N74F38N
U60 61	1033-273	IC 74LS244
U73 74	1033-626	IC AM25LS2521PCB
U77 78	1033-627	IC 74LS645-1ND
U9 54	1033-715	IC 2018-84PLCC

TABLE 5.1D
AVME9510-I PARTS LIST

LOCATION	ACROMAG #	DESCRIPTION
C1 3 6 8 9 13 15 18 20 21 22 23 C24 25 26 28-36 40 44-46 48 50 C53-57 59 61 66 67 68 69 70 72 C73 73 75 76 81 82 83 84 85 86 C88-90 92 93 94 95 98	1002-530	CAP .1UF
C10 11	1002-315	CAP 10UF 35V
C12 14 27 77 78	1002-321	CAP 10UF
C79 80 87	1002-321	CAP 10UF
C16 42 91	1002-314	CAP 150UF
C17 19	1002-319	CAP 3.3UF
C38	1002-549	CAP 100PF
C39 96 97	1002-438	CAP .001UF
C41	1002-312	CAP 22UF
C43	1002-316	CAP .22UF
C51 52 62 63	1002-320	CAP 1UF
C37 47 58 64	1002-428	CAP 100PF
C49 60 71	1002-442	CAP .01UF
C65 100	1002-434	CAP 560PF
C99 101	1002-422	CAP 33PF
D1 2 3 4	1001-168	DIODE DAP801
D5 15 16	1001-113	DIODE 1N914B
D7 8 11 12 13 14	1001-167	DIODE FAST REC.
D9	1001-165	LED GREEN
D10	1001-166	LED RED
F1	1030-471	FUSE 10 AMP
J1 3 6 8 12 13 17-20 24 TP1-TP3	1004-410	HEADER 1R 2P
J9 10 21 25 27	1004-333	HEADER 1R 3P
J11	1004-374	HEADER 2R 6P
J14 J15	1004-377	HEADER 2R 8P
J16	1004-365	HEADER 1R 4P
J23	1004-383	HEADER 2R 12P
J26	1004-379	HEADER 2R 16P
L1 2 3 4 5	1016-005	INDUCTOR 47UH
L6	1016-061	INDUCTOR 1UH
P1	1004-505	CONN. EDGE 96 MALE
P2	1004-528	CONN. EDGE 64 MALE
P3	1004-529	CONNECTOR BNC RIGHT
P4 5	1004-592	DBL 50 PIN HDR CON

TABLE 5.1D
AVME9510-I PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
Q1 2	1023-117	TRANS. MTP50N06V
R2 4 22 23	1100-490	RES NETWORK 1K
R8 12 18 26	1100-495	RES NETWORK 470 OHM
R9	1000-817	RES 68 OHM
R10 11 13 25	1100-496	RES NETWORK 680 OHM
R5 27	1100-268	RES NETWORK 4.7K
R19	1000-822	RES 180 OHM
R14	1000-834	RES 1.8K
R16	1006-775	RES 7.15K
R17	1000-811	RES 22 OHM
R21	1006-672	RES 604 OHM
R24	1000-713	POT 200 OHM
R28 29 35 36 43 54	1100-145	POT 10K
R30 31	1006-693	RES 1K
R32 39	1006-943	RES 402K
R33 40	1006-518	RES 15 OHM
R34 41	1000-872	RES 2.7M
R37	1100-492	RES NETWORK 33 OHM
R38	1100-493	RES NETWORK 68 OHM
R45 46 47 48	1100-522	RES MATCHED SET
R49 50	1000-837	RES 3.3K
R51	1006-568	RES 49.9 OHM
R52	1006-616	RES 158 OHM
R53	1100-139	POT 100 OHM
R55	1008-885	RES 100K
R56	1006-827	RES 24.9K
R57	1006-585	RES 75 OHM
R58	1006-643	RES 300 OHM
R59 60	1100-494	RES NETWORK 1K
R61	1006-867	RES 64.9K
R62	1006-780	RES 8.06K
R63 65	1000-825	RES 330 OHM
R64	1000-828	RES 560 OHM
T1	1014-095	TRANS. PICO #10769

TABLE 5.1D
AVME9510-I PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
U1 2 3 4 5 6 7 8	1033-346	IC 1489PD
U9 54	1033-715	IC 2018-84PLCC
U10	9000-151	----------
U11-14 33 34 35 49-51 70 71	1033-720	IC HCPL-2631
U15	1033-719	IC 74ALS136
U16	1033-146	IC 4069
U17	1033-323	IC 4047
U18	1033-234	IC 79M15
U19	1033-222	IC 78M15
U20 21 28 29	1033-515	IC 5801ABU
U22 23 24 25 26 27	1033-657	IC 74LS175N
U30 32 57 58	1033-658	IC 74LS164N
U31	1033-340	IC LM78L05
U36	1033-671	IC QP8254-5
U37	1033-259	IC 74LS14
U38	9000-155	----------
U39 53	1033-670	IC 74LS174N3
U40	1033-724	IC 74LS374
U41 42	1033-712	IC 74LS165N
U43 44	1033-656	IC DAC80
U45	1033-269	IC 74LS139
U46	1033-288	IC HI-201
U47	1033-321	IC LF-353
U48	1033-255	IC 74LS04ND
U52	9000-152	----------
U55	9000-153	----------
U56 60 61	1033-273	IC 74LS244
U59	1033-623	IC N74F38N
U62 63 64 65	1033-292	IC HI1-0508A-7
U67	1033-582	IC AD524AD
U68	1033-677	IC SHC5320
U69	1033-290	IC HI1-574
U72	1033-048	IC 7445N
U73 74	1033-626	IC AM25LS2521PCB
U75	1033-276	IC 74LS423ND
U76	1033-284	IC 74LS393ND
U77 78	1033-627	IC 74LS645-1ND

TABLE 5.1E
AVME9510 PARTS LIST

LOCATION	ACROMAG #	DESCRIPTION
C1 3 6 8 13 15 18 20-26 C28-33 35-36 40 44-46 48 50 C53-57 59 61 66 67 68 69 70 72 C73 73 75 76 81 82 83 84 85 86 C88 92 93 94 95 98	1002-530	CAP .1UF
C10 11	1002-315	CAP 10UF 35V
C12 14 27 77 78	1002-321	CAP 10UF
C79 80 87	1002-321	CAP 10UF
C16 42 91	1002-314	CAP 150UF
C17 19	1002-319	CAP 3.3UF
C39 96 97	1002-438	CAP .001UF
C41	1002-312	CAP 22UF
C43	1002-316	CAP .22UF
C51 52 62 63	1002-320	CAP 1UF
C37 47 58 64	1002-428	CAP 100PF
C49 60 71	1002-442	CAP .01UF
C65 100	1002-434	CAP 560PF
C99 101	1002-422	CAP 33PF
D1 2 3 4	1001-168	DIODE DAP801
D5 15 16	1001-113	DIODE 1N914B
D7 8 11 12 13 14	1001-167	DIODE FAST REC.
D9	1001-165	LED GREEN
D10	1001-166	LED RED
F1	1030-471	FUSE 10 AMP
J1 3 6 8 12 13 17-20 24 TP1-TP3	1004-410	HEADER 1R 2P
J9 10 21 25 27	1004-333	HEADER 1R 3P
J11	1004-374	HEADER 2R 6P
J14 J15	1004-377	HEADER 2R 8P
J16	1004-365	HEADER 1R 4P
J22	2002-234	JUMPER .4
J23	1004-383	HEADER 2R 12P
J26	1004-379	HEADER 2R 16P
J28-51	2002-305	JUMPER .3
L1 2 3 4 5	1016-005	INDUCTOR 47UH
L6	1016-061	INDUCTOR 1UH
P1	1004-505	CONN. EDGE 96 MALE
P2	1004-528	CONN. EDGE 64 MALE
P3	1004-529	CONNECTOR BNC RIGHT
P4 5	1004-592	DBL 50 PIN HDR CON

TABLE 5.1E
AVME9510 PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
Q1 2	1023-117	TRANS. MTP50N06V
R2 4 22 23	1100-490	RES NETWORK 1K
R9	1000-817	RES 68 OHM
R5 27	1100-268	RES NETWORK 4.7K
R19	1000-822	RES 180 OHM
R14	1000-834	RES 1.8K
R16	1006-775	RES 7.15K
R17	1000-811	RES 22 OHM
R24	1000-713	POT 200 OHM
R28 29 35 36 43 54	1100-145	POT 10K
R30 31	1006-693	RES 1K
R32 39	1006-943	RES 402K
R33 40	1006-518	RES 15 OHM
R34 41	1000-872	RES 2.7M
R37	1100-492	RES NETWORK 33 OHM
R38	1100-493	RES NETWORK 68 OHM
R45 46 47 48	1100-522	RES MATCHED SET
R49 50	1000-837	RES 3.3K
R51	1006-568	RES 49.9 OHM
R52	1006-616	RES 158 OHM
R53	1100-139	POT 100 OHM
R55	1008-885	RES 100K
R56	1006-827	RES 24.9K
R57	1006-585	RES 75 OHM
R58	1006-643	RES 300 OHM
R59 60	1100-494	RES NETWORK 1K
R61	1006-867	RES 64.9K
R62	1006-780	RES 8.06K
R63 65	1000-825	RES 330 OHM
R64	1000-828	RES 560 OHM
T1	1014-095	TRANS. PICO #10769

TABLE 5.1E
AVME9510 PARTS LIST
(CONTINUED)

LOCATION	ACROMAG #	DESCRIPTION
U1 2 3 4 5 6 7 8	1033-346	IC 1489PD
U9 54	1033-715	IC 2018-84PLCC
U10	9000-151	----------
U15	1033-719	IC 74ALS136
U16	1033-146	IC 4069
U17	1033-323	IC 4047
U18	1033-234	IC 79M15
U19	1033-222	IC 78M15
U20 21 28 29	1033-515	IC 5801ABU
U22 23 24 25 26 27	1033-657	IC 74LS175N
U30 32 57 58	1033-658	IC 74LS164N
U31	1033-340	IC LM78L05
U36	1033-671	IC QP8254-5
U38	9000-154	----------
U39 53	1033-670	IC 74LS174N3
U40	1033-724	IC 74LS374
U41 42	1033-712	IC 74LS165N
U43 44	1033-656	IC DAC80
U45	1033-269	IC 74LS139
U46	1033-288	IC HI-201
U47	1033-321	IC LF-353
U48	1033-255	IC 74LS04ND
U52	9000-152	----------
U55	9000-153	----------
U56 60 61	1033-273	IC 74LS244
U59	1033-623	IC N74F38N
U62 63 64 65	1033-292	IC HI1-0508A-7
U67	1033-582	IC AD524AD
U68	1033-677	IC SHC5320
U69	1033-290	IC HI1-574
U72	1033-048	IC 7445N
U73 74	1033-626	IC AM25LS2521PCB
U75	1033-276	IC 74LS423ND
U76	1033-284	IC 74LS393ND
U77 78	1033-627	IC 74LS645-1ND

Operating temperature	0 to +70 deg. C
Storage temperature	-25 to +85 deg. C
Physical characteristics:	
Length	9.187 in. (233.3 mm)
Width	6.299 in. (160.0 mm)
Board thickness	0.062 in. (1.59 mm)
Component height	0.550 in. (13.97 mm)
Recommended card spacing	0.800 in. (20.32 mm)
Mating connectors:	
P1	96 pin 603-2-IEC class 2
P2	64 pin 603-2-IEC class 2
P3	BNC jack
Power requirements:	
+ 5 Volts	2.5A typ.
+ 12 Volts	20 mA

ANALOG INPUT SECTION (935X-I & 9510-X)

Input type	voltage
Input configuration	16 differential or 32 single ended
Input range	+/- 10 Volts bipolar or +/- 5 bipolar 0 to 10 Volts unipolar
Programmable gain	x1, x2, x4, x8
Input overvoltage protection	+/- 32 Volts continuous
Input resistance	1000 Mohms
Input bias current	150 pA typical
Isolation mode rejection (60 Hz)	96 db (AVME9XXXX-I only)
Common mode rejection ratio (60Hz)	71 db
Channel to channel rejection ratio (60Hz)	71 db
RFI resistance @27MHz, 151MHz, and 467MHz	< 0.25% of FSR at 10V/m Field Intensity
Settling time: 20 V step	24 uS to 0.01% of FSR
Sample and hold acquisition time	3 uS max.
A/D conversion time	25 uS max.
A/D resolution	12 bits
No missing codes over temperature	12 bits
A/D nonlinearity	+/- 1/2 LSB
System accuracy	0.04% of FSR
Overall throughput rate	31K conversions/second (max) (32.0 uS/conversion)
Gain temperature coefficient	50 ppm/deg. C max.
Offset temperature coefficient	24 ppm/deg. C max.
Total temperature coefficient	74 ppm/deg. C max.

VMEbus ACCESS TIME*	5.8 uS For Accessing Digital I/O Ports, Analog Output and Analog Input Registers 940nS For all Other Registers

Measured from the edge of AS to the rising edge of DTACK*.

ANALOG OUTPUT SECTION (9351-I & 9510-X)

Output type	Non-isolated voltage
Output ranges	+/- 2.5V, +/- 5V, +/- 10V, 0 to 5V, 0 to 10V
Number of channels	2
Resolution	12 bits
Monotonicity over temperature	12 bits
Nonlinearity	+/- 1/2 LSB
System accuracy	0.025% of FSR
Output noise	1.5mVrms in a 20MHz bandwidth, typical.
Capacitive loading w/o oscillation	0.01 uF max.
Output impedance	< 1 ohm
Short circuit protection	Continuous
Settling time: 20 V step	6 uS to 0.01% of FSR
Settling time: 20 V step w/bus access time	10 uS to .01% of FSR
Default output on reset	0V for USB and BTC, -FSR for BOB
Gain temperature coefficient	25 ppm/deg. C max.
Offset temperature coefficient	15 ppm/deg. C max.
Total temperature coefficient	40 ppm/deg. C max.
Resistance to RFI 27MHz, 151MHz, 467MHz	< 0.25% of FSR at 10 V/m Field Intensity

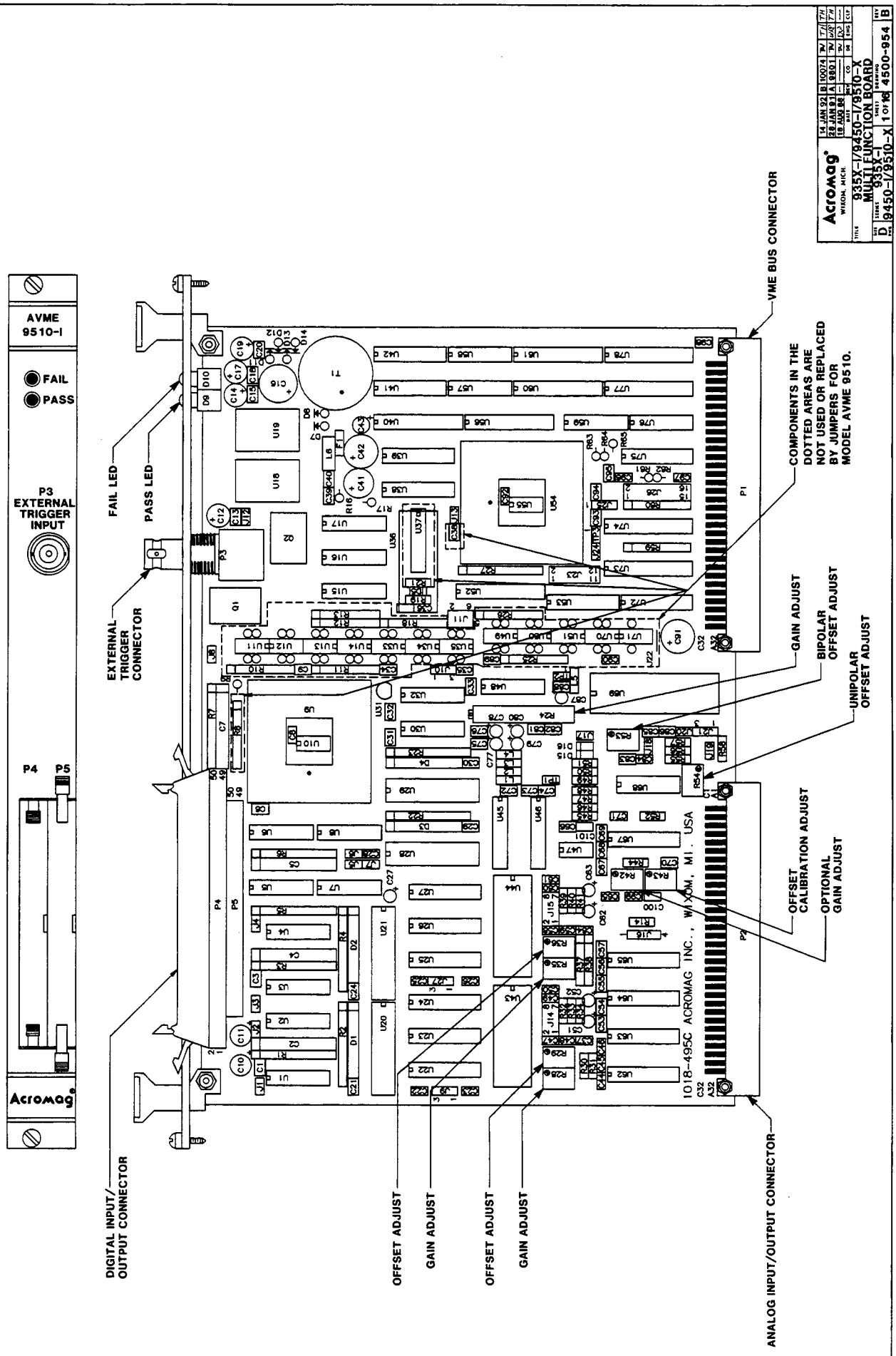
DIGITAL INPUT/OUTPUT (9450-I & 9510-X)

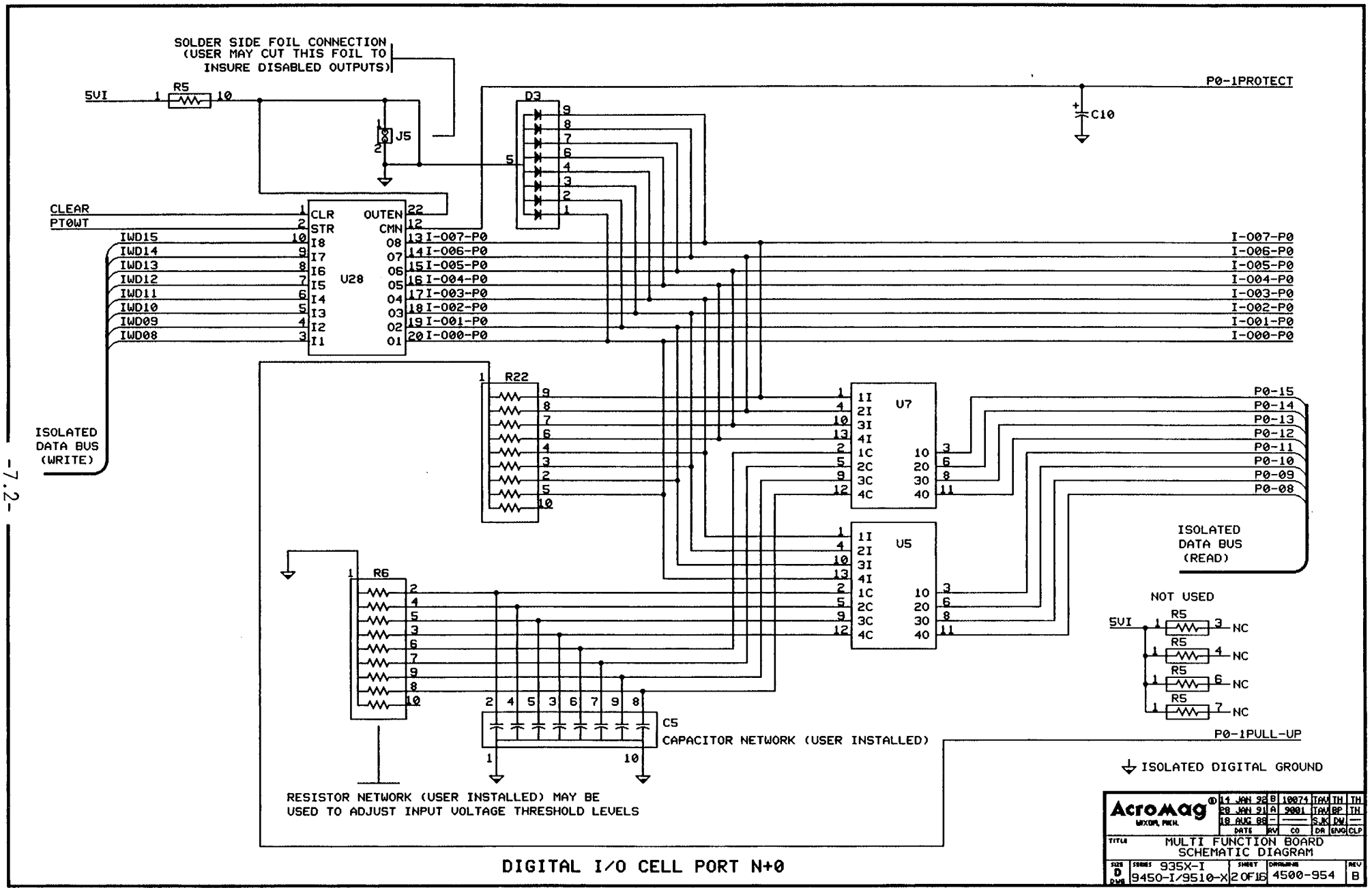
Input Voltage Range	-0.3 to 30 V DC
Input Threshold (L to H)	1.3 V DC nominal (resistor adjustable)
Input Threshold (H to L)	1.0 V DC nominal (resistor adjustable)
Input Hysteresis	0.3 V DC nominal
Input Resistance	3.8 K typ. (pull-up resistors removed)
Input Current	7.8 mA at 30 V DC (pull-up resistors removed)
Points per Card	32 (4 groups of 8 channels)
Programmability	Each point software programmable as an input or output.
Output Type	Open collector with optional pull-up resistor.
Input Response	220nS 5 Volt pulse (filter caps removed)

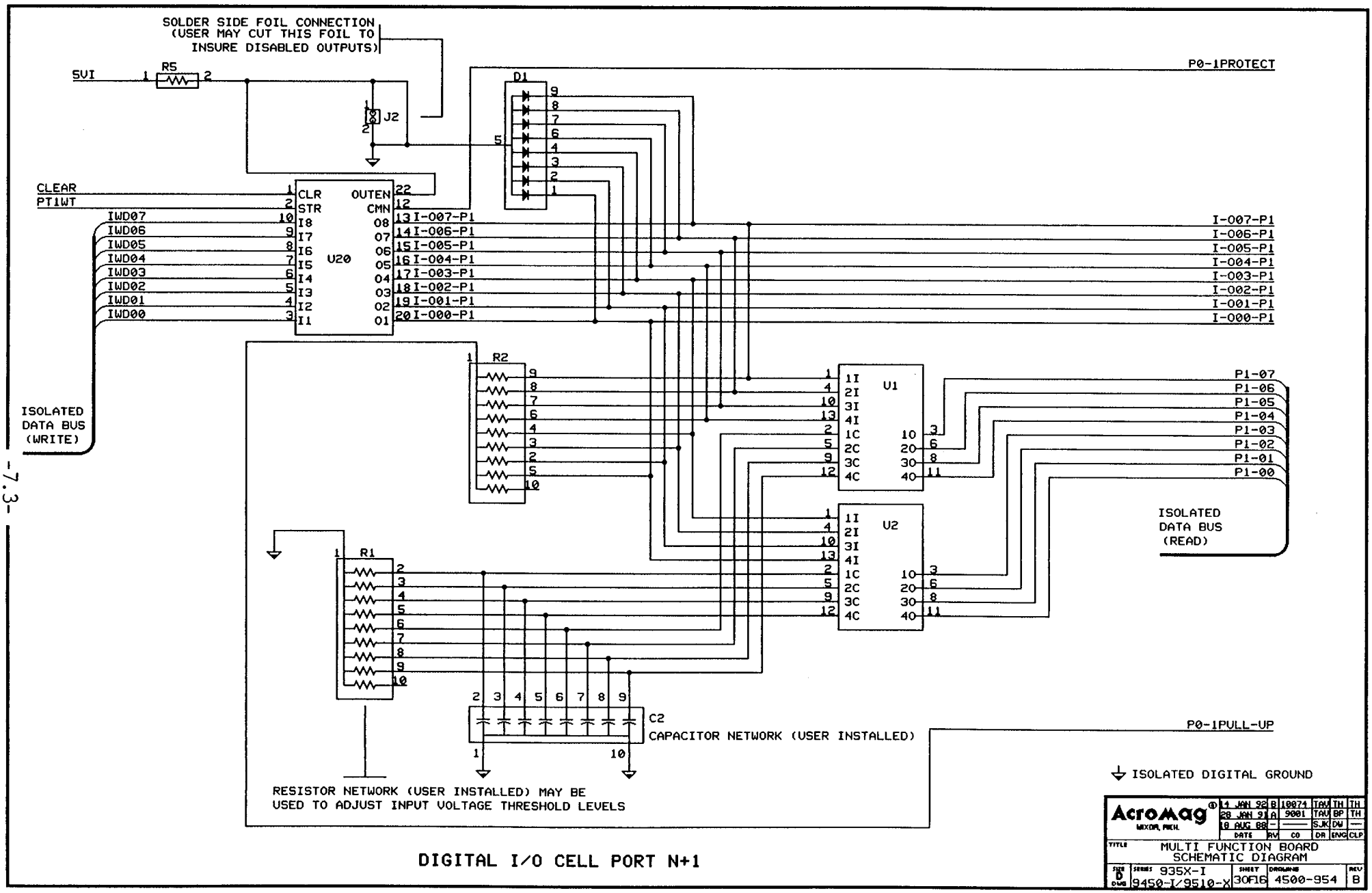
Output Voltage Range	0 to 30 V DC.
Output Current Sink	100 mA max.
Output Saturation Voltage @ 100 mA	1.1 V max., 0.9V typ.
Logic Compatibility	TTL, LSTTL, CMOS, and others.

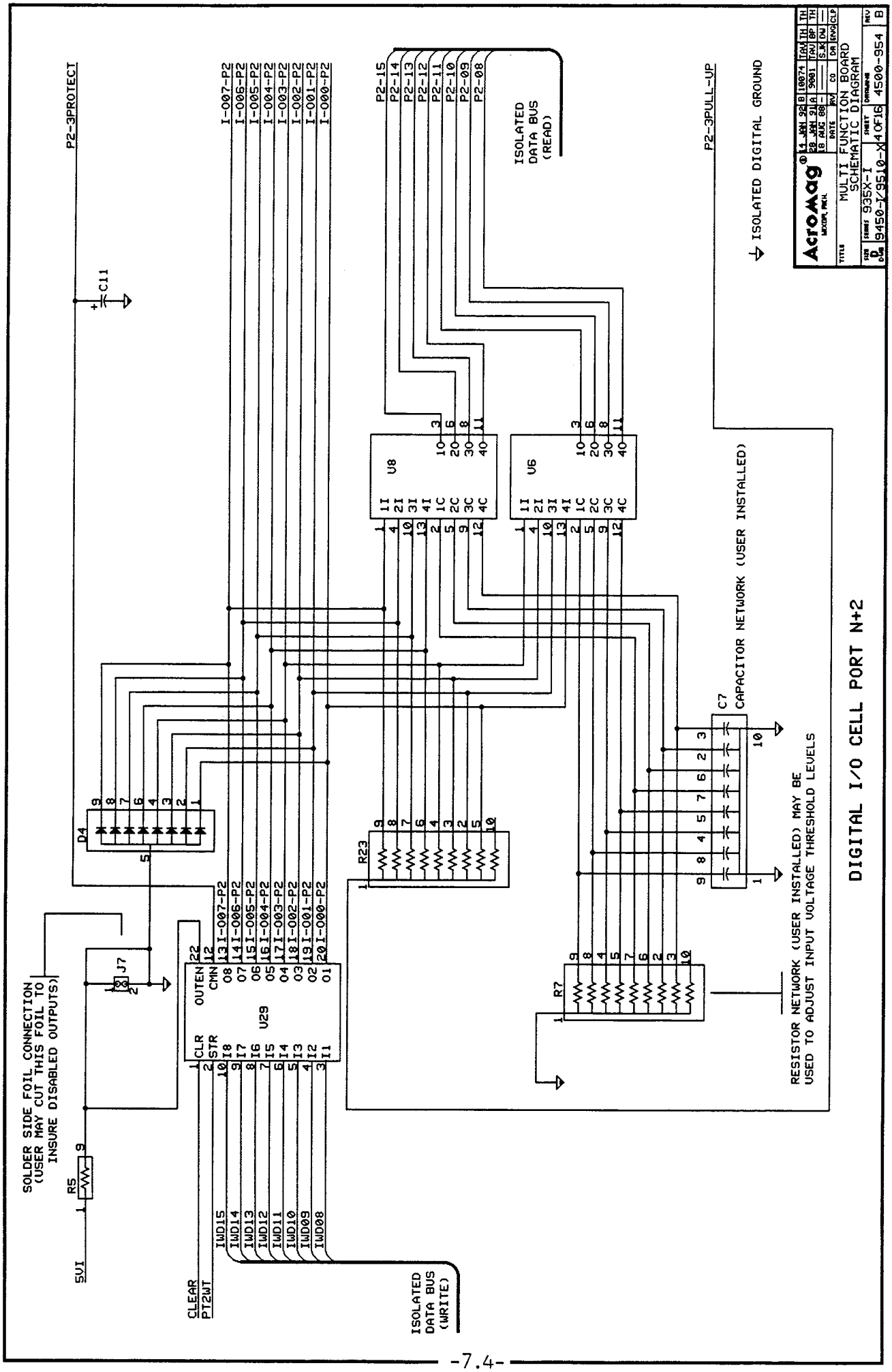
DATA BUS ISOLATION VOLTAGE (935X-I, 9450-I, & 9510-I)

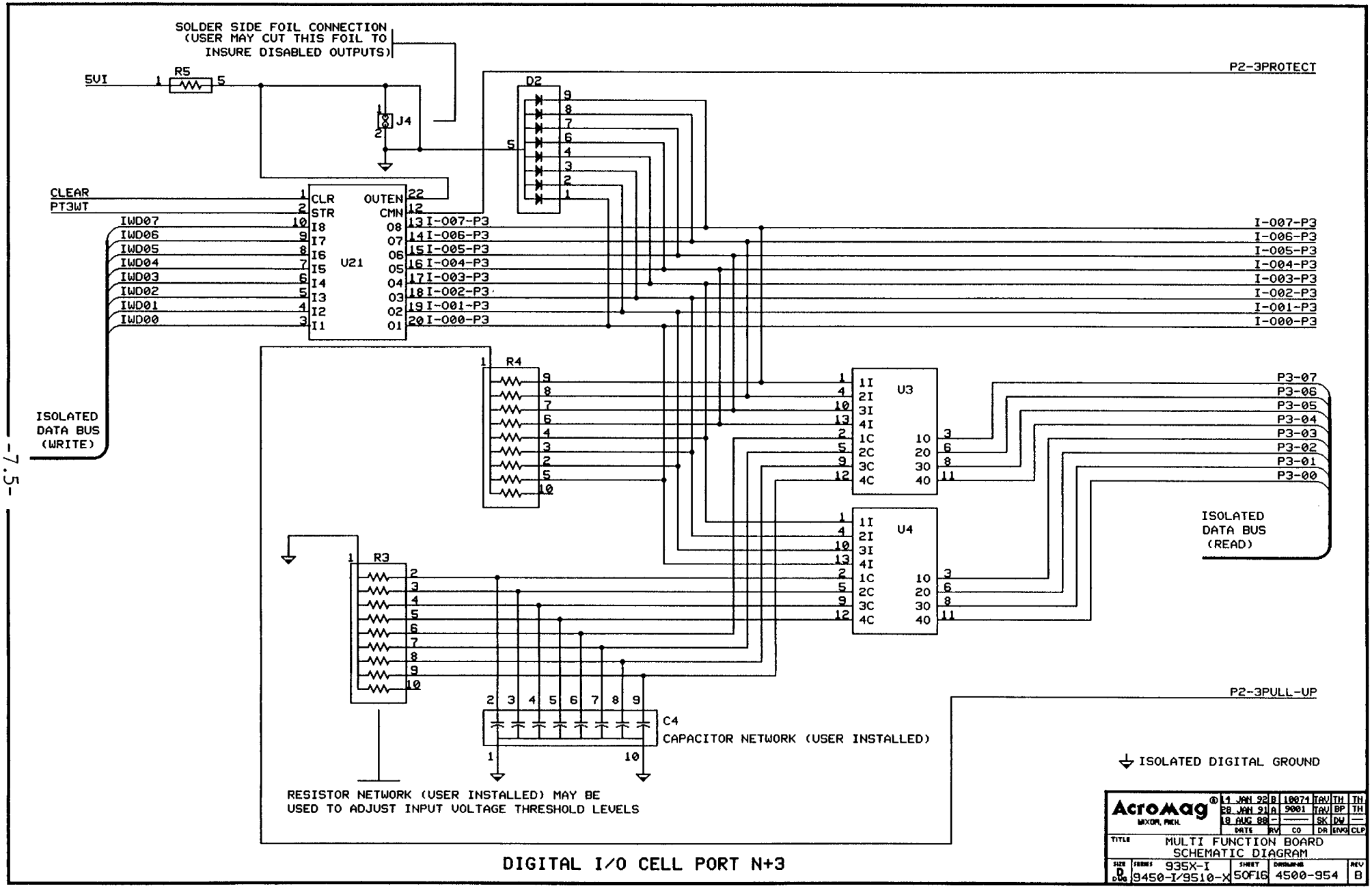
250V (60Hz) Between Computer Bus and the input/output circuitry.

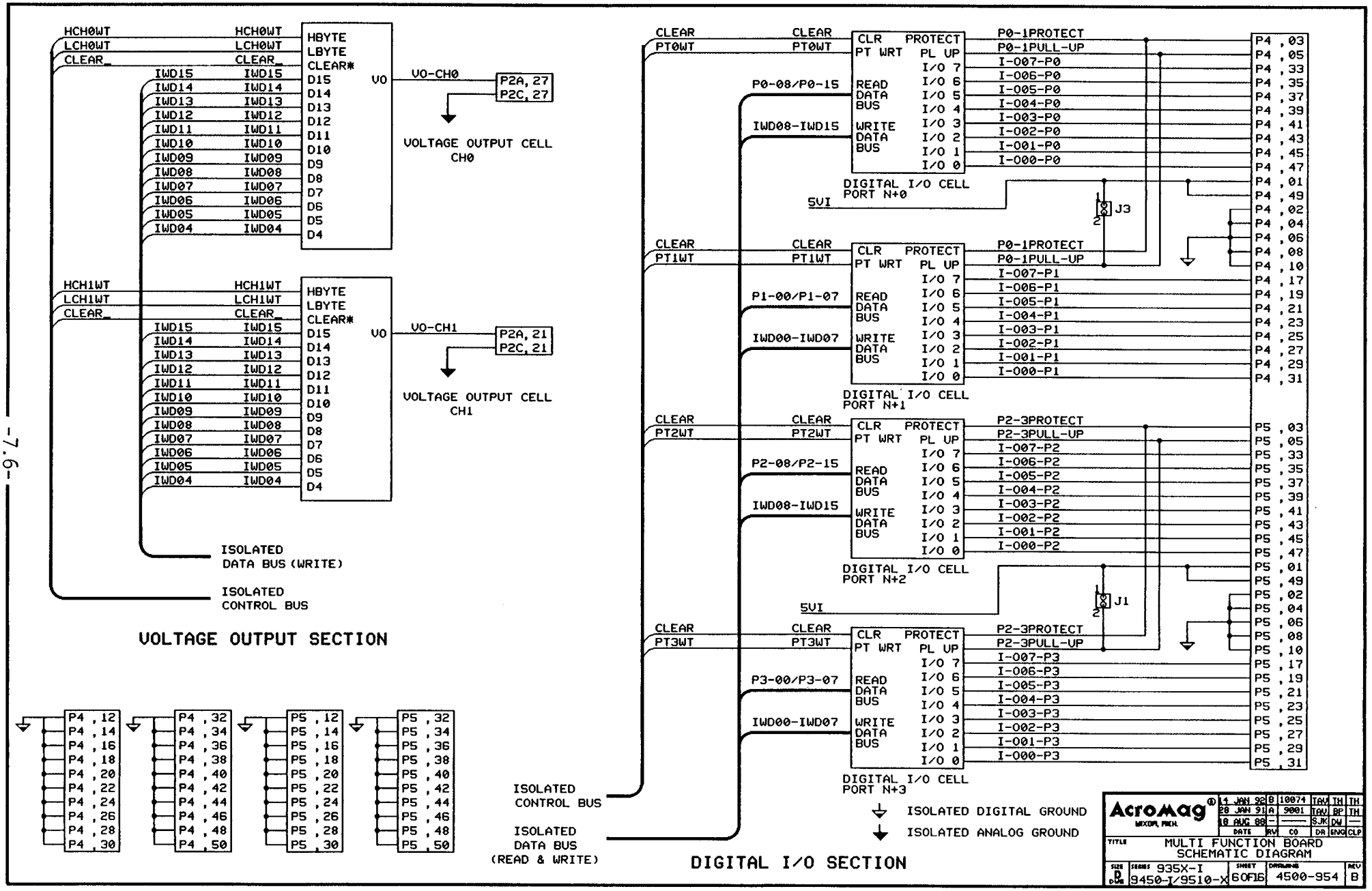


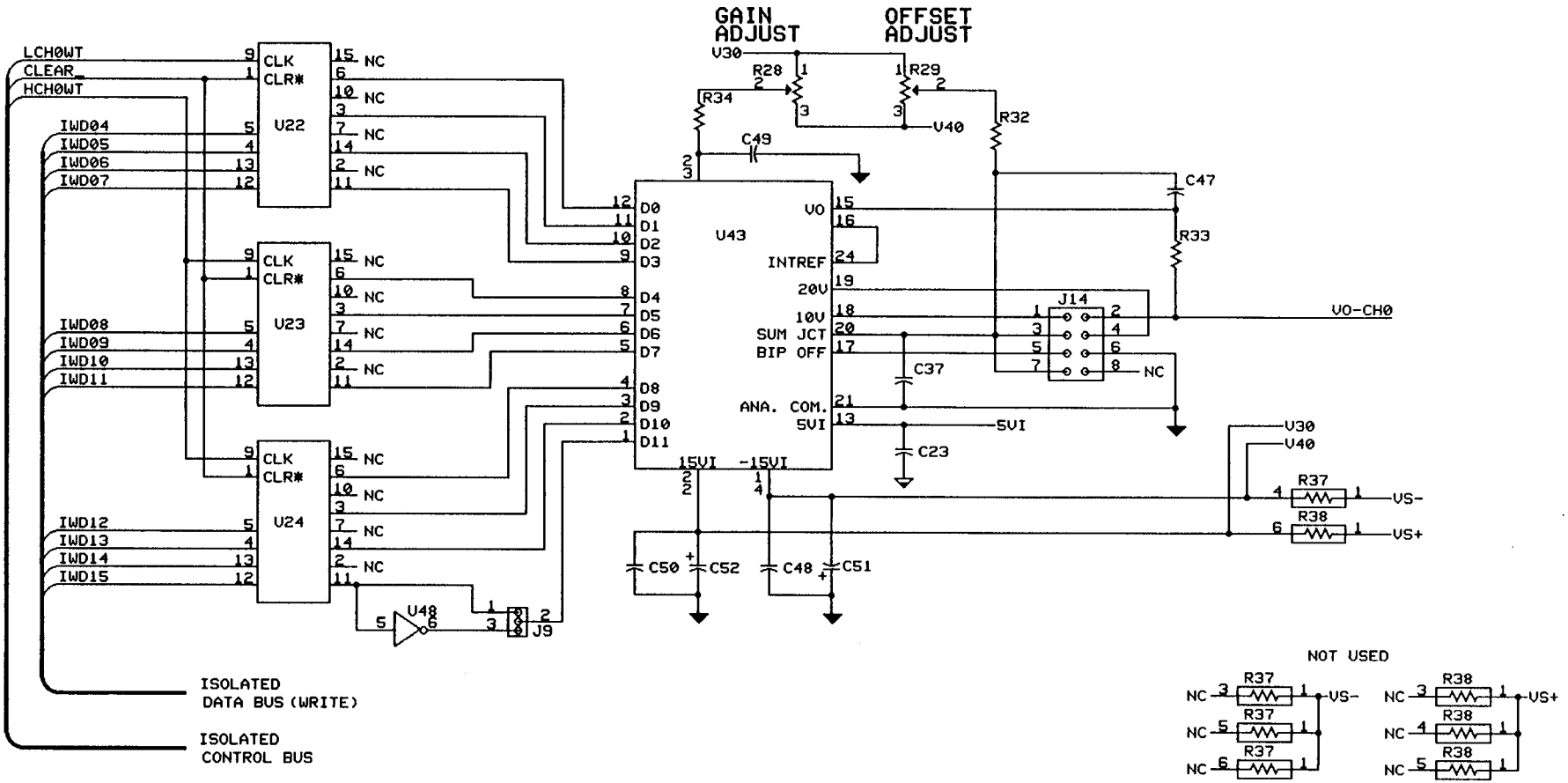








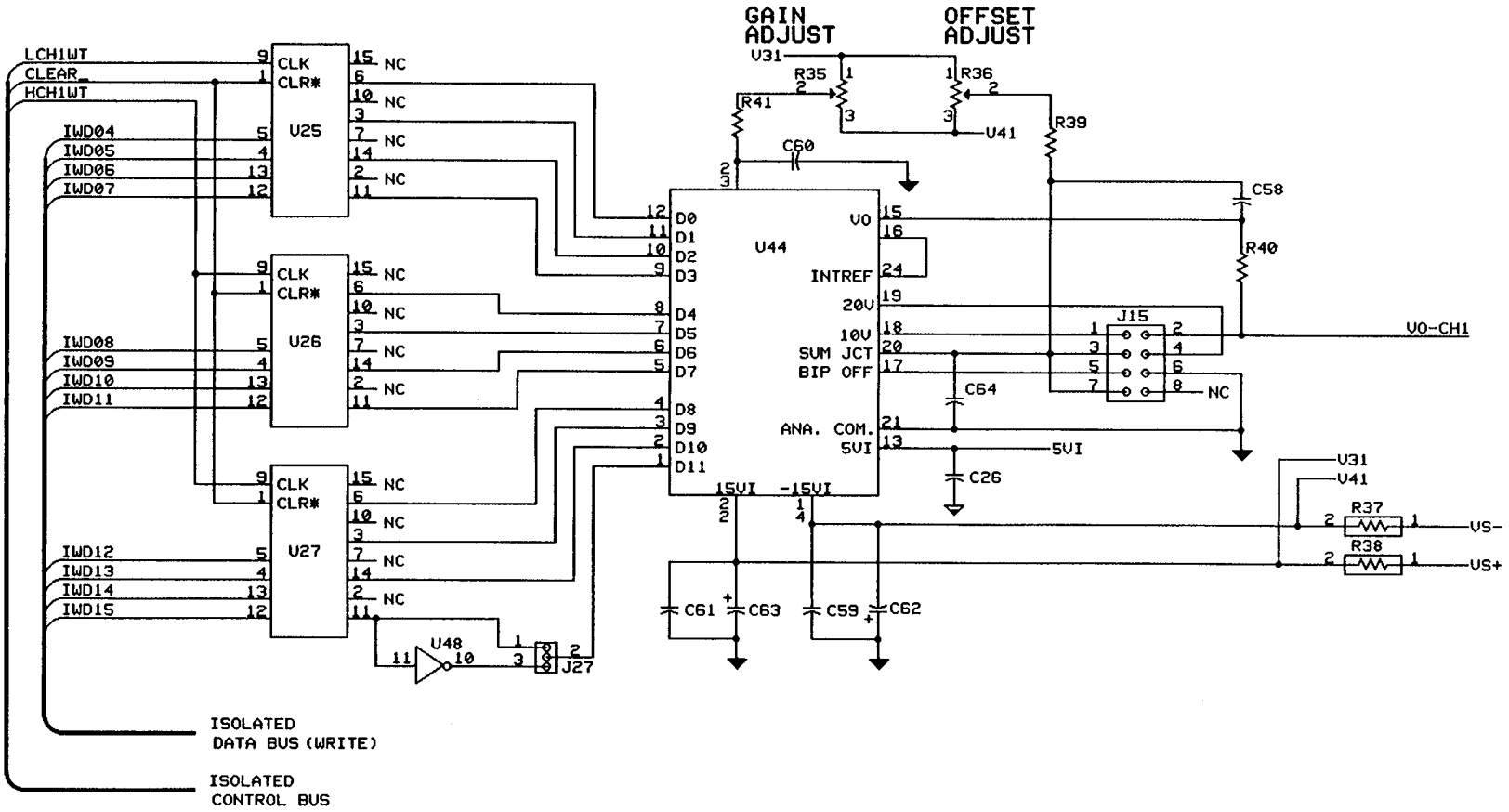




VOLTAGE OUTPUT CELL CHANNEL 0

Acromag WIXOM, MICH.	11 JAN 92	B	10071	TAV	TH	TH
	28 JAN 91	A	9001	TAV	BP	TH
	18 AUG 88	-	———	SJK	DW	—
	DATE	RV	CO	DR	ENG	CLP

TITLE: MULTI FUNCTION BOARD SCHEMATIC DIAGRAM				
SIZE D DWG	SERIES 935X-I 9450-I/9510-X	SHEET 7OF16	DRAWING 4500-954	REV B



VOLTAGE OUTPUT CELL CHANNEL 1

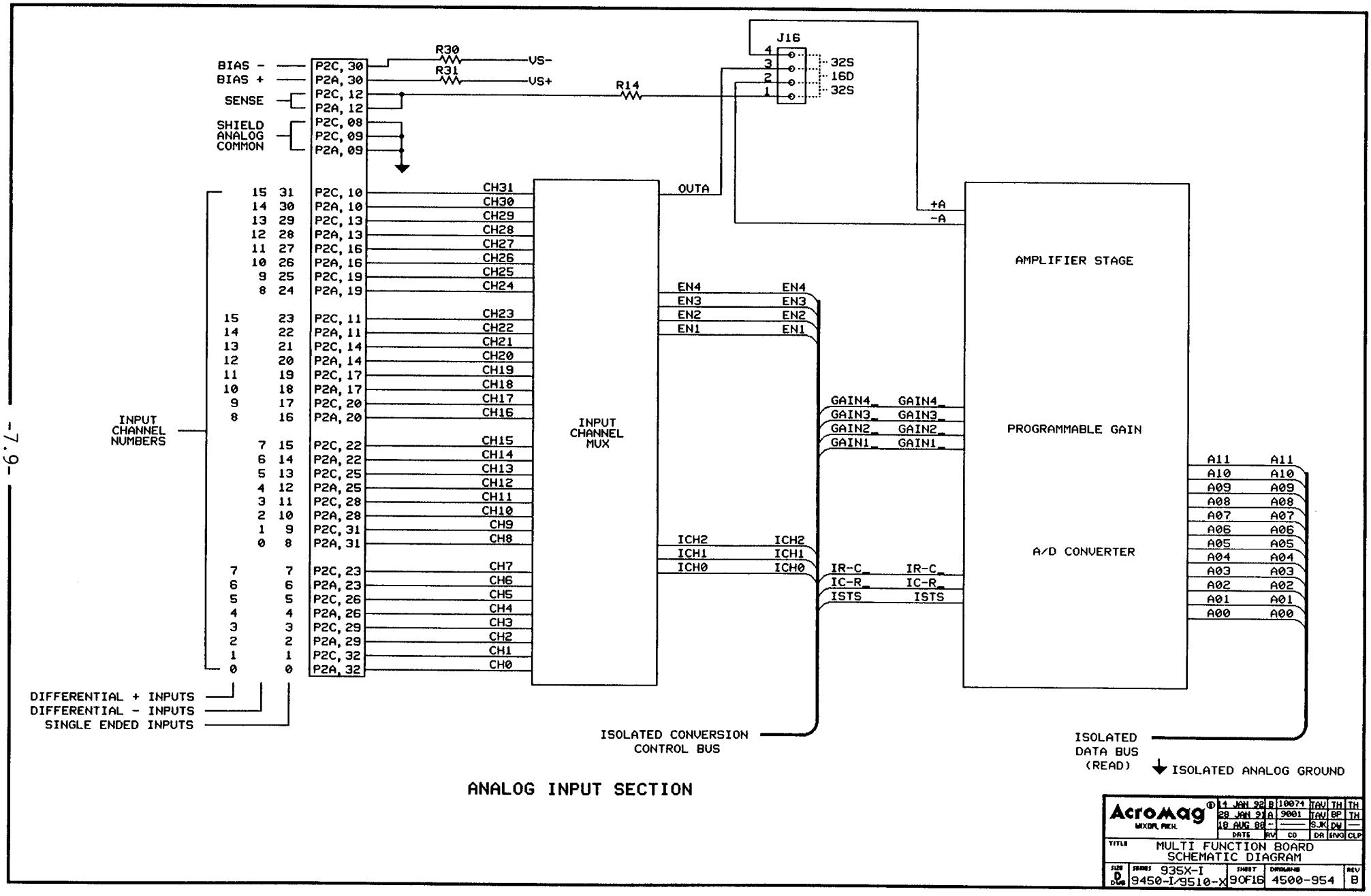
ISOLATED DIGITAL GROUND

ISOLATED ANALOG GROUND

AcroMag MIXOM, MICH.	14 JAN 92	B	10074	TAV	TH	TH
	28 JAN 91	A	9001	TAV	BP	TH
	10 AUG 88	-	——	S.K	DV	—
	DATE	REV	CO	DR	ENG	CLP

TITLE: MULTI FUNCTION BOARD SCHEMATIC DIAGRAM

SIZE	SERIES	SHEET	DRAWING	REV
D	935X-I 9450-I/9510-X	8OF16	4500-954	B

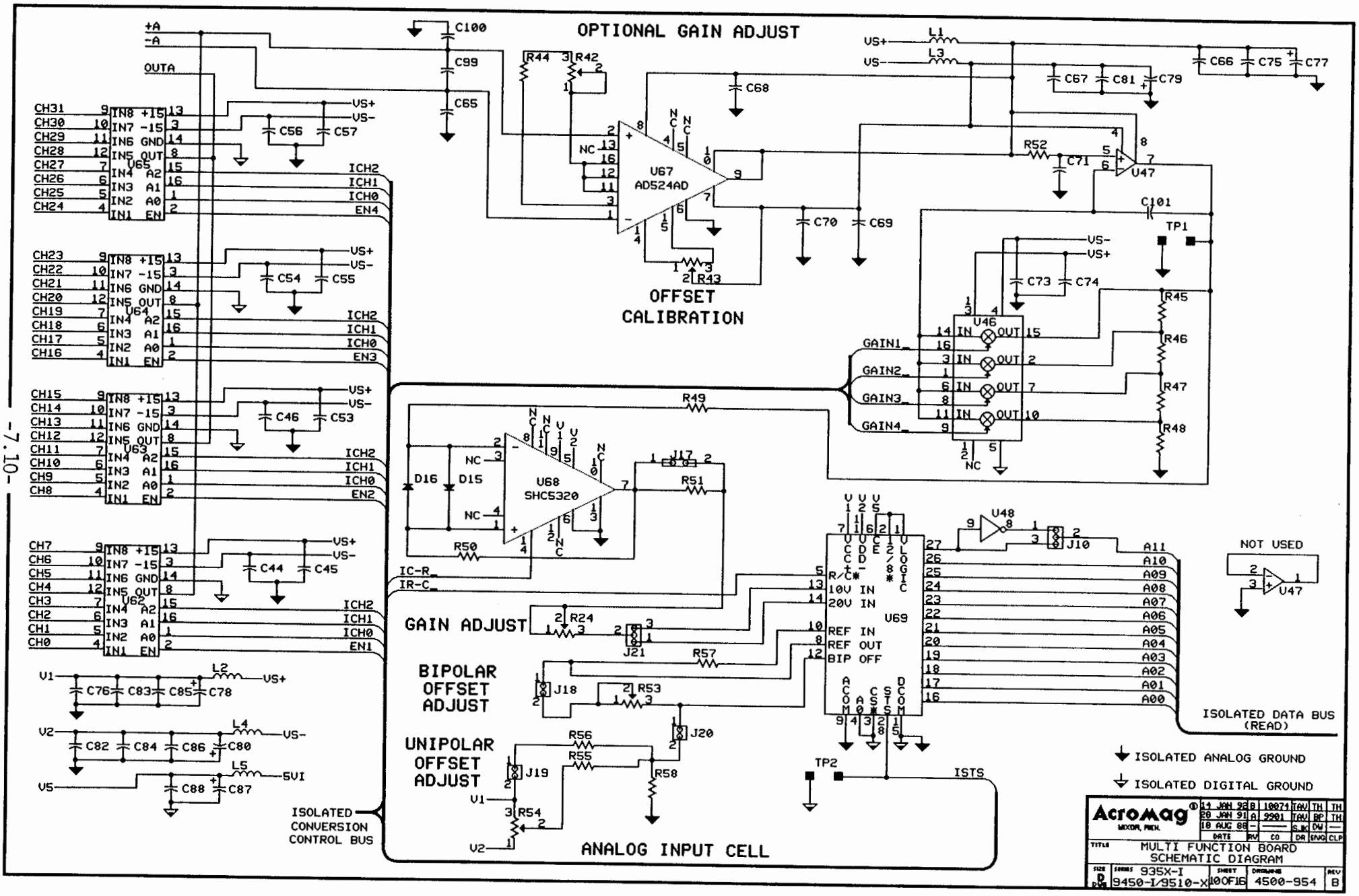


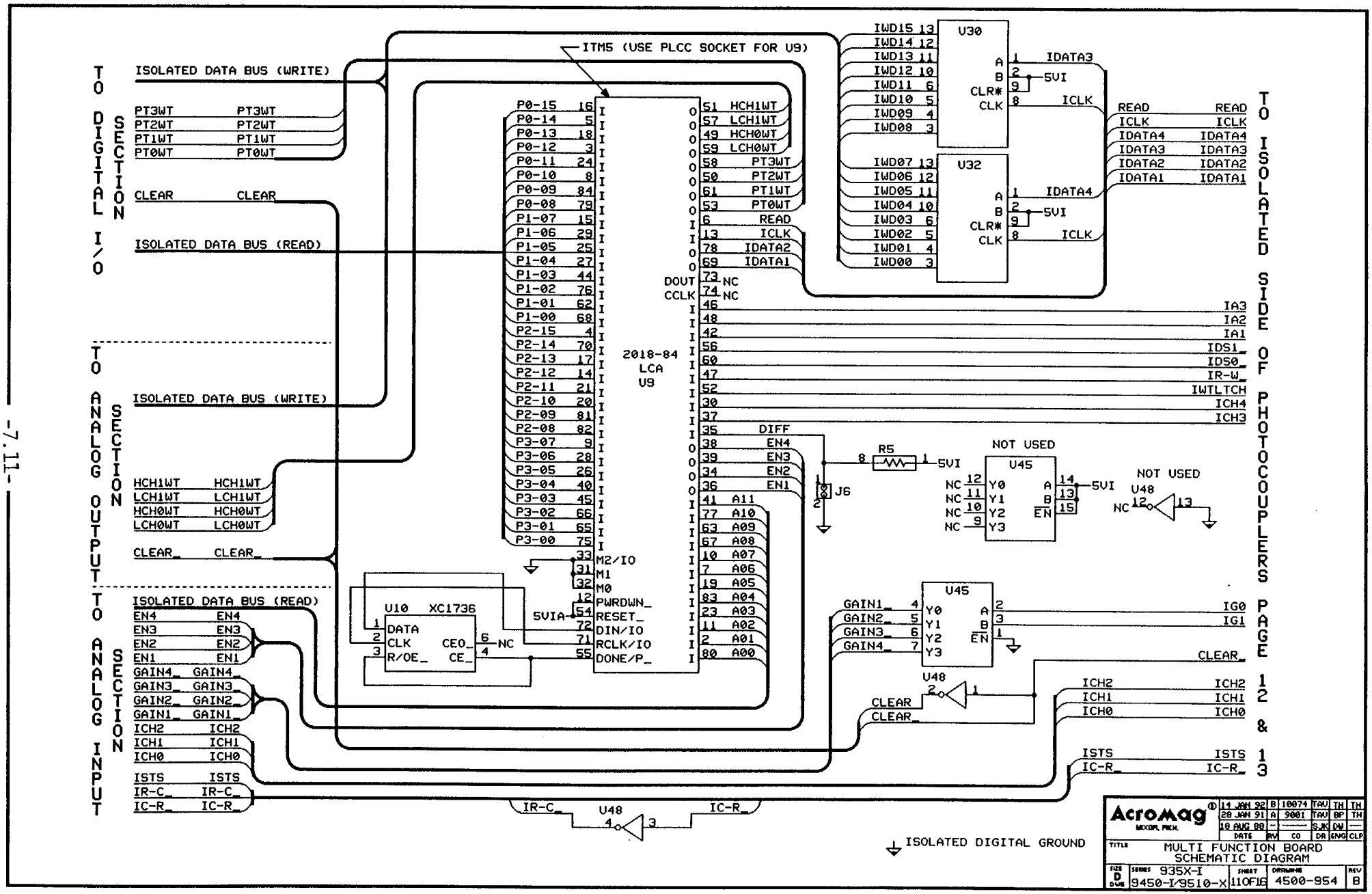
ANALOG INPUT SECTION

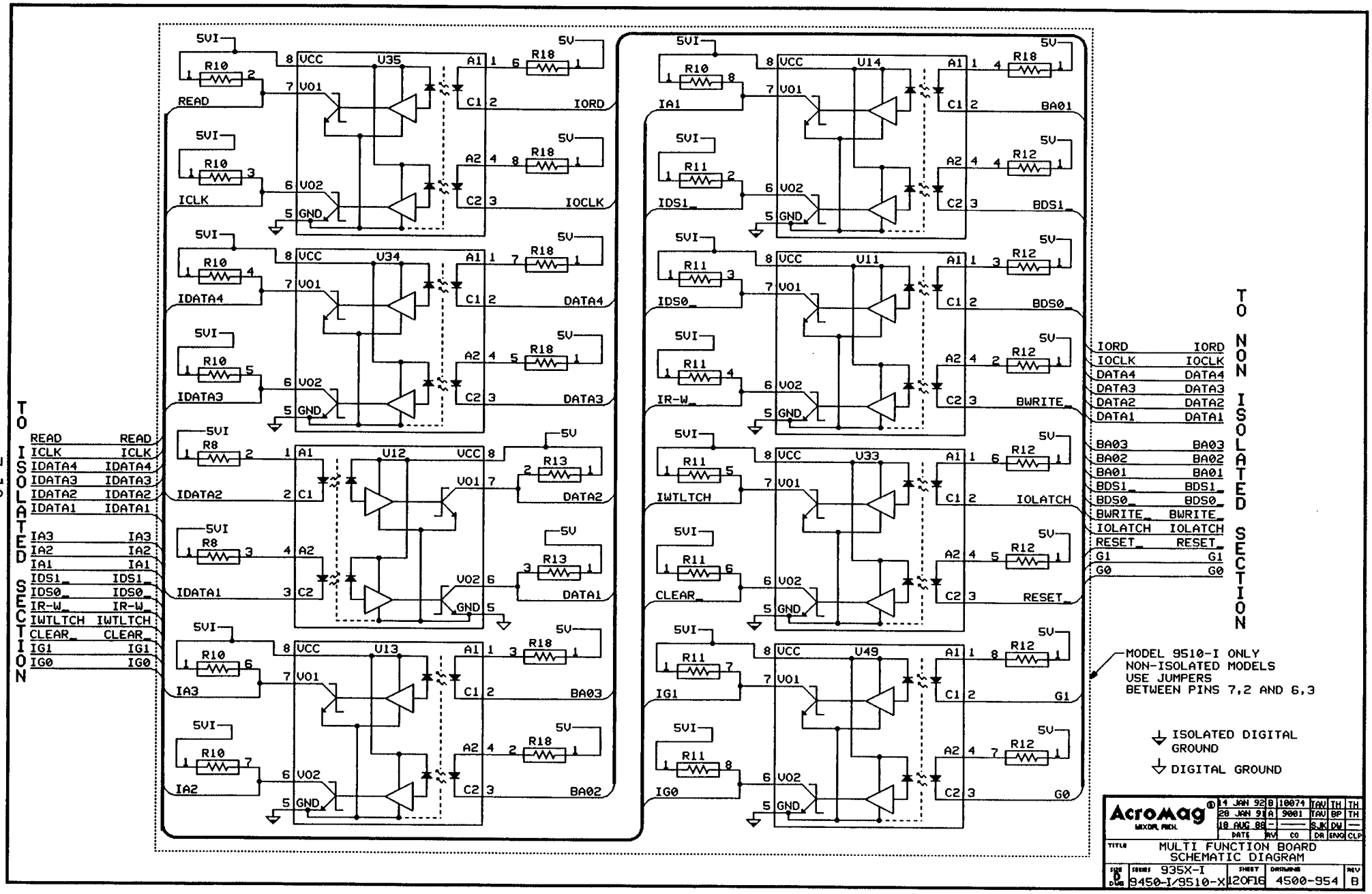
Acromag WIXOM, MICH.	14 JAN 92	B	10074	TAV	TH	TH
	28 JAN 91	A	9001	TAV	BP	TH
	18 AUG 88	-	——	SJK	DW	—
	DATE	RV	CO	DR	ENG	CLP

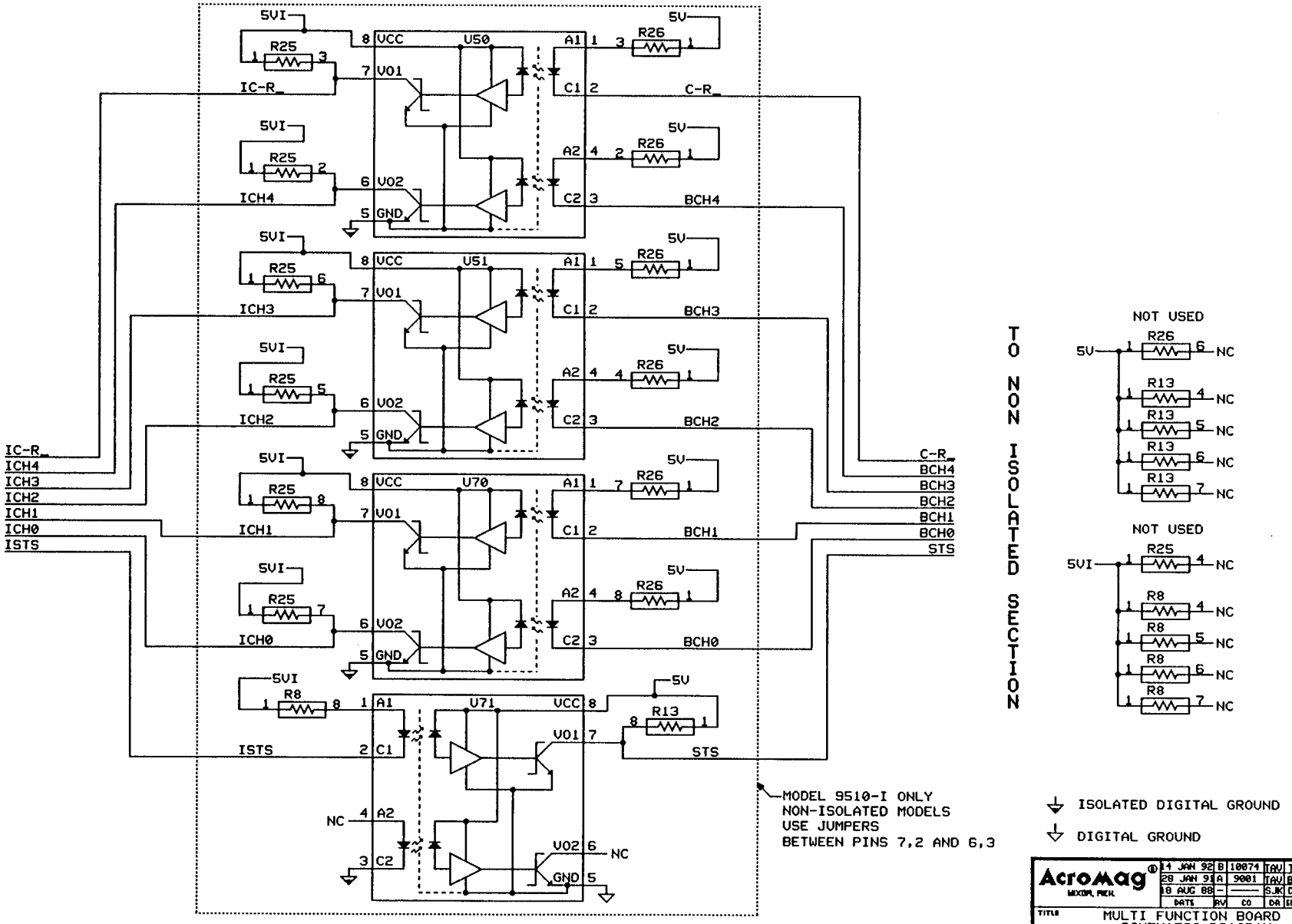
TITLE: MULTI FUNCTION BOARD SCHEMATIC DIAGRAM

SIZE D DWG	SERIES 935X-I 9450-I/9510-X	SHEET 9OF16	DRAWING 4500-954	REV B









AcroMag® MIXOM, MICH.	14 JAN 92	B	10074	TAV	TH	TH
	28 JAN 91	A	9001	TAV	BP	TH
	18 AUG 88	-	——	S.JK	DW	—
	DATE	RV	CO	DR	ENG	CLP

TITLE: MULTI FUNCTION BOARD SCHEMATIC DIAGRAM

SIZE	SERIES	SHEET	DRAWING	REV
D DWG	935X-I 9450-I/9510-X	13OF16	4500-954	B