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IP-ADC-8413
16 Channel 16 Bit ADC
User Manual

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CONTENTS

1. Description

The Hytec IP-ADC-8413 is an Industry Pack that provides 16 channels of simultaneously sampled analogue digitisation with the following characteristics:-

- 16 independent channels (one ADC per input)
- 16 bits resolution – 15 bits no missing codes
- Single full-scale trim for hardware gain adjustment.
- Software calibration by software driver possible using stored offset and gain parameters.
- True full differential inputs.
- +/-10V full-scale standard programmable to +/-5V full-scale resolution all inputs.
- Front-end instrumentation amplifiers can be factory set for gains of up to x1000.
- FIFO memories for single sample and triggered sample readout (256K external samples)
- +/10V Low offset error - +/- 2.5mV without software calibration. (+/-2LSBs after software calibration)
- +/-5V Low offset error - +/- 2.5mV without software calibration. (+/-4LSBs after software calibration)
- +/-5V Low gain error - +/- 0.5% FS without software calibration.(+/-4LSBs after software calibration)
- +/-10V Low gain error - +/- 0.5% FS without software calibration.(+/-2LSBs after software calibration)
- Low error drift - 2ppm per deg C
- High input impedance – 1Gohms.
- DC +/-50V overload
- Up to 150KHz sampling rate from an external clock (valid only on 32MHz IP clock frequency)
- Simultaneous sampling – 70ns aperture delay time. Uncertainty time and channel matching 3ns.
- System to plant isolation to 100V when externally powered by DC/DC converter option
- Serial number, PCB issue and firmware issue held in ID PROM
- 8/32MHz IP system clock operation
- EPICS driver support

2. Overall Specifications

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of channels:	16
ADC resolution:	16 bits
Diff. Non-linearity:	Monotonic to 15 bits (at 160kHz throughput)
Int. Non-linearity:	+/-2LSBs max.
Offset error:	+/-2.5mV uncorrected.
Offset drift:	+/-0.5ppm per deg C typical
Gain error:	+/-2LSB typical with correction operating over +/-5V and +10V to -9.5V ranges, +/-0.5% uncorrected
Gain drift:	+/-2 ppm per deg C typical
Range:	+/-10V full-scale (+ve input referred to –ve input).
Cross-talk:	+/-1LSB channel to channel for FS input on adjacent channel.
CMRR	Greater than 80dB
CMV:	+/-12V (Note Common mode plus signal voltage +/-12V maximum without DC/DC converter, 100V with converter fitted).
Over-voltage:	+/-50V.
Throughput:	150 KHz max from an external clock(valid only at 32MHz IP system clock)
Aperture time:	70ns typical (conversion start to hold) (16 register mode)
Conversion time:	3us (plus 1.6 us readout to register)
Bandwidth (-3dB):	100kHz (factory set – other cut-offs can be specified)
SNR:	-90dB at 1kHz typical
SINAD:	-90dB at 1kHz typical
Isolation:	100V via opto-isolators (if externally powered)
Data format:	16 bits two's complement, program to support straight binary (see data format)
Memory:	Buffer register for each ADC conversion and FIFO for all 16 conversions On-board FIFO:256K (16384 samples per 16 channels conversion values with half full and full flags
Power:	+5V @ 300mA typical, +/-12V @ 200mA typical from VME or 8912.

3. Operating Modes

There are three operating modes:-

1. Internal FIFO

When set to this mode, the conversions of the last sample are stored into an internal FIFO. To perform this operation the unit must first be armed, (set bit 15 in the CSR), then the inputs are sampled at the programmed clock rate or external clock rate, if selected. The internal FIFO can only store the last sample of all 16 channels; this will then generate an interrupt to indicate the FIFO is full and set the full flag high, F bit 0 CSR register. The FIFO may be readout as it is filling. The FIFO is cleared just before the next sample data is stored, therefore the FIFO only holds the last sampled result.

The purpose of this FIFO is to increase the speed of communication over IP using block transfer.

2. Register mode

In this mode the last sampled results of the inputs are stored in the ADC registers when armed, at the programmed clock rate or external clock rate, if selected. The ADC reading may be read at random from each addressed ADC register. Therefore, in this mode the user can chose which channels to monitor instead of all 16.

3. Triggered sampling

When the board is armed (set bit 15 in the CSR), and either a software or hardware trigger is detected, conversions are then stored in a 256K external FIFO. This FIFO can store up to 16,384 samples of each 16 channels. An interrupt request is generated when the FIFO is full and the full flag will be set TF bit 1 in the CSR register. The FIFO can be readout as it is filling. The data is stored in groups of 16, sample 1 of all 16 channels, then sample 2 of all 16 channels and so on up to sample 16384 of all 16 channels. Therefore, even though the data can be read out of the FIFO at any time, groups of 16 reads should be performed to keep the sample format intact.

4. Application Registers

There are eight (I/O) registers; the CSR, ACR, the clock rate, the interrupt vector value, Internal FIFO & External FIFO, External FIFO fullness counter, trigger sample number . There are also 16 ADC buffer registers.

4.1 Control & Status Register (CSR)

Control

Write Address: 0 hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	ET	ST	XC	EG	Ext	ETF	EF	EHF	x	DRE	RST	x	X	x	X

Status

Read Address: 0 hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ARM	ET	ST	XC	EG	Ext	ETF	EF	EHF	TE	DRE	RST	THF	FE	TF	F

X = Not Used

ARM When set, arm the ADCs and allows sampling of the inputs at the sample clock rate.

ET Enable trigger. If set allows external trigger or software trigger to route sampled conversions to the external FIFO. The action is synchronised to the first sample clock after the rising edge of trigger.

ST Software trigger. Allows trigger action to be initiated by software command and store the sampled conversions into the External FIFO

XC Enable External Clock

EG ***Enable Go. Please note not used on this version.***

Ext ***If set to 0, the internal 16MHz clock is used to derive the sample rate. If set to 1 the external clock (Strobe*) is used. Please note not used on this version.***

ETF When set enables interrupt IntReq0*, when the external FIFO is full.

EF When set enables interrupt IntReq0*, when the internal FIFO is full.

EHF When set enables interrupt IntReq0*, when the external FIFO is half full.

TE Set high when the external FIFO is empty

DRE DMA request. When set to 1 allows DMA request between the IP and carrier card. DMAREQ0 set when external FIFO is full and DMAREQ1 set when internal FIFO full.

RST Resets the internal and external FIFOs when set to 1.

THF Set high indicates that the external FIFO is half full.

FE Set high indicates that the internal FIFO is empty

TF Set high indicates that the external FIFO is full.

F Set high indicates that the internal FIFO is full. The FIFO contains the last ADC conversions. Cleared when FIFO is read completely or when a new conversion has finished

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4.2 Trigger Sample Number Register LS

Please note: At present this register is not available. Unused Register
Read/write Address: 2 hex
The least significant word of the sample number stored when trigger occurs

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

4.3 Trigger Sample Number Register MS

Please note: At present this register is not available. Unused Register
Read/write Address: 4 hex
The most significant word of the sample number stored when trigger occurs

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T31	T30	T29	T28	T27	T26	T25	T24	T23	T22	T21	T20	T19	T18	T17	T16

4.4 Internal Clock Rate

Read/write Address: 6 hex
The internal clock rate can be programmed for a variety of fixed clock frequencies. The clock rate register is a four bit register which enables codes 0 – 16 to generate frequencies of 1 Hz to 160kHz in multiples of 1,2,5 or 10. (E.g. 0=1Hz, 1=2Hz, 2=5Hz, 3=10Hz and so on, see table below) Each clock pulse will initiate simultaneous ADC conversions and store them into the internal FIFO and external FIFO when triggered.

Clock Rate Register Frequency Table

Register Value	Clock Rate Frequency	Register Value	Clock Rate Frequency
0	1Hz	9	1KHz
1	2Hz	10	2KHz
2	5Hz	11	5KHz
3	10Hz	12	10KHz
4	20Hz	13	20KHz
5	50Hz	14	50KHz
6	100Hz	15	100KHz
7	200Hz	16	160KHz
8	500Hz	--	--

Please note: The 160KHz operation is only valid on 32MHz IP clock frequencies. When the system clock is 8MHz only a maximum of 100KHz is available.

4.5 Vector

Read/write Address: 8 hex
The vector register is a 16 bit register which stores the interrupt vector value.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

4.6 ADC Internal FIFO

Read Address: a hex
Read the internal FIFO memory (16 conversions, one sample per channel).

Internal FIFO Memory Map			
Last Sample	**Channel Number**	**FIFO Location**	**FIFO Contents**
1	1	1	16 bit sample 1 of channel 1
1	2	2	16 bit sample 1 of channel 2
1	3	3	16 bit sample 1 of channel 3
1	4	4	16 bit sample 1 of channel 4
1	5	5	16 bit sample 1 of channel 5
1	6	6	16 bit sample 1 of channel 6
1	7	7	16 bit sample 1 of channel 7
1	8	8	16 bit sample 1 of channel 8
1	9	9	16 bit sample 1 of channel 9
1	10	10	16 bit sample 1 of channel 10
1	11	11	16 bit sample 1 of channel 11
1	12	12	16 bit sample 1 of channel 12
1	13	13	16 bit sample 1 of channel 13
1	14	14	16 bit sample 1 of channel 14
1	15	15	16 bit sample 1 of channel 15
1	16	16	16 bit sample 1 of channel 16

Internal FIFO Memory Map

4.7 ADC External FIFO

Read Address: c hex
Read the external FIFO memory (256K conversions, 16384 samples per channel).

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

4.7.1 External FIFO Format

The external FIFO when triggered will store 16384 16bit samples of each channel as shown in the figure below. Once the FIFO is triggered it will continue to store all 16384 samples of each channel until it is full.

External FIFO Memory Map			
Sample Numbe	***Channel Number***	***FIFO Location***	***FIFO Contents***
1	1	1	16 bit sample 1 of channel 1
1	2	2	16 bit sample 1 of channel 2
1	3	3	16 bit sample 1 of channel 3
1	4	4	16 bit sample 1 of channel 4
1	5	5	16 bit sample 1 of channel 5
1	6	6	16 bit sample 1 of channel 6
1	7	7	16 bit sample 1 of channel 7
1	8	8	16 bit sample 1 of channel 8
1	9	9	16 bit sample 1 of channel 9
1	10	10	16 bit sample 1 of channel 10
1	11	11	16 bit sample 1 of channel 11
1	12	12	16 bit sample 1 of channel 12
1	13	13	16 bit sample 1 of channel 13
1	14	14	16 bit sample 1 of channel 14
1	15	15	16 bit sample 1 of channel 15
1	16	16	16 bit sample 1 of channel 16
2	1	17	16 bit sample 2 of channel 1
2	2	18	16 bit sample 2 of channel 2
--	--	--	--
Repeat	Repeat	Repeat	Repeat
--	--	--	--
16384	13	262141	16 bit sample 16384 of channel 13
16384	14	262142	16 bit sample 16384 of channel 14
16384	15	262143	16 bit sample 16384 of channel 15
16384	16	262144	16 bit sample 16384 of channel 16

External FIFO Memory Map

The FIFO may be readout as it is filling. The data is stored in groups of 16, sample 1 of all 16 channels, then sample 2 of all 16 channels and so on up to sample 16384 of all 16 channels. Therefore, even though the data can be read out of the FIFO at any time, groups of 16 reads should be performed to keep the sample format intact.

4.8 External FIFO Fullness Counter

Read Address: e hex

16 bit counter which count conversions as they are entered / read from the external FIFO. At the end of each trigger and readout sequence to empty the FIFO, the value in the registers should be zero. When the FIFO is full (TF) the counter will display 16384 Dec 4000Hex for 256K.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
CNT 15	CNT 14	CNT 13	CNT 12	CNT 11	CNT 10	CNT 9	CNT 8	CNT 7	CNT 6	CNT 5	CNT 4	CNT 3	CNT 2	CNT 1	CNT 0

4.9 ADC Registers

There are sixteen ADC buffer registers (addresses 10hex – 2Ehex) which store the last sampled conversions and may be read at any time. The channel order is channel 1 at address 10hex to channel 16 at address 2E. Additionally there are two additional ADC registers to monitor the 0V Reference (address 30Hex) and 2.5V Reference (address 32Hex).
All ADC registers are updated simultaneously

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
MSB															LSB

4.9.1 Data Format

The ADC data can be configured to straight binary or 2's complement format dependent upon 2C bit 3 of the Auxiliary Control Register. Set this bit to 1 for straight binary and 0 for 2's complement operation.

The ADC range can also be set to +/-10V or +/-5V dependent upon bit 0 of the Auxiliary Control Register RGE. Set this bit to 1 for +/-5V and set to 0 for +/-10V operation.

At switch on the default will be 2's complement and +/-10V operation

Range (RGE) bit from ACR Register (34hex)	2's Complement (2C) bit from ACR Register (34hex)	Range	ADC Value Negative Full Scale	ADC Value Positive Full Scale
0	0	-10V to +10V	8000h	7FFFh
0	1	-10V to +10V	0000h	FFFFh
1	0	-5V to +5V	8000h	7FFFh
1	1	-5V to +5V	0000h	FFFFh

Data Representation dependent upon gain and format

Read Address: 10hex – 32hex
The first sixteen ADC buffer registers store the last sample conversions and may be read at any time. The seventeenth is used to monitor the 0V reference and the eighteenth is used to monitor the 2.5V reference or in table form…

Register Address (Hex)	Description	Register Address (Hex)	Description
10	ADC 0	22	ADC 9
12	ADC 1	24	ADC 10
14	ADC 2	26	ADC 11
16	ADC 3	28	ADC 12
18	ADC 4	2A	ADC13
1A	ADC 5	2C	ADC 14
1C	ADC 6	2E	ADC 15
1E	ADC 7	30	0V Reference
20	ADC 8	32	2.5V Reference

4.10 Auxiliary Control Register (ACR)

This register is reset to all zeros at switch on and must be set for correct operation

Control

Read/write Address: 34hex

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	X	PG2	PG1	PG0	2C	N/S	X	RGE

X = Not Used

RGE Sets the range of the ADCs. 0 - +/- 10V and 1 - +/-5V.
N/S 0 – Standby Mode, 1 – Normal Operation.
2C 0 – ADC Values in 2's Complement (default), 1 – ADC Values 0000 (Neg FS)-FFFF (Pos FS).
PG0 Bit 0 of ID PROM Paging.*
PG1 Bit 1 of ID PROM Paging.*
PG2 Bit 2 of ID PROM Paging.*

*Since some carrier devices only support 64 locations in the ID PROM, and the 8413 have up to 80 16-bit calibration values. Therefore it is required to page the ID PROM, these two bits are used to switch between pages of the ID PROM.

PG2	PG1	PG0	PAGE	NOTES
0	0	0	0 (Default)	Normal VITA4 format for ID PROM.
0	0	1	1	Calibration Values for +/-10V Scan ADC Channel 0-5.
0	1	0	2	Calibration Values for +/-10V Scan ADC Channel 6-11.
0	1	1	3	Calibration Values for +/-10V Scan ADC Channel 12-16.
1	0	0	4	Calibration Values for +/-5V Scan ADC Channel 0-5.
1	0	1	5	Calibration Values for +/-5V Scan ADC Channel 6-11.
1	1	0	6	Calibration Values for +/-5V Scan ADC Channel 12-16.

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5. ADC Operation

5.1 FIFOs and Interrupts

To initiate a conversion the unit must first be armed, set bit 15 ARM in the CSR register, and then the rising edge of the sample clock causes conversions of the 16 ADCs. The sample clock can be the programmed clock, 1Hz to 160 KHz, or it can be an external clock at any frequency up to a maximum rate of 160 KHz. To select the external clock, set bit 12 of the CSR register XC high. The resulting conversion fills the internal FIFO and generates an interrupt IntReq0* to the carrier board to indicate the FIFO is full, if the enable interrupt EF has been set, CSR register bit 8. The internal FIFO can only store the last sample of all 16 channels; this will then be cleared just before the next sample has been converted by the ADCs and then this sample will be stored. The FIFO may be readout as it is filling. Thus throughput is limited by the block read time.

At the maximum sample clock rate of 160 KHz normal IP reads will not be able to read out the internal FIFO contents before the next rising edge of the next sample clock writes in the new converted results. At 160 KHz there is only 6.25uS before the FIFO is updated, this is running with a system clock of 32MHz. The only way to read at this frequency reliably is block transfer mode.

To initiate conversion to be stored to the external FIFO, firstly again the unit must be armed and then either the software or hardware trigger must be set. Once the external hardware or software triggered has been detected, conversions are then written to the external FIFO which has space for 16384 samples per 16 channels. When this has been filled it will indicate Full and generate and interrupt IntReq0*, if the ETF bit 9 of the CSR has been enabled. Similarly the external FIFO will generate an interrupt IntReq0* when the FIFO is half full, if the EHF bit 7 of the CSR has been enabled. Complete readout of external FIFO will restore it to an empty state as indicated by FIFO empty. The FIFOs may be reset at any time by setting the reset bit (Bit4) in the CSR high.

5.2 DMA Requests

In this mode the unit can perform DMA requests when the internal or external FIFOs are full. When DRE bit 5 in the CSR register is set high, if the internal FIFO is full DMARequest0 is set and if the external FIFO is full the DMARequest1 is set.

5.3 Software Trigger

The unit can be triggered by a software trigger by writing a ‘1’ to the Software Trigger (ST) bit 13 and enabling the trigger ET bit 14 of the CSR register. The trigger state remains asserted conversions are steered to the external FIFO until the ST bit is cleared.

5.4 External Hardware Trigger

To trigger the unit from an external hardware source, firstly the enable trigger ET bit 14 of the CSR register must be set high. Then connect the external signal to XTRIG on the I/O connector. (See the I/O connector section for the appropriate pins). When the external trigger is high the conversions will be stored in the External FIFO. When low the conversions are halted to the external FIFO

5.5 External Clock

To use an external source for the sample clock, set the XC bit 12 of the CSR register high. Then connect the external clock signal to XCLK on the I/O connector. (See the I/O connector section for the appropriate pins). The maximum clock rate is 160 KHz. This clock is then the sample clock rate.

6. ID PROM

As some IP Carrier Cards only support 64 16-Bit locations in the ID Space, we page the ID Space to provide extra space for ADC calibration data. To switch between pages, there are control bits in the Auxiliary Control Register (ACR). The default setting is the standard 'VITA4' layout, but there are additional pages as shown below…

PG2	PG1	PG0	PAGE	NOTES
0	0	0	0 (Default)	Normal VITA4 format for ID PROM.
0	0	1	1	Calibration Values for +/-10V Scan ADC Channel 0-5.
0	1	0	2	Calibration Values for +/-10V Scan ADC Channel 6-11.
0	1	1	3	Calibration Values for +/-10V Scan ADC Channel 12-16.
1	0	0	4	Calibration Values for +/-5V Scan ADC Channel 0-5.
1	0	1	5	Calibration Values for +/-5V Scan ADC Channel 6-11.
1	1	0	6	Calibration Values for +/-5V Scan ADC Channel 12-16.

Normal VITA format for ID PROM is:-

Base+80	ASCII 'VI'	5649h	
Base+82	ASCII 'TA'	5441h	
Base+84	ASCII '4 '	3420h	
Base+86	Hytec ID high byte	0080h	
Base+88	Hytec ID low word	0300h	
Base+8A	Model number	8413h	
Base+8C	Revision	0101h	This shows PCB Iss 1 Xilinx V1
Base+8E	Reserved	0000h	
Base+90	Driver ID	0000h	
Base+92	Driver ID	0000h	
Base+94	Flags	0002h	
Base+96	No of bytes used	001Ah	
Base+98	Cal Type	xxxxh	0 = No Calibration, 1,2 = Calibration factors Stored.
Base+9A	Serial Number	xxxxdec	
Base+9C	Not used	xxxxh	
Base+9E	WLO	5555h	

7. Calibration

The type of calibration factors held in the ID PROM are specified by the Cal Type held at Base+98 in the ID PROM:-

0 = No Calibration factors held in ID PROM.
1 = 3 Point Calibration factors Stored in ID PROM.
2 = 5 Point Calibration factors Stored in ID PROM.

The Calibration Factors are held in the ID PROM pages 1 to 3 as shown the following Tables and as described in SECTION 7. These are the stored ADC values, derived from reading the ADC at the following specified voltages…

Value	Calibration Voltage
nFS	-10V
nHS	-5V
zero	0V
pHS	+5V
pFS	+10V

These values can then be used in the following equations to correct the offset and gain errors of the individual cannels of the ADC8413 IP card.

$$rawval > pHS$$
$$CalVal = \frac{(rawval - pHS) \times 0x3FF8}{pFS - pHS} + BFF8$$

$$zero < rawval \leq pHS$$
$$CalVal = \frac{(rawval - zero) \times 0x3FF8}{pHS - zero} + 8000$$

$$zero => rawval \geq nHS$$
$$CalVal = \frac{(rawval - zero) \times 0x3FF9}{zero - nHS} + 8000$$

$$rawval < nHS$$
$$CalVal = \frac{(rawval - nHS) \times 0x3FF9}{nHS - nFS} + 4007$$

7.1 ID Page 1 (PG2 = 0, PG1 = 0, PG0 = 1) +/-10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 2
Base+80	ADC0 Cal data nFS
Base+82	ADC0 Cal data nHS
Base+84	ADC0 Cal data Zero
Base+86	ADC0 Cal data pHS
Base+88	ADC0 Cal data pFS
Base+8A	ADC1 Cal data nFS
Base+8C	ADC1 Cal data nHS
Base+8E	ADC1 Cal data Zero
Base+90	ADC1 Cal data pHS
Base+92	ADC1 Cal data pFS
Base+94	ADC2 Cal data nFS
Base+96	ADC2 Cal data nHS
Base+98	ADC2 Cal data Zero
Base+9A	ADC2 Cal data pHS
Base+9C	ADC2 Cal data pFS
Base+9E	ADC3 Cal data nFS
Base+A0	ADC3 Cal data nHS
Base+A2	ADC3 Cal data Zero
Base+A4	ADC3 Cal data pHS
Base+A6	ADC3 Cal data pFS
Base+A8	ADC4 Cal data nFS
Base+AA	ADC4 Cal data nHS
Base+AC	ADC4 Cal data Zero
Base+AE	ADC4 Cal data pHS
Base+B0	ADC4 Cal data pFS
Base+B2	ADC5 Cal data nFS
Base+B4	ADC5 Cal data nHS
Base+B6	ADC5 Cal data Zero
Base+B8	ADC5 Cal data pHS
Base+BA	ADC5 Cal data pFS

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data nHS - Negative Half Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.2 ID Page 2 (PG2 = 0, PG1 = 1, PG0 = 0) +/-10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 2
Base+80	ADC6 Cal data nFS
Base+82	ADC6 Cal data nHS
Base+84	ADC6 Cal data Zero
Base+86	ADC6 Cal data pHS
Base+88	ADC6 Cal data pFS
Base+8A	ADC7 Cal data nFS
Base+8C	ADC7 Cal data nHS
Base+8E	ADC7 Cal data Zero
Base+90	ADC7 Cal data pHS
Base+92	ADC7 Cal data pFS
Base+94	ADC8 Cal data nFS
Base+96	ADC8 Cal data nHS
Base+98	ADC8 Cal data Zero
Base+9A	ADC8 Cal data pHS
Base+9C	ADC8 Cal data pFS
Base+9E	ADC9 Cal data nFS
Base+A0	ADC9 Cal data nHS
Base+A2	ADC9 Cal data Zero
Base+A4	ADC9 Cal data pHS
Base+A6	ADC9 Cal data pFS
Base+A8	ADC10 Cal data nFS
Base+AA	ADC10 Cal data nHS
Base+AC	ADC10 Cal data Zero
Base+AE	ADC10 Cal data pHS
Base+B0	ADC10 Cal data pFS
Base+B2	ADC11 Cal data nFS
Base+B4	ADC11 Cal data nHS
Base+B6	ADC11 Cal data Zero
Base+B8	ADC11 Cal data pHS
Base+BA	ADC11 Cal data pFS

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data nHS - Negative Half Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.3 ID Page 3 (PG2 = 0, PG1 = 1, PG0 = 1) +/-10V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 2
Base+80	ADC12 Cal data nFS
Base+82	ADC12 Cal data nHS
Base+84	ADC12 Cal data Zero
Base+86	ADC12 Cal data pHS
Base+88	ADC12 Cal data pFS
Base+8A	ADC13 Cal data nFS
Base+8C	ADC13 Cal data nHS
Base+8E	ADC13 Cal data Zero
Base+90	ADC13 Cal data pHS
Base+92	ADC13 Cal data pFS
Base+94	ADC14 Cal data nFS
Base+96	ADC14 Cal data nHS
Base+98	ADC14 Cal data Zero
Base+9A	ADC14 Cal data pHS
Base+9C	ADC14 Cal data pFS
Base+9E	ADC15 Cal data nFS
Base+A0	ADC15 Cal data nHS
Base+A2	ADC15 Cal data Zero
Base+A4	ADC15 Cal data pHS
Base+A6	ADC15 Cal data pFS
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data nHS - Negative Half Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.4 ID Page 4 (PG2 = 1, PG1 = 0, PG0 = 0) +/-5V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 2
Base+80	ADC0 Cal data nFS
Base+82	ADC0 Cal data nHS
Base+84	ADC0 Cal data Zero
Base+86	ADC0 Cal data pHS
Base+88	ADC0 Cal data pFS
Base+8A	ADC1 Cal data nFS
Base+8C	ADC1 Cal data nHS
Base+8E	ADC1 Cal data Zero
Base+90	ADC1 Cal data pHS
Base+92	ADC1 Cal data pFS
Base+94	ADC2 Cal data nFS
Base+96	ADC2 Cal data nHS
Base+98	ADC2 Cal data Zero
Base+9A	ADC2 Cal data pHS
Base+9C	ADC2 Cal data pFS
Base+9E	ADC3 Cal data nFS
Base+A0	ADC3 Cal data nHS
Base+A2	ADC3 Cal data Zero
Base+A4	ADC3 Cal data pHS
Base+A6	ADC3 Cal data pFS
Base+A8	ADC4 Cal data nFS
Base+AA	ADC4 Cal data nHS
Base+AC	ADC4 Cal data Zero
Base+AE	ADC4 Cal data pHS
Base+B0	ADC4 Cal data pFS
Base+B2	ADC5 Cal data nFS
Base+B4	ADC5 Cal data nHS
Base+B6	ADC5 Cal data Zero
Base+B8	ADC5 Cal data pHS
Base+BA	ADC5 Cal data pFS

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data nHS - Negative Half Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.5 ID Page 5 (PG2 =1, PG1 = 0, PG0 = 1) +/-5V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 2
Base+80	ADC6 Cal data nFS
Base+82	ADC6 Cal data nHS
Base+84	ADC6 Cal data Zero
Base+86	ADC6 Cal data pHS
Base+88	ADC6 Cal data pFS
Base+8A	ADC7 Cal data nFS
Base+8C	ADC7 Cal data nHS
Base+8E	ADC7 Cal data Zero
Base+90	ADC7 Cal data pHS
Base+92	ADC7 Cal data pFS
Base+94	ADC8 Cal data nFS
Base+96	ADC8 Cal data nHS
Base+98	ADC8 Cal data Zero
Base+9A	ADC8 Cal data pHS
Base+9C	ADC8 Cal data pFS
Base+9E	ADC9 Cal data nFS
Base+A0	ADC9 Cal data nHS
Base+A2	ADC9 Cal data Zero
Base+A4	ADC9 Cal data pHS
Base+A6	ADC9 Cal data pFS
Base+A8	ADC10 Cal data nFS
Base+AA	ADC10 Cal data nHS
Base+AC	ADC10 Cal data Zero
Base+AE	ADC10 Cal data pHS
Base+B0	ADC10 Cal data pFS
Base+B2	ADC11Cal data nFS
Base+B4	ADC11 Cal data nHS
Base+B6	ADC11 Cal data Zero
Base+B8	ADC11 Cal data pHS
Base+BA	ADC11 Cal data pFS

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data nHS - Negative Half Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

7.6 ID Page 6 (PG2 = 1. PG1 = 1, PG0 = 0) +/-5V Scan Calibration Values Layout.

The layout of the calibration pages is additionally dependant on the 'Cal Type' Value from the Default (Page 0) page of the ID PROM Section.

Address	Cal Type = 2
Base+80	ADC12 Cal data nFS
Base+82	ADC12 Cal data nHS
Base+84	ADC12 Cal data Zero
Base+86	ADC12 Cal data pHS
Base+88	ADC12 Cal data pFS
Base+8A	ADC13 Cal data nFS
Base+8C	ADC13 Cal data nHS
Base+8E	ADC13 Cal data Zero
Base+90	ADC13 Cal data pHS
Base+92	ADC13 Cal data pFS
Base+94	ADC14 Cal data nFS
Base+96	ADC14 Cal data nHS
Base+98	ADC14 Cal data Zero
Base+9A	ADC14 Cal data pHS
Base+9C	ADC14 Cal data pFS
Base+9E	ADC15 Cal data nFS
Base+A0	ADC15 Cal data nHS
Base+A2	ADC15 Cal data Zero
Base+A4	ADC15 Cal data pHS
Base+A6	ADC15 Cal data pFS
Base+A8	
Base+AA	
Base+AC	
Base+AE	
Base+B0	
Base+B2	
Base+B4	
Base+B6	
Base+B8	
Base+BA	

Table Key -

Cal data nFS - Negative Full Scale Calibration Factor.
Cal data nHS - Negative Half Scale Calibration Factor.
Cal data Zero - Zero (0 Volts) Calibration Factor.
Cal data pHS - Positive Half Scale Calibration Factor.
Cal data pFS - Positive Full Scale Calibration Factor.

8. Basic Register Setup

Set the following registers in the following sequence to initiate a conversion of the inputs.

8.1 Internal FIFO Operating Mode

Listed below is the recommended sequence to set the control and application registers to allow correct operation of the unit using the internal FIFO.
As an example, to scan the unit using the internal FIFO operation, at a programmable clock rate of 1 KHz, no enable trigger, interrupts IntReq0* not enabled, DMA request not enabled, +/-10V range and 2's complement, set the registers to the following settings:

- Reset the FIFOs by setting RST bit 4 high in the CSR register 0Hex, by writing 0010Hex
- Clear reset by clearing RST bit 4 low in the CSR register 0Hex, by writing 0000Hex
- Set the ACR register 34Hex , for +/-10V range and 2's complement format write 4Hex
- Set the programmable clock rate register 6Hex, for example for a frequency of 1KHz write 9Hex
- Set the IP interrupt vector value, register 8Hex
- Set the other control bits in the CSR register 0Hex, but without the ARM bit 15 set. For example write 0000Hex, no enable trigger, no external clock, on interrupts enabled, no DMA requests and running from the programmable clock rate.
- Lastly arm the unit by setting the ARM bit 15 high in the CSR register 0Hex, by writing 8000Hex. This will then continuously sample the inputs at the programmable clock rate and store the results in the internal FIFO.

8.2 Register Mode

The same setup for the internal FIFO operating mode can be used, but instead of reading the FIFO the ADC registers are accessed instead.

8.3 External FIFO Operating Mode

Listed below is the recommended sequence to set the control and application registers to allow correct operation of the unit using the external FIFO.
As an example, to scan the unit using the external FIFO, operation at a programmable clock rate of 1 KHz, software enabled trigger, interrupts IntReq0* not enabled, DMA request not enabled, +/-5V range and straight binary, set the registers to the following settings:

- Reset the FIFOs by setting RST bit 4 high in the CSR register 0Hex, by writing 0010Hex
- Clear reset by clearing RST bit 4 low in the CSR register 0Hex, by writing 0000Hex
- Set the ACR register 34Hex , for +/-5V range and straight binary format write DHex
- Set the programmable clock rate register 6Hex, for example for a frequency of 1KHz write 9Hex
- Set the IP interrupt vector vale, register 8Hex
- Set the other control bits in the CSR register 0Hex, but without the ARM bit 15 set. For example write 6000Hex, enable trigger and select enable software trigger, no external clock, on interrupts enabled, no DMA requests and running from the programmable clock rate.
- Lastly arm the unit by setting the ARM bit 15 high in the CSR register 0Hex, by writing E000Hex. This will then sample the inputs at the programmable clock rate with the software trigger and store the results in the external FIFO.

9. Isolation

The ADC 8413 +/-12 volt power supply can be derived either internally (non-isolated) from the carrier card (VME +/-12V) or from external isolating DC-DC converters (type 8912) mounted on an 8211 transition card. The source is selected using jumpers J1, J2 and the GND-AGND link.

J1 External +12V connect 1 & 2, Internal +12V connect 2 & 3
J2 External -12V connect 1 & 2, Internal -12V connect 2 & 3
J3 Reserved
J4 Factory set (boot jumper)

GND-AGND Link
IN for internal +/-12V (non-isolated)
OUT for external +/-12V (isolated and supplied from transition card DC-DC converter).

10. I/O Connector – 50 way on 8413 ADC Board

Pin	Signal	Pin	Signal
1	Input 1 +	26	Input 13 -
2	Input 1 -	27	Input 14 +
3	Input 2 +	28	Input 14 -
4	Input 2 -	29	Input 15 +
5	Input 3 +	30	Input 15 -
6	Input 3 -	31	Input 16 +
7	Input 4 +	32	Input 16 -
8	Input 4 -	33	
9	Input 5 +	34	
10	Input 5 -	35	XTrig+
11	Input 6 +	36	XTrig-
12	Input 6 -	37	N.C.
13	Input 7 +	38	N.C.
14	Input 7 -	39	XClk+
15	Input 8 +	40	XClk-
16	Input 8 -	41	+12VX
17	Input 9 +	42	AGND
18	Input 9 -	43	+12VX
19	Input 10 +	44	AGND
20	Input 10 -	45	-12VX
21	Input 11 +	46	AGND
22	Input 11 -	47	-12VX
23	Input 12 +	48	AGND
24	Input 12 -	49	AGND
25	Input 13 +	50	AGND

11. Transition Card Connections

TB 8213 I/O Connector – 50 way on transition

Connectors 1-4

Pin	Signal	Pin	Signal
1	Inp1 -	26	Inp1 +
2	Inp2 -	27	Inp2 +
3	Inp3 -	28	Inp3 +
4	Inp4 -	29	Inp4 +
5	Inp5 -	30	Inp5 +
6	Inp6 -	31	Inp6 +
7	Inp7 -	32	Inp7 +
8	Inp8 -	33	Inp8 +
9	Inp9 -	34	Inp9 +
10	Inp10 -	35	Inp10 +
11	Inp11 -	36	Inp11 +
12	Inp12 -	37	Inp12 +
13	Inp13 -	38	Inp13 +
14	Inp14 -	39	Inp14 +
15	Inp15 -	40	Inp15 +
16	Inp16 -	41	Inp16 +
17		42	
18	Xtrig -	43	Xtrig +
19		44	
20	XClk -	45	XClk +
21	AGnd	46	+12V
22	AGnd	47	+12V
23	AGnd	48	-12V
24	AGnd	49	-12V
25	AGnd	50	

12. Example Code

The following codes are extracts from our device driver and are provided as sample illustrations only.

12.1 Setting Up The Register Map

Below is an example of setting up the 8413 Register Map using 'C' structures and then positioning them in Memory using the VxWorks ipmBaseAddr function.

```
/* The registers are captured in this data structure. */
typedef struct
{
   USHORT Status;                /* 0x00 */
   USHORT Offset;                /* 0x02 */
   USHORT NumConversions;        /* 0x04 */
   USHORT ClockRate;             /* 0x06 */
   USHORT Vector;                /* 0x08 */
   USHORT INTFIFO;               /* 0x0A - 8413 Only            */
   USHORT EXTFIFO;               /* 0x0C - 8413 Only            */
   USHORT FIFOCount;             /* 0x0E - 8413 Only             */
   USHORT Data[16];              /* 0x10 - 0x1F (0x2F for 8413)  */
   USHORT Ref0V;                /* 0x30 - 8413 Only             */
   USHORT Ref2_5V;               /* 0x32 - 8413 Only             */
   USHORT AuxControl;            /* 0x34 - 8413 Only             */
} REGISTERS;

/* The application registers, ID PROM and calibration data are laid out
 * as a contiguous block. */
typedef struct
{
   REGISTERS reg;                              /* 0x00 - 0x1F */
} IO_MEMORY;

IO_MEMORY * pMem; /* register space */

/* register the card in the A16 address space */
card->pMem = ipmBaseAddr(card->vmeslotnum, card->ipslotnum, ipac_addrIO);
```

12.2 Simple ADC Reading

12.2.1 Set Up

To obtain the ADC Values straight from the ADC registers, the below setup is the minimum required for the 8413. The setup steps required are…

1. Set the Auxiliary Control Register for the Voltage Range and Data Format you require.
2. Set the Clock Rate you require.
3. Arm the ADCs (Set the Arm bit in the Control Status Register).

For Example…

```
/* Switch to Page 0 / Default / Standard of ID Prom – Clear ACR Bits 4,5 and 6 */
/* Range +/- 10V  - Clear ACR Bit 0 */
/* ADC Values 0000 - FFFF rather Than 2's Complement – Set ACR Bit 3 */
/* Normal Operation – Set ACR Bit 2 */
card->pMem->reg.AuxControl = 0x000C;

/* Set clock rate to 15 (100KHz) */
card->pMem->reg.ClockRate = 15;

/* Just ARM the ADCs */
card->pMem->reg.Status = 0x8000;
```

12.2.2 Reading ADC and Reference Values

After the above setup, the ADC and Reference Values can be read straight from the ADC registers. For Example…

```
/* Read all the ADC Channels */
for (channel = 0; channel < 16; channel++)
{
   val[channel] = card->pMem->reg.Data[channel];
}

 /* Read 0V Reference */
val_0V_ref = card->pMem->reg.Ref0V;

 /* Read 2.5V Reference */
val_2_5V_ref = card->pMem->reg. Ref2_5V;
```

12.3 FIFOs and Interrupts

12.3.1 Set Up

To use the external FIFO instead or indeed as well (you can read the ADC Registers directly and whilst the FIFO is updating and obtain valid data), as is simply as of modifying the previous setup by changing the value written to CSR register. The value required by the CSR is to set the following bits (ARM, ST and ET). The FIFO can be monitored by simply checking the CSR FIFO Full Flag or count registers, but this is a very wasteful methodology. By far the best method is using the interrupts. The interrupts can be setup by additionally setting the FIFO Full Interrupt bit (ETF) in the CSR and setting a valid interrupt vector. For example…

```
/* Switch to Page 0 / Default / Standard of ID Prom */
/* Range +/- 10V */
/* ADC Values 0000 - FFFF rather Than 2's Complement */
card->pMem->reg.AuxControl = 0x000C;

/* Set clock rate to 15 (100KHz) */
card->pMem->reg.ClockRate = 15;

/* Setup Interrupt Vector for FIFO Full */
card->pMem->reg.Vector = 20;

/* Enable FIFO, FIFO Full Interrupt and Trigger FIFO */
card->pMem->reg.Status = 0xE200;
```

12.3.2 Reading ADC Values from the External FIFO

It is not good practise to read out the external 256K FIFO samples in an interrupt routine. One technique is to flag a suspended task to read out the FIFO after an interrupt. We arrange for the FIFO Full Interrupt to do two things…

1. Set a flag indicating which IP Card's FIFO is full.
2. Resume a suspended task used to read the FIFO.

The 16 ADC channels are fed into and therefore read out of the FIFO in the following order….

ADC 1 Sample 1
ADC 2 Sample 1
ADC 3 Sample 1
…
…
ADC 16 Sample 1
ADC 1 Sample 2
…
…
ADC 16 Sample 2
ADV 1 Sample 3
…
…
ADC 16 Sample 2
ADV 1 Sample 3
…
…
ADC 16 Sample 2
ADV 1 Sample 3
…
…
…
…
ADC 16 Sample 16384

A simple 2 level nested loop ('ADC channel' inner loop and 'Which Sample' outer loop) can be used to read ADC Readings from the FIFO as shown in the following example...

This sample is from our driver code where CARDINFO is a linked list data structure containing status and storage data for all IP cards initialised by the driver.

```
static void Hy8401IntProcTask( int arg1, int arg2, int arg3,int arg4, int arg5…. int arg10)
{
/* declare local variables */
CARDINFO *card;
USHORT   sample, channel;

while(1)
    {
    /* search for the card in the known card list */
     for (card = cardlst; card != NULL; card = card->next)
         {
       /* Has this Card any Interrupts to Process ? */
       if (card->iInterruptFlag == TRUE)
       {
            /* Clear the Flag for the Next Interrupt */
            card->iInterruptFlag = FALSE;

            /* As the 8413 uses a FIFO you can NOT 'Cherry Pick' Data as with RAM */
              /* We have to read all the channels from the FIFO into a Global RAM Copy */
            for (sample = 0; sample < 16384; sample ++)
             {
                 for (channel = 0; channel < 16; channel ++)
                  {
                  /* Write FIFO Read Values to the Global array for each IP Card */
                   card->waveform_memory[channel][sample] = card->pMem->reg.PostTrigFIFO;
                  }
            }

              /* Suspend Task Until Called from Interrupt */
            taskSuspend(InterruptTaskID);
       }
}
```