IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: PACSystems™ RX3i CPU

IC695CPU310-DH with Firmware Version 3.50

Release 3.50 of the RX3i CPU includes support for the following features:

Support for IO Variables – IO modules can now have their status data configured for symbolic variables in addition to reference addresses.

Support for Symbolic Variables in EGD – Segments within EGD exchanges can be configured for symbolic variables in addition to mapped variables and reference addresses.

Support for Access to Variables from C Blocks – Symbolic and Mapped variables can now be accessed through new access functions.

Support for IEC 61131-3 compliant Function Block Diagram programming language – Users can now download, upload, and execute programs developed using the FBD programming language.

Support for IEC Timers (TP, TON, TOF) – Includes IEC 61131-3 compliant timer function blocks for pulse timer, on-delay timer, and off-delay timer.

Support for RX3i Analog Modules with HART – Includes the following new modules: Input IC695ALG626/IC695ALG628, Output IC695ALG728

Support for RX3i High-Density Discrete Module – Includes the following new modules: Input IC693MDL260, IC694MDL260

Support for RX3i AC Isolated Discrete Modules – Includes the following new modules: Input IC693MDL250, IC694MDL250, Output IC693MDL350, IC694MDL350

Support for the Series 90-30 DeviceNet Master module (IC693DNM200) – Please note that the module is supported in the Main Rack and Expansion Racks only. The module is NOT supported in Remote Racks. Please see GFK-2194C for additional module functionality restrictions and additional operational issues.

ATEX agency approval has been added.

Version Identification

Hardware Identification	
Catalog Number	**Circuit Board ID**
IC695CPU310-DH	CP4A1

Firmware Identification	
Firmware ID	**Version**
CPU Primary	3.50 Build 36A2 BOC Rev 0104 Build 03A1
CPU Boot	3.50 Build 31A1

Updates

IC695CPU310 can be field-upgraded to firmware version 3.50 using the firmware upgrade utility. The upgrade kit can be ordered or downloaded at no charge from http://www.gefanuc.com/

Upgrade Kit: 44A752290-G09

Product Documentation

PACSystems CPU Reference Manual, GFK-2222

PACSystems RX3i Hardware and Installation Manual, GFK-2314

TCP/IP Ethernet Communications for the PACSystems, GFK-2224

C Toolkit for PACSystems User's Manual, GFK-2259

DeviceNet Modules for PACSystems RX3i and Series 90-30 User's Manual, GFK-2196

IPI, DeviceNet Modules for PACSystems RX3i and Series 90-30, GFK-2194C

Proficy™ Machine Edition Getting Started, GFK-1868

Proficy Logic Developer – PLC Programming Software Getting Started, GFK-1918

Datasheet, PACSystems RX3i CPU, GFK-2316

IPI, PACSystems RX3i CPU, GFK-2329L (this document)

CPU Functional Compatibility

Subject	*Description*
Programmer Version Requirements	Proficy Machine Edition Logic Developer 5.5 or later must be used for new features in PACSystems 3.50. Proficy Machine Edition Logic Developer 5.0 or later must be used to configure and program the RX3i. Service Pack 3 is required to support the new features in PACS 3.00.
C Toolkit Compatibility	C Toolkit Release 3.50 Build 34A1 is required for new features in PACSystems Release 3.50 (Use of variables in C Blocks). The C Toolkit for PACSystems is distributed with Proficy® Machine Edition Logic Developer 5.0 or greater. Toolkit Release 2.50 build 50A1 or later is required for use with the RX3i. Please note: The Series 90 Toolkit (IC641SWP709/719) is not compatible with PACSystems.
Series 90-30 Module Compatibility	The following Series 90-30 modules are supported by the PACSystems RX3i: Discrete Input Modules: IC693ACC300, IC693MDL230/231/240/241/250/260/632/634/645/646/648/654/655 IC693MDL660 – To operate in a CPU Release 3.0 system, the module firmware must be updated to version 1.10 Discrete Output Modules: IC693MDL310/330/340/350/390/730/731/732/733/734/740/741/742/748/752/753/760/930/931/940 IC693MDL754 – To operate in a CPU Release 3.0 system, the module firmware must be updated to version 1.10 Discrete Combinational: IC693MAR590, IC693MDR390 Analog I/O Modules: IC693ALG220/221/222/223/390/391/392/442 High Speed Counter: IC693APU300 FANUC I/O Link: IC693BEM320, IC693BEM321 Motion Control: IC693DSM314, IC693DSM324 GENIUS: IC693BEM331 DeviceNet Master: IC693DNM200 Serial IO Processor: IC693APU305 Temperature Control: IC693TCM302, IC693TCM303 Power Transducer: IC693PTM100, IC693PTM101 All other Series 90-30 modules are currently not supported.

Subject	*Description*
IC694 (blue) Module Compatibility	Discrete Input Modules: IC694ACC300, IC694MDL230/231/240/241/250/260/632/634/645/646/654/655 IC694MDL660 – To operate in a CPU Release 3.0 system, the module firmware must be updated to version 1.10 Discrete Output Modules: IC694MDL310/330/340/350/390/732/734/740/741/742/752/753/930/931/940 IC694MDL754 – To operate in a CPU Release 3.0 system, the module firmware must be updated to version 1.10 Analog I/O Modules: IC694ALG220/221/222/223/390/391/392/442 High Speed Counter: IC694APU300 Motion Control: IC694DSM314, IC694DSM324 Expansion Backplanes: IC694CHS392/398 Expansion Power Supplies: IC694PWR321/330/331 FANUC I/O Link: IC694BEM320, IC694BEM321 GENIUS: IC694BEM331 Device Net Master: IC694DNM200 Serial IO Processor: IC694APU305
IC695 (PCI) Module Compatibility	Ethernet Interface: IC695ETM001 Universal Analog Input Module: IC695ALG600 PROFIBUS: IC695PBM300 (Master) PROFIBUS: IC695PBS301 (Slave) Non-isolated Analog Input Modules: IC695ALG616/608 Non-isolated Analog Output Modules: IC695ALG708/704 Analog Input Modules with HART: IC695ALG626/628 Analog Output Module with HART: IC695ALG72
Series 90-30 Expansion Rack Compatibility	Series 90-30 expansion racks, both local and remote, are supported by the PACSystems RX3i. PACSystems RX3i CPU does not operate in a Series 90-30 Rack.
Series 90-30 Main Rack Compatibility	Series 90-30 Main Racks cannot be used in a PACSystems RX3i system. Series 90-30 CPUs do not operate in PACSystemsRX3i Racks.
Isolated 24V power	In applications that use the IC69xALG220/221/222, consult *PACSystems RX3i Hardware and Installation Manual*, GFK-2314 for details of wiring the 24V power.
COMMREQ to PBM300	In Release 3.0, the behavior of the COMMREQ fault output on a COMMREQ sent to the PROFIBUS master module IC695PBM300 has been changed to be compatible with the Series 90-30 CPU366 PROFIBUS Master. Previously, the fault output is enabled when the module receives a COMMREQ and it is busy. Now, the busy condition does not result in the fault output enabled.
Recommended IC200ALG240 revision	When a VersaMax™ system Genius® Network Interface Unit (IC200GBI001) interoperates with a Genius Bus Controller located in a PACSystems PLC, and the VersaMax system contains an IC200ALG240 Analog Input Module, it is recommended to update the IC200ALG240 firmware to Revision 1.10 or later. Use firmware update kit 44A752313-G01, available in Knowledge Base Article i023269 at http://globalcare.gefanuc.com.
Configuration of IC694MDL754	Always configure 16 bits of module status when using this module. Configuring 0 bits of module status will result in invalid data in the module's ESCP status bits.

Problems Resolved by Release 3.50

The following problems are resolved in version 3.50 of the firmware.

Subject	*Description*
Power Cycle During Online Edit	If the user stores a folder to flash that is configured to power up from flash and then subsequently power is cycled in the middle of a Online Edit session, the programmer will still indicate that the Online Edit session is in progress after the power cycle. The user should cancel the Online Edit session to continue.
RAND_MAX and rand() Function Incompatible	In the C Toolkit, the RAND_MAX system variable is defined as a 32-bit integer. However, the rand() function returns a 16-bit integer. By definition, rand() should return an integer between 0 and RAND_MAX.
Timed interrupt response time increased	A GBC in the system may impact response time for timed interrupts. The worst case interrupt response time for a PLC system with a GBC and no other Genius devices is 0.5 milliseconds. The worst case interrupt response time for a PLC system with a GBC and maximum amount of Genius data is 50 milliseconds.
COMMREQ Status Words Declared in Bit Memory Types Must Be Byte-Aligned	In previous releases, the CPU allowed configuration of COMMREQ Status Words in bit memory types on a non-byte-aligned boundary. Even though the given reference was not byte-aligned, the firmware would adjust it to the next-lowest byte boundary before updating status bits, overwriting the bits between the alignment boundary and specified location. To ensure that the application operates as expected, release 3.50 requires configuration of COMMREQ Status Words in bit memory types to be byte-aligned.
Possible ME disconnect when multiple GBCs are present in expansion/remote racks within a system.	If a system contains multiple GBCs in expansion/remote racks, then it is possible for ME to timeout its connection to the PLC on a clear operation or a store of configuration. For each GBC located in an expansion/remote rack there is a 3 second delay added to the time required for a clear/store of configuration. The default connection timeout is 10 seconds and the default request timeout is 16 seconds. These values should be increased by at least 3 seconds per each GBC physically located in an expansion/remote rack. This is true for both Ethernet and serial connections.
Repeated store of folder containing C blocks	After many stores of a folder that contains C blocks, the PLC CPU and/or Ethernet module may cease operation. Power-cycle the main PLC rack to recover. The possibility of undesired operation may be avoided completely by power-cycling the main PLC rack after every 5th store of a C block folder.
Power supply overtemperature reporting	In previous releases, if an RX3i power supply detects an overtemperature condition, the reported fault specifies group 24 and results in the %SA0008 OVR_TMP bit being set and the user's configured fault action being executed. This fault group and bit are intended to reflect CPU overtemperature conditions only. In release 3.50, only a CPU overtemperature condition results in the %SA0008 OVR_TMP bit being set.
Configuration store failure	In previous releases, repeated stores of a configuration that contains serial bus transmitter module IC695LRE001 to a system that does not physically contain the module will eventually result in failure of the store attempt. Power cycle the main rack to restore normal operation. Removing the non-present module from the configuration will eliminate the possibility of the behavior. This problem has been corrected in release 3.50
Service Request 6: rounding of length parameter	Processing for Service Request 6 C*hange/Read Number of Words to Checksum* incorrectly rounds the specified length to the next largest multiple of 8 bytes, rather than 8 words. Consequently, each sweep may checksum fewer words than expected.
Serial Port Lock-up after Bad Modbus Message	If a badly formed Modbus RTU message is sent to the PLC, the serial port will lock up. Power must be cycled to recover proper port operation.

The following problems were resolved in version C of the hardware.

Subject	*Description*
At high temperatures, some CPUs don't power up properly	In earlier hardware versions, some CPUs may not complete powering up when operating at high temperature (above 52°C with hot neighbors, higher without hot neighbors). The CPU will power up properly if it is powered down and allowed to cool for a few minutes. Version C of the hardware corrects this problem.

New CPU Features and Enhancements in Release 3.50

The RX3i CPU provides the following new features and enhancements:

- Support for IO Variables (Symbolic Variables) in hardware configuration.
- Support for Symbolic Variables in EGD configuration.
- Support for Access to Symbolic and Mapped Variables from C Blocks.
- Support for IEC 61131-3 compliant Function Block Diagram programming language.
- Support for IEC 61131-3 compliant timer function blocks for pulse timer, on-delay timer, and off-delay timer.
- Support for new RX3i Analog Modules with HART – Includes the following new modules: Input IC695ALG626, IC695ALG628, Output IC695ALG728
- Support for RX3i High-Density Discrete Module – Includes the following new modules: Input IC693MDL260, IC694MDL260
- Support for RX3i AC Isolated Discrete Modules – Includes the following new modules: Input IC693MDL250, IC694MDL250, Output IC693MDL350, IC694MDL350
- Support for the Series 90-30 DeviceNet Master module (IC693DNM200)
- ATEX agency approval has been added.

CPU Restrictions and Open Issues

Subject	*Description*
Battery installation	When installing a new battery, when there currently is no battery installed, the battery must be installed while the CPU has power. Failing to follow this procedure could result in the CPU not powering up. If a battery is installed while power is off (and there was no battery previously installed), and the CPU fails to power up, simply remove the battery, power cycle the CPU and then install the battery.
Ethernet Disconnect During Word-for-Word Change	If the Ethernet connection is broken during a word-for-word change, the programmer may not allow a subsequent word-for-word change after reconnecting due to the fact that it thinks another programmer is currently attached. If this occurs, you should go offline and then back online again.
Simultaneous Clears, Loads and Stores Not Supported	Currently, PACSystems CPUs do not support multiple programmers changing CPU contents at the same time. The programming software may generate an error during the operation. Simultaneous loads from a single PLC are allowed.
Power Cycle During Write to Flash	If the CPU is power cycled during the process of writing to flash, and is configured to power up from flash, a fault will be generated on power up.
Hardware Configuration Not Equal After Changing Target Name	If the user stores a hardware configuration to flash that sets "Logic/Config Power up Source" to "Always Flash" or "Conditional Flash" and then subsequently changes the name of the target in the programming software, the hardware configuration will go Not Equal and will not Verify as equal.

Subject	*Description*
PLC and IO Fault Tables May Need to be Cleared Twice to Clear Faulted State	Both PLC and IO fault tables may need to be cleared to take the CPU out of Stop/Fault mode. If one of the tables contains a recurring fault, the order in which the tables is cleared may be significant. If the CPU is still in Stop/Fault mode after both tables are cleared, try clearing the fault tables again.
Setting Force On/Off by Storing Initial Value	Once a force on or force off has been stored to the PLC, the user cannot switch from force on to force off or vice-versa directly by downloading initial values. The user can turn off the force by doing a download, and then change the force on or off by another download.
Number of Active Programs Returned as Zero	The SNP request Return Controller Type and ID currently returns the number of active programs as zero.
Serial I/O Failure at 115K During Heavy Interrupt Load	Rare data corruption errors have been seen on serial communications when running at 115K under heavy interrupt load on the PLC. Under heavy load applications, users should restrict serial communications to 57K or lower.
Incorrect Commreq Status For Invalid Program Name	The program name for PACSystems is always "LDPROG1". When another program name is used in a commreq accessing %L memory, an Invalid Block Name (05D5) error is generated.
SNP ID not always provided	Unlike the Series 90-30, the RX3i CPU's SNP ID will not appear in the Machine Edition programmer Show Status display. Service Request 11 will always return zeros.
Second programmer can change logic while in Test & Edit mode	While currently active in a Test and Edit session using Machine Edition on one PC, Machine Edition running on another PC is not prevented from storing new logic to the PLC.
Must Have Logic If Powering-Up From Flash	If the application will configure the CPU to retrieve the contents of flash memory at power-up, be sure to include logic along with hardware configuration when saving to flash memory.
CPU may not detect low-battery condition	PACSystems CPUs may not detect a low-battery condition early enough to provide a meaningful warning to the user to replace the battery. A battery with very low capacity may still have a terminal voltage high enough to report that it is a good battery. In this case, when the battery starts supplying the memory power (battery backup), the battery voltage would quickly drop to unacceptable levels, with little warning to the user before failure. To insure against data loss, users should replace batteries in accordance with the guidelines provided in the CPU Reference Manual, GFK-2222. Additionally, users could save logic and hardware configuration to flash.
Two loss of module faults for Universal Analog Module	Occasionally, the hot removal of the Universal Analog Input Module (IC695ALG600) results in two "Loss of I/O Module" faults instead of one.
Power up of HSC may take as long as 20 seconds	As power is applied to a 90-30 High-Speed Counter, the "module ready" bit in the status bits returned each sweep from the module may not be set for as long as 20 seconds after the first PLC sweep, even though there is no "loss of module" indication. I/O data exchanged with the module is not meaningful until this bit is set by the module. For details, see "Data Transfer Between High Speed Counter and CPU" in the *Series 90-30 High Speed Counter User's Manua*l, GFK-0293C.
Info fault at power up	Intermittently during power-up, an Informational non-critical CPU software fault may be generated with fault extra data of 01 91 01 D6. This fault will have no effect on the normal operation of the PLC. But, if the hardware watchdog timer expires after this fault and before power has been cycled again, then the outputs of I/O modules may hold their last state, rather than defaulting to zero.
Extended Memory Types for IO Triggers	%R, %W and %M cannot be used as IO triggers.
Possible Machine Edition inability to connect	Infrequently, an attempt to connect a programmer to a PLC via Ethernet will be unsuccessful. The normal connection retry dialog will not be displayed. Rebooting the computer that is running the programmer will resolve the behavior.
SNP Update Datagram message	If an Update Datagram message requests 6 or less bits or bytes of data, the PLC will return a Completion Ack without Text Buffer. The protocol specifies that the returned data will be in the Completion Ack message, but it may not be.

Subject	*Description*
GBC30 may not resume operation after power cycle	In rare instances, a GBC30 in an expansion rack may not resume normal operation after a power cycle of either the expansion rack or the main rack.
Configuration of third-party modules	Do not specify a length of 0 in the configuration of a third-party module. The module will not work properly in the system.
Power supply status after CPU firmware update	The PLC will report a “Loss of or missing option module” fault for the IC695PSD140 RX3i power supply following an update of PLC CPU firmware. Also, the slot will appear empty in the programmer’s online status detail view. The power supply continues to operate normally. Power cycle to restore normal status reporting.
Power supply status after power cycling	Rarely, turning a power supply on or off may not result in an add or loss fault. Also, the slot will appear empty in the programmer’s online status detail view. The power supply continues to operate normally. Power cycle to restore normal status reporting.
“Clear All” operation may timeout	A Clear All to a system with a very large hardware configuration may timeout, with the error: Error 8097: Server Error - Transfer Error: Host driver timed out. [0x6A][0x01] The selected memory could not be cleared ME does not disconnect when the error occurs and a retry is usually successful.
Don’t use multiple targets	In a system in which the hardware configuration is stored from one target and logic is stored from a different target, powering-up from flash will not work. The observed behavior is that, following a power up from flash, ME reports hardware configuration and logic "not equal".
Missing “Loss of terminal block” fault	The IC695ALG600/608/616 analog input modules do not produce a “Loss of terminal block” fault when hardware configuration is stored or the module is hot-inserted, and the terminal block is not locked into place.
Sequence Store Failure	In systems with very large hardware configurations, it is possible to encounter a “PLC Sequence Store Failure” error when writing the configuration to flash. To work around this error, either: 1. Perform an explicit clear of flash prior to performing the write. 2. Increase the operation timeout used by Machine Edition software prior to performing the write.
IC694MDL754: Must configure module status bits	Always configure 16 bits of module status when using this module. Configuring 0 bits of module status will result in invalid data in the module’s ESCP status bits.
IC695ALG600 Lead Resistance Compensation setting	A configuration store operation will fail if a channel is configured for 3-wire RTD and Lead Resistance Compensation is set to Disabled. A Loss of Module fault will be logged in the I/O Fault table at the end of the store operation. To recover the lost module, the configuration must be changed to enable Lead Resistance Compensation and module must be power cycled.
C Toolkit PlcMemCopy Documentation Incorrect	This routine does allow the destination and source pointers to be outside of reference memory. If the destination points to discrete reference memory, overrides and transitions will be honored. Note that the header for PlcMemCopy has been updated in Release 3.50 of the C toolkit.
Genius Device I/O Enable LED Does Not Illuminate If No Output Module Present on Genius Bus	If a Genius Bus contains no output Genius devices, the I/O Enable LEDs for the input Genius devices will not illuminate when the PLC is placed in RUN Mode. The modules will function properly even though the status LED is not lit. If an output Genius device is present on the Genius bus, the I/O Enable LED will illuminate for all input and output Genius devices when the PLC is placed in RUN Mode as expected.

Issues Related to the IC695ALG626/628/728 Analog Modules with HART

HART Input Modules are not Re-acquired after CPU Firmware Update	After WinLoading Firmware to the RX3i CPU, Analog Input modules with HART, IC695ALG626 and IC695ALG628, are not reacquired by the CPU. Loss of module faults are logged in the fault table and the module is unresponsive. Power cycling the entire system or hot removing and reinserting the affected Input modules recovers the modules.

Issues Related to the IC693DNM200 DeviceNet Master Module

Please see GFK-2194C for open issues related to the IC693DNM200 DeviceNet Master Module.

CPU Operational Notes

Subject	*Description*
Important Installation Instructions for Battery	A battery is shipped with the CPU unit behind the battery door on the faceplate but it is not connected. Do not connect the battery until the CPU is installed in the rack and the rack powered on. The battery may then be attached to either of the two terminals in the battery compartment. Once that is done, the CPU may be powered down and normal battery back up operation will begin. To save battery life, do not connect the battery for the first time until the CPU is powered up.
LD-PLC operations	Machine Edition LD-PLC no longer supports a function which connects to the PLC, downloads, then disconnects from the PLC. The connect and download functions are now separate. To perform a download to the PLC, you must first connect to the PLC.
Logic Executed in Row Major Instead of Column Major	Logic execution in PACSystems RX3i is performed in row major order (similar to the Series 90-30). This is different from the Series 90-70, which executes in column major order. This means that some complicated rungs may execute slightly differently on PACSystems RX3i and Series 90-70. For specific examples, see the programming software on-line help.

<table>
<tr><th>Subject</th><th>Description</th></tr>
<tr><td>Slot numbering, power supply placement, CPU placement and reference</td><td>
1. The A/C Power-Supply (IC695PSA040) for the RX3i is a doublewide module whose connector is left justified as viewed when installed in a rack. It cannot be located in Slot 11 of a 12-slot rack nor Slot 15 of a 16-slot rack. No latch mechanism is provided for the last (right-most) slot in a rack, therefore it is not possible to place the power-supply in the second to last slot.
2. The RX3i CPU (IC695CPU310) is a doublewide module whose connector is right justified as viewed when installed in a rack. It is referenced for configuration and by user logic applications by the leftmost slot that it occupies. For example, if the RX3i CPU has its physical connector inserted in to slot 4, which means it occupies slots 3 and 4, the CPU is referenced as being located in slot 3. The referenced location of the CPU is not determined by what slot the physical connector is located in, but rather by the left most slot occupied by the entire module.
3. Due to item #2 above, the RX3i CPU may be located in Slot 0 of a rack (physical connector in Slot 1). In addition the CPU cannot be located in Slot 11 of a 12-slot rack nor Slot 15 of a 16-slot rack, since doing so would require the physical connector to be located in the slot reserved for an expansion module.
4. When migrating a Series 90-30 CPU system to a PACSystems RX3i CPU, be aware that to maintain the Slot 1 location of the CPU, only a singlewide power-supply may be used in Slot 0. Either DC power supply can be used (IC695PSD040 or IC695PSD140). Therefore, if the application using an existing Series 90-30 system must maintain a Slot 1 CPU and uses an AC power-supply, the RX3i system must have the RX3i AC power-supply located in a slot to the right of the RX3i CPU in Slot 1.
5. In deciding to place the CPU in slots other than Slot 1, the user should be aware of the possible application migration issues that could arise. The following lists the areas that could be affected when migrating an application from one CPU slot to another.
<table>
<tr><th colspan="2">Item Affected</th><th>How Affected</th></tr>
<tr><td rowspan="3">User Logic</td><td>Service Request #15 (Read Last-Logged Fault Table Entry)</td><td rowspan="2">Location of CPU faults will not be the standard 0.1 location, but will reflect the slot the CPU is located in. User logic that decodes fault table entries retrieved by these service requests may need updating.</td></tr>
<tr><td>Service Request #20 (Read Fault Tables)</td></tr>
<tr><td>Communications Request (Commreq)</td><td>Commreqs directed to the CPU (e.g. those directed to the serial ports of the CPU) will need to be updated with the correct CPU slot reference.</td></tr>
<tr><td>H/W Configuration</td><td>CPU Slot location</td><td>Slot location of the CPU must be updated in the HW Configuration to reflect the CPU’s true location.</td></tr>
<tr><td>Fault Tables</td><td>Faults logged for the CPU</td><td>The location of faults logged for the CPU in the fault table will not be the standard 0.1 (rack.slot) location, but will reflect the CPU’s actual slot.</td></tr>
<tr><td rowspan="6">External Devices</td><td colspan="2">Series 90 PLCs</td></tr>
<tr><td colspan="2">Remote Series 90 PLCs that use SRTP Channels COMMREQs expect the CPU to be in slot 1. In order to support communications with Series 90 SRTP clients such as Series 90 PLCs using SRTP Channels, the RX3i internally redirects incoming SRTP requests destined for {rack 0, slot 1} to {rack 0, slot 2}, provided that the CPU is located in rack 0 slot 2 (and the remote client has not issued an SRTP Destination service on the connection to discover the rack and slot of the CPU). This special redirection permits Series 90-30 applications that expect the power supply to be located leftmost and the CPU to be located to the right of the power supply to function. Attempts to establish channels with CPUs in slots other than 1 or 2 will fail if initiated from Series 90 PLCs.</td></tr>
<tr><td colspan="2">HMI and External Communication Devices</td></tr>
<tr><td colspan="2">All external communication devices that interact with the CPU should be checked for compatibility with CPU slot locations other than slot 1. Problems may arise with, but are not limited to, initial connection sequences and fault reporting. Machine Edition View customers should select “GE SRTP” as their communications driver – it can communicate with a CPU in any slot.</td></tr>
<tr><td colspan="2">Host Communications Toolkit (HCT)</td></tr>
<tr><td colspan="2">Applications that utilize the Host Communications Toolkit may require updated drivers.</td></tr>
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Subject	*Description*
NaN handled differently than in Series 90-30	The PACSystems RX3i CPU may return slightly different values for Not A Number as compared to Series 90-30 CPUs. In these exception cases (e.g., 0.0/0.0), power flow out of the function block is identical to Series 90-30 operation and the computed value is still Not A Number.
PID Algorithm Improved	The PID algorithm used in PACSystems has been improved and therefore PID will function slightly differently on PACSystems RX3i than on the Series 90-30. The differences are that the elapsed time is computed in 100 µS instead of 10 mS units. This smoothes the output characteristic, eliminating periodic adjustments that occurred when the remainder accumulated to 10mS. Also, previous non-linear behavior when the integral gain is changed from some value to 1 repeat/second was eliminated.
Some Service Requests different from 90-30 or no longer supported	■ Service Requests 6, 15, and 23 have slightly different parameters. Refer to GFK-2222. ■ PACSystems PLCs support Service Request 26/30 functionality via fault locating references. ■ Service Request 13 requires a valid value in the input parameter block (Refer to GFK-2222 for details). On the Series 90-30 and Series 90-70 the parameter block value was ignored. ■ Service Requests 48 and 49 are no longer supported (there is no auto-restart) because most faults can be configured to be not fatal.
IL and SFC	IL and SFC are not available.
DO I/O Instruction	The Series 90-30 Enhanced DO I/O instruction is converted to a standard DO I/O instruction (the ALT parameter is discarded and ignored.)
END Instruction	The Series 90-30 END instruction is not supported. Alternate programming techniques should be used.
Non-nested JUMP, LABEL, MCR, & ENDMCR Instructions	Non-nested JUMPs, LABELs, MCRs, & ENDMCRs are translated to the corresponding nested JUMPs, LABELs, MCRs, & ENDMCRs when converting from Series 90-30 to PACSystems RX3i.
Changing IP Address of Ethernet Interface While Connected	Storing a hardware configuration with a new IP address to the RX3i while connected via Ethernet will succeed, then immediately disconnect because the RX3i is now using a different IP address than the Programmer. You must enter a new IP address in the Target Properties in the Machine Edition Inspector window before reconnecting.
Duplicate Station Address for Modbus Will Conflict with Other Nodes	The default serial protocol for the RX3i is Modbus RTU. The default Station Address is 1. If the PLC is added to a multi-drop network, care must be taken that the PLC is configured with a unique Station Address. Nodes with duplicate Station Addresses on the same network will not work correctly.
Timer Operation	Care should be taken when timers (ONDTR, TMR, and OFDTR) are used in program blocks that are NOT called every sweep. The timers accumulate time across calls to the sub-block unless they are reset. This means that they function like timers operating in a program with a much slower sweep than the timers in the main program block. For program blocks that are inactive for large periods of time, the timers should be programmed in such a manner as to account for this catch up feature. Related to this are timers that are skipped because of the use of the JUMP instruction. Timers that are skipped will NOT catch up and will therefore not accumulate time in the same manner as if they were executed every sweep.
Constant Sweep	**Constant Sweep** time, when used, should be set at least 10 milliseconds greater than the normal sweep time to avoid any over-sweep conditions when monitoring or performing on-line changes with the programmer. Window completion faults will occur if the constant sweep setting is not high enough.

Subject	*Description*
Large Number of COMM_REQs Sent to Module in One Sweep Causes Faults	A large number of COMM_REQs (typically greater than 8) sent to a given board in the same sweep may cause Module Software faults to be logged in the PLC fault table. The fault group is MOD_OTHR_SOFTWR (16t, 10h) and the error code is COMMREQ_MB_FULL_START (2). When this occurs, the “FT” output of the function block will also be set. To prevent this situation, COMM_REQs issued to a given board should be spread across multiple sweeps so that only a limited number (typically 8 or less) of COMM_REQs are sent to a given board in each sweep. In addition, the FT output parameter should be checked for errors. If the FT output is set (meaning an error has been detected), the COMM_REQ could be re-issued by the application logic.
C Block Standard Math Functions Do Not Set errno	In C Blocks, standard math functions (e.g. sqrt, pow, asin, acos) do not set errno to the correct value and do not return the correct value if an invalid input is provided.
Upgrading Firmware	1. The process of upgrading the CPU firmware with the WinLoader utility may fail when multiple IO modules are in the main rack, due to the time it takes to power cycle the rack system. If the upgrade process fails, move the CPU to a rack without IO modules and restart the upgrade process. 2. Winloader initial connect baud rate is fixed at 19200 baud. Note that the firmware download will occur at 115.2K baud by default. 3. Note that if you have hyperterm open on a port, and then try to use Winloader on the same port, Winloader will often say “Waiting for Target” until the hyperterm session is closed.
Hot Swap	Hot Swap of power supplies or CPUs is not supported in this release
Serial Port Configuration COMMREQs	With the following combination of circumstances, it is possible to render serial communications with the CPU impossible: 1. User configuration disables the Run/Stop switch 2. User configures the power up mode to Run or Last 3. Logic is stored in FLASH and user configures CPU to load from FLASH on power up 4. User application issues COMMREQs that set the protocol on both of the serial ports to something that does not permit communications to the ME programmer.
Incorrect Commreq Status For Invalid Program Name	The program name for PACSystems is always "LDPROG1". When another program name is used in a CommReq accessing %L memory, an Invalid Block Name (05D5) error is generated.
FANUC I/O Master and Slave operation	Scansets on the master do not work properly for the first operation of the scanset after entering RUN mode. They do work properly for subsequent scans. After downloading a new hardware configuration and logic, a power cycle may be required to resume FANUC I/O operation. Use PLCs of similar performance in FANUC I/O networks. If a master or slave is located in an RX3i system, the other PLCs should be RX3is or Series 90-30 CPU374s. Repeated power up/down cycles of an expansion rack containing FANUC I/O slaves may result in failure of the slaves’ operation, with the RDY LED off.
Lost count at power up for Serial IO Processor	The serial IO Processor (IC693APU305) will lose the first count after every power up or every time the module receives a configuration.
COMMREQ Status Words Declared in Bit Memory Types Must Be Byte-Aligned	In previous releases, the CPU allowed configuration of COMMREQ Status Words in bit memory types on a non-byte-aligned boundary. Even though the given reference was not byte-aligned, the firmware would adjust it the next-lowest byte boundary before updating status bits, overwriting the bits between the alignment boundary and specified location. To ensure that the application operates as expected, release 3.50 requires configuration of COMMREQ Status Words in bit memory types to be byte-aligned. For example if the user specified status bit location of %I3, the CPU aligns the status bit location at %I1. Release 3.50 firmware requires the user to specify the appropriate aligned address (%I1) to ensure that the utilized location is appropriate for their application. Note that the actual reference location utilized is not changed, but now is explicitly stated for the user.

Installation in Hazardous Locations

The following information is for products bearing the UL marking for Hazardous Locations:

- WARNING - EXPLOSION HAZARD - SUBSTITUTION OF COMPONENTS MAY IMPAIR SUITABILITY FOR CLASS I, DIVISION 2;
- WARNING - EXPLOSION HAZARD - WHEN IN HAZARDOUS LOCATIONS, TURN OFF POWER BEFORE REPLACING OR WIRING MODULES; AND
- WARNING - EXPLOSION HAZARD - DO NOT DISCONNECT EQUIPMENT UNLESS POWER HAS BEEN SWITCHED OFF OR THE AREA IS KNOWN TO BE NONHAZARDOUS.
- EQUIPMENT LABELED WITH REFERENCE TO CLASS I, GROUPS A, B, C & D, DIV. 2 HAZARDOUS LOCATIONS IS SUITABLE FOR USE IN CLASS I, DIVISION 2, GROUPS A, B, C, D OR NON-HAZARDOUS LOCATIONS ONLY
- The tightening torque range for the control terminals is 9.6-11.5 in. lb. Use only wire rated for 90°C. Be sure to observe any additional ratings that are provided with the modules.
- Batteries: Replace Battery with Matsushita Part No. BR2477A Only. Use of another battery may present a risk of fire or explosion.” “Caution, Battery may explode if mistreated. Do Not recharge, disassemble or dispose of in fire”. The correct battery type is available as Accessory Kit IC698ACC701.