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USER MANUAL

CPU-71-17

VXS/VMEbus CPU board

First edition – September 2014 – B33036C0-MN002-00_UserMan_En_1

Preface

Thank you for choosing the CPU-71-17. Please read this manual before using the CPU-71-17 so that you may obtain the greatest benefit from using the device.

This manual presents the specifications, functions, and method of use of the CPU-71-17.

Eurotech has made every effort to carefully inspect each product and has taken great care to package and to ship the product. In the unlikely event of the product's failure to operate normally due to problems in shipping or otherwise, the company will repair or replace the product at its own responsibility.

If you have any questions, contact your local Eurotech Sales Office.

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Revision history

Revision	Description	Date
1	First release	2 September 2014

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1. Important User Information

In order to lower the risk of personal injury, electric shock, fire, or equipment damage, users must observe the following precautions as well as good technical judgment, whenever this product is installed or used.

All reasonable efforts have been made to ensure the accuracy of this document; however, Eurotech assumes no liability resulting from any error/omission in this document or from the use of the information contained herein.

Eurotech reserves the right to revise this document and to change its contents at any time without obligation to notify any person of such revision or changes. Reproduction of all or part of this document without Eurotech's permission is prohibited.

1.1 Safety Notices and Warnings

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Eurotech assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Eurotech is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Alerts that can be found throughout this manual

The following alerts are used within this manual and indicate potentially dangerous situations.

Danger, electrical shock hazard:
Information regarding potential electrical shock hazards:
- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Warning:
Information regarding potential hazards:
- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Information and/or Notes:
These will highlight important features or instructions that should be observed.

Protect the device from vibration and impact

Do not place the product in a location where it can fall or can be subject to vibration or impact because this may cause device failure.

Do not modify the device

For safety reasons, under no circumstances should you modify the device. Eurotech will not repair products that have been modified.

Protect the product from water and chemicals

Contact between the product and water or chemicals can result in product failure, electrocution, or fire.

Protect the product from foreign material

Make sure that foreign material does not get into the product during use, storage, or transport because this can result in product failure.

Use precautions in handling to ensure that you are not injured

The sharp projections on this product may cause injury. Take care in handling this product in order to avoid injury.

Do not disassemble the product

In order to maintain guaranteed product performance, do not disassemble this product under any circumstances.

Keep the product away from radios and TVs

Do not use the product near radios, television sets, or other devices generating strong magnetic or electrical fields. This could result in failure or malfunction.

Keep the product away from flame, humidity, and direct sunlight

Do not use or store the product in any of the following locations, as this could result in product failure:

- Places where there is fire
- Locations high in humidity or exposed to rain
- Locations exposed to direct sunlight
- Dusty or dirty locations
- Locations containing excessive water or chemical vapors

Install the product in well-ventilated locations

Install the product in well-ventilated locations to efficiently disperse heat generated by the product.

Remove the power plug from the receptacle when not using the product

Turn off the main switch and remove the power plug from the receptacle when not using the product or when there is the risk of lightning strike.

Use the device within rated parameters

Be sure to use the product within the ratings specified in this manual. Failure to do so may result in malfunction.

Use care when cleaning the product

If the product becomes dirty, wipe it with a dry soft cloth. A thinned neutral cleaner may be used if the product is particularly dirty. Do not use benzene, thinners, or other solvents under any circumstances.

Ground the product in order to prevent electrocution

Be sure to ground the product by connecting it to a 3-pole AC receptacle or by using an AC receptacle having a grounding terminal.

Dispose of the product properly

Use appropriate methods for handling industrial wastes when disposing of this product.

Wire the product correctly

Failure to wire the product correctly can result in malfunction or fire. Read this manual and wire the product correctly.

Use antistatic precautions

This product comprises electronic parts that are highly susceptible to static electricity. Static electricity can cause the product to malfunction. Take care not to touch any of the terminals, connectors, ICs, or other parts with the hands.

Do not use a malfunctioning product

Stop using the product if you believe it is malfunctioning. Continuing to use a malfunctioning product can cause the malfunction to spread to other products and can cause short circuits or fire.

1.2 Life Support Policy

Eurotech products are not authorized for use as critical components in life support devices or systems without the express written approval of Eurotech.

1.3 Warranty

For warranty terms and conditions users should contact their local Eurotech Sales Office.

Refer to the back covers of this manual for full contact details.

1.4 RoHS

This device, including all its components, subassemblies and the consumable materials that are an integral part of the product, has been manufactured in compliance with the European directive 2011/65/EU known as the RoHS directive (Restrictions on the use of certain Hazardous Substances). This directive targets the reduction of certain hazardous substances previously used in electrical and electronic equipment (EEE).

In the case of having VXS, contact the sales staff.

1.5 Technical Assistance

If you have any technical questions, cannot isolate a problem with your device, or have any enquiry about repair and returns policies, contact your local Eurotech Technical Support Team.

See the back cover for full contact details.

Transportation

When transporting any module or system, for any reason, it should be packed using anti-static material and placed in a sturdy box with enough packing material to adequately cushion it.

Warning:
Any product returned to Eurotech that is damaged due to inappropriate packaging will not be covered by the warranty.

1.6 Conventions

The following table describes the conventions for signal names used in this document.

Convention	Explanation
GND	Digital ground plane
#	Active low signal
+	Positive signal in differential pair
-	Negative signal in differential pair
NC	No connection
RSVD	Use is reserved to Eurotech

1.7 Electromagnetic Compatibility

This product is intended for industrial assembly only and is not for commercial use. Therefore, this product is not an apparatus and so does not need to be subject to the EMC Directive.

2. Summary

CPU-71-17 is a single board computer equipped with the 4th generation Intel Core ™ mobile processor conforming to VXS/VME bus standards. VXS enables high-speed serial communication while maintaining the existing VME bus properties. In VXS, communication speed between boards becomes theoretically 6.25 times faster than that of VME.

The 4th Intel Core ™ mobile processor uses 22nm process 3D transistor technology realizing improved performance of floating-point calculations by Intel AVX2.0 and enhanced security operation by Intel AES-NI.

The main memory contains memory with DDR3L ECC functions on board which assures high reliability. The maximum memory capacity is 8GB. One bit error among 72 bits can be automatically corrected and 2 bit errors can be detected.

I/O ports consist of mSATA, USB2.0, eUSB, XMC, PMC, Gigabit Ethernet, and Serial ports. As options, 3 ports to USB2.0, VGA or DisplayPort, and USB3.0 can be added.

OS currently supports Windows 7 and Wind River VxWorks. Also it will support Windows 8 and WindRiver Linux.

CPU-71-17 has the following features:

- 4th Generation Intel® Core ™ Processor
- ECC supported DDR3 memory direct-mounted on board (maximum capacity of memory: 8GB)
- Max 4 ports of USB2.0 interface
- 1 socket of mSATA interface
- 2 ports of 10/100/1000BASE-T ethernet
- 1 port RS-232C serial poart(RJ-45 connector)
- 2 slots PMC/XMC single size
- 1 port Analog VGA interface (*1)
- 1 port DisplayPort (*1)
- VME interface using the IDT PCI-VME bridge Tsi148
- VXS interface using the IDT PCIe-sRIO bridge Tsi721 (*1)
- RoHS compliant (2011/65/EU) (*2)

*1 : Mounting option

*2 : In the case of having VXS, contact the sales staff.

3. Specifications

Table 1. Board Specifications

Item	Specifications	
CPU	Processor	1. Intel® Core™ i7-4700EQ processor 4 core/8 threads 37W 2. Intel® Core™ i5-4402E processor 2 core /4 threads 25W 3. Intel® Core™ i3-4102E processor 2 core /4 threads 25W <Mounting option>
	Processor operation frequency	1. 2.4GHz (Turbo Boost, 3.4GHz max) 2. 1.6GHz (Turbo Boost, 2.7GHz max) 3. 1.6GHz
	L1 cache	1 to 3. 32kB for data, 32kB for instruction (per core)
	L2 cache	1 to 3. 256kB for data and instruction (per core)
	L3 cache	1. 6MB for data and instruction (shared by all cores) 2,3. 3MB for data and instruction (shared by all cores)
Memory	Boot ROM	SPI-FLASH memory, 16MB
	Main Memory	DDR3L-1600 SDRAM 4GB or 8GB ECC function support < Mounting option > It supports ECC, automatically corrects 1-bit error, and also detects 2-bit errors.
On board IO	mSATA	Serial ATA Revision 3.0 OS can be booted.
	eUSB	USB2.0 OS can be booted.
	PMC/XMC slot 1	IEEE1386.1 / VITA42.3 / VITA42.2, Single size (PMC) PCI32/64bit, 33/66MHz, VIO3.3V (XMC) PCIe Gen2 X4 lanes (*1), sRIO Gen2 4X lanes < Maximum power supply >: Up to15W in total for 2 slots < Maximum supply current >: As for 3.3V, up to 4A in total for 2 slots
	PMC/XMC slot 2	IEEE1386.1 / VITA42.3, Single size (PMC) PCI32/64bit, 33/66MHz, VIO3.3V (XMC) PCIe Gen2 X8 lanes (*1) < Maximum power supply >: Up to15W in total for 2 slots < Maximum supply current >: As for 3.3V, up to 4A in total for 2 slots
Front I/O	Ethernet	10/100/1000BASE-T, RJ-45 connector, 2 ports
	Serial port	RS232C, RJ-45 connector, 1 port
	USB	USB2.0, USB-Type A connector, 1 port
	Options 1 (*2) <CPU-71-17-Opt1>	USB2.0: 3 ports, USB2.0, USB-Type A connector Analog VGA: 1 port, 15 pins are high density D-sub connector
	Options 2 (*2) <CPU-71-17-Sub>	USB3.0: 1 port, USB3.0, USB-Type A connector DisplayPort: 1 port, DisplayPort connector
VME **P1/P2 connector**	VMEbus	VMEbus C.3 ANSI/VITA1-1994 VME64 ANSI/VITA1.1-1997 VME64 Extensions ANSI/VITA1.5-2003 2eSST
VXS **P0 connector**	VXS	ANSI/VITA41.2-2006 VXS Serial RapidIO Serial Rapid IO Gen2 4x: 2 ports 5.0, 3.125, 2.5, 1.25GBaud
Display・operation section	Front panel	Power status / Disk access LED(Green / Orange) sRIO link LED(Orange / Green) Reset switch
	On board	Clear CMOS jumper Post Battery holder for holding date and time data (CR2032)
RAS function	Watchdog timer	QM87 built-in function is used.
	Temperature monitor	CPU junction temperature, PCH junction temperature, Board surface temperature (upper part, lower part) can be monitored.

Item	Specifications	
Power source specifications	Power Supply	Powered from the P1 / P2 connector DC5V±5% (DC12V±5%) (DC-12V±5%) To use +12V or -12V power source at PMC slot, the same power supply is separately needed.)
	Current consumption	DC5V: 7.6A max (4402E, nVXS) DC5V: 9.2A max (4700EQ, nVXS) DC5V:11.6A max (4700EQ, VXS) (Without PMC / XMC both)
	Battery	Lithium primary battery CR2032 is used. Backup the CMOS area and real-time clock. Turn off the power for about three years retention. (25℃ at the time) Low battery voltage alarm bit. It is available without a battery.
Mechanical Specifications	Form Factor	6U, 4HP(1slot width) Ejector handle is used for the panel handle.
	Weight	500g
Environmental specifications	Operating temperature range	0 to 60℃(Air flow 2m/s or more) (*3)
	Operating humidity range	Under 95%RH(No condensation)
	Storage temperature range	-40 to 85℃
	Storage humidity range	Under 95%RH(No condensation)
Other	RoHS	Compliant(2011/65/EU)(*4)

*1 : Contact us for connecting PCI Express Gen3 device.

*2 : When option 1 or option 2 is chosen, PMC/XMC slot 2 cannot be used.

*3 : When selecting Corei7 4700EQ and using it at upper limit temperature 60℃, an air flow of 3m/s or more is required.

*4 : In the case of having VXS, contact the sales staff.

Table 2. Board Product Number

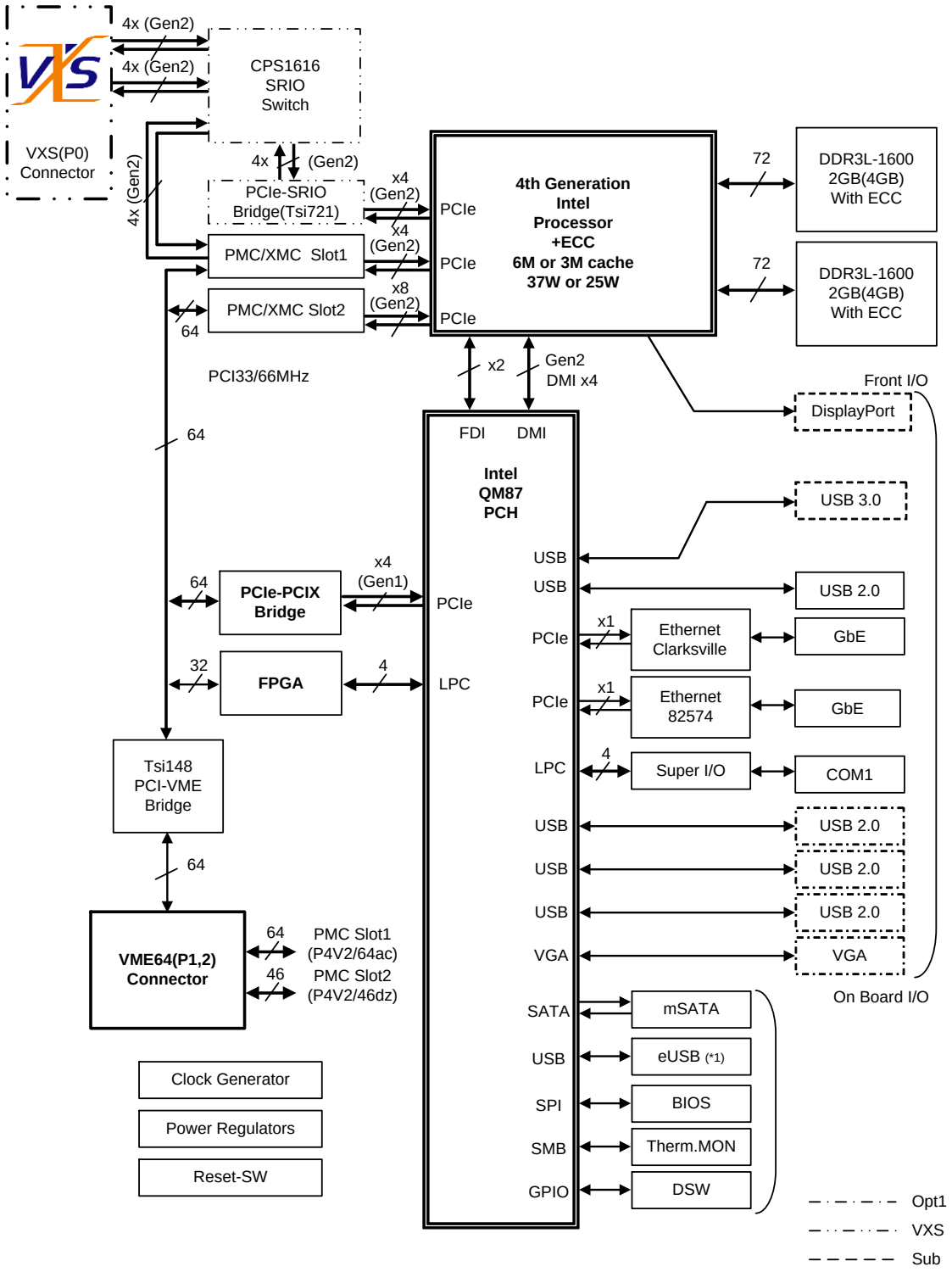
Product Number	Contents
CPU-71-17 Std (4700EQ,8GB,VXS) (*1)	Corei7 4700EQ, 8GB, VXS, PMC/XMC x2, USB x1
CPU-71-17 Std (4700EQ,4GB,nVXS) (*1,2)	Corei7 4700EQ, 4GB, VXS none, PMC/XMC x2, USB x1
CPU-71-17 Opt1(4402E,4GB,nVXS) (*2)	Corei5 4402E, 4GB, VXS none, PMC/XMC x1, USB x4,VGA
CPU-71-17 Sub	Sub board

*1 : eUSB is not equipped to Corei7 4700EQ.

*2 : VXS connector and sRIO I/F (TSI721, CPS1616) are not equipped in case of no VXS.

4. Block Diagram

CPU-71-17 Block Diagram is shown in Figure.1.



*1 : When Corei7 4700EQ is selected, eUSB cannot be used.

Figure 1. Block Diagram

5. Setting

5.1. Panel Components

Figure 2 indicates CPU-71-17-Std board component, and Figure 3 indicates CPU-71-17-Opt1 board component.

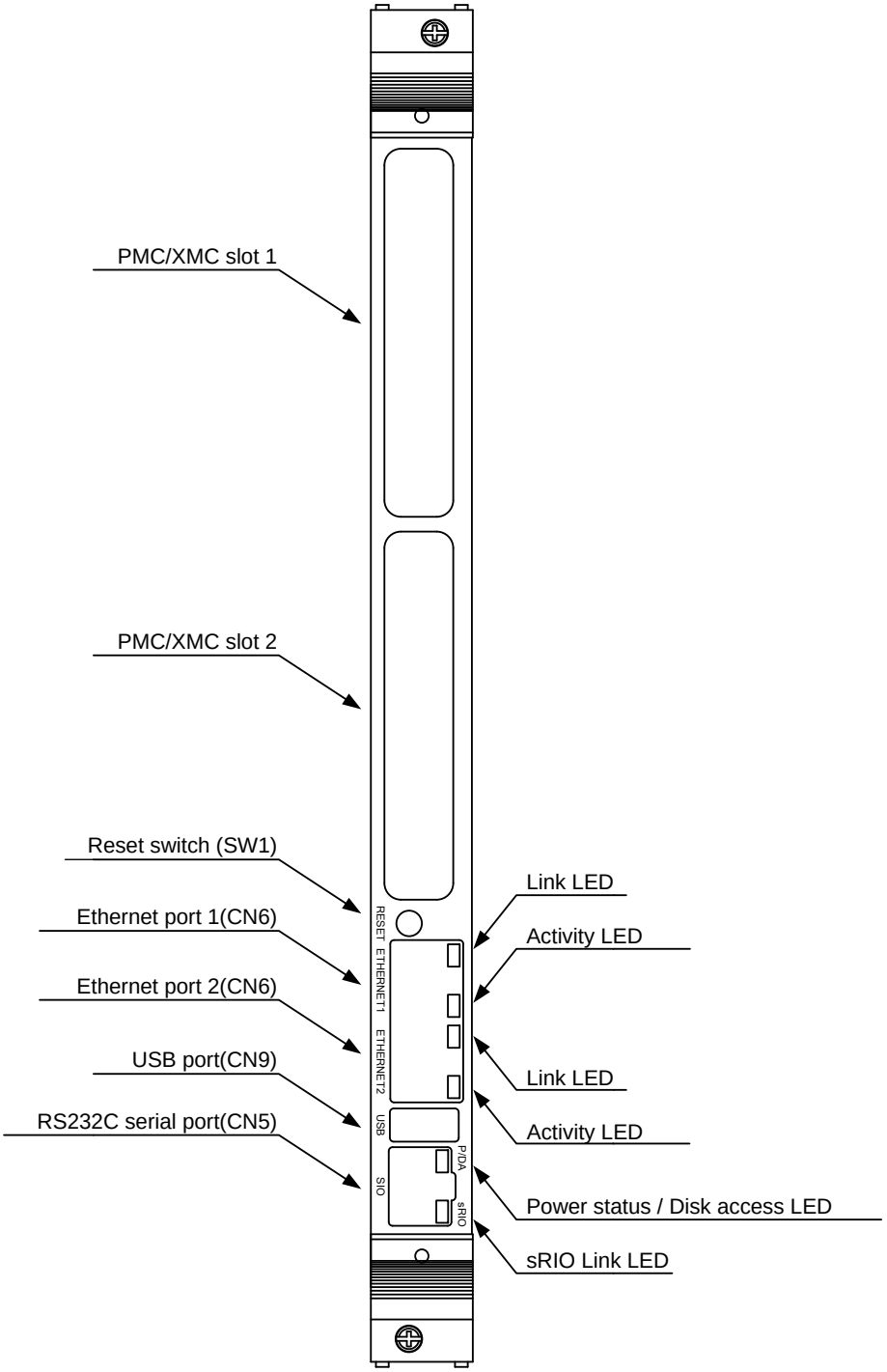


Figure 2. CPU-71-17-Std panel components

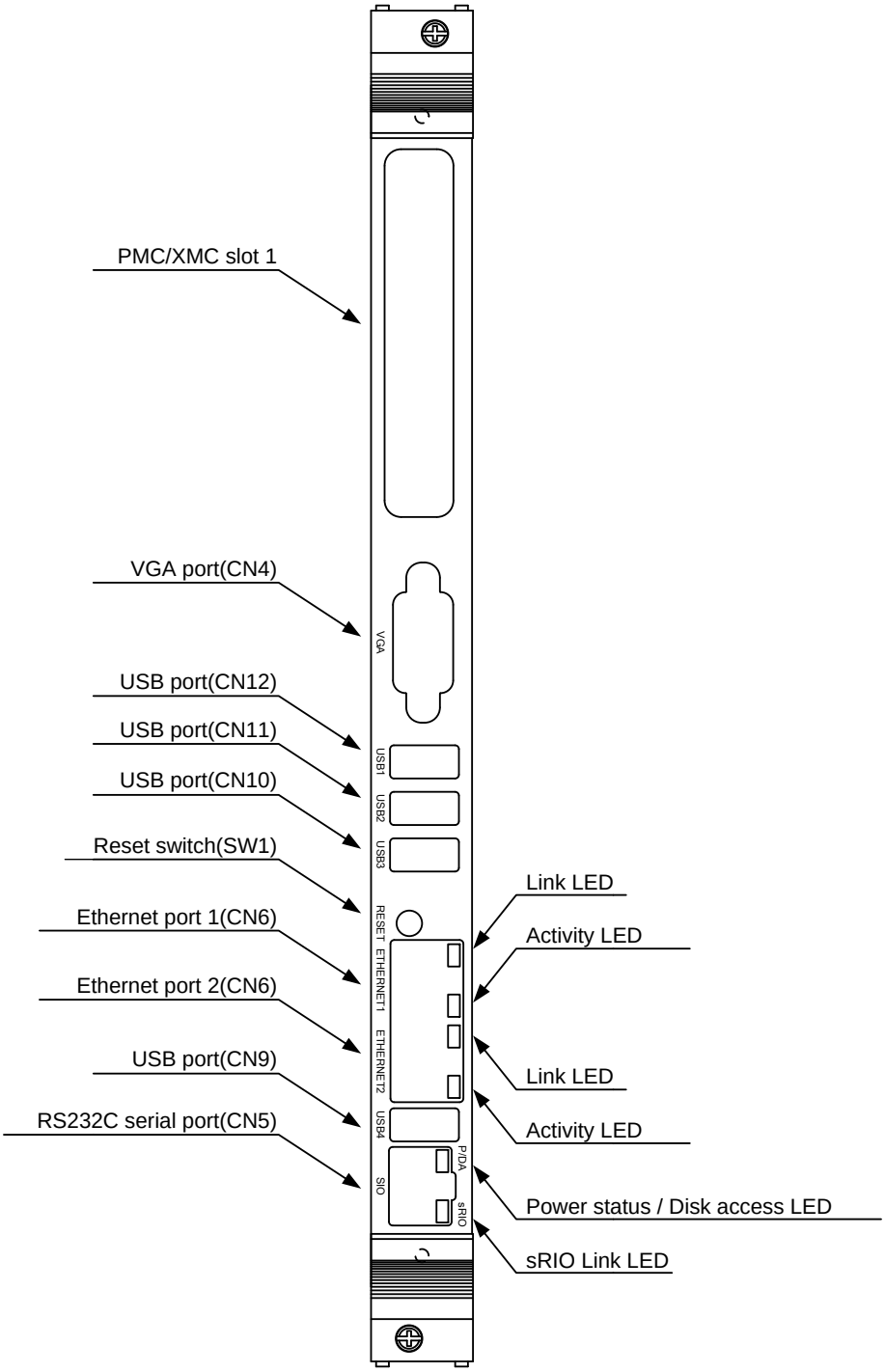


Figure 3. CPU-71-17-Opt1 panel components

5.1.1. Power status / Disk access LED

This is the status LED indicating the board's energized condition and mSATA/eUSB's disk access. LED indicator meanings are as follows.

Status	Power status / Disk access LED
Power off	OFF
Power on	Green ON
Disk access	Orange ON

5.1.2. sRIO link LED

This is the LED indicating VXS's sRIO link status. The LED indicator meanings are as follows.

Status	sRIO link LED
No link	OFF
Single-channel link	Orange ON
Both channels link	Green ON

5.1.3. Reset switch

Pressing the reset switch executes board reset in a single action.

When the reset switch is pushed, both this board and VME buses are reset. VME bus setting (reset/ no reset) is selectable according to DIP switch (SW3) setting.

5.1.4. USB port

This is the USB port connector. This port is controlled by QM87 PCH-integrated USB controller.

5.1.5. RS232C serial port

This is the RS232C serial port connector. This port is controlled by Super I/O. Supported baud rate is 115,200bps maximum. When you connect or disconnect to this connector please turn off the power.

5.1.6. Ethernet port 1,2

10/100/1000BASE-T Ethernet connector. The link LED turns on when the link is established, and the activity LED turns on in Yellow when transmission and reception take place.

5.1.7. PMC/XMC slot 1,2

It is a slot for equipping with a PMC/XMC module. A blank panel is provided so that the inside of the board is not exposed when a PMC/XMC module is not installed. Remove this when using a PMC/XMC module.

5.2. Sub board Components

Figure 4 and Figure 5 indicate CPU-71-17-Sub board components.

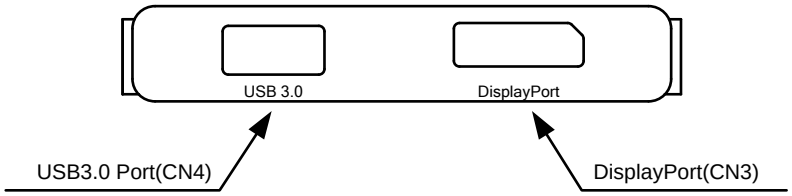


Figure 4. CPU-71-17 Sub panel components

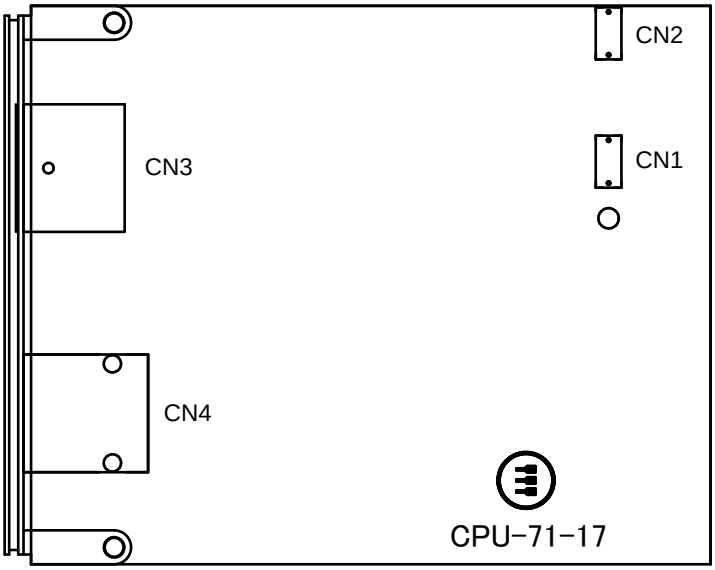


Figure 5. Component placement diagram

- CN1,2 : main board mounting connector
- CN3 : DisplayPort connector
- CN4 : USB3.0 port connector

5.2.1. USB Port

This is the USB 3.0 port connector. This port is controlled by QM87 PCH-integrated controller. USB3.0's SSC is set to OFF.

5.2.2. DisplayPort

This is the DisplayPort connector. This port is controlled by CPU-integrated display controller. It corresponds to DisplayPort 1.1a, and its maximum resolution is 2560x1600.

5.2.3. CN1,2 (main board mounting connector)

It interfits CN7, 8 of CPU-71-17 main board.

5.3. On board Components

Figure 6 indicate CPU-71-17 component placement diagram.

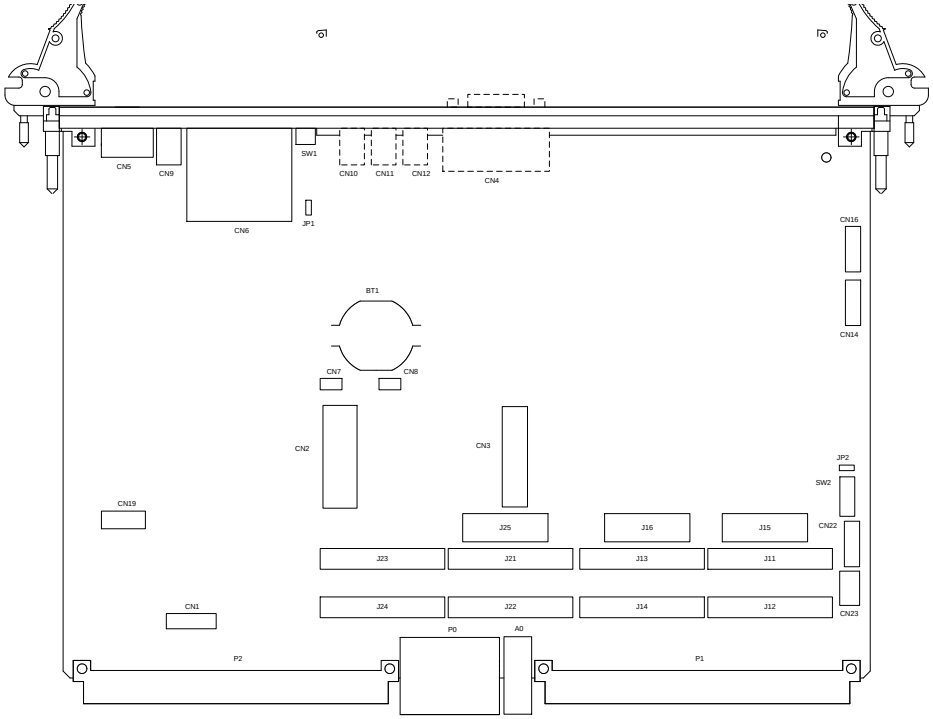


Figure 6. Component placement diagram

- CN1 : BIOS code writing connector (5.3.1. CN1(BIOS code writing connector) page 20)
- CN2,3 : mSATA SSD socket(5.3.2. CN2,3(mSATA SSD socket) page 20)
- CN4 : VGA connector (5.3.3. CN4(VGA connector) page 20)
- CN5 : Serial port connector (5.3.4. CN5(serial port connector) page 20)
- CN6 : Ethernet connector (5.3.5. CN6(Ethernet connector) page 20)
- CN7,8 : Options Sub Board mounting connector (5.3.6. CN7,8(Options Sub board mounting connector) page 20)
- CN9 to 12 : USB port connector (5.3.7. CN9 to 12(USB connector) page 20)
- CN14 : Internal control logic writing connector 1 (5.3.8. CN14(Internal control logic writing connector 1) page 21)
- CN16 : Internal control logic writing connector 2 (5.3.9. CN16(Internal control logic writing connector 2) page 21)
- CN19 : eUSB connector (5.3.10. CN19(eUSB connector) page 21)
- CN22 : Internal control firmware writing connector (5.3.11. CN22(Internal control firmware writing connector) page 21)

- CN23 : Internal control firmware writing connector (5.3.12. CN23(Internal control firmware debug connector) page 21)
- BT1 : CMOS backup battery (5.3.13. BT1(CMOS backup battery) page 21)
- SW1 : Reset switch(5.3.14. SW1(reset switch) page 21)
- SW2 : Clear CMOS / sRIO setting (5.3.15. SW2(Clear CMOS / sRIO setting) page 22)
- JP1 : RTCRST pin(5.3.16. JP1(RTCRST pin)page 22)
- JP2 : Internal control logic writing setting jumper (5.3.17. JP2(Internal control logic writing setting jumper) page 22)
- A0 : VXS positioning socket
- P0 : VXS connector (5.3.18. P0(VXS connector) page 22)
- P1,2 : VME bus connector
- J15,16 : XMC1 connector (5.3.19. J15~16,J25(XMC connector) page 22)
- J25 : XMC2 connector (5.3.19. J15~16,J25(XMC connector) page 22)
- J11-14 : PMC1 connector (5.3.20. J11~14, J21~24(PMC connector) page 23)
- J21-24 : PMC2 connector (5.3.20. J11~14, J21~24(PMC connector) page 23)

5.3.1. CN1(BIOS code writing connector)

CN1 is a connector for writing BIOS code to the on-board SPI-FLASH memory.

Do not connect anything during normal operation.

5.3.2. CN2,3(mSATA SSD socket)

CN2,3 are the mSATA SSD socket. Use SSD that conforms to Serial ATA mSATA standard. Do not conduct hot swapping. Part height of mSATA upper face is up to 2mm.

5.3.3. CN4(VGA connector)

CN4's maximum resolution is 1920x1080 using the VGA connector. It is an option , and PMC/XMC slot 2 cannot be used when installed. Do not conduct hot swapping.

5.3.4. CN5(serial port connector)

CN5 is the RS232C serial port connector.

5.3.5. CN6(Ethernet connector)

CN6 is the Ethernet connector of two ports.

5.3.6. CN7,8(Options Sub board mounting connector)

CN7,8 are the options sub PCB mounting connector.

By mounting an optional sub board, a DisplayPort output port and a USB3.0 host interface port can be added.

5.3.7. CN9 to 12(USB connector)

CN9 to 12 is the USB host interface connector.

Power current capacity that can be supplied to USB device is up to 500mA for each port. Exceeding this value, the overcurrent protection circuit activates and the USB device connected to the port cannot be used.

When overcurrent factors are removed, the protection circuit automatically recovers and the port can be used again.

CN10 to 12 are optional. It is a PMC/XMC slot 2 cannot be used when installed.

5.3.8. CN14(Internal control logic writing connector 1)

CN14 is a connector for writing programmable logic in the board.
Do not connect anything during normal operation.

5.3.9. CN16(Internal control logic writing connector 2)

CN16 is a connector for writing programmable logic in the board.
Do not connect anything during normal operation.

5.3.10. CN19(eUSB connector)

CN19 is an eUSB host interface connector. It can be connected to a 5V, standard profile Embedded USB Drive. ACT# pin's signalling level is 3.3V LVTTL and has 10kΩ on board pull-up.
Do not conduct hot swapping.

5.3.11. CN22(Internal control firmware writing connector)

CN22 is a connector for writing micro controller in the board.
Do not connect anything during normal operation.

5.3.12. CN23(Internal control firmware debug connector)

CN23 is a connector to debug the micro controller on the board.
Do not connect anything during normal operation.

5.3.13. BT1(CMOS backup battery)

BT1 is a holder to mount the battery for CMOS backup.
Battery to be used is CR2032.
Be aware of the following when mounting and removing the battery.

1. Do not touch the battery with a conductive object such as a screw driver.
   Using a conductive object is dangerous as it can cause the circuit or battery to short circuit.
2. Do not strongly impact the battery such as by dropping it.
3. Before replacing the battery, turn off the power source, and install the battery paying attention to the battery polarity.

CPU-71-17 is equipped with battery under voltage detection, and battery's status can be confirmed from PCH's GPIO34(GP_LVL2 register).

State	PCH GPIO34
Battery voltage is normal.	'1' = High
Battery voltage is low.	'0' = Low

- When using this without a battery, the following should be noted.
  - CMOS information, time, and date are cleared when power is turned off.
  - Do not mix CPU-71-17 with battery/without battery in the same rack.

5.3.14. SW1(reset switch)

SW1 is the board reset switch.
Pressing the SW1 executes board reset in a single action.

5.3.15. SW2(Clear CMOS / sRIO setting)

SW2 setting is indicated in Table 3.

Bit8 is a switch to return BIOS's individual settings to initial values. Bit8 usage is not usually required, so use it with power OFF. Only when the BIOS setup screen is not displayed due to improper operations, etc., clear CMOS as described below.

(1) Turn off power to the CPU-71-17.

(2) Turn on SW2 Bit8.

(3) When the CPU-71-17 turns on, BIOS's individual settings start up at initial values.

(4) Turn off power and turn off the SW2 Bit8.

Bit1 to 7 are switches to set sRIO bridge Tsi721. When Bit1 is turned ON, SLAVE activates, and when OFF, HOST activates. Bit2 is the initial value setting of destination ID. Turning ON when Slave is activating, it becomes 0xFE, and turning OFF, it becomes 0xFF. Turning ON when Host is activating, it becomes 0x00, and turning OFF, it becomes 0x01. When turning Bit3 ON, I^2C EEPROM is read when starting up to perform register settings. It is usually used with ON. Bit4-6 is communication speed setting. Bit7 is sRIO boot setting. It is usually used with OFF.

Table 3. SW2 Setting

SW2	Function	ON(1)	OFF(0)
Bit1	SP_HOST	SLAVE	HOST
Bit2	SP_DEVID	0/FE	1/FF
Bit3	I^2C_LOAD	Enable	Disable
Bit4 **Bit5** **Bit6**	STRAP_RATE[0] STRAP_RATE[1] STRAP_RATE[2]	[2] [1] [0] 1 1 1 1.25 Gbaud 1 1 0 2.5 Gbaud 1 0 1 5.0 Gbaud 0 1 0 3.125 Gbaud	
Bit7	SR_BOOT	AUTO	MANUAL
Bit8	CMOS_CLEAR	Enable	Disable

5.3.16. JP1(RTCRST pin)

JP1 is connected to QM87's RTCRST#.

Do not connect anything during normal operation.

5.3.17. JP2(Internal control logic writing setting jumper)

JP2 is a jumper used when writing the programmable logic in the board.

Do not connect anything during normal operation.

5.3.18. P0(VXS connector)

This is a connector to connect with VXS back plane. In CPU-71-17, sRIO signal is connected. It can communicate with payload card and switch card that conform to VITA41.2 standards.

This is not equipped when VXS does not exist.

5.3.19. J15~16,J25(XMC connector)

This is a connector to install XMC module. PCI Express Gen1 and Gen2 XMC module can be used. XMC slot 1 corresponds to x4 links. XMC slot 2 corresponds to x8 links.

When VXS exists, sRIO signal is connected to XMC slot 1. (J16 connector) To use the XMC module using the P16 connector with CPU-71-17, confirm the signal is for sRIO.

When VXS does not exist, J16 connector is not equipped.

5.3.20. J11~14, J21~24(PMC connector)

This is a connector to install PMC module.

PCI bus in this board is directly connected to PMC connector.

Signalling voltage 3.3V PMC module can be used with this board. Refer to Table 1: Specification List for details.

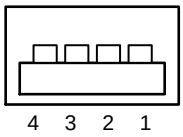
PMC slot 1's use I/O pin (equivalent to J14) connects all 64 pins to A and C columns of P2 connector. Also, PMC slot 2's I/O pin (equivalent to J24) connects 46 pins to D and Z columns of P2 connector. Refer to Chapter 6.6 to 6.10 for each pin assignment. When using the PMC module using P4 connector signal, confirm how corresponding signals on the back plane are connected before using.

6. Connector

6.1. USB Connector (USB)

Connector used: JST UBAL-4R-D14-4S(LF)(SN)

Pin	Name
1	+5V
2	-DATA
3	+DATA
4	GND

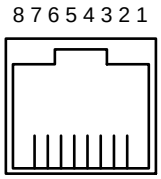


(Panel)

6.2. Serial ports (COM1)

Connector used: HIROSE TM11R-5M2-88-LP(33)

Pin	Name
1	DCD
2	RTS
3	GND
4	TXD
5	RXD
6	GND
7	CTS
8	DTR



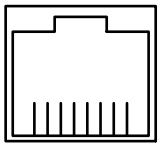
(Panel)

6.3. Ethernet Connector (ETHERNET1,2)

Connector used: BELFUSE 0826-1X2T-23-F

Pin	Name
1	A+
2	A-
3	B+
4	C+
5	C-
6	B-
7	D+
8	D-

8 7 6 5 4 3 2 1



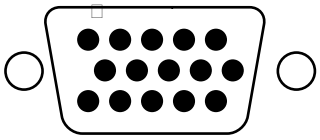
(Panel)

6.4. VGA Connector (VGA)

Connector used: JST KEY-15S-2A3A[LF][SN]

Pin	Name
1	RED
2	GRN
3	BLU
4	NC
5	GND
6	GND
7	GND
8	GND
9	5V
10	GND
11	NC
12	I2C_DAT
13	HSYNC
14	VSYNC
15	I2C_CK

5 ... 1
10 ... 6
15 ... 11



(Panel)

6.5. mSATA Connector (CN2)

Connector used: JAE MM60-52B1-B1

Pin	Name	Pin	Name
1	NC	**27**	GND
2	+3.3V	**28**	+1.5V
3	NC	**29**	GND
4	GND	**30**	TWI
5	NC	**31**	-A
6	+1.5V	**32**	TWI
7	NC	**33**	+A
8	NC	**34**	GND
9	GND	**35**	GND
10	NC	**36**	NC
11	NC	**37**	GND
12	NC	**38**	NC
13	NC	**39**	+3.3V
14	NC	**40**	GND
15	GND	**41**	+3.3V
16	NC	**42**	NC
17	NC	**43**	NC
18	GND	**44**	GND
19	NC	**45**	NC
20	NC	**46**	NC
21	GND	**47**	NC
22	NC	**48**	+1.5V
23	+B	**49**	NC
24	+3.3V	**50**	GND
25	-B	**51**	NC
26	GND	**52**	+3.3V

6.6. PMC J11(J21) Connector

Connector used: KYOCERA ELCO 24-5015-064-100-861+

Pin	Name	Pin	Name
1	NC	**2**	-12V
3	GND	**4**	INTA#
5	INTB#	**6**	INTC#
7	BUSMODE1#	**8**	+5V
9	INTD#	**10**	NC
11	GND	**12**	NC
13	PCICLK	**14**	GND
15	GND	**16**	GNT#
17	REQ#	**18**	+5V
19	+3.3V(VIO)	**20**	AD31
21	AD28	**22**	AD27
23	AD25	**24**	GND
25	GND	**26**	C/BE3#
27	AD22	**28**	AD21
29	AD19	**30**	+5V
31	+3.3V(VIO)	**32**	AD17
33	FRAME#	**34**	GND
35	GND	**36**	IRDY#
37	DEVSEL#	**38**	+5V
39	GND	**40**	LOCK#
41	SDONE#	**42**	SBO#
43	PAR	**44**	GND
45	+3.3V(VIO)	**46**	AD15
47	AD12	**48**	AD11
49	AD9	**50**	+5V
51	GND	**52**	C/BE0#
53	AD6	**54**	AD5
55	AD4	**56**	GND
57	+3.3V(VIO)	**58**	AD3
59	AD2	**60**	AD1
61	AD0	**62**	+5V
63	GND	**64**	REQ64#

6.7. PMC J12(J22) Connector

Connector used: KYOCERA ELCO 24-5015-064-100-861+

Pin	Name	Pin	Name
1	+12V	**2**	NC
3	NC	**4**	NC
5	NC	**6**	GND
7	GND	**8**	NC
9	NC	**10**	NC
11	BUSMODE2#	**12**	+3.3V(VIO)
13	RST#	**14**	BUSMODE3#
15	+3.3V(VIO)	**16**	BUSMODE4#
17	PME#	**18**	GND
19	AD30	**20**	AD29
21	GND	**22**	AD26
23	AD24	**24**	+3.3V(VIO)
25	IDSEL	**26**	AD23
27	+3.3V(VIO)	**28**	AD20
29	AD18	**30**	GND
31	AD16	**32**	C/BE2#
33	GND	**34**	NC
35	TRDY#	**36**	+3.3V(VIO)
37	GND	**38**	STOP#
39	PERR#	**40**	GND
41	+3.3V(VIO)	**42**	SERR#
43	C/BE1#	**44**	GND
45	AD14	**46**	AD13
47	M66EN	**48**	AD10
49	AD8	**50**	+3.3V(VIO)
51	AD7	**52**	NC
53	+3.3V(VIO)	**54**	NC
55	NC	**56**	GND
57	NC	**58**	NC
59	GND	**60**	NC
61	ACK64#	**62**	+3.3V(VIO)
63	GND	**64**	NC

6.8. PMC J13(J23) Connector

Connector used: KYOCERA ELCO 24-5015-064-100-861+

Pin	Name	Pin	Name
1	NC	**2**	GND
3	GND	**4**	C/BE7#
5	C/BE6#	**6**	C/BE5#
7	C/BE4#	**8**	GND
9	+3.3V(VIO)	**10**	PAR64
11	AD63	**12**	AD62
13	AD61	**14**	GND
15	GND	**16**	AD60
17	AD59	**18**	AD58
19	AD57	**20**	GND
21	+3.3V(VIO)	**22**	AD56
23	AD55	**24**	AD54
25	AD53	**26**	GND
27	GND	**28**	AD52
29	AD51	**30**	AD50
31	AD49	**32**	GND
33	GND	**34**	AD48
35	AD47	**36**	AD46
37	AD45	**38**	GND
39	+3.3V(VIO)	**40**	AD44
41	AD43	**42**	AD42
43	AD41	**44**	GND
45	GND	**46**	AD40
47	AD39	**48**	AD38
49	AD37	**50**	GND
51	GND	**52**	AD36
53	AD35	**54**	AD34
55	AD33	**56**	GND
57	+3.3V(VIO)	**58**	AD32
59	NC	**60**	NC
61	NC	**62**	GND
63	GND	**64**	NC

6.9. PMC J14 Connector

Connector used: KYOCERA ELCO 24-5015-064-100-861+

Pin	Name	Pin	Name
1	J14_1(VME-P2-1C)	**2**	J14_2(VME-P2-1A)
3	J14_3(VME-P2-2C)	**4**	J14_4(VME-P2-2A)
5	J14_5(VME-P2-3C)	**6**	J14_6(VME-P2-3A)
7	J14_7(VME-P2-4C)	**8**	J14_8(VME-P2-4A)
9	J14_9(VME-P2-5C)	**10**	J14_10(VME-P2-5A)
11	J14_11(VME-P2-6C)	**12**	J14_12(VME-P2-6A)
13	J14_13(VME-P2-7C)	**14**	J14_14(VME-P2-7A)
15	J14_15(VME-P2-8C)	**16**	J14_16(VME-P2-8A)
17	J14_17(VME-P2-9C)	**18**	J14_18(VME-P2-9A)
19	J14_19(VME-P2-10C)	**20**	J14_20(VME-P2-10A)
21	J14_21(VME-P2-11C)	**22**	J14_22(VME-P2-11A)
23	J14_23(VME-P2-12C)	**24**	J14_24(VME-P2-12A)
25	J14_25(VME-P2-13C)	**26**	J14_26(VME-P2-13A)
27	J14_27(VME-P2-14C)	**28**	J14_28(VME-P2-14A)
29	J14_29(VME-P2-15C)	**30**	J14_30(VME-P2-15A)
31	J14_31(VME-P2-16C)	**32**	J14_32(VME-P2-16A)
33	J14_33(VME-P2-17C)	**34**	J14_34(VME-P2-17A)
35	J14_35(VME-P2-18C)	**36**	J14_36(VME-P2-18A)
37	J14_37(VME-P2-19C)	**38**	J14_38(VME-P2-19A)
39	J14_39(VME-P2-20C)	**40**	J14_40(VME-P2-20A)
41	J14_41(VME-P2-21C)	**42**	J14_42(VME-P2-21A)
43	J14_43(VME-P2-22C)	**44**	J14_44(VME-P2-22A)
45	J14_45(VME-P2-23C)	**46**	J14_46(VME-P2-23A)
47	J14_47(VME-P2-24C)	**48**	J14_48(VME-P2-24A)
49	J14_49(VME-P2-25C)	**50**	J14_50(VME-P2-25A)
51	J14_51(VME-P2-26C)	**52**	J14_52(VME-P2-26A)
53	J14_53(VME-P2-27C)	**54**	J14_54(VME-P2-27A)
55	J14_55(VME-P2-28C)	**56**	J14_56(VME-P2-28A)
57	J14_57(VME-P2-29C)	**58**	J14_58(VME-P2-29A)
59	J14_59(VME-P2-30C)	**60**	J14_60(VME-P2-30A)
61	J14_61(VME-P2-31C)	**62**	J14_62(VME-P2-31A)
63	J14_63(VME-P2-32C)	**64**	J14_64(VME-P2-32A)

6.10. PMC J24 Connector

Connector used: KYOCERA ELCO 24-5015-064-100-861+

Pin	Name	Pin	Name
1	J24_1(VME-P2-D1)	2	J24_2(VME-P2-Z1)
3	J24_3(VME-P2-D2)	4	J24_4(VME-P2-D3)
5	J24_5(VME-P2-Z3)	6	J24_6(VME-P2-D4)
7	J24_7(VME-P2-D5)	8	J24_8(VME-P2-Z5)
9	J24_9(VME-P2-D6)	10	J24_10(VME-P2-D7)
11	J24_11(VME-P2-Z7)	12	J24_12(VME-P2-D8)
13	J24_13(VME-P2-D9)	14	J24_14(VME-P2-Z9)
15	J24_15(VME-P2-D10)	16	J24_16(VME-P2-D11)
17	J24_17(VME-P2-Z11)	18	J24_18(VME-P2-D12)
19	J24_19(VME-P2-D13)	20	J24_20(VME-P2-Z13)
21	J24_21(VME-P2-D14)	22	J24_22(VME-P2-D15)
23	J24_23(VME-P2-Z15)	24	J24_24(VME-P2-D16)
25	J24_25(VME-P2-D17)	26	J24_26(VME-P2-Z17)
27	J24_27(VME-P2-D18)	28	J24_28(VME-P2-D19)
29	J24_29(VME-P2-Z19)	30	J24_30(VME-P2-D20)
31	J24_31(VME-P2-D21)	32	J24_32(VME-P2-Z21)
33	J24_33(VME-P2-D22)	34	J24_34(VME-P2-D23)
35	J24_35(VME-P2-Z23)	36	J24_36(VME-P2-D24)
37	J24_37(VME-P2-D25)	38	J24_38(VME-P2-Z25)
39	J24_39(VME-P2-D26)	40	J24_40(VME-P2-D27)
41	J24_41(VME-P2-Z27)	42	J24_42(VME-P2-D28)
43	J24_43(VME-P2-D29)	44	J24_44(VME-P2-Z29)
45	J24_45(VME-P2-D30)	46	J24_46(VME-P2-Z31)
47	NC	48	NC
49	NC	50	NC
51	NC	52	NC
53	NC	54	NC
55	NC	56	NC
57	NC	58	NC
59	NC	60	NC
61	NC	62	NC
63	NC	64	NC

6.11. XMC J15 Connector

Connector used: SAMTEC ASP-103612-02

Pin	A	B	C	D	E	F
1	PET0p0	PET0n0	+3.3V	PET0p1	PET0n1	+5V
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	+3.3V	PET0p3	PET0n3	+5V
4	GND	GND	TCK	GND	GND	NC
5	NC	NC	+3.3V	NC	NC	+5V
6	GND	GND	TMS	GND	GND	+12V
7	NC	NC	+3.3V	NC	NC	+5V
8	GND	GND	TDI	GND	GND	-12V
9	NC	NC	NC	NC	NC	+5V
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	NC	PER0p1	PER0n1	+5V
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	+3.3V	PER0p3	PER0n3	+5V
14	GND	GND	GA2	GND	GND	MSDA
15	NC	NC	NC	NC	NC	+5V
16	GND	GND	MVMRO	GND	GND	MSCL
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK+0	REFCLK-0	NC	WAKE#	ROOT0#	NC

6.12. XMC J16 Connector

Connector used: SAMTEC ASP-103612-02

Pin	A	B	C	D	E	F
1	S0_TD0+	S0_TD0-	XMC_GEN1_LINK	S0_TD1+	S0_TD1-	NC
2	GND	GND	XMC_GEN2_LINK	GND	GND	NC
3	S0_TD2+	S0_TD2-	RP_SDA	S0_TD3+	S0_TD3-	NC
4	GND	GND	RP_SCL	GND	GND	NC
5	NC	NC	CPS1616_TCK	NC	NC	NC
6	GND	GND	CPS1616_TRST#	GND	GND	NC
7	NC	NC	CPS1616_TDI	NC	NC	NC
8	GND	GND	CPS1616_TMS	GND	GND	NC
9	NC	NC	CPS1616_TDO	NC	NC	NC
10	GND	GND	TSI721_TCK	GND	GND	NC
11	S0_RD0+	S0_RD0-	TSI721_TRST#	S0_RD1+	S0_RD1-	NC
12	GND	GND	TSI721_TDI	GND	GND	NC
13	S0_RD2+	S0_RD2-	TSI721_TMS	S0_RD3+	S0_RD3-	NC
14	GND	GND	TSI721_TDO	GND	GND	NC
15	NC	NC	NC	NC	NC	NC
16	GND	GND	NC	GND	GND	NC
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	NC	NC	NC	NC	NC	NC

6.13. XMC J25 Connector

Connector used: SAMTEC ASP-103612-02

Pin	A	B	C	D	E	F
1	PET0p0	PET0n0	+3.3V	PET0p1	PET0n1	+5V
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	+3.3V	PET0p3	PET0n3	+5V
4	GND	GND	TCK	GND	GND	NC
5	PET0p4	PET0n4	+3.3V	PET0p5	PET0n5	+5V
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	+3.3V	PET0p7	PET0n7	+5V
8	GND	GND	TDI	GND	GND	-12V
9	NC	NC	NC	NC	NC	+5V
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	NC	PER0p1	PER0n1	+5V
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	+3.3V	PER0p3	PER0n3	+5V
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC	PER0p5	PER0n5	+5V
16	GND	GND	MVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	NC	PER0p7	PER0n7	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK+0	REFCLK-0	NC	WAKE#	ROOT0#	NC

6.14. VME P1 Connector

Connector used: HARTING 0201-160-2101

Pin	Row z	Row a	Row b	Row c	Row d
1	NC	D0	BBSY#	D8	+5V
2	GND	D1	BCLR#	D9	GND
3	NC	D2	ACFAIL#	D10	NC
4	GND	D3	BGI0#	D11	NC
5	NC	D4	BGO0#	D12	NC
6	GND	D5	BGI1#	D13	NC
7	NC	D6	BGO1#	D14	NC
8	GND	D7	BGI2#	D15	NC
9	NC	GND	BGO2#	GND	GAP#
10	GND	SYSCLK	BGI3#	SYSFAIL#	GA0#
11	NC	GND	BGO3#	BERR#	GA1#
12	GND	DS1#	BR0#	SYSRESET#	NC
13	NC	DS0#	BR1#	LWORD#	GA2#
14	GND	WRITE#	BR2#	AM5	NC
15	NC	GND	BR3#	A23	GA3#
16	GND	DTACK#	AM0	A22	NC
17	NC	GND	AM1	A21	GA4#
18	GND	AS#	AM2	A20	NC
19	NC	GND	AM3	A19	NC
20	GND	IACK#	GND	A18	NC
21	NC	IACKIN#	NC	A17	NC
22	GND	IACKOUT#	NC	A16	NC
23	NC	AM4	GND	A15	NC
24	GND	A7	IRQ7#	A14	NC
25	NC	A6	IRQ6#	A13	NC
26	GND	A5	IRQ5#	A12	NC
27	NC	A4	IRQ4#	A11	NC
28	GND	A3	IRQ3#	A10	NC
29	NC	A2	IRQ2#	A9	NC
30	GND	A1	IRQ1#	A8	NC
31	NC	-12V	NC	+12V	GND
32	GND	+5V	+5V	+5V	+5V

6.15. VME P2 Connector

Connector used: HARTING 0201-160-2101

Pin	Row z	Row a	Row b	Row c	Row d
1	J24_2(PMC-P24-2)	J14_2(PMC-P14-2)	+5V	J14_1(PMC-P14-1)	J24_1(PMC-P24-1)
2	GND	J14_4(PMC-P14-4)	GND	J14_3(PMC-P14-3)	J24_3(PMC-P24-3)
3	J24_5(PMC-P24-5)	J14_6(PMC-P14-6)	RETRY#	J14_5(PMC-P14-5)	J24_4(PMC-P24-4)
4	GND	J14_8(PMC-P14-8)	A24	J14_7(PMC-P14-7)	J24_6(PMC-P24-6)
5	J24_8(PMC-P24-8)	J14_10(PMC-P14-10)	A25	J14_9(PMC-P14-9)	J24_7(PMC-P24-7)
6	GND	J14_12(PMC-P14-12)	A26	J14_11(PMC-P14-11)	J24_9(PMC-P24-9)
7	J24_11(PMC-P24-11)	J14_14(PMC-P14-14)	A27	J14_13(PMC-P14-13)	J24_10(PMC-P24-10)
8	GND	J14_16(PMC-P14-16)	A28	J14_15(PMC-P14-15)	J24_12(PMC-P24-12)
9	J24_14(PMC-P24-14)	J14_18(PMC-P14-18)	A29	J14_17(PMC-P14-17)	J24_13(PMC-P24-13)
10	GND	J14_20(PMC-P14-20)	A30	J14_19(PMC-P14-19)	J24_15(PMC-P24-15)
11	J24_17(PMC-P24-17)	J14_22(PMC-P14-22)	A31	J14_21(PMC-P14-21)	J24_16(PMC-P24-16)
12	GND	J14_24(PMC-P14-24)	GND	J14_23(PMC-P14-23)	J24_18(PMC-P24-18)
13	J24_20(PMC-P24-20)	J14_26(PMC-P14-26)	+5V	J14_25(PMC-P14-25)	J24_19(PMC-P24-19)
14	GND	J14_28(PMC-P14-28)	D16	J14_27(PMC-P14-27)	J24_21(PMC-P24-21)
15	J24_23(PMC-P24-23)	J14_30(PMC-P14-30)	D17	J14_29(PMC-P14-29)	J24_22(PMC-P24-22)
16	GND	J14_32(PMC-P14-32)	D18	J14_31(PMC-P14-31)	J24_24(PMC-P24-24)
17	J24_26(PMC-P24-26)	J14_34(PMC-P14-34)	D19	J14_33(PMC-P14-33)	J24_25(PMC-P24-25)
18	GND	J14_36(PMC-P14-36)	D20	J14_35(PMC-P14-35)	J24_27(PMC-P24-27)
19	J24_29(PMC-P24-29)	J14_38(PMC-P14-38)	D21	J14_37(PMC-P14-37)	J24_28(PMC-P24-28)
20	GND	J14_40(PMC-P14-40)	D22	J14_39(PMC-P14-39)	J24_30(PMC-P24-30)
21	J24_32(PMC-P24-32)	J14_42(PMC-P14-42)	D23	J14_41(PMC-P14-41)	J24_31(PMC-P24-31)
22	GND	J14_44(PMC-P14-44)	GND	J14_43(PMC-P14-43)	J24_33(PMC-P24-33)
23	J24_35(PMC-P24-35)	J14_46(PMC-P14-46)	D24	J14_45(PMC-P14-45)	J24_34(PMC-P24-34)
24	GND	J14_48(PMC-P14-48)	D25	J14_47(PMC-P14-47)	J24_36(PMC-P24-36)
25	J24_38(PMC-P24-38)	J14_50(PMC-P14-50)	D26	J14_49(PMC-P14-49)	J24_37(PMC-P24-37)
26	GND	J14_52(PMC-P14-52)	D27	J14_51(PMC-P14-51)	J24_39(PMC-P24-39)
27	J24_41(PMC-P24-41)	J14_54(PMC-P14-54)	D28	J14_53(PMC-P14-53)	J24_40(PMC-P24-40)
28	GND	J14_56(PMC-P14-56)	D29	J14_55(PMC-P14-55)	J24_42(PMC-P24-42)
29	J24_44(PMC-P24-44)	J14_58(PMC-P14-58)	D30	J14_57(PMC-P14-57)	J24_43(PMC-P24-43)
30	GND	J14_60(PMC-P14-60)	D31	J14_59(PMC-P14-59)	J24_45(PMC-P24-45)
31	J24_46(PMC-P24-46)	J14_62(PMC-P14-62)	GND	J14_61(PMC-P14-61)	GND
32	GND	J14_64(PMC-P14-64)	+5V	J14_63(PMC-P14-63)	+5V

6.16. VXS P0 Connector

Connector used: TYCO 1410147

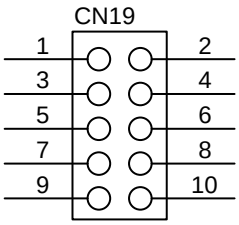
Payload side

Pin	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	NC	GND	PA_TX0-	PA_TX0+	GND	PA_RX0-	PA_RX0+
2	GND	PA_TX1-	PA_TX1+	GND	PA_RX1-	PA_RX1+	GND
3	NC	GND	PA_TX2-	PA_TX2+	GND	PA_RX2-	PA_RX2+
4	GND	PA_TX3-	PA_TX3+	GND	PA_RX3-	PA_RX3+	GND
5	NC	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	NC	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	NC	GND	NC	NC	GND	NC	NC
12	GND	PB_TX0-	PB_TX0+	GND	PB_RX0-	PB_RX0+	GND
13	NC	GND	PB_TX1-	PB_TX1+	GND	PB_RX1-	PB_RX1+
14	GND	PB_TX2-	PB_TX2+	GND	PB_RX2-	PB_RX2+	GND
15	NC	GND	PB_TX3-	PB_TX3+	GND	PB_RX3-	PB_RX3+

6.17. eUSB CN19 Connector

Connector used: SAMTEC TSM-105-01-S-DV-P-TR

Pin	Name
1	+5V
2	NC
3	-DATA
4	NC
5	+DATA
6	NC
7	GND
8	NC
9	NC
10	ACT#



7. Address Map

7.1. I/O space

I/O space Address Map is shown in Table 4.
PCI device that can be freely configured in the memory space is not listed in this table.

Table 4. I/O space Address Map

Address		Device
0000h - 001Fh	PCH Registers	DMA Controller
0020h - 002Dh		Interrupt Controller
002Eh - 002Fh	Super I/O Registers	
0030h - 003Dh	PCH Registers	Interrupt Controller
0040h - 0043h		Timer/Counter
004Eh - 004Fh		LPC SIO
0050h - 0053h		Timer/Counter
0060h		Microcontroller
0061h		NMI Controller
0062h - 0066h		Microcontroller
0070h - 0077h		RTC Controller
0080h - 0091h		DMA Controller
0092h		Reset Generator
0093h - 009Fh		DMA Controller
00A0h - 00B1h		Interrupt Controller
00B2h - 00B3h		Power Management
00B4h - 00BDh		Interrupt Controller
00C0h - 00DFh		DMA Controller
00F0h		FERR# / Interrupt Controller
0170h - 0177h		Serial ATA
01F0h - 01F7h		Serial ATA
0200h – 020Fh		Game port
0280h – 028Fh	Reserved	
0376h	PCH Register	Serial ATA
03F6h		Serial ATA
04D0h - 04D1h		Interrupt Controller
0CF9h		Reset Generator

7.2. Memory space

Memory space Address Map is shown in Table 5.

Table 5. Memory space Address Map

Address	Device	
0000 0000h ~0009 FFFFh	Main Memory (640kB)	
000A 0000h ~000B FFFFh	VGA Frame Buffer (128kB)	
000C 0000h ~000D FFFFh	Boot ROM or Main Memory (192kB)	
000E 0000h ~000F FFFFh	PCH	Boot ROM (SPI) (128kB)
0010_0000h ~ TSEGMB (*1)	Main Memory	
TSEGMB ~TOLUD (*2)	CPU	Internal Graphics
TOLUD ~DFFF FFFFh	PCI Memory Range	
E000 0000h ~EFFF FFFFh	PCI Express Configuration Space(256MB)	
F000 0000h ~FEBF FFFFh	CPU	DMI Interface(236MB)
FEC0 0000h ~FEC0 0040h	PCH	I/O APIC inside PCH
FEC1 0000h ~FEC1 7FFFh		PCI Express Port 1
FEC1 8000h ~FEC4 7FFFh	APIC Configuration Space	
FEC4 8000h ~FEC4 FFFFh	PCH	PCI Express Port 8
FEC5 0000 ~FEC7 FFFFh	APIC Configuration Space	
FEC8 0000h ~FECF FFFFh	CPU	CPU APIC
FED0 X000h ~FED0 X3FFh (*3)	PCH	High Precision Event Timers
FED4 0000h ~FED4 BFFFh		TPM on LPC
FED0 0000h ~FEDF FFFFh	PCI Memory Range (subtractive decode)	
FEE0 0000h ~FEEF FFFFh	CPU	MSI Interrupt Memory Space
FEF0 0000h ~FEFF FFFFh	PCI Memory Range	
FF00 0000h ~FFFF FFFFh	PCH	Boot ROM(SPI) (16MB)

*1 : TSEGMB(TSEG Memory Base address) Refer to the data sheet of the CPU for more information.

*2 : TOLUD (Top of Low Usable physical memory) Register is automatically set depending on the PCI memory device. Change BIOS setting to manual set.

*3 : High Precision Timer Configuration It can be set with the register.

Table 6. Device list that uses memory space

Use area	Device	
128kB in 4GB	PCH	LAN Controller
1kB in 4GB		LAN Controller
1kB in 4GB		USB EHCI Controller
1kB in 4GB		USB EHCI Controller
64kB in 4GB		USB xHCI Controller
64kB in 4GB		LPC
16kB in 4GB		Root Complex Register Block
32Bytes in 64bit address		SMBus
2kB in 64kB to 4GB		SATA Host Controller
Memory Base/Limit in 4GB		PCI Express Root Ports 1,8
Prefetchable Memory Base/Limit in 64bit address		PCI Express Root Ports 1,8
4kB in 64bit address		Thermal Reporting
4kB in 64bit address		Thermal Reporting
4kB	CPU (D0)	PxP registers
32kB		MCH registers
4kB		DMI registers
0 to 512MB in Main Memory		Graphics Mode Select
0 to 2MB in Main Memory		GTT Graphics Memory
128MB, 256MB, 512MB	CPU (D2)	Internal graphics translation
64kB in 4GB	PCI-VME Bridge	A16 Memory Address Space
16MB in 4GB		A24 Memory Address Space
256MB in 4GB (128MB,512MB) (*1)		A32 Memory Address Space1
256MB in 4GB (128MB,512MB) (*1)		A32 Memory Address Space2

*1 : Use area can be changed. Contact us for details.

7.3. PCI Device

PCI devices are shown in Table 7.

Table 7. List of PCI devices

Bus number	Device number	Function number	Device	
00h	00h	00h	CPU	Host and DRAM Controller
	01h	00h		PCI Express Controller (XMC2)
		01h		PCI Express Controller (XMC1)
		02h		PCI Express Controller (Tsi721)
	02h	00h		Integrated Graphics Device
	03h	00h		Audio Controller
	20h	00h	PCH	xHCI Controller
	25h	00h		Ethernet Controller
	26h	00h		USB EHCI Controller #2
	28h	00h		PCI Express Port 1 (PCIe-PCI Bridge)
		07h		PCI Express Port 8 (82574)
	29h	00h		USB EHCI Controller #1
	31h	00h		LPC Controller
		02h		SATA Controller #1
		03h		SMBus Controller
–	–	–	XMC Slot2	
–	–	–	XMC Slot1	
M	00h	00h	PCIe-sRIO Bridge(Tsi721)	
M+1	00h	00h	PCIe-PCI Bridge(PEX8114)	
M+2	00h	00h	FPGA	
M+3	01h	00h	PCI-VME Bridge(Tsi148)	
M+3	02h	–	PMC Slot1	
M+3	03h	–	PMC Slot2	
N	00h	00h	Ethernet Controller(82574)	

*1 : M and N depends on the largest bus number shown on XMC slot and PMC slot.

7.4. SMBus Address Map

SMBus(System Management Bus) Address Map is shown in Table 8.

Table 8. SMBus Address Map

Address	Device
1001 000b	Thermal monitor IC (DS1631Z+)upper
1001 001b	Thermal monitor IC (DS1631Z+)lower
1010 101b	XMC1
1010 100b	XMC2

8. sRIO

Device and connectors of sRIO switch's connection destination are described in Table 9.

Table 9. s About the connection destination of the sRIO switch

Port	Device/Connector
Port0	Tsi721
Port4	XMC Slot1 (J16)
Port8	VXS Port A (P0)
Port12	VXS Port B (P0)

9. VME bus

Use bus timer provided by VME bus system controller at 128us or less. To use CPU-71-17 with the system controller, set TSI148 VCTRL register GTO[3:0] to 0100b(128us).

10. BIOS Setup

CPU-71-17 is equipped with BIOS, a customized Phoenix Technologies Ltd.'s SecureCore Tiano 3.0.
This chapter describes the BIOS setup procedure.
To start BIOS setup, press the F2 key while the BIOS starting screen is displayed. (*1)
To display the boot menu, press F5 while the BIOS start up screen is displayed.
Only date and time setting are required for normal use.

《Caution》

If the BIOS starting screen or the BIOS setup screen is not displayed properly due to a change in the BIOS setting, execute CMOS clear according to the instructions 5.3.15. SW2(Clear CMOS / sRIO setting) on page 22.

10.1. Main Menu

10.1.1. System Date

Table 10. System Date Menu Setting

Setting	Contents
System Date	View or set system date. Sets [month： day： year]

10.1.2. System Time

Table 11. System Time Menu Setting

Setting	Contents
System Time	View or set system date. Sets [hour：minute：second]

10.1.3. System Information

Current system information is displayed.

*1 : To enter the BIOS setup from Tera Term, read FUNCTION.CNF.

10.1.4. Boot Features

Table 12. Boot Features Menu Setting

Setting	Contents
Num Lock	Selects Power-on state for Numlock. • On (initial value) • Off
Timeout	Setting time to accept BIOS setup key (F2) • 1 second (initial value)
CSM support	Setting the Compatibility Support Module. • Yes(initial value)－Enabled • No－Disabled
QuickBoot	Enable/Disable quick boot. • Disabled(initial value) • Enabled
BIOS Level USB	Enable/Disable all BIOS support for USB in order to reduce boot time. Note that this will prevent using a USB keyboard in setup or a USB biometric scanner such as a finger print reader to control access to setup, but does not prevent the operating system from supporting such hardware. • Disabled • Enabled(initial value)
USB Legacy	Enable/Disable USB BIOS SMM support for mouse, keyboard, mass storage, etc, in Legacy operating systems such as DOS. • Disabled • Enabled(initial value)
Console Redirection	Enable/Disable Universal Console Redirection. • Disabled • Enabled(initial value)
Terminal Type	Setting the terminal type. • ANSI • VT100(initial value) • VT100+ • UTF8
Baudrate	Setting the baud rate. • 9600bps • 19200bps • 38400bps • 57600bps • 115200bps(initial value)
Flow Control	Setting the Flow Control. • None (initial value) • RTS/CTS • XON/XOFF
Continue C.R. after POST	Setting whether or not console redirection is enabled even after OS is loaded. • Disabled • Enabled (initial value)
UEFI Boot	Setting the UEFI Boot. • Disabled • Enabled(initial value)
Legacy Boot	Setting the Legacy Boot. • Disabled • Enabled(initial value)
Boot in Legacy Video Mode	Booting the Legacy Video mode. • Disabled(initial value) • Enabled
Load OPROM	Load all OPROMs or on demand according to the boot device. • All - All OPROM load • On Demand(initial value) - On Demand load
Allow > 4GB PMEM with Legacy OPROM	32bit memory resource is assigned to the device equipped with Option ROM. To assign 64bit memory resource to Option ROM equipped device, set Enabled. If it is set to enabled, problems such as hang up may occur depending on the device. • Disabled(initial value) • Enabled

10.1.5. Network Stack

Table 13. Network Stack Menu Setting

Setting	Contents
Network Stack	Setting the UEFI Network Stack. • Disabled • Enabled(initial value)
IPv4	Setting the IPv4. • Disabled • Enabled(initial value)
IPv6	Setting the IPv6. • Disabled • Enabled(initial value)
UEFI PXE Boot Priority	Setting UEFI PXE boot priority • IPv4 First(initial value) – Priority to IPv4. • IPv6 First – Priority to IPv6.

10.1.6. Error Manager

Table 14. Error Manager Menu Setting

Setting	Contents
View Error Manager Log	Display Error Manager Log information.
Clear Error Manager Log	Clear Error Manager Log.

10.2. Advanced Menu

10.2.1. Select Language

Table 15. Select Language Setting

Setting	Contents
Select Language	Select Language • English(initial value) • Japanese • French • Korean • Chinese

10.2.2. Silicon Information

CPU's frequency and PCH stepping information are displayed.

10.2.3. ACPI Configuration

Table 16. ACPI Configuration Setting

Setting	Contents
FACP-RTC S4 Flag Value	Valid Only for ACPI. Controls the value for the RTC S4 flag in the FACP table. • Disabled • Enabled(initial value)
APIC-IO APIC Mode	This is valid only for WIN2000, WindowsXP. A fresh install of OS must occur when APIC mode is enabled. The APIC table will be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits are set in the PCH. • Disabled • Enable(initial value)
ALS Support	Vald only for ACPI. Legacy = ALS support through the IGD INT10 function. ACPI = ALS support through an ACPI ALS driver. • Legacy(initial value)- ALS support by IGD INT10 • ACPI - ALS support by ACPI ALS driver
EMA Support	Valid only for ACPI. Controls the EMA device in an ACPI environment. • Disabled(initial value) • Enabled
MEF Support	Valid only for ACPI. Controls the Mobile East Fork feature support in an ACPI environment. • Disabled(initial value) • Enabled
Enabled PTID	Enable/Disable Rower and Temperature Instrumentation Details. • Disabled(initial value) • Enabled
FACP-PM Timer Flag Value	Valid only for ACPI. Controls the PM Timer Flag in the FACP table. • Disabled(initial value) • Enabled
CPPC	Setting the CPPC. • Disabled • Enabled(initial value)
CPPC Platform Sci enable	Setting the CPPC Platform Sci. • Disabled • Enabled(initial value)
Native PCI Express	Setting the Native PCI Express. • Disabled(initial value) • Enabled

10.2.4. Processor Configuration

Table 17. Processor Configuration Setting

Setting	Contents
Active Processor Cores	Number of cores to enable in each processor package. • All (initial value)- active all cores • 1 - One core is enabled. • 2 - Two cores are enabled. • 3 - Three cores are enabled.
Intel(R) HT Technology	When Disabled only one thread per enabled core is enabled. • Disabled • Enabled(initial value)
CPU Flex Ratio Override	Enable/Disable CPU Flex Ratio Programming. • Disabled(initial value) • Enabled
Enabled XD	Setting Execute Disable function. Also known as Data Execution Prevention (DEP • Disabled • Enabled (initial value)
Limit Cpuid Maxim value	Limiting CPUID maximum value • Disabled (initial value) • Enabled
Enable for BIST	Enable/Disable BIST(Bulit-In Self Test) on reset. • Disabled(initial value) • Enabled
Machine Check	Setting the machine check of processor. • Disabled • Enabled (initial value)
Intel(R) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities. • Disabled • Enabled(initial value)
Intel(R) Streamer Prefetcher	Intel Streamer Prefetcher. • Disabled • Enabled(initial value)
Intel(R) Spatial Prefetcher	Intel Spatial Prefetcher. • Disabled • Enabled(initial value)

10.2.4.1. Processor Power Management

Table 18. Processor Power Management Setting

Setting	Contents
Intel Speed Step (R)	Enable processor performance state (P state). • Disabled • Enabled(initial value)
Boot Performance mode	Select the performance state that the BIOS sets before OS handoff. • Max Performance(initial value) • Max Battery • Auto
Turbo Mode	Enable processor Turbo mode. EMTTM must also be enabled. • Disabled • Enabled(initial value)
Turbo Mode Power Limit Lock	Enable/Disable Locking of turbo settings. When enabled, TURBO_POWER_LIMIT of MSR will be locked and a reset will be required to unlock the register. • Disabled • Enabled(initial value)
Long Power Limit	Turbo Mode Long Duration Power Limit (aka power Limit 1) in Watts. The value may vary from 0 to Fused Value. If the Value is 0, the fused value will be programmed. A value greater than fused TDP value will not be programmed.. • initial value :0
Long Power Limit Time	Long Duration Time Window (aka Power Limit 1 Time) value in seconds. The value may vary from 0 to 28. Indicates the time window over which TDP value should be maintained. If the value is 0, the fused value will be programmed. • initial value : 28
Short Power Limit	Turbo Mode Short Duration Power Limit(aka Power Limit 2) in Watts. The value may vary from 0 to Fused Value. If the value is 0, the fused value will be programmed. A value grater than fused TDP value will not be programmed. • initial value : 0
Short Duration Turbo Mode	Setting the short duration turbo mode. • Disabled • Enabled(initial value)
Energy Efficient Enable	Enable Energy Efficient for processor. • Disabled • Enabled(initial value)
Configure TDP Boot Mode	Don't change. • Nominal(initial value)
Lock TDP setting	Lock of TDP MSR_CONFIG_TDP_CONTROL. • Disabled (initial value) • Enabled
TDP Custom Setting	Set custom TDP. Don't change. • Disabled • Enabled
Custom Configurable TDP Setting	Don't change.
C-States	Enable processor idle power saving states(C-states). • Disabled(initial value) • Enabled

10.2.5. Peripheral Configuration

Table 19. Peripheral Configuration Setting

Setting	Contents
PCIe SR-IOV Support	Setting the Set IO Virtualization. • Disabled(initial value) • Enabled

10.2.6. HDD Configuration

Table 20. HDD Configuration Setting

Setting	Contents
SATA Device	Enable/Disable SATA Device. • Disabled • Enabled(initial value)
Interface Combination	Select the SATA controllers operation mode. • IDE • AHCI(initial value) • RAID
Aggressive Link Power	Setting the Aggressive Link Power Management. • Disabled • Enabled (initial value)
Serial ATA port X	Display the identity of the device attached.
Hot Plug	Designates the port as Hot Pluggable. Note: Requires hardware support. • Disabled(initial value) • Enabled
External Port	Configure system to theat the Port as internal or external. • Disabled(initial value) - disable • Enabled - enable
SATA Device Type	Select 'Solid State Drive' only if a Solid State Drive is connected to this SATA port. • Hard Disk Drive • Solid State Drive(initial value)

10.2.7. Memory Configuration

Table 21. Memory Configuration Setting

Setting	Contents
Memory Frequency Limiter	Maximum Memory Frequency Selections in Mhz. • Auto (initial value) • 1067 • 1333 • 1600
Max TOLUD	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller. • Dynamic (initial value) • 1 GB • 1.25 GB • 1.5 GB • 1.75 GB • 2 GB • 2.25 GB • 2.5 GB • 2.75 GB • 3 GB • 3.25 GB
NMode Support	Enable/Disable system to support N Mode(command rate mode). • Auto (initial value) • 1 N mode • 2 N mode
Memory Remap	Setting memory remap exceeding 4GB. • Enabled(initial value) • Disabled
MRC FastBoot	Setting the MRC FastBoot. • Enabled(initial value) • Disabled

10.2.8. System Agent (SA) Configuration

Table 22. System Agent (SA) Configuration Setting

Setting	Contents
Above 4GB MMIO BIOS assignment	To enable 64bit memory resource assignment, change to Enabled. • Disabled (initial value) • Enabled
CPU Audio Device(B0:D3:F0)	Setting the CPU Audio Device. • Disabled • Enabled (initial value)

10.2.8.1. DMI Settings

Table 23. DMI Settings Setting

Setting	Contents
DMI Link ASPM Control	Enable/Disable the control of Active State Power Management on SA side of the DMI Link. • Disabled (initial value) • L0S • L1 • L0S and L1 • Auto
DMI Gen2 Support Control	Setting the Gen2 support of DMI. • Disabled • Enabled • Auto (initial value)

10.2.8.2. Intel (R) VT for Directed I/O (VT-d)

Table 24. Intel (R) VT for Directed I/O(VT-d)Setting

Setting	Contents
Intel (R) VT for Directed I/O(VT-d)	Enable/Disable Intel Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables • Disabled (initial value) • Enabled

10.2.8.3. Graphics Configuration

Table 25. Graphics Configuration Setting

Setting	Contents
Primary Display Selection	Select the primary display device. • IGD • PEG • PCI • Auto (initial value)
Internal Graphics	Enable/Disable the Internal Graphics Device. This has no effect if external graphics are present. • Disabled • Enabled • Auto (initial value)
GTT Size	Gtt memory size of IGD. • 1MB • 2MB (initial value)
Aperture Size	Graphics Aperture size. • 128MB • 256MB (initial value) • 512MB
DVMT Pre-Allocated	Select Pre-Allocated Graphics Memory size used by the Internal Graphics Device. This has no effect if external graphics are present. • 32MB (initial value) • 64MB • 128MB
DVMT Total Gfx Mem	DVMT5.0 DVMT Graphic Memory Size. This has no effect if external graphics present. • 128MB • 256MB (initial value) • Max
Gfx Low Power Mode	Setting the Gfx Low Power Mode. • Disabled • Enabled (initial value)

10.2.8.3.1. IGD Configuration

Table 26. IGD Configuration Setting

Setting	Contents
IGD – Boot Type	Select the video Device activated during POST. This has no effect if external graphics are present. • VBIOS Default (initial value)
Spread Spectrum clock chip	Select SSC.Don't change. • Off (initial value) • Hardware：Spread is controlled by chip • Software：Spread is controlled by BIOS

10.2.8.4. PEG Port Configuration

Table 27. PEG Port Configuration Setting

Setting	Contents
PEG 0 – Gen X	Configure PEG0 B0:D1:F0 speed. • Auto (initial value) • Gen1 • Gen2 • Gen3
PEG 1 – Gen X	Setting PEG1 B0:D1:F1 link speed. • Auto (initial value) • Gen1 • Gen2 • Gen3
PEG 2 – Gen X	Setting PEG2 B0:D1:F2 link speed. • Auto (initial value) • Gen1 • Gen2 • Gen3
Always Enable PEG	Enable PEG. • Disabled • Enabled (initial value)
PEG ASPM	PEG ASPM Settings. • Disabled (initial value) • L0s • L1 • L0s and L1 • Auto
De-emphasis Control	De-emphasis control for PEG. • -6 dB • -3.5 dB (initial value)
Swing Control	Swing control for PEG. • Full(initial value) • Half • Reduced
Gen3 Equalization	Perform PEG Gen3 Equalization steps. • Disabled • Enabled (initial value)
PEG Gen3 Equalization Phase2	Enable/Disable PEG Gen3 Equalization phase2. • Disabled (initial value) • Enabled
Gen3 Root Port Preset	Root port preset value for Gen3 Equalization. • 1 to 11 (initial value : 8)
Gen3 End Port Preset	Endpoint preset value for Gen3 Equalization. • 0 to 10 (initial value : 7)
PEG Sample Calibrate	Enable/Disable PEG Sample Calibrate. • Disabled • Enabled • Auto (initial value)

10.2.9. South Bridge Configuration

Table 28. South Bridge Configuration Setting

Setting	Contents
SMBUS Device	Setting the SMBUS device. • Disabled • Enabled (initial value)
Port 80h Cycles	Setting the addressee of 80 cycles of Port(s). • LPC Bus(initial value) • PCI Bus
HPET Support	Control the High Precision Event Timer through this setup option. When enabled, the RSDT points to the HPET table and the proper enable bits are set. • Disabled • Enabled (initial value)
HPET Memory Map BAR	Select the HPET Memory Map Base Address. • FED00000 (initial value) • FED01000 • FED02000 • FED03000

10.2.9.1. SB PCI Express Configuration

Table 29. SB PCI Express Configuration Setting

Setting	Contents
PCI Express Root Port Clock Gating	Enable/Disable PCI Express Root Port Clock Gating. • Disabled • Enabled (initial value)
DMI Link ASPM Control	The control of Active State Power Management of the DMI link. • Disabled (initial value) • L0S • L1 • L0S and L1 • Auto
DMI Link Extended Sync Control	The Control of Extended synchronous on SB side of the DMI Link. • Disabled (initial value) • Enabled

10.2.9.2. PCI Express Port 1 Configuration (PCIe/PCI-Bridge)

Table 30. PCI Express Port 1 Configuration (PCIe/PCI-Bridge)Setting

Setting	Contents
PCI Express Port 1	Setting about PCI Express Root Port. When disable Port1, PCI, VME and PMC will be also disabled since PCI is connected from Port1. • Disabled • Enabled (initial value)
PCIe Speed	Select PCIe Speed to Gen1 or Gen2. • Auto (initial value) • Gen1 • Gen2
ASPM	Control PCIe Active State Power Management Settings. • Disabled (initial value) • L0s • L1 • L0s and L1 • Auto
Hot Plug	PCI Express Hot Plug Enable/Disabled. • Disabled (initial value) • Enabled
PME Interrupt	Root PCI Express PME Interrupt Enable/Disable. • Disabled (initial value) • Enabled
PME SCI	PCI Express PME SCI Enable/Disable. • Disabled • Enabled (initial value)

10.2.9.3. PCI Express Port 8 Configuration (82574)

Table 31. PCI Express Port 8 Configuration(82574)Setting

Setting	Contents
PCI Express Port 8	Setting about PCI Express Root Port. When disable Port8, ETHERNET2 will be also disabled since 82574 is connected from Port8. • Disabled • Enabled (initial value)
PCIe Speed	Select PCIe Speed to Gen1 or Gen2. • Auto (initial value) • Gen1 • Gen2
ASPM	Control PCIe Active State Power Management Settings. • Disabled (initial value) • L0s • L1 • L0s and L1 • Auto
Hot Plug	PCI Express Hot Plug Enable/Disabled. • Disabled (initial value) • Enabled
PME Interrupt	Root PCI Express PME Interrupt Enable/Disable. • Disabled (initial value) • Enabled
PME SCI	PCI Express PME SCI Enable/Disable. • Disabled • Enabled (initial value)

10.2.9.4. SB USB Configuration

Table 32. SB USB Configuration Setting

Setting	Contents
xHCI Mode	Mode of operation of xHCI controller. • Disabled • Enabled • Auto • Smart Auto (initial value)
EHCI2	Control the USB ECHI (USB2.0) functions. • Disabled • Enabled (initial value)
USB Per-Port Disable Control	Controls each of the USB ports(0~1) Enable/Disable • Disabled (initial value) • Enabled

10.2.9.5. SB Azalia Configuration

Table 33. SB Azalia Configuration Setting

Setting	Contents
Azalia	Setting the Azalia device. • Auto (initial value) • Disabled • Enabled

10.2.9.6. SB Serial IRQ Configuration

Table 34. SB Serial IRQ Configuration Setting

Setting	Contents
Enable Serial IRQ	Setting the Serial IRQ. • Enabled • Disabled
Serial IRQ Mode	In 'Quiet' mode Serial IRQ is active only when needed, In 'Continuous' it is active all the time. • Quiet (initial value) • Continuous
Start Frame	The number of start frames at the beginning of the serial IRQ • 4 Frames • 6 Frames • 8 Frames

10.2.9.7. SB Security Configuration

Table 35. SB Security Configuration Setting

Setting	Contents
GPIO Lockdown	Setting the Lockdown function of PCH GPIO. • Enabled • Disabled (initial value)
RTC Lock	Setting the RTC lock. • Enabled (initial value) • Disabled
BIOS Lock	Setting the lock of BIOS region. • Enabled • Disabled (initial value)

10.2.10. Network Configuration

Table 36. Network Configuration Setting

Setting	Contents
PCH Internal LAN	Enable/Disable PCH Internal LAN. When set to Disabled, ETHERNET1 is disabled. • Disabled • Enabled (initial value)
LAN OPROM Selection	This is used to select LAN OPRAM for quick boot minimal configuration. • Disabled • Enabled (initial value)
Wake on PCH LAN	Enable PCH Internal Wake on LAN capability at Moff. • Disabled • Enabled (initial value)
ASF Support	Enable/Disable Alert Specification Format. • Disabled • Enabled (initial value)

10.2.11. SuperIO 1 Configuration

Table 37. SuperIO 1 Configuration Setting

Setting	Contents
Onboard UART1	This option controls the Onboard UART1 address. When enable, UART1 uses address 0x3F8h and IRQ4. • Disabled • Enabled (initial value)
UART1 Base Address	This option controls UART1 Address. • 3F8(initial value) • 2F8 • 3E8 • 2E8
UART1 IRQ	This option controls UART1 IRQ. • IRQ 3 • IRQ 4(initial value)
Onboard CIR(UART2)	This option controls the Onboard UART1 address. When enable, UART1 uses address 0x3F8h and IRQ4. • Disabled (initial value) • Enabled

10.2.12. SMBIOS Event Log

Table 38. SMBIOS Event Log Setting

Setting	Contents
Event Log	Enabling/disabling Event log. • Disabled • Enabled (initial value)
View SMBIOS event log	View SMBIOS event log. • Displays log with “Enter”
Mark SMBIOS events as read	Mark SMBIOS events as read. Marked SMBIOS events won’t be displayed
Clears SMBIOS events	Clears SMBIOS events.

10.2.13. AMT Configuration

Table 39. AMT Configuration Setting

Setting	Contents
Intel(R) AMT	Enable/Disable Intel(R) Active Management Technology. • Disabled (initial value) • Enabled

10.2.14. ME Configuration

Table 40. ME Configuration Setting

Setting	Contents
Intel(R) ME	Enable/Disable Intel(R) Management Engine. • Disabled (initial value) • Enabled

10.2.15. Thermal Configuration

10.2.15.1. CPU Thermal Configuration

Table 41. CPU Thermal Configuration Setting

Setting	Contents
Thermal Monitor	Setting processor's temperature monitor/thermal control. • Enabled (initial value) • Disabled
DTS	Setting processor's digital temperature sensor functions. • Enabled • Disabled (initial value)

10.2.15.2. Platform Thermal Configuration

Table 42. Platform Thermal Configuration Setting

Setting	Contents
Automatic Thermal Reporting	Configure _CRT, _PSV, and _AC0 automatically based on values recommended in BIOS Writes Guide's Thermal Reporting for Thermal Management settings. Set to Disabled for manual configuration. • Disabled • Enabled (initial value)
Critical Trip Point (*1)	This value controls the temperature of the ACPI Active Trip Point – the point where the OS turns the processor fan on high. Note: Target value (POR) with all Intel(R) mobile processors is 100 degrees C. • POR (initial value) / 15℃ / 23℃ / 31℃ / 39℃ / 47℃ / 55℃ / 63℃ / 71℃ / 79℃ / 87℃ / 95℃ / 103℃ / 111℃ / 119℃
Passive Trip Point (*1)	Setting temperature of ACPI passive trip point (a point where OS starts throttling. • Disabled / 15℃ / 23℃ / 31℃ / 39℃ / 47℃ / 55℃ / 63℃ / 71℃ / 79℃ / 87℃ / 95℃(initial value) / 103℃ / 111℃/119℃
Passive TC1 Value	This value sets the TC1 value for the ACPI passive cooling Formula. Use '+' and '-' keys to change Value. • Preset value : 1 to 16 • initial value : 1
Passive TC2 Value	This value sets the TC2 value for the ACPI passive cooling Formula. Use '+' and '-' keys to change Value. • Preset value : 1 to 16 • initial value : 5
Passive TSP Value	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS reads the temperature when passive cooling is enabled. Use '+' and '-' keys to change value. • Preset value : 2 to 32(Only even number) • initial value : 10
PCH Thermal Device Thermal Sensor Device Enable	Enable thermal sensor device. • Disabled (initial value) • Enabled

*1 : possible to set by changing Automatic Thermal Reporting to "Disable"

10.2.16. ICC Configuration

10.2.16.1. Clock 3Setting

Settings, BCLK, DMI, PEG, PCIe, PCI33, SATA, USB3 clock

Table 43. BCLK, DMI, PEG, PCIe, PCI33, SATA, USB3 Setting

Setting	Contents
New frequency[10KHz]	Frequency in 10KHz increments. Don't change. • initial value :10000(100MHz)
New SSC mode	Spread spectrum clock mode. Determines method of clock spectrum distribution around base frequency. Don't change. • Up • Center • Down (initial value)
New SSC spread percent[0.01%]	Clock spectrum spread in 0.01% increments. Determines spectrum deviation away from base frequency. Don't change. • Preset value :0 to 50(0.5%) • initial value :0

10.2.17. Intel Rapid Start Technology

Table 44. Intel Rapid Start TechnologySetting

Setting	Contents
iRST Support	Setting iRST. • Disabled (initial value) • Enabled

10.3. Security Menu

Table 45. Security Menu Setting

Setting	Contents
Set Supervisor Password	Set or clear the supervisor account's password.
Supervisor Hint String	Enter a hint for supervisor password.
Set User Password	Set or clear user password.
User Hint Sting	Enter a hint for user password.
Min. password lengs	Set the minimum number of characters for password (1-20)

10.4. BootMenu

Table 46. BootMenu Setting

Setting	Contents
Boot Priority Order	Selection Boot priority setting procedure. The initial value is as follows: 1. USB HDD 2. USB CD 3. USB FDD 4. ATAPI CD 5. ATA HDD0 6. ATA HDD1 7. ATA HDD2 8. ATA HDD3 9. ATA HDD4 10.ATA HDD5 11.Other HDD 12.Internal Shell 13.PCI LAN

10.5. Misc Menu

Table 47. Misc Menu Setting

Setting	Contents
Intel Ethernet Connection I217-LM	Chip information and a MAC Address are displayed.
Intel 82574L Gigabit Network Connection	Chip information and a MAC Address are displayed.

10.6. Exit Menu

Table 48. Exit Menu Setting

Setting	Contents
Exit Saving Changes	Exits the setup menu with saving all the changes same as F10, then resets the system automatically.
Exit Discarding Changes	Exits the setup menu without saving the change same as Esc.
Load Setup Defaults	Loads the setup default value same as F9.
Load Optimized Defaults	Loads optimized defaults by boot time and system performance.

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