ADM-XRC-5LX

PCI Mezzanine Card

User Guide

Version 2.0

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1. Introduction

The ADM-XRC-5LX is a high performance PCI Mezzanine Card (PMC) designed for supporting development of applications using the Virtex-5LX series of FPGAs from Xilinx.

The card uses an FPGA PCI bridge developed by Alpha-Data supporting PCI-X and PCI. A high-speed multiplexed address/data bus connects the bridge to the target (user) FPGA.

1.1. Specifications

The ADM-XRC-5LX supports high performance PCI-X / PCI operation without the need to integrate proprietary cores into the user FPGA.

- Physically conformant to IEEE P1386-2001 Common Mezzanine Card standard
- High performance PCI and DMA controllers
- Local bus speeds of up to 80 MHz
- Four banks of 64Mx32 DDRII SDRAM (1GB total)
- User clock programmable between 20MHz and 500MHz
- Stable low-jitter 200MHz clock for precision IO delays
- User front panel adapter with up to 146 free IO signals
- User rear panel PMC connector with 64 free IO signals
- Programmable 2.5V or 3.3V I/O on front and rear interfaces
- Supports 3.3V PCI or PCI-X at 64 bits

2. Hardware Installation

This chapter explains how to install the ADM-XRC-4 (LX/SX) onto a PMC motherboard.

2.1. Motherboard requirements

The ADM-XRC-5LX supports 3.3V only signalling on the PCI Bus. It is not compatible with systems that use 5V signalling.

The ADM-XRC-5T1 must be installed in a PMC motherboard that supplies +5.0V and +3.3V power to the PMC connectors. Ensure that the motherboard satisfies this requirement before powering it up. +12V and -12V may also be required for certain XRM modules.

2.2. Handling instructions

Observe SSD precautions when handling the cards to prevent damage to components by electrostatic discharge.

Avoid flexing the board.

2.3. Installing the ADM-XRC-5LX onto a PMC motherboard

Note: This operation should not be performed while the PMC motherboard is powered up.

The ADM-XRC-4 (LX/SX) must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the PMC motherboard.

2.4. Installing the ADM-XRC-5LX if fitted to an ADC-PMC

The ADM-XRC-4 (LX/SX) can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC refer to the supplied documentation for information on jumper settings. All that is required for installation is a PCI slot that has enough space to accommodate the full-length card. The ADC-PMC is compatible with 5V and 3V PCI (32 and 64 bit) and PCI-X slots.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XRC-4 (LX/SX) and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine.

3. Software Installation

Please refer to the SDK installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

4. Board Description

The ADM-XRC-5LX follows the architecture of the ADM-XRC series and decouples the "target" FPGA from the PCI interface, allowing user applications to be designed with minimum effort and without the complexity of PCI design.

A separate Bridge / Control FPGA interfaces to the PCI bus and provides a simpler Local Bus interface to the target FPGA. It also performs all of the board control functions including the configuration of the target FPGA, programmable clock setup and the monitoring of on-board voltage and temperature.

DDR2 SDRAM and serial flash memory connect to the target FPGA and are supported by Xilinx or third party IP.

IO functionality is provided using XRM modules connecting to a 180 pin SAMTEC QSH connector.

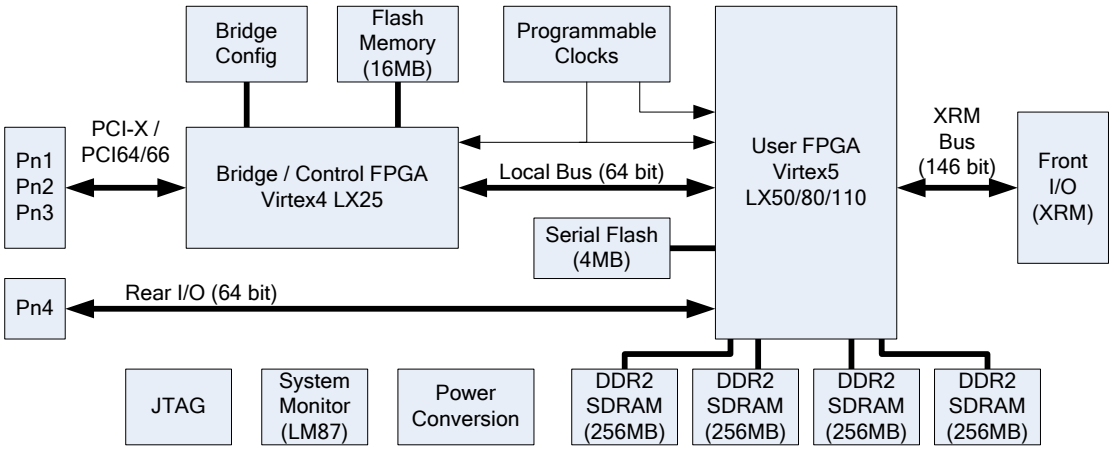

Figure 1 ADM-XRC-5LX Block Diagram

4.1. Local Bus

The ADM-XRC-5LX implements a multi-master local bus between the bridge and the target FPGA using a 32- or 64-bit multiplexed address and data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCI bus clock to suit the requirements of the user design.

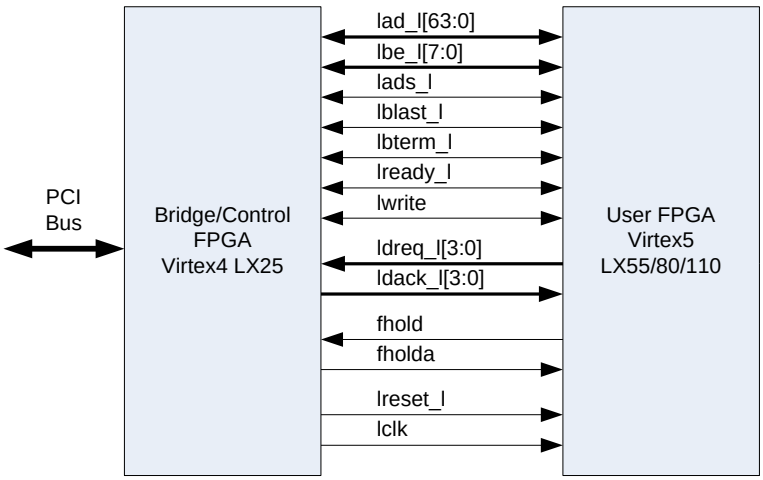

Figure 2 Local Bus Interface

Signal	Type	Purpose
lad[0:63]	bidir	Address and data bus.
lbe_l[0:7]	bidir	Byte qualifiers
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lwrite	bidir	Indicates a write transfer from master
ldreq_l[0:3]	unidir	DMA request from target to bridge
ldack_l[0:3]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge
lreset_l	unidir	Reset to target
lclk	unidir	Clock to synchronise bridge and target

Table 1 Local Bus Interface Signal List

4.2. Flash Memory

The ADM-XRC-5LX is fitted with two separate Flash memories: one connected to the Bridge / Control FPGA and the other to the User FPGA.

4.2.1. Board Control Flash

An Intel PC28F256P30 flash memory is used for storing a configuration bitstream for the User FPGA. Once the Bridge / Control FPGA is configured, it checks for a valid bitstream in flash and, if present, automatically loads it into the User FPGA. This process can be inhibited by setting a jumper on the JTAG connector. See the description of the “FBS” signal in Section 4.4 for further information.

Access to this flash device is only possible through control logic registers. The flash is not directly mapped onto the local bus.

Programming, erasing and verification of the flash are supported by the ADM-XRC SDK and driver. Utilities are provided to load bitstreams into the flash. These also verify the bitstream is compatible with the target FPGA.

4.2.2. User FPGA Flash

An ST M25P32 flash memory with SPI interface is connected to the User FPGA for the storage of application-specific information.

Note: This device is not connected to the SPI configuration pins on the User FPGA and cannot be used for configuration.

4.3. Health Monitoring

The ADM-XRC-5LX has the ability to monitor temperature and voltage of key parts of the PMC to maintain a check on the operation of the board. The monitoring is implemented by a National Semiconductor LM87 and is supported by the board control logic connected using I^2C.

The Control Logic scans the LM87 when instructed by host software and stores all current voltage and temperature measurements in a blockram. This allows the values to be read without the need to communicate directly with the monitor.

The following supplies and temperatures, as shown in Table 2, are monitored.

Monitor	Purpose
1.0V	User FPGA Core Supply
1.2V	Bridge FPGA Core Supply
1.8V	Memories, User FPGA Memory I/O, Local Bus I/O Config CPLD Core Supply
2.5V	Source voltage for Front, Rear I/O
5.0V	Board Input Supply
PCI_VIO	Monitors the PCI signalling supply – VIO
XRM_VCCIO	Either 2.5V or 3.3V Front Panel I/O Voltage
Temp1	User FPGA die temperature
Temp2	LM87 on die temperature for board/ambient

Table 2 Voltage and Temperature Monitors

An application is provided in the SDK that permits the reading of the health monitor. The typical output of the monitor is shown below, provided by the SYSMON program.

4.4. JTAG

A JTAG header is provided to allow download of the FPGA using the Xilinx tools and serial download cables. This also allows the use of ChipScope PRO ILA to debug an FPGA design. It should be noted that four devices will be detected when the SCAN chain is initialised.

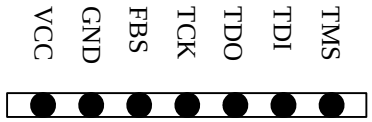

Figure 3 JTAG Header

The VCC supply provided on J5 to the JTAG cable is +2.5V and is protected by a poly fuse with a rating of 350mA.

FBS

The FBS signal is an input to the control logic and provides control of the cold boot process. By default with no link fitted, the control logic will load a bitstream from flash into the FPGA if one is present. Shorting FBS to the adjacent GND pin will disable this process and can be used to recover situations where rogue bitstreams have been stored in flash.

4.5. Clocks

The ADM-XRC-5LX is provided with numerous clock sources, as shown in Figure 4 below:

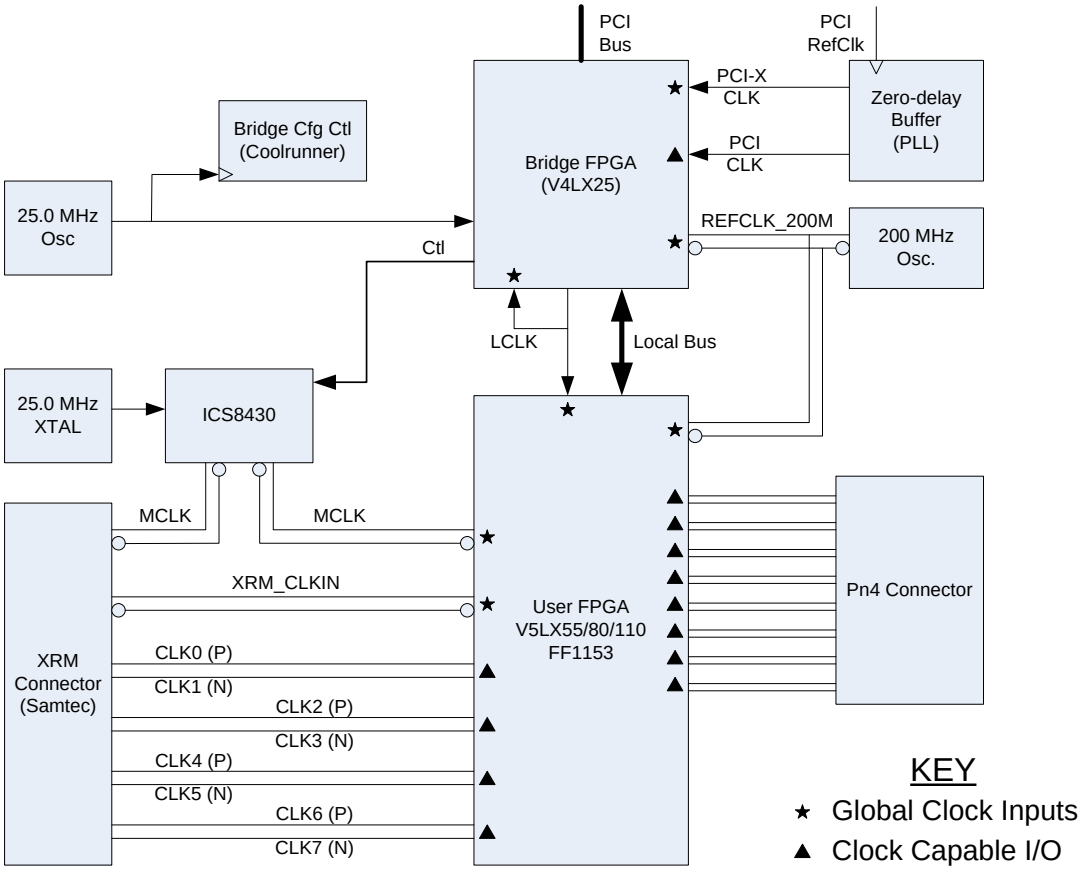

Figure 4 Clock Structure

4.5.1. LCLK

The Local Bus can be used at up to 80 MHz and all timing is synchronised to LCLK between the Bridge and User FPGAs. LCLK is generated from a 200MHz reference by a DCM within the bridge FPGA. The minimum LCLK frequency (determined by the DCM specification) is 32MHz.

The LCLK frequency is set by writing to the board control logic. (See SDK for details and example application).

Note: If the user FPGA application includes a DCM driven by LCLK (or one of the other programmable clocks), the clock frequency should be set prior to FPGA configuration.

4.5.2. MCLK

MCLK is an LVPECL clock generated by an ICS8430-61 synthesiser with a base 25MHz crystal. The synthesiser has two outputs of the same clock, one of which is routed to the User FPGA whilst the other is routed to the XRM connector. Both are terminated using LVPECL terminations.

MCLK can be programmed to between 20MHz and 500MHz.

4.5.3. REFCLK

In order to make use of the IODELAY features of Virtex™-5, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADM-XRC-5LX is fitted with a 200MHz LVPECL (LVDS optional) oscillator connected to global clock resource pins. This reference clock can also be used for application logic if required.

4.5.4. XRM Clocks

Global Clock Input

The XRM interface provides a differential input to the User FPGA global clocking resources. The default on-board terminations are suitable for an LVPECL clock.

Regional Clocks

The XRM interface provides 8 clock lines that can be either be used single-ended or as 4 LVDS differential pairs. These clocks are routed to Clock-Capable I/O on the User FPGA, providing access to its regional clock capabilities.

Each clock pair is in a different clock region alongside 16 pairs of XRM bus signals, as shown in Table 3 below:

XRM Clocks	FPGA Bank	XRM bus pairs
0 & 1 (Pair 0)	26	1 – 16
2 & 3 (Pair 1)	22	17 – 32
4 & 5 (Pair 2)	18	33 – 48
6 & 7 (Pair 3)	14	49 – 64

Table 3 XRM Bus Regional Clocks

4.5.5. Rear (Pn4) Clocks

There are no dedicated clock lines between the Pn4 connector and the user FPGA. However, the following signal pairs are routed to clock-capable I/O on the User FPGA, providing access to its regional clock capabilities.

FPGA Bank	Pn4 bus pairs
11	22, 23, 24 & 25
13	6, 7, 8 & 9

Table 4 Rear (Pn4) Regional Clocks

4.5.6. PCI Clocks

The PCI Interface within the bridge FPGA requires a regional clock input for 66MHz PCI operation or a global clock input for PCI-X. To comply with the single-load requirement in the PCI specification, a zero-delay clock buffer is used to route the PCI clock to the two different clock inputs.

The clock buffer has a PLL with a minimum input frequency of 24MHz, potentially causing problems in applications that use the PCI 33MHz mode with a slow clock. In this case, the buffer can be removed to provide full PCI 33MHz compatibility.

4.6. User FPGA

4.6.1. Configuration

The ADM-XRC-5LX performs configuration from the host at high speed using SelectMAP. The FPGA may also be configured from flash or by JTAG via header J5.

Download from the host is the fastest way to configure the User FPGA with 8 bit SelectMAP mode enabled. This permits a configuration speed of up to 40MB/s.

The ADM-XRC-5LX can be configured to boot the User FPGA from flash on power-up if a valid bit-stream is detected in the flash. Booting from flash will also configure the clocks and I/O voltages as appropriate.

4.6.2. I/O Bank Voltages

Bank	Voltage	Description
0	2.5V	Configuration I/F
5, 12, 15, 16, 19, 20, 23, 24	1.8V	DDRII DRAM I/O
2	1.8V	SelectMAP I/F
3, 4	3.3V	Clocks, Serial Flash
11, 13	2.5V or 3.3V	Pn4 Interface
14, 18, 26, 22	2.5V or 3.3V	XRM Interface
6, 17, 21, 25	1.8V	Local Bus

Table 5 User FPGA I/O Bank Voltages

4.6.3. Memory Interfaces

The ADM-XRC-5LX has 4 independent banks of DDRII SDRAM. Each bank consists of two memory devices in parallel to provide a 32 bit datapath. 1Gb Micron MT47H64M16 devices are fitted as standard to provide 256MB per bank. The board will support higher capacity devices when they become available.

Details of the signalling standards, bank numbers etc. are given in the tables below:

Name	Direction	I/O Standard
DDR1_ad[15:0], DDR1_ba[2:0], DDR1_rasn, DDR1_casn, DDR1_wen, DDR1_csn, DDR1_cke, DDR1_odt	Output	SSTL18_I
DDR1_ck0, DDR1_ckn0	Output	DIFF_SSTL18_II
DDR1_dq[15:0]	BiDir	SSTL18_II
DDR1_dm[1:0]	Output	SSTL18_I
DDR1_dqs[1:0], DDR1_dqsn[1:0]	BiDir	DIFF_SSTL18_II
DDR1_ck1, DDR1_ckn1	Output	DIFF_SSTL18_II
DDR1_dq[31:16]	BiDir	SSTL18_II
DDR1_dm[3:2]	Output	SSTL18_I
DDR1_dqs[3:2], DDR1_dqsn[3:2]	BiDir	DIFF_SSTL18_II
DDR1_read_en_out	Output	
DDR1_read_en_in	Input	

Table 6 DDR Memory Bank Configuration

4.7. XRM Bus and Front Panel I/O

A major benefit of the ADM-XRC series of boards that use the XRM Bus interface is the versatility of I/O options that result. The ADM-XRC-5LX maintains this interface and thus compatibility with a wide range of I/O modules to suit many diverse needs.

The XRM interface uses the 180 pin Samtec QSH series connector, CN1.

4.7.1. XRM Signalling Voltage

The signalling voltage on the XRM connector (and User FPGA Banks 14, 18, 22 & 26) is selectable by jumper J6.

J6	XRM I/O voltage
Link p1 & p2	3.3V
Link p3 & p4	2.5V
Link p5 & p4	1.8V

Table 7 XRM I/O Voltage Selection

4.7.2. XRM Interface – Connector Pinout

The XRM interface is implemented on CN1, a 180 pin Samtec connector type QSH, with the pin-out as detailed in tables Table 8 to Table 10.

In turn, the signals that connect to CN1 are provided in the main from three banks of the User FPGA, Banks 9, 11 and 13. These banks share a common VCCO that can be 2.5V or 3.3V powered, selectable under user control.

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_1	AL6	1	2	AN4	N_2
P_1	AL5	3	4	AN5	P_2
N_3	AL4	5	6	AP5	P_4
P_3	AM5	7	8	AP4	N_4
N_5	AM6	9	10	AM7	N_6
P_5	AN7	11	12	AM8	P_6
N_7	AN8	13	14	AL10	N_8
P_7	AN9	15	16	AM10	P_8
P_9	AP7	17	18	AN10	P_10
N_9	AP6	19	20	AM11	N_10
N_11	AM17	21	22	AP17	N_12
P_11	AN17	23	24	AP16	P_12
N_13	AP12	25	26	AM15	P_14
P_13	AP11	27	28	AM16	N_14
N_15	AN14	29	30	AP15	P_16
P_15	AP14	31	32	AN15	N_16
N_17	AA11	33	34	AA9	N_18
P_17	AA10	35	36	AA8	P_18
WIRE_S_1	AL8	37	38	AP9	CLK0
+3.3V		39	40	AP10	CLK1
+3.3V		41	42		XRM_SERID
+3.3V		43	44		RESERVED
+5V		45	46		XRM_VREF
+5V		47	48		XRM_VCCIO
VBAT		49	50		XRM_VCCIO
+12V		51	52		XRM_VCCIO
+12V		53	54		-12V
PRESENCE_L		55	56		XRM_TDI
XRM_TCK		57	58		XRM_TRST
XRM_TMS		59	60		XRM_TDO

Table 8 XRM Interface - part 1

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_19	AB10	61	62	AB7	N_20
P_19	AB11	63	64	AB8	P_20
N_21	AJ6	65	66	AD7	N_22
P_21	AJ7	67	68	AE7	P_22
N_23	AH7	69	70	AC9	N_24
P_23	AG7	71	72	AD9	P_24
N_25	AH8	73	74	AC10	P_26
P_25	AG8	75	76	AD10	N_26
P_27	AE9	77	78	AG10	N_28
N_27	AF9	79	80	AF10	P_28
N_29	AK8	81	82	AG11	P_30
P_29	AK9	83	84	AF11	N_30
N_31	AH10	85	86	AE11	N_32
P_31	AJ10	87	88	AD11	P_32
CLK2	AE8	89	90	AH9	WIRE_S_4
CLK3	AF8	91	92	W7	WIRE_S_5
WIRE_S_2	AN13	93	94	AE4	WIRE_S_6
WIRE_S_3	AC8	95	96	AC3	WIRE_S_7
CLK4	AA4	97	98	Y9	N_34
CLK5	AB5	99	100	W9	P_34
N_33	W11	101	102	AG1	CLK6
P_33	Y11	103	104	AG2	CLK7
WIRE_S_8	AH2	105	106	AF18	S_10
S_9	AE18	107	108	AG20	XRM_CLKIN_N
RESERVED		109	110	AH19	XRM_CLKIN_P
RESERVED		111	112	AF19	XRM_SDA
XRM_PECL_N		113	114	AF20	XRM_SCL
XRM_PECL_P		115	116		RESERVED
RESERVED		117	118		RESERVED
RESERVED		119	120		RESERVED

Table 9 XRM Interface - part 2

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
P_35	W10	121	122	V9	P_36
N_35	V10	123	124	V8	N_36
N_37	V5	125	126	Y7	P_38
P_37	W5	127	128	Y8	N_38
P_39	Y6	129	130	AA6	P_40
N_39	W6	131	132	AA5	N_40
N_41	W4	133	134	AC5	N_42
P_41	Y4	135	136	AB6	P_42
P_43	AD5	137	138	AE6	N_44
N_43	AD6	139	140	AF5	P_44
P_45	AH4	141	142	AG6	N_46
N_45	AJ4	143	144	AF6	P_46
N_47	AJ5	145	146	W1	P_50
P_47	AK4	147	148	V2	N_50
P_49	V4	149	150	AH5	N_48
N_49	V3	151	152	AG5	P_48
P_51	Y3	153	154	Y1	N_52
N_51	Y2	155	156	W2	P_52
N_53	AA1	157	158	AA3	N_54
P_53	AB1	159	160	AB3	P_54
P_55	AC2	161	162	AD2	N_56
N_55	AD1	163	164	AE2	P_56
N_57	AE1	165	166	AE3	N_58
P_57	AF1	167	168	AF3	P_58
N_59	AK3	169	170	AH3	N_60
P_59	AK2	171	172	AG3	P_60
N_61	AM1	173	174	AP2	N_62
P_61	AL1	175	176	AN2	P_62
N_63	AL3	177	178	AN3	N_64
P_63	AM2	179	180	AM3	P_64

Table 10 XRM Interface - part 3

4.8. Pn4 I/O

Up to 32 pairs of differential or 64 single-ended signals are available on Pn4 and are sourced from Banks 11 & 13 of the User FPGA. All of the signal traces are routed as 100 Ohm differential pairs and each pair is matched in length. The worst case difference in trace length between any two pairs is 10mm.

Signal	FPGA Pin	Pn4 Pin	Pn4 Pin	FPGA Pin	Signal
PN4_P1	AN34	1	2	AM33	PN4_P2
PN4_N1	AN33	3	4	AM32	PN4_N2
PN4_P3	AL34	5	6	AJ32	PN4_P4
PN4_N3	AL33	7	8	AK32	PN4_N4
PN4_P5	AK34	9	10	AD32	PN4_P6
PN4_N5	AK33	11	12	AE32	PN4_N6
PN4_P7	AH34	13	14	AF34	PN4_P8
PN4_N7	AJ34	15	16	AE34	PN4_N8
PN4_P9	AF33	17	18	AC33	PN4_P10
PN4_N9	AE33	19	20	AB33	PN4_N10
PN4_P11	AC32	21	22	AC34	PN4_P12
PN4_N11	AB32	23	24	AD34	PN4_N12
PN4_P13	AA34	25	26	AA33	PN4_P14
PN4_N13	Y34	27	28	Y33	PN4_N14
PN4_P15	W34	29	30	V33	PN4_P16
PN4_N15	V34	31	32	V32	PN4_N16
PN4_P17	U33	33	34	R33	PN4_P18
PN4_N17	T34	35	36	R32	PN4_N18
PN4_P19	T33	37	38	P32	PN4_P20
PN4_N19	R34	39	40	N32	PN4_N20
PN4_P21	L33	41	42	K33 [CC]	PN4_P22
PN4_N21	M32	43	44	K32 [CC]	PN4_N22
PN4_P23	L34 [CC]	45	46	H34 [CC]	PN4_P24
PN4_N23	K34 [CC]	47	48	J34 [CC]	PN4_N24
PN4_P25	J32 [CC]	49	50	G33	PN4_P26
PN4_N25	H33 [CC]	51	52	F34	PN4_N26
PN4_P27	E32	53	54	F33	PN4_P28
PN4_N27	E33	55	56	E34	PN4_N28
PN4_P29	C34	57	58	C32	PN4_P30
PN4_N29	D34	59	60	D32	PN4_N30
PN4_P31	B33	61	62	B32	PN4_P32
PN4_N31	C33	63	64	A33	PN4_N32

Table 11 Pn4 to FPGA Assignments

In Table 11, pins marked [CC] are clock capable and may be used to access the regional clocking resources in the FPGA.

Banks 11 & 13 are fitted with resistors to allow DCI terminations on Pn4 signals.

4.8.1. Pn4 Signalling Voltage

User FPGA Banks 11 & 13 and Pn4 can use 3.3V or 2.5V signalling standards selectable by switch SW2B.

SW2B	Pn4 voltage
Open	2.5V
Closed	3.3V

Table 12 Pn4 Voltage Selection

It should be noted that the switch does not directly route power to Banks 11 & 13. The link position is monitored by the board control logic which, in turn, sets a power multiplexer to be either 2.5V or 3.3V.

5. XRM IO146 Interface

The following tables provide the user with information on the pin-out of the XRM-IO146 when fitted to an ADM-XRC-5LX card.

The signal names P_1/N_1 etc are internal to the ADM-XRC-5LX. The important mapping is between the Mictor pin and the FPGA pin.

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_1	AL5	3	1	2	6	AP5	P_4
N_1	AL6	1	3	4	8	AP4	N_4
P_3	AM5	7	5	6	4	AN5	P_2
N_3	AL4	5	7	8	2	AN4	N_2
P_5	AN7	11	9	10	12	AM8	P_6
N_5	AM6	9	11	12	10	AM7	N_6
P_7	AN9	15	13	14	16	AM10	P_8
N_7	AN8	13	15	16	14	AL10	N_8
P_9	AP7	17	17	18	18	AN10	P_10
N_9	AP6	19	19	20	20	AM11	N_10
P_11	AN17	23	21	22	24	AP16	P_12
N_11	AM17	21	23	24	22	AP17	N_12
P_13	AP11	27	25	26	26	AM15	P_14
N_13	AP12	25	27	28	28	AM16	N_14
P_15	AP14	31	29	30	30	AP15	P_16
N_15	AN14	29	31	32	32	AN15	N_16
S_1	AL8	37	33	34	38	AP9	CLK0
S_2	AN13	93	35	36	40	AP10	CLK1
+5V		-	37	38	90	AH9	S_4

Table 13 IO146 Mictor Connector Pins 1 – 38

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_17	AA10	35	39	40	36	AA8	P_18
N_17	AA11	33	41	42	34	AA9	N_18
P_19	AB11	63	43	44	64	AB8	P_20
N_19	AB10	61	45	46	62	AB7	N_20
P_21	AJ7	67	47	48	68	AE7	P_22
N_21	AJ6	65	49	50	66	AD7	N_22
P_23	AG7	71	51	52	72	AD9	P_24
N_23	AH7	69	53	54	70	AC9	N_24
P_25	AG8	75	55	56	74	AC10	P_26
N_25	AH8	73	57	58	76	AD10	N_26
P_27	AE9	77	59	60	80	AF10	P_28
N_27	AF9	79	61	62	78	AG10	N_28
P_29	AK9	83	63	64	82	AG11	P_30
N_29	AK8	81	65	66	84	AF11	N_30
P_31	AJ10	87	67	68	88	AD11	P_32
N_31	AH10	85	69	70	86	AE11	N_32
S_8	AH2	105	71	72	89	AE8	CLK2
S_9	AE18	107	73	74	91	AF8	CLK3
+5V		-	75	76	95	AC8	S_3

Table 14 IO146 Mictor Connector Pins 39 - 76

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_33	Y11	103	77	78	100	W9	P_34
N_33	W11	101	79	80	98	Y9	N_34
P_35	W10	121	81	82	122	V9	P_36
N_35	V10	123	83	84	124	V8	N_36
P_37	W5	127	85	86	126	Y7	P_38
N_37	V5	125	87	88	128	Y8	N_38
P_39	Y6	129	89	90	130	AA6	P_40
N_39	W6	131	91	92	132	AA5	N_40
P_41	Y4	135	93	94	136	AB6	P_42
N_41	W4	133	95	96	134	AC5	N_42
P_43	AD5	137	97	98	140	AF5	P_44
N_43	AD6	139	99	100	138	AE6	N_44
P_45	AH4	141	101	102	144	AF6	P_46
N_45	AJ4	143	103	104	142	AG6	N_46
P_47	AK4	147	105	106	152	AG5	P_48
N_47	AJ5	145	107	108	150	AH5	N_48
S_5	W7	92	109	110	97	AA4	CLK4
S_6	AE4	94	111	112	99	AB5	CLK5
+5V		-	113	114	-		+5V

Table 15 IO146 Mictor Connector Pins 77 – 114

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_49	V4	149	115	116	146	W1	P_50
N_49	V3	151	117	118	148	V2	N_50
P_51	Y3	153	119	120	156	W2	P_52
N_51	Y2	155	121	122	154	Y1	N_52
P_53	AB1	159	123	124	160	AB3	P_54
N_53	AA1	157	125	126	158	AA3	N_54
P_55	AC2	161	127	128	164	AE2	P_56
N_55	AD1	163	129	130	162	AD2	N_56
P_57	AF1	167	131	132	168	AF3	P_58
N_57	AE1	165	133	134	166	AE3	N_58
P_59	AK2	171	135	136	172	AG3	P_60
N_59	AK3	169	137	138	170	AH3	N_60
P_61	AL1	175	139	140	176	AN2	P_62
N_61	AM1	173	141	142	174	AP2	N_62
P_63	AM2	179	143	144	180	AM3	P_64
N_63	AL3	177	145	146	178	AN3	N_64
S_7	AC3	96	147	148	102	AG1	CLK6
S_10	AF18	106	149	150	104	AG2	CLK7
+5V		-	151	152	-		+5V

Table 16 IO146 Mictor Connector Pins 115 - 152

6. Revision History

Date	Revision	Nature of Change
22-08-2006	1.0	First Release.
17-12-2007	1.1	Revised wording of motherboard power requirements.
16-01-2008	2.0	Updated to reflect changes to lclk and Front IO voltage selection on Rev2 PCBs.