Raggedstone3 User Manual

Issue – 1.0

Kit Contents

You should receive the following items with your Raggedstone3 development kit:

1 - Raggedstone3 Board
2 - 4 Digit, 7 Segment LED display (fitted)
3 – PCI mounting bracket (fitted)
3 – Prog2 (parallel port) or Prog3 (USB) programming cable

Contents

Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR RAGGEDSTONE3 BOARD. PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

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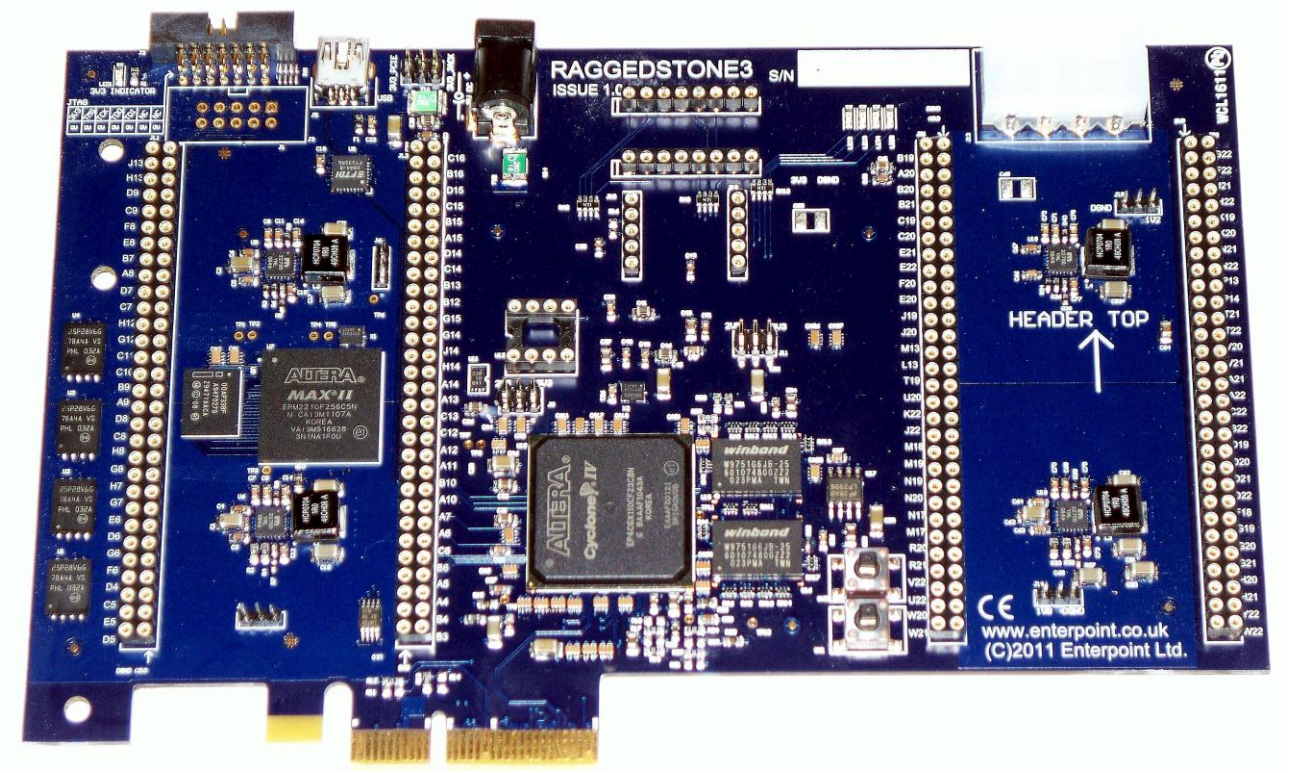


Figure 1 – Raggedstone3 Board.

Introduction

Welcome to your Raggedstone3 board. Raggedstone3 is Enterpoint's Cyclone™-IV PCIE version of the very popular Raggedstone1 FPGA development board.

The aim of this manual is to assist in using the main features of Raggedstone3. There are features that are beyond the scope of the manual. Should you need to use these features then please email support@enterpoint.co.uk for detailed instructions.

Raggedstone3 comes in two main variants either based on an EP4CGX110 or EP4CGX150 Cyclone™-IV FPGA. Should you need a non-standard size, speed grade, or temperature grade of Cyclone™-IV FPGA fitted to your Raggedstone3 please contact Enterpoint sales for a quote.

In addition Raggedstone3 is supported by a wide range of add-on modules. Some examples of these include:

ADC 7927 MODULE
LED DOT MATRIX MODULE
BUTTONS/SWITCHES/SATA/MEMORY MODULE
RS232 AND RS485 HEADER MODULES
DP83816 ETHERNET MODULE
SD CARD MODULE
DDR2 MODULE
IDE/5V TOLERANT CPLD MODULE
USB2 MODULE
D/A CONVERTER MODULE
ADV7202 MODULE
OLED DISPLAY MODULE
FT4232 4-CHANNEL USB MODULE
SPI ETHERNET MODULE
ACCELEROMETER MODULE
XC3S3400A ACCELERATOR MODULE
X1 XC6SLX150 ACCELERATOR MODULE
X2 XC6SLX150 ACCELERATOR MODULE

New modules are regularly added to our range

We can also offer custom DIL Header modules should you require a function not covered by our current range of modules. Typical turn around for this service is 6-8 weeks depending upon quantity ordered and availability of components.

Raggedstone3 Board

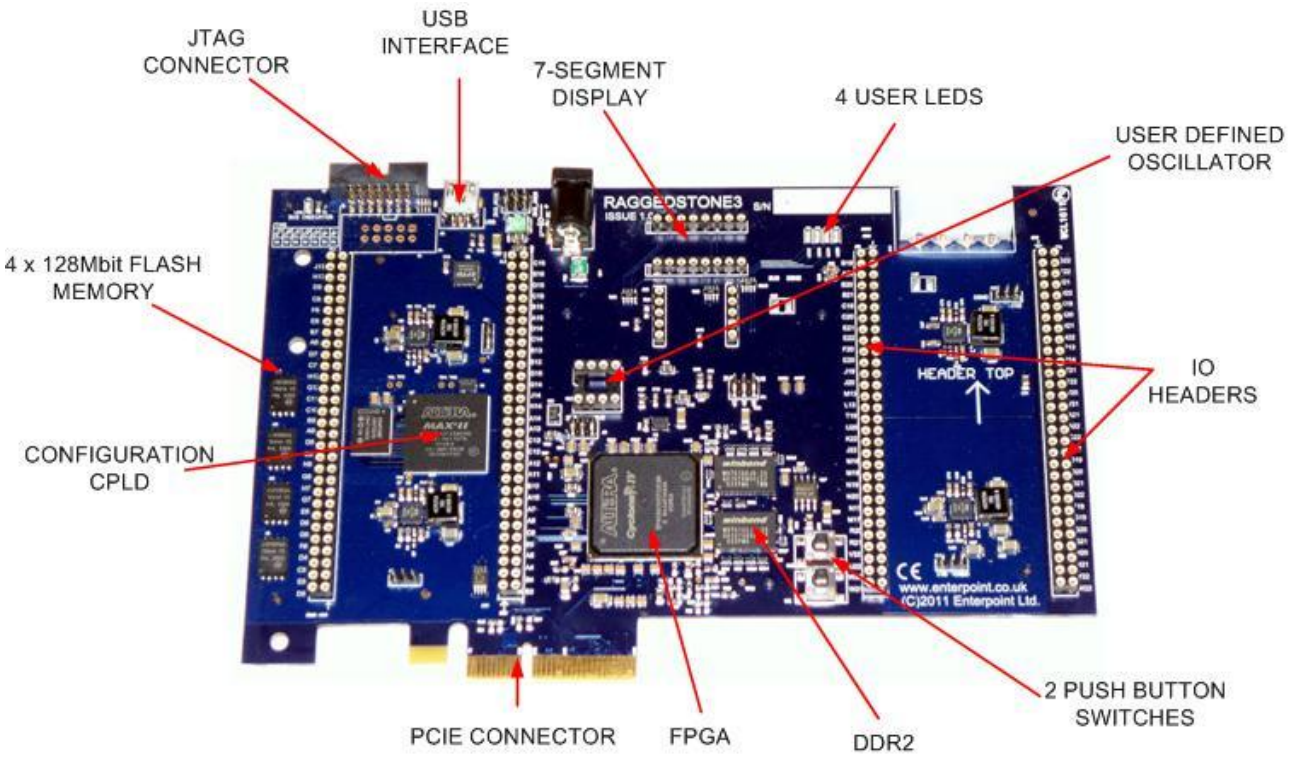


Figure 2 – Raggedstone3 MAIN FEATURES.

Getting Started

Your Raggedstone3 will be supplied with a default setting of jumpers fitted.

(1) Fit the LED 7 segment display into its connector (may already be fitted),

(2) Either connect the Raggedstone3 board to a powered PCIe connector or plug in a 5V power supply using the 2.1mm Jack socket.

(3) Fit an oscillator into the oscillator socket (may already be fitted).

(4) Switch on your power source.

Selecting the FPGA Bank voltages.

The User I/O pins of the Cyclone™-IV on Raggedstone3 are divided into 2 banks. The left hand side header pins are routed to Banks 7 and 8 of the FPGA, the Right hand side headers are routed to Banks 5 and 6. The IO voltages are set to either 3.3V or 2.5V using jumpers on the 6-pin headers: J11 for Banks 5 and 6, and J9 for Banks 7 and 8. Alternatively a user-generated Bank IO voltage could be introduced on pin 2 of J9 or J11. There is a 0V reference on pin 5 of J9 and J11 for this purpose. If you choose to use this option please refer to the Cyclone™-IV user manual from www.altera.com to check the allowed IO voltage range for the FPGA.

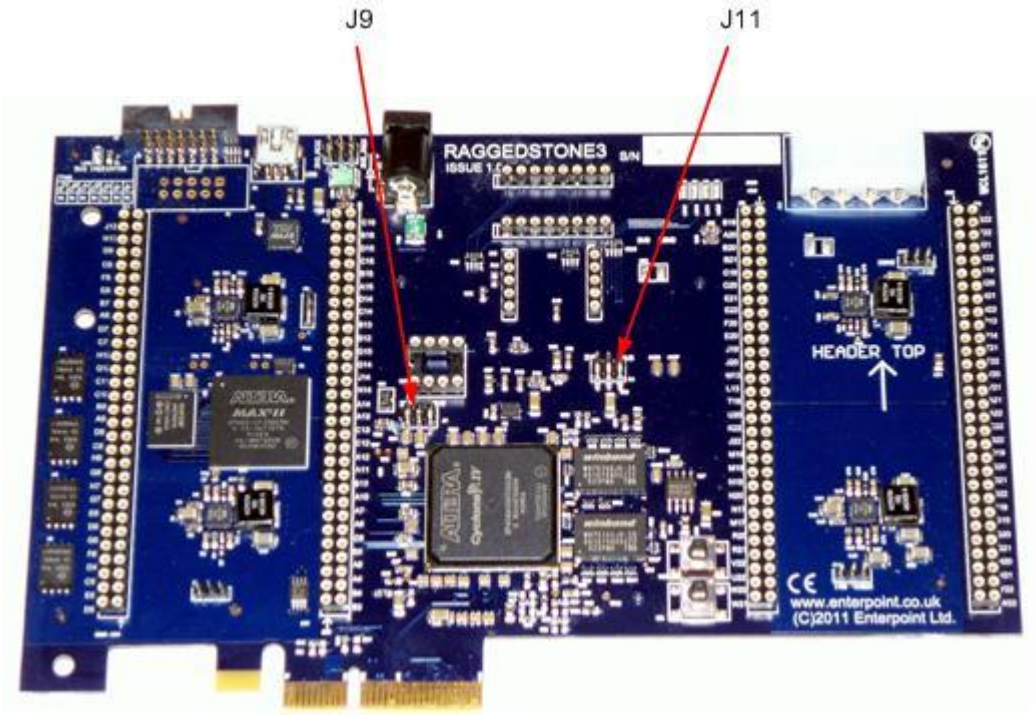


Figure 4 – Raggedstone3 VCCO Supply Selection.

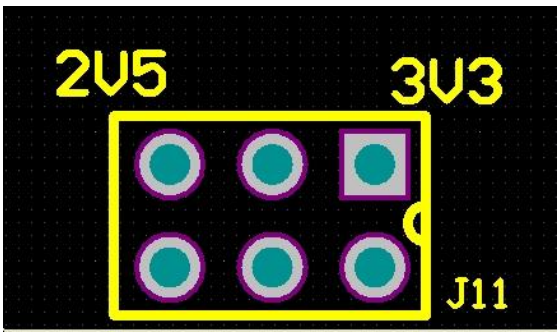


Figure 4a – Pin allocation of J11 (J9 is identical)

Programming Raggedstone3

The programming of the FPGA and SPI Flash on Raggedstone3 is achieved using the JTAG connection. There is a single JTAG chain on Raggedstone3. The JTAG chain allows the programming of the Cyclone™-IV, the configuration CPLD and the SPI Flash devices.

There are 2 JTAG connector sites on Raggedstone3. The first (J2) is a 2x7x2mm right angled connector which is used with the Enterpoint PROG4 programming cable. This JTAG connector has a layout as follows:

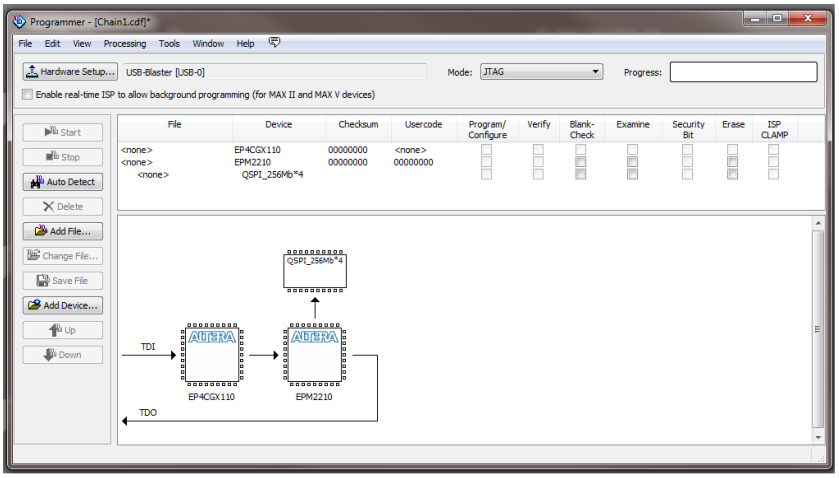
Top edge of board

GND	GND	GND	GND	GND	GND	GND
NC	NC	TDI	TDO	TCK	TMS	3V3

The second JTAG connector site (J1) is designed to accept the 2x5x0.1inch header used by the Altera USB-blaster programming cable. The pinout is shown below:

TDI	NC	TMS	TDO	TCK
GND	NC	NC	3V3	GND

Using the Quartus Programmer and Auto Detect the JTAG chain appears like this:



1. Programming the FPGA directly.

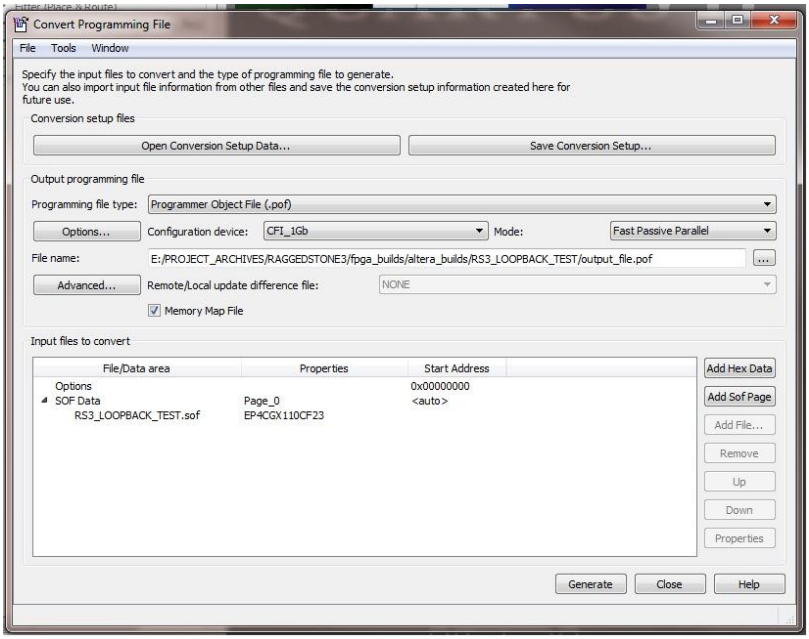
Direct JTAG programming of the Cyclone™-IV FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 below).
Direct JTAG programming of the FPGA using a .sof file is useful for fast, temporary programming during development of FPGA programs. Right click the word <none> to the left of 'EP4CGX110' above. Choose 'Add File'. Navigate to your .sof file. Then check the 'Program/Configure' box on the same line as the Cyclone™-IV device and click on the 'Start' button on the left. The progress bar at the top left of the screen should turn green as programming proceeds. This process is very quick (typically 10-15 seconds).

2. Programming the SPI flash memory.

This is a 2-stage process: converting the .sof file into a .pof file, then programming the flash memory.

a. Converting the file.

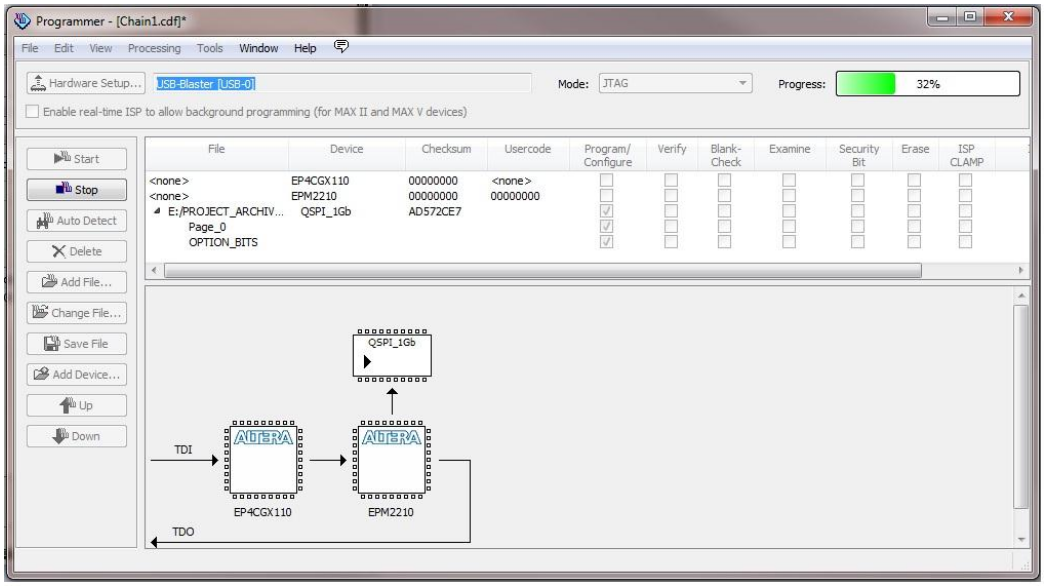
On the Quartus screen file menu choose ‘convert programming files’. This screen will appear:



Choose the options shown above, right clicking in the white window to activate the ‘add file’ button and navigating to your .sof file. Click ‘Generate’. The .pof file will appear at the location chosen.

b. **Programming the flash memory**.

Return to the Quartus programmer.



Right-click on the <none> to the left of ‘QSPI_1Gb’ and navigate to your .pof file. Check the boxes in the ‘Program/Configure’ column (it is only necessary to check the top of the 3 checked boxes, the others check automatically). Click on the ‘Start’ button. The SPI flash devices will program. This will take 5-10 minutes.

Raggedstone3 Features

Power Inputs and Pick-ups

Raggedstone3 is powered from 3.3V input direct from the PCIe edge connector or the 3.3V output from an on-board Micrel MIC22600 6A regulator circuit. This regulator circuit produces 3.3V from an input 5V supply. The choice of which of these 3.3V supplies is used is determined by the settings of J7.

When using the on-board 5V to 3.3V regulator the 5V input power that powers the board is supplied either through the DC Jack J8 or the disk drive connector J13 (5V pin). Only a single input 5V supply should be used as these inputs are hard connected together on Raggedstone3 and differential inputs will cause large currents to flow between the input 5V options. Care should also be taken not to exceed 5.5V on either of these inputs as an overvoltage will damage the regulator circuit.

The 1.2V, 1.8V and 2.5V power rails are derived from the internal 3.3V rails using 3 further MIC22600 regulator circuits. Fig.3 below shows the locations of test points where you can check voltages on the Raggedstone3.

For powering add-on modules Raggedstone3 has 30 header pins with 3.3V and 0V available on each side of the board allowing users to access power for their own add-on circuitry. These pins are arranged on a 0.1inch grid to enable users to plug in their own stripboard designs.

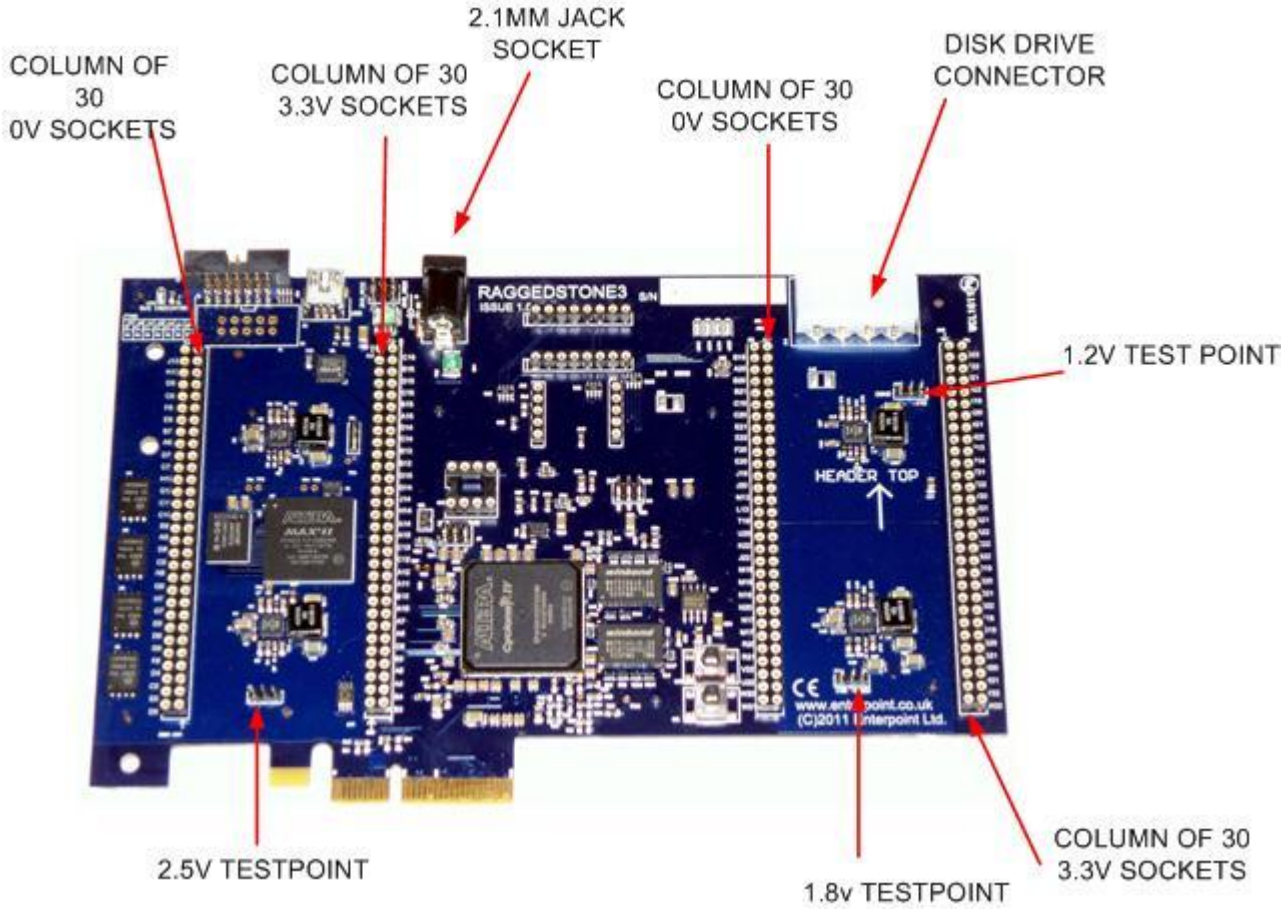


Figure 5 – Raggedstone3 Power Supply Features

Power Regulators

WARNING – THE REGULATORS MAY BECOME HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE RAGGEDSTONE3 BOARD IS IN OPERATION.

Raggedstone3 has four Micrel MIC22600 switching regulator circuits. These regulators are each capable of delivering 6 amps but may be limited by input supply and fusing restrictions. As standard a 2.6A fuse is fitted limiting the power usage of Raggedstone to about 8.6W but for special OEM build this fuse can be replaced with a higher capacity link allowing a higher board power envelope. In such special configurations the board power envelope can rise to 10W when powered from the PCIe connector or 20W when using one of the 5V input options. For OEM customers of this board we can also offer a MIC22700 in any on the MIC22600 regulator positions offering a slightly higher 7A capability if needed.

If more current is drawn the resettable fuse will cut the supply to the board, if this happens the power supply must be switched off and time given for the fuse to reset, which occurs when the fuse has cooled and reconnected its internal contacts. This typically takes 1-2 seconds.

A fifth linear regulator (LP2996) provides a 0.9V reference for the DDR2 memory devices.

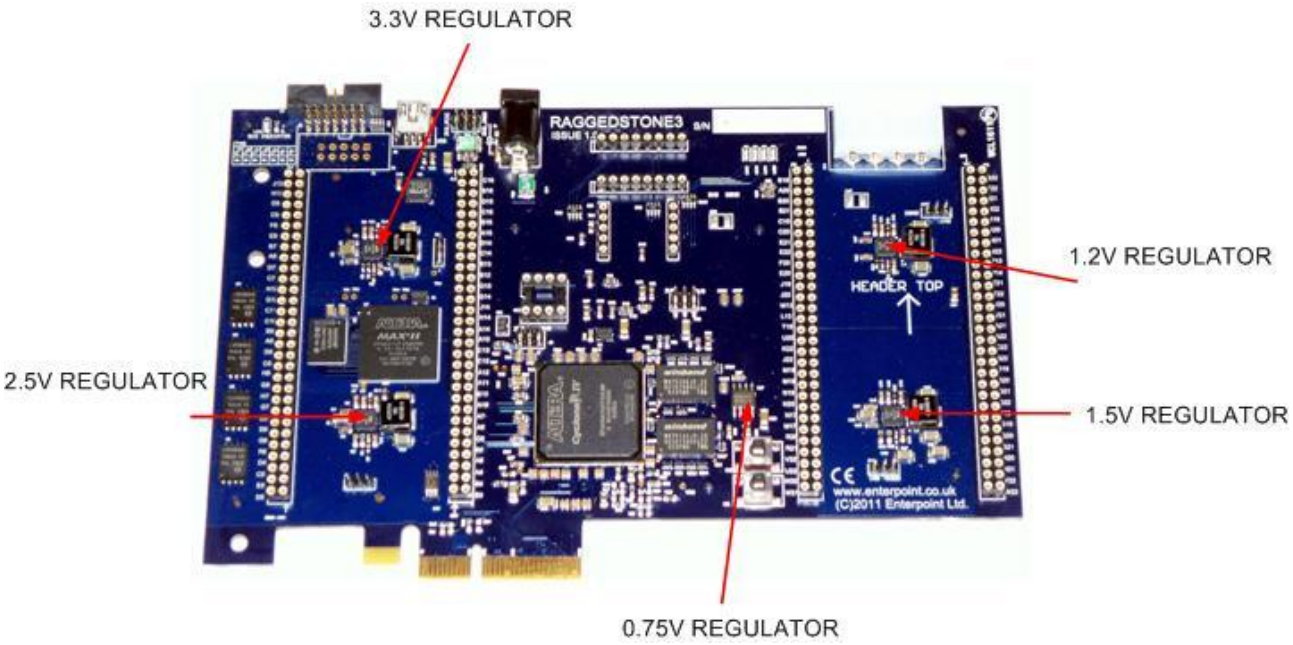


Figure 6 – Raggedstone3 POWER REGULATORS.

DIL Headers

The four 2x30 DIL Headers provide a simple mechanical and electrical interface for add-on modules. The connectors on this header are on a 0.1inch, 2.54mm pitch and allow either custom modules or strip board to be fitted. The headers have a row of permanent positive power sockets (3.3V) to the left of JL2 and JR2 and a row of permanent GND (0V) sockets to the right of the JL1 and JR1.

Voltages outside the range 0V to 3.3V must not be applied to the DIL headers. The Cyclone™-IV has an absolute maximum IO input voltage of 3.9V. The connections between the DIL the headers and the FPGA are shown below:

	LEFT DIL HEADER						RIGHT DIL HEADER				
	JL1			JL2			JR1			JR2	
1	J13	0V		3.3V	C16		B19	0V		3.3V	G22
2	H13	0V		3.3V	B16		A20	0V		3.3V	F22
3	D9	0V		3.3V	D15		B20	0V		3.3V	J21
4	C9	0V		3.3V	C15		B21	0V		3.3V	H22
5	F8	0V		3.3V	B15		C19	0V		3.3V	K19
6	E8	0V		3.3V	A15		C20	0V		3.3V	K20
7	B7	0V		3.3V	D14		E21	0V		3.3V	N21
8	A8	0V		3.3V	C14		E22	0V		3.3V	N22
9	D7	0V		3.3V	B13		F20	0V		3.3V	R19
10	C7	0V		3.3V	B12		E20	0V		3.3V	T20
11	H12	0V		3.3V	G15		J19	0V		3.3V	T19
12	G12	0V		3.3V	G14		J20	0V		3.3V	U20
13	C11	0V		3.3V	J14		M13	0V		3.3V	V20
14	C10	0V		3.3V	H14		L13	0V		3.3V	V21
15	B9	0V		3.3V	A14		T21	0V		3.3V	A21
16	A9	0V		3.3V	A13		T22	0V		3.3V	A22
17	D8	0V		3.3V	C13		K22	0V		3.3V	C22
18	C8	0V		3.3V	C12		J22	0V		3.3V	B22
19	E6	0V		3.3V	A12		M18	0V		3.3V	D19
20	D6	0V		3.3V	A11		M19	0V		3.3V	D20
21	H7	0V		3.3V	B10		N19	0V		3.3V	D21
22	G7	0V		3.3V	A10		N20	0V		3.3V	D22
23	C4	0V		3.3V	A7		N17	0V		3.3V	F18
24	C3	0V		3.3V	A6		M17	0V		3.3V	G19
25	C2	0V		3.3V	C6		R20	0V		3.3V	G20
26	C1	0V		3.3V	B6		R21	0V		3.3V	G21
27	D4	0V		3.3V	A5		V22	0V		3.3V	H20
28	C5	0V		3.3V	A4		U22	0V		3.3V	H21
29	E5	0V		3.3V	B4		W20	0V		3.3V	Y22
30	D5	0V		3.3V	B3		W21	0V		3.3V	W22

The signals on the DIL headers are arranged in LVDS pairs and routed such that the trace lengths approximately match and skew is minimised within pair. Adjacent LVDS_P and LVDS_N form the matched pair at the DIL Header and the Cyclone™-IV FPGA. For example H12 and G12 form one pair.

All LVDS pairs can be used as general inputs/outputs from the Cyclone™-IV.

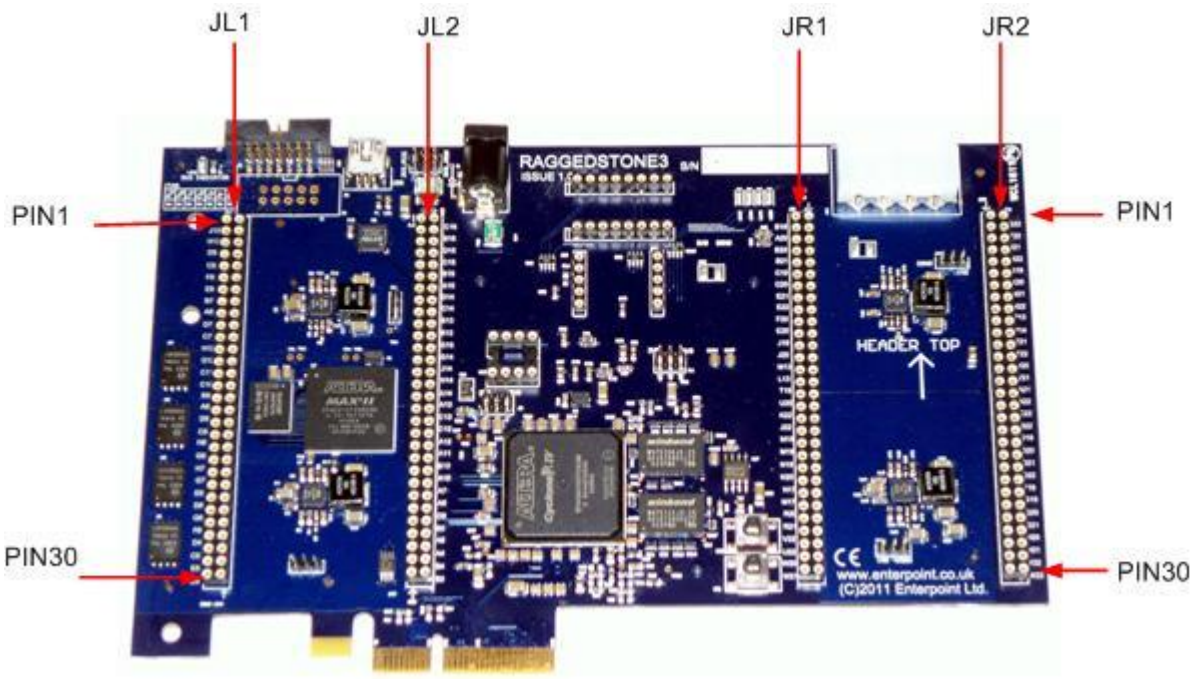


Figure 7 – Raggedstone3 DIL Headers

SIL Headers

There are 4 SIP headers on Raggedstone3. They are arranged as 2 pairs. J10 and J12 form the Clock Module header and have 5 pins each. The two 8-pin SIL headers are usually used to support the LTC-C4627JR 4-digit 7-segment display (U14), however the 7 segment display to make these pins available to the user. Voltages outside the range 0V to 3.3V must not be applied to the SIL headers. The Cyclone™-IV has a maximum IO input voltage of 3.9V.

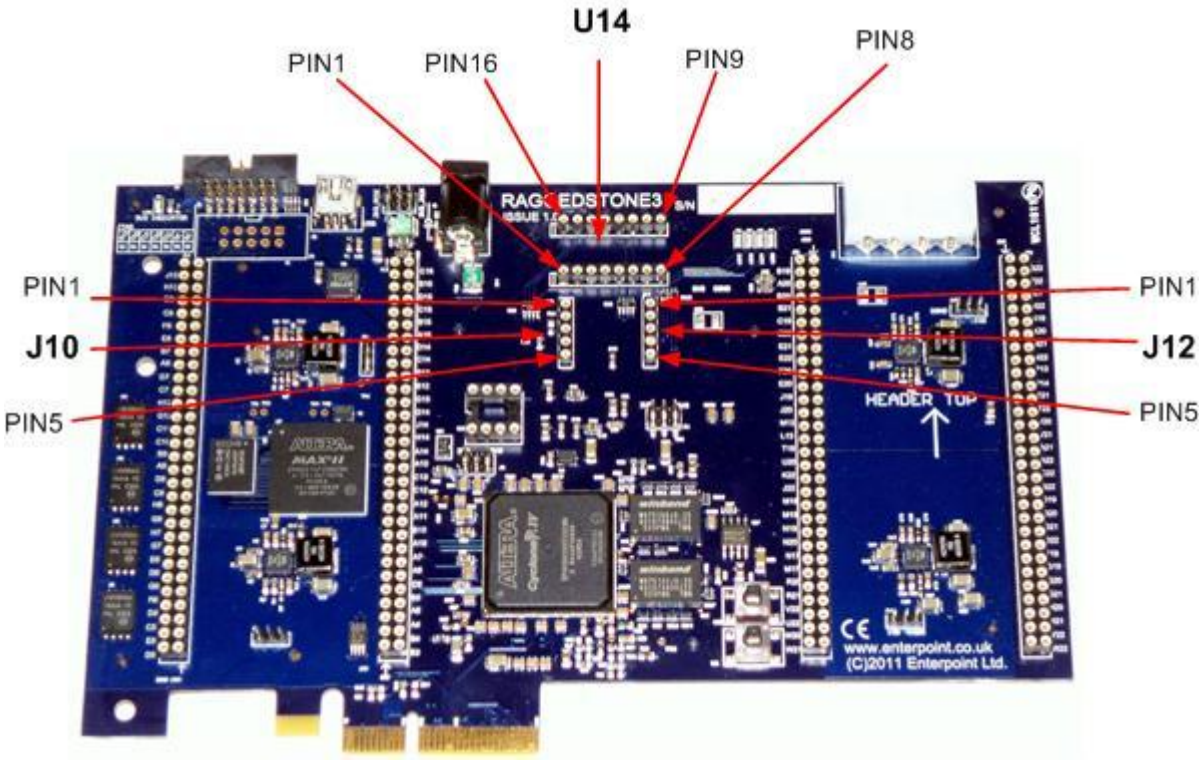


Figure 8 – Raggedstone3 SIL Headers

1. CLOCK MODULE HEADER

These header pins are designed to allow the Enterpoint Clock module to be fitted. This module is fitted with an ICS8442 700MHZ, Crystal Oscillator-To-Differential LVDS Frequency Synthesizer device. If this module is not fitted the header pins are available to the user.

J12 has a permanent positive power pin (3V3) at the top position. J10 has a GND (0V) connection at the top position. The connections to the FPGA are shown below with the Bank number in parentheses:

J10				J12		
SIGNAL NAME	**J10 PIN NUMBER**	**FPGA PIN**		**SIGNAL NAME**	**J12 PIN NUMBER**	**FPGA PIN**
DGND	PIN1	0V		VD3V3	PIN1	3.3V
GCLK1	PIN2	M7(3)		CLKHDR1	PIN2	P20(5)
GCLK0	PIN3	N7(3)		CLKHDR2	PIN3	P22(5)
CLKHDR5	PIN4	L19(6)		CLKHDR3	PIN4	R16(5)
CLKHDR6	PIN5	L20(6)		CLKHDR4	PIN5	R17(5)

The connections to J10 are LVDS pairs connecting to Differential Clock inputs on the FPGA. The connections to R16/R17 and L19/L20 are on LVDS pairs.. The Connections to P20 and P22 are to general purpose IO pins.

The horizontal distance between J12 and J10 is 0.6inch (15.25mm).

2. 7-SEGMENT DISPLAY HEADER

The two 8-pin headers which form the 7-segment display holder U14 have 14 connections to the FPGA. Of these 14 connections 8 (shown **BOLD**) have series 470ohm resistors, which are normally used as current-limiting resistors for the 7 segment display. This should be taken into account if this header is used for other purposes. The connections between U14 and the FPGA are shown below (Bank number in parentheses):

PIN16 D11(8)	**PIN15 F12(7)**	**PIN 14 D12(8)**	**PIN13 H17(6)**	PIN12 J15(6)	**PIN11 A18(7)**	PIN10 NC	PIN9 NC
PIN1 G10(8)	PIN2 D10(8)	**PIN3 D13(7)**	PIN4 H9(8)	**PIN5 G16(6**)	PIN6 G17(6)	**PIN7 A19(7)**	PIN8 D16(7)

The vertical distance between the upper and lower pins of U6 is 0.4inch (10.2mm).

FPGA

Raggedstone3 supports Cyclone™-IV devices in the 484-pin package. Raggedstone3 is normally available with the EP4CGX110 FPGA fitted, which has 109,424 logic elements or the larger EP4CGX150 (149,760 Logic elements). Should you have an application that needs industrial or faster speed grades please contact sales for a quote at boardsales@enterpoint.co.uk

Oscillator

The oscillator socket U12 on Raggedstone3 supports 3.3V, 8-pin DIL outline, oscillator crystals. This clock signal is routed directly through to the FPGA on pin **K10,** Bank 8, which is a Clock input to the FPGA.

A fixed 25MHz ASEM oscillator is also fitted to Raggedstone3. The signal from this oscillator is connected to the FPGA on pins L21 and L22, Bank 6, which are Clock inputs to the FPGA.

The Cyclone™-IV has Digital Clock Multipliers (DCMs) to produce multiples, divisions and phases of clock signals. Please consult the Cyclone™-IV datasheet available from the Altera website at http://www.altera.com if multiple clock signals are required.

LEDs

On Raggedstone3 there are 5 LEDS. LED1 is situated on the top left corner of the board and indicates the presence of the 3.3v power rail. It is not available for other uses. LEDs 2 to 5, which are situated the top of the board to the right of the 7-segment display, are user LEDs and are connected to the FPGA as indicated below:

LED2	LED3	LED4	LED5
R22	L15	T18	T17

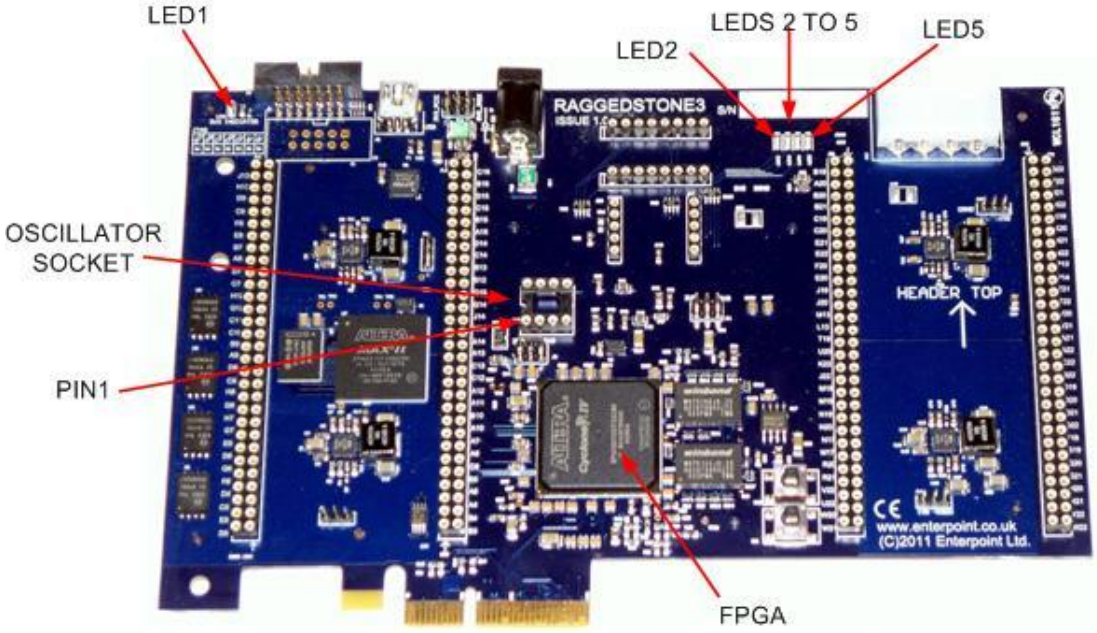


Figure 8 – Raggedstone3 FPGA, Oscillator socket and LEDs

USB

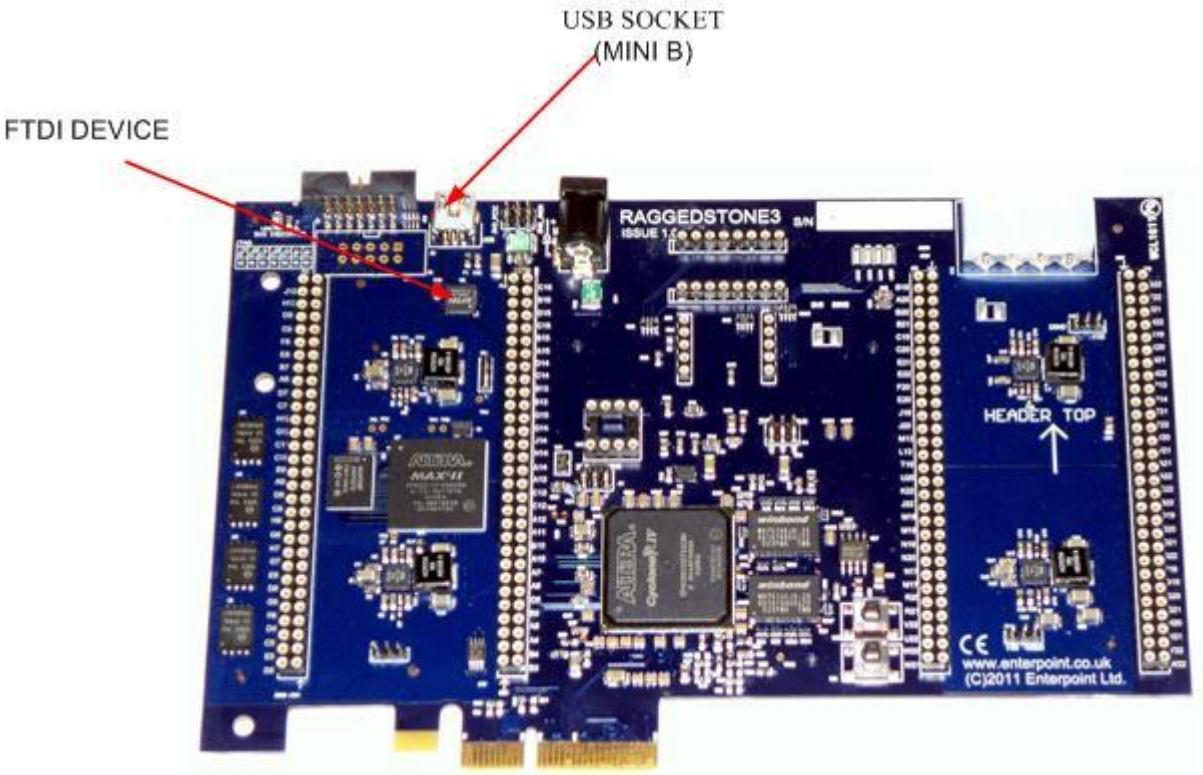


Figure 10 – Raggedstone3USB interface.

The USB interface on the Raggedstone3 is achieved using an FT232R USB to serial UART interface. The datasheet and drivers for this device are available from http://www.ftdichip.com. When appropriate drivers are installed the Raggedstone3 USB port should be detected as a serial port. Alternative data optimised drivers are also available from FTDI.

The FT232R is connected to the Cyclone™-IV and provided a simple UART, or other converter, is implemented then the data sent over the USB serial port can be used either as control and/or data information. This allows a host computer to act in a number of ways including system control and data storage functions. The connections between the USB device and the FPGA are shown below:

FT232R	FPGA PIN
CTS#	D17
DCD#	C17
DSR#	A17
RI#	E17
RTS#	J10
DTR#	A16
TXD	F16
RXD	F17

Push Button Switches

Raggedstone3 has two tactile push-button switches. To use these switches it is necessary to set the IO pins connected to the switches to have a pull up resistor setting in the constraints file. Any switch pressed, or made, will then give a LOW signal at the FPGA otherwise a HIGH is seen. The two push button switches are connected to the following IO pins.

SWITCH 1	SWITCH 2
L14	H8

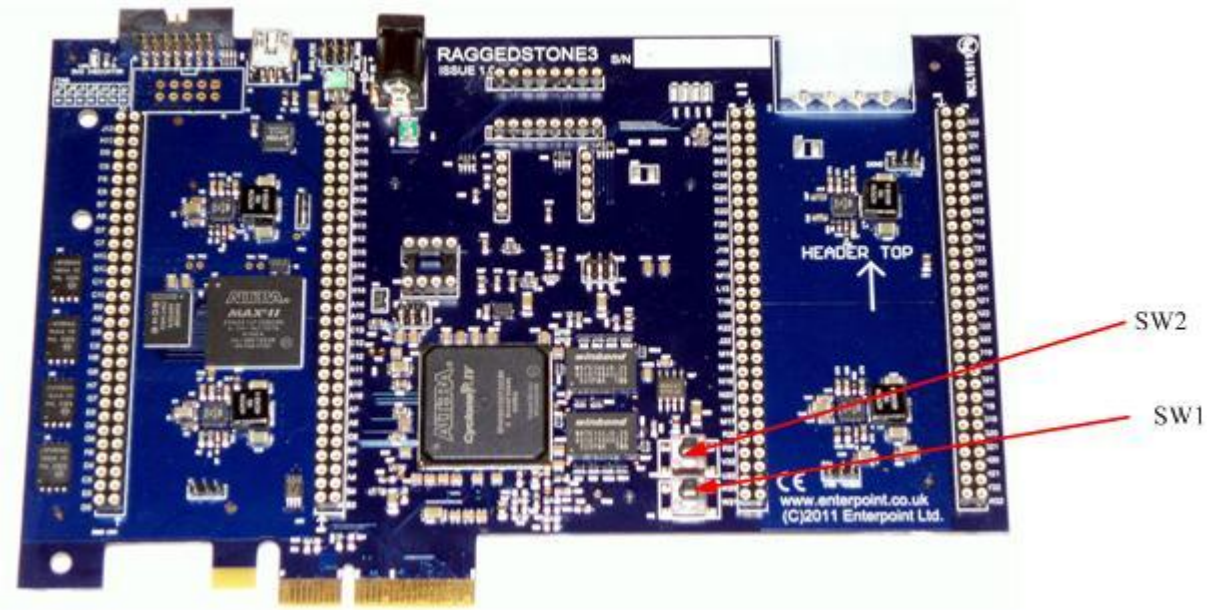


Figure 10 – Raggedstone3 Switches

DDR2

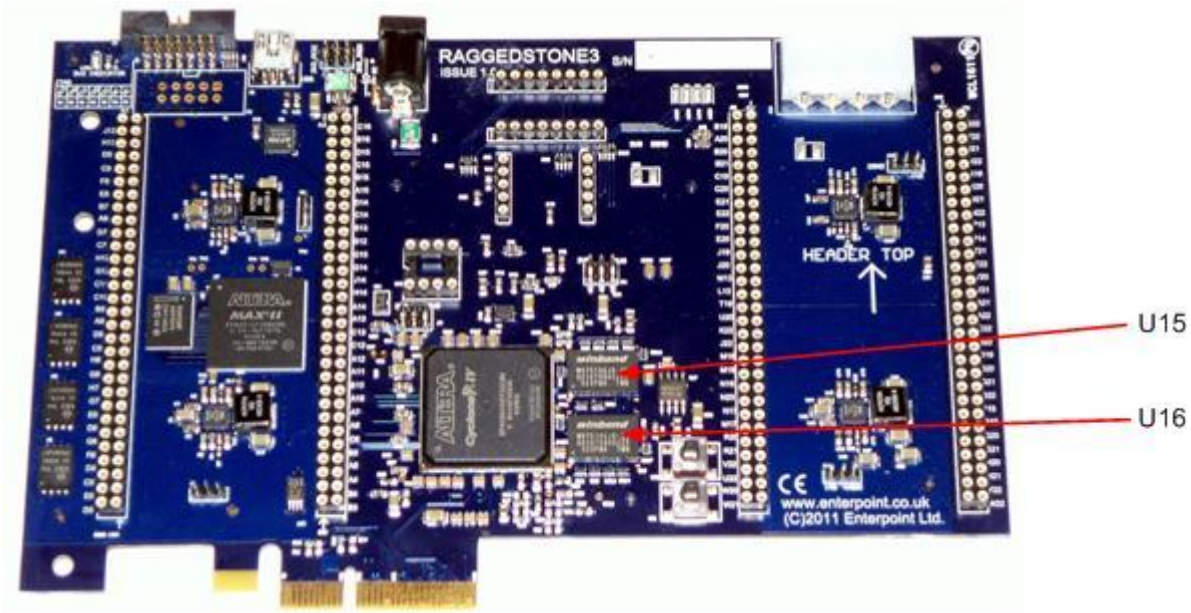


Figure 10 – Raggedstone3 DDR2

Raggedstone3 has two Micron MT47H32M16BN or Winbond W9751G6JB-25 DDR2 devices as standard. These devices are organised as 8 Meg x 16 x 4 banks. These devices are supported by the hard core memory controller that is in the Cyclone™-IV FPGA. To add this core to your design use the Megafunction wizard tool, part of the Quartus suite, which will generate implementation templates in VHDL or Verilog for the configuration that you want to use. More details on the memory controller can be found in the user guide http://www.altera.com.

The DDR2 devices use 16 address lines and 32 data lines to address all the available memory, which can be accessed at speeds of 2.5ns. The Address lines A[0:15] are common to the two DDR2 devices, as are the ODT, BA[0:2], CS, RAS, CAS, WE and all the Clock signals. The remaining signals from each DDR2 device are routed separately to the FPGA, U16 connects via data lines DQ[0:15], DM[0:1] and DQS[0:1] while U15 connects via DQ[16:31], DM[2:3] and DQS[2:3].

More details of the DDR2 can be found from www.micron.com.

All the signals are terminated with appropriate resistors.

There is a timing loop implemented between pins AA12 and AB12.

The connections between the FPGA and the DDR2 devices are shown below:

The DDR2 sites have the following connections to the FPGA:

DDR2 SIGNAL	FPGA PIN	DDR2 PIN		DDR2 SIGNAL	FPGA PIN	DDR2 PIN
DDR_A0	R11	M8		DDR_DQ0	AA10	G8(U16)
DDR_A1	AB11	M3		DDR_DQ1	W11	G2(U16)
DDR_A2	AB5	M7		DDR_DQ2	Y11	H7(U16)
DDR_A3	AA7	N2		DDR_DQ3	Y12	H3(U16)
DDR_A4	AB7	N8		DDR_DQ4	AB8	H1(U16)
DDR_A5	AB9	N3		DDR_DQ5	AA9	H9(U16)
DDR_A6	W12	N7		DDR_DQ6	Y9	F1(U16)
DDR_A7	T9	P2		DDR_DQ7	W9	F9(U16)
DDR_A8	AA13	P8		DDR_DQ8	AB4	C8(U16)
DDR_A9	AB13	P3		DDR_DQ9	Y6	C2(U16)
DDR_A10	T14	M2		DDR_DQ10	Y7	D7(U16)
DDR_A11	U14	P7		DDR_DQ11	W7	D3(U16)
DDR_A12	AB16	R2		DDR_DQ12	T11	D1(U16)
DDR_A13	Y17	R8		DDR_DQ13	Y5	D9(U16)
DDR_A14	AB21	R3		DDR_DQ14	W6	B1(U16)
DDR_A15	AB19	R7		DDR_DQ15	W5	B9(U16)
DDR_BA0	AB22	L2		DDR_DQ16	AA16	G8(U15)
DDR_BA1	W18	L3		DDR_DQ17	AB18	G2(U15)
DDR_BA2	AB17	L1		DDR_DQ18	W17	H7(U15)
DDR_CS_N	AA20	L8		DDR_DQ19	U15	H3(U15)
DDR_RAS_N	AA21	K7		DDR_DQ20	Y16	H1(U15)
DDR_WE_N	R14	K3		DDR_DQ21	Y18	H9(U15)
DDR_CAS_N	AA19	L7		DDR_DQ22	AA18	F1(U15)
DDR_CKE	U6	K2		DDR_DQ23	Y19	F9(U15)
DDR_CLK	U7	J8		DDR_DQ24	W15	C8(U15)
DDR_CLK_N	V7	K8		DDR_DQ25	Y14	C2(U15)
DDR_DM_0	AB6	F3(U16)		DDR_DQ26	W14	D7(U15)
DDR_DM_1	AA6	B3(U16)		DDR_DQ27	AB15	D3(U15)
DDR_DM_2	Y15	F3(U15)		DDR_DQ28	R13	D1(U15)
DDR_DM_3	AB10	B3(U15)		DDR_DQ29	AB14	D9(U15)
DDR_DQS_0	Y10	F7(U16)		DDR_DQ30	Y13	B1(U15)
DDR_DQS_1	Y8	B7(U16)		DDR_DQ31	W13	B9(U15)
DDR_DQS_2	AA15	F7(U15)		DDR_ODT	AA22	K9
DDR_DQS_3	T13	B7(U15)				

PCIe Edge Connector

The Raggedstone3 has a x4 PCIe Interface. The pin out of the Cyclone™-IV FPGA has been chosen such that the PCI interface follows the pinout for the Altera Cyclone™-IV hard core for PCIe which can be generated automatically by the Quartus software.

The configuration arrangement of Raggedstone3 allows the FPGA to configure within the time requirements for the PCIe specification.

The connections between the PCIe connector and the FPGA are shown below.

SIGNAL NAME	PCIE CONNECTOR PIN	FPGA PIN
PCIE_CLK_P	A13	M11
PCIE_CLK_N	A14	N11
PCIE_TX0_P	A16	V2
PCIE_TX0_N	A17	V1
PCIE_RX0_P	B14	Y2
PCIE_RX0_N	B15	Y1
PCIE_PWRGD	A11	M20
PCIE_PRESENT#1	A1 TO B32	
PCIE_PRESENT#2	B17	
PCIE_PRESENT#3	B32 TO A1	
PCIE_TX1_P	A21	P2
PCIE_TX1_N	A22	P1
PCIE_RX1_P	B19	T2
PCIE_RX1_N	B20	T1
PCIE_TX2_P	A25	K2
PCIE_TX2_N	A26	K1
PCIE_RX2_P	B23	M2
PCIE_RX2_N	B24	M1
PCIE_TX3_P	A29	F2
PCIE_TX3_N	A30	F1
PCIE_RX3_P	B27	H2
PCIE_RX3_N	B28	H1

Serial EEPROM

Raggedstone3 has a 16K Two-Wire Atmel AT24C16BY6 EEPROM device which uses a simple Parallel address and single serial data line and clock. There is also a write protect line which can be used to electronically safeguard the information contained in the device

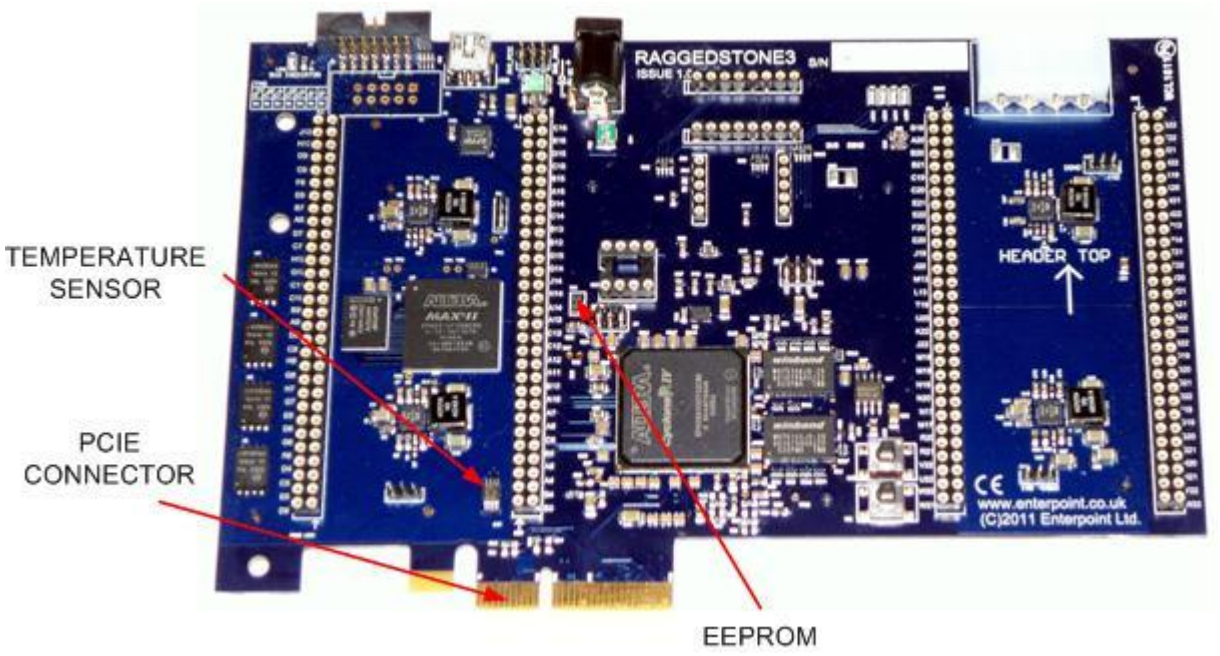
The EEPROM has 3 address lines which are permanently connected to 0V. It can run at speeds up to 400 kHz. This serial memory has 2048 words of 8 bits and employs a byte or page programming system. The connections between the EEPROM and the FPGA are shown below:

EEPROM SIGNAL	FPGA PIN
SDA	B18
SCL	C18
WP	G18

Temperature Sensor

There is a temperature sensor (type LM75C) on Raggedstone3 which has a 2-wire serial interface and an output which behaves as an over-temperature warning. The connections to the FPGA are shown below:

SIGNAL	FPGA PIN
SDA	B1
SCL	A2
OVER-TEMPERATURE	A1



Configuration CPLD

Raggedstone3 uses an EPM2210F256C5 CPLD to configure the Cyclone™-IV FPGA from four 128Mbit SPI flash memory devices. This device is preloaded with a core which takes the configuration data from the 4 flash memory devices and sends it in an 8 bit parallel format to the FPGA. A 50 MHz oscillator drives the configuration rate. The connections between the CPLD and the FPGA are:

SIGNAL NAME	CYCLONE™-IV FPGA	CPLD PIN
CFG_DATA0	K4	M15
CFG_DATA1	D1	L12
CFG_DATA2	G8	M16
CFG_DATA3	G6	M13
CFG_DATA4	F6	L14
CFG_DATA5	W4	N14
CFG_DATA6	Y4	M14
CFG_DATA7	R9	P15
CONF_DONE	U5	N15
NSTATUS	R8	N16
DCLK	D3	L13
NCONFIG	H4	L11

SPI Flash Memory

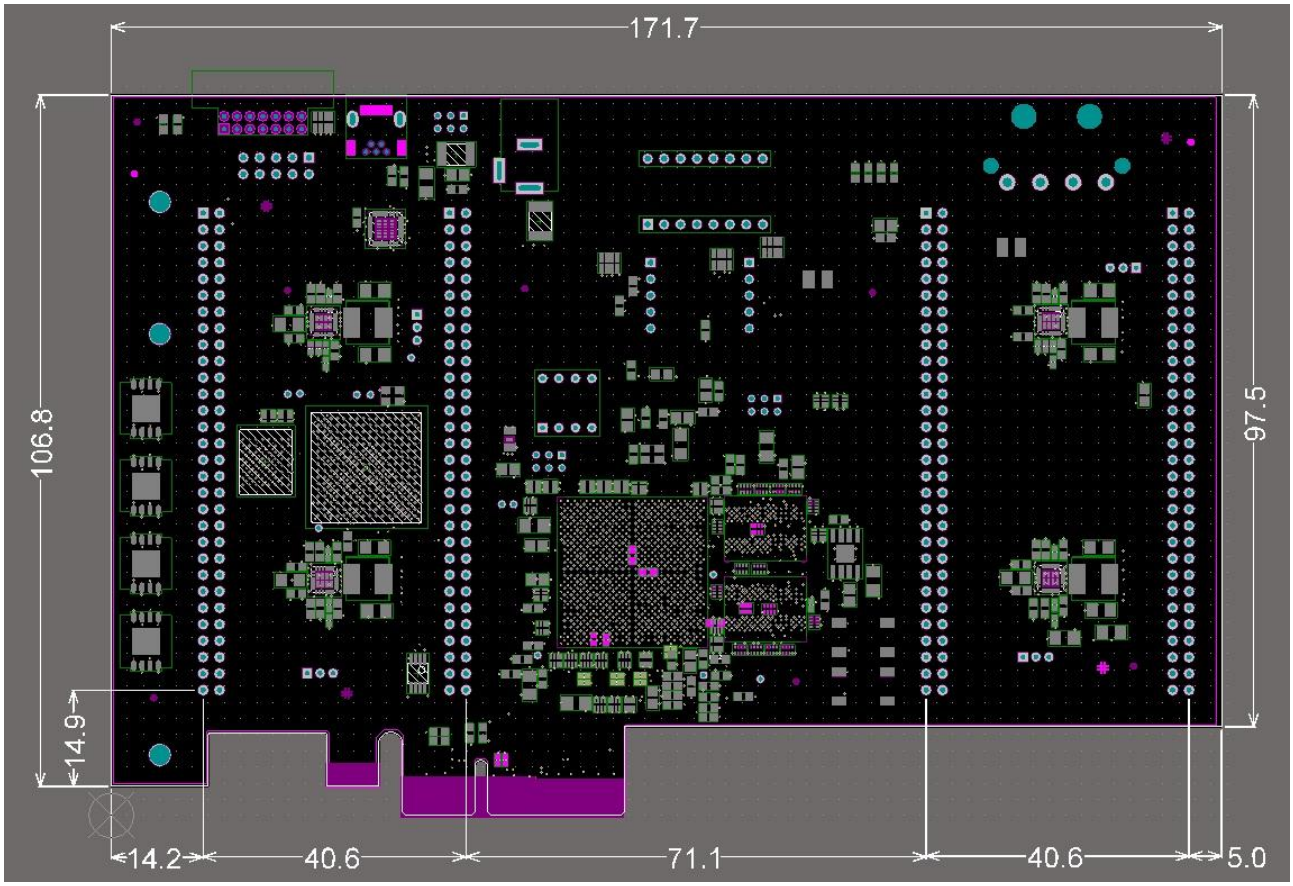
The four MX25L25635ENZI Quad flash memory devices hold the configuration code for the FPGA when it is powered providing a suitable .pof file is programmed into the devices.

The combined capacity of the four 256Mbit flash memory devices is 1GBit, with a single configuration bitstream for Raggedstone3 taking 3.5MBits. Advanced users may wish to use the remaining space in the four flash memory devices for alternative configuration data files or user code and data storage. This will entail modifying the configuration file in the CPLD.

After configuration the SPI Flash devices can be accessed via the following pins of the CPLD: The pin number on the flash memory device appears in parentheses following the signal name.

SIGNAL	MX25 PIN	MEMORY DEVICE			
		U1	U2	U3	U4
CS	1	P13	M12	M11	R7
Q/MISO1	2	R16	R13	N9	T6
WP/MISO2	3	P12	P11	R8	M7
HOLD/MISO3	7	T15	T13	N8	R6
CCLK	6	N12	N11	T7	N7
D/MISO0	5	R14	R12	P8	T5

Mechanical information



All dimensions are shown in millimetres AND are subject to manufacturing tolerances.

The maximum height of the components on the board is approximately 13mm measured from the lower surface of the PCB to the upper surface of the 7-segment display. If the display is not fitted the maximum height is approximately 12.5mm measured from the lower surface of the PCB to the upper surface of the 2.1mm jack socket. If you need any further mechanical information please contact us. Contact information is shown on page 27 of this manual.

Medical and Safety Critical Use

Raggedstone3 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accepts no liability for any failure or defect of the Raggedstone3 board, or its design, when it is used in any medical or safety critical application.

Warranty

Raggedstone3 comes with a 90 day return to base warranty. Do not attempt to solder connections to the Raggedstone3. Enterpoint reserves the right not honour a warranty if the failure is due to soldering or other maltreatment of the Raggedstone3 board.

Outside warranty Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Raggedstone3 has been maltreated or otherwise deliberately damaged. Please contact support if need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Raggedstone3 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone - ++44 (0) 121 288 3945
Email - support@enterpoint.co.uk