NPMC-860-SIO
CPU PMC Module
Technical Reference Manual V1.7
HW Revision 1.1

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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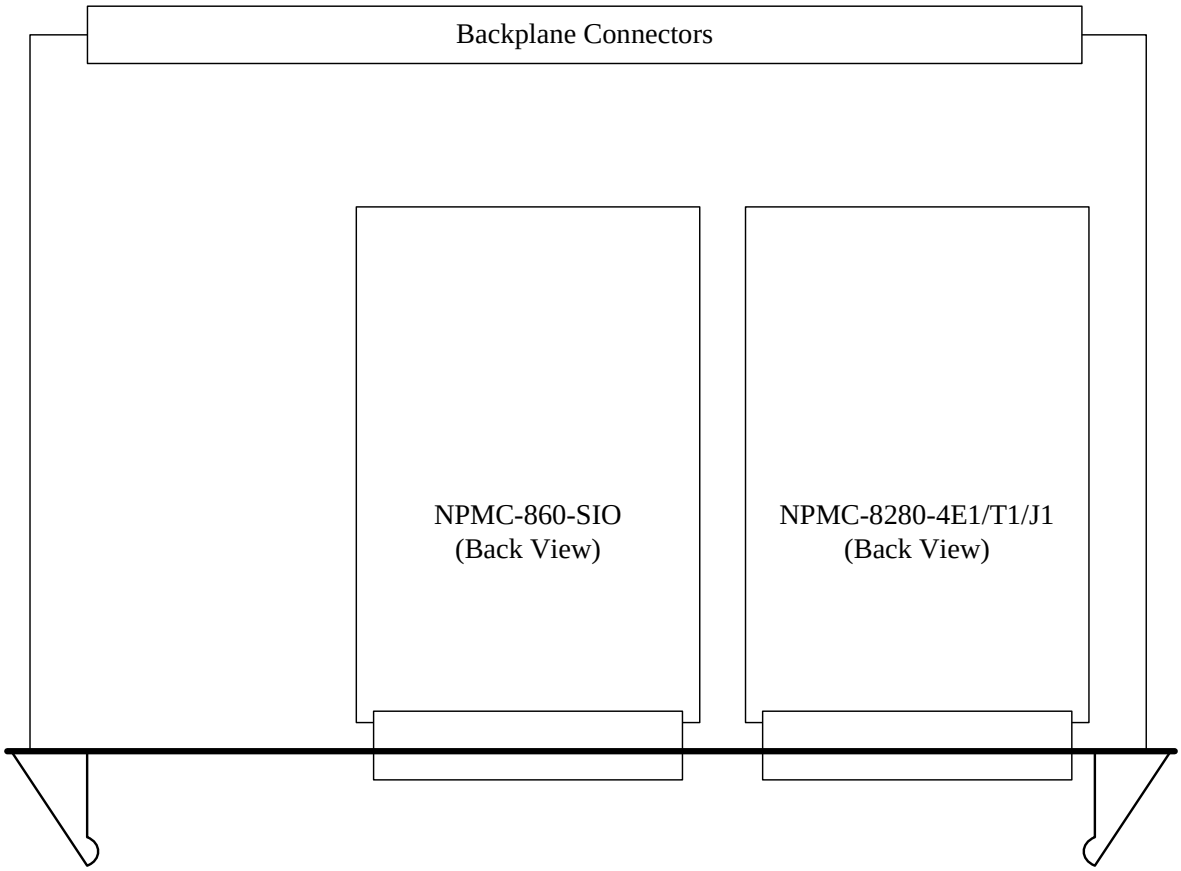
1 Introduction

The **NPMC-860-SIO** is a high performance standard CPU PCI Mezzanine Card Type 1. It can be plugged onto any carrier board supporting PMC standards:

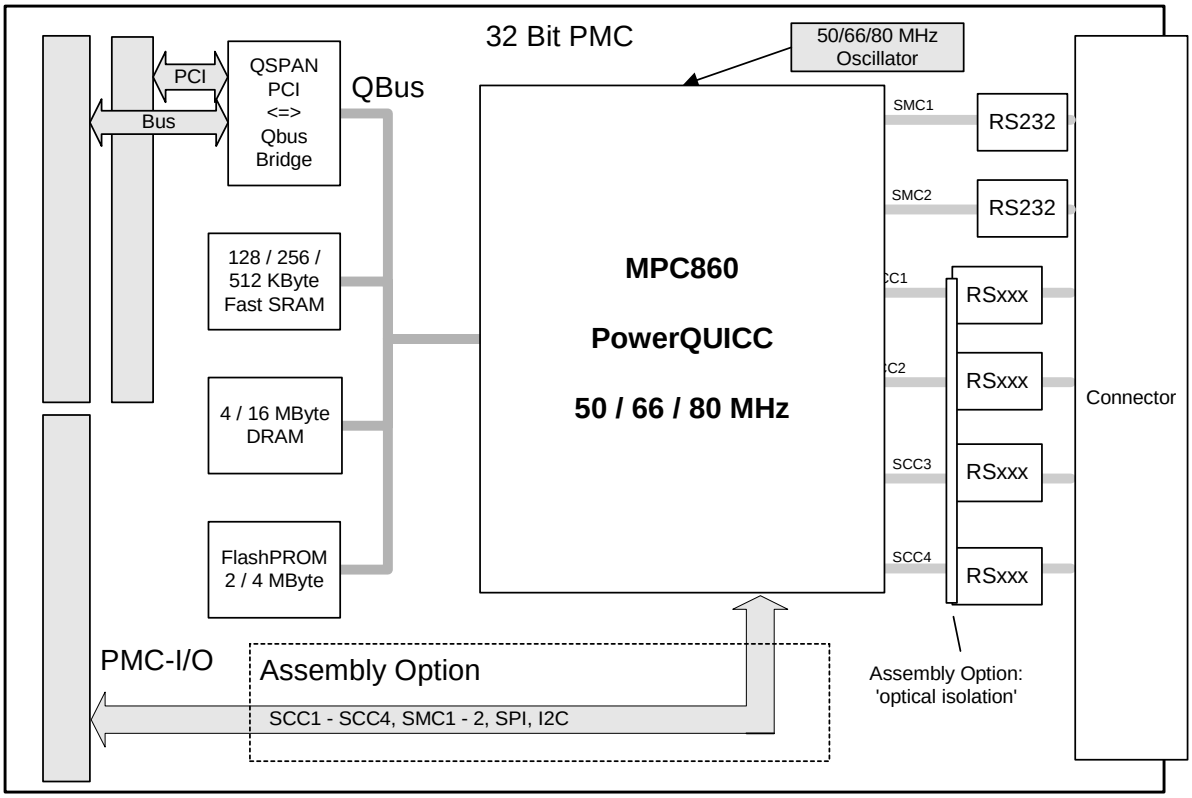
Figure 1: NPMC-860-SIO on a VMEbus carrier



The **NPMC-860-SIO** has the following major features on-board:

- PowerQUICC MPC860 based Embedded PowerPC Architecture
- Front-panel I/O
- PCI Bus interface
- Single Slot VME solution together with the PMC carrier board

Figure 2: NPMC-860-SIO Block Diagram



The onboard devices are in detail as follows:

- **Memory**

  DRAM: The **NPMC-860-SIO** provides 4 or 16 MByte EDO DRAM on board. The DRAM is 32 bit wide. Default: 16 MByte assembled

  Flash PROM: The 8 bit boot Flash PROM provides a maximum capacity of 4 MByte. Default: 2 MByte assembled

  SRAM: The high speed 32 bit SRAM capacity is 512 KByte (max.). Default: 128 KByte assembled

- **Interfaces**

  The **NPMC-860-SIO** includes a 32 bit 33 MHz PCI bus interface.

- **I/O**

  The 4 SCC channels and the 2 SMC channels are connected to the front panel connector by serial transceivers, which optionally can form RS232, RS422, or RS485 interfaces. All SCC channels may be optically decoupled separately. The SMC channels are hard-wired to 2 RS232 ports (no handshake).

  Alternatively, all signals of the SCCs, the SMCs, the SPI- and the I²C-ports are available on the PMC I/O connector. To be used there, all front panel transceivers have to be disabled.

  The normal data rate supported for RS232 is 115 KBaud, for RS422 and RS485 it is 500 KBaud. As an assembly option, special drivers may be installed to support RS422 and RS485 data rates up to 10 Mbaud. Depending on the application running and the number of interfaces used with high data rates, the 80 MHz option CPU option may be applicable.

- **CPU**

  Depending on the used CPU the PowerQUICC runs with a minimum frequency of 33 MHz (40 / 50 / 66 or 80 MHz are optionally available). Default: 50 MHz CPU assembled

1.1 Specification

Processor	PowerQUICC MPC860 based Embedded PowerPC Architecture
PMC-Module	Standard PCI Mezzanine Card Type 1
PCI to QBUS bridge	QSPAN
I/O	Micro SCSI connector
Main Memory	4 / 16 MByte EDO DRAM
Flash PROM	2 / 4 MByte Flash PROM. On board programmable.
Fast SRAM	(opt.) up to 512kByte fast SRAM
serial Interfaces	RS232: 115 KBaud RS422 and RS485: 500 KBaud, up to 10MBaud (opt.)
Firmware	PSOS BSP, VxWorks BSP (on request)
Power consumption	3.3V 0,5A 5.0V 0,6A
Environm. conditions Temperature (operating) Temperature (storage) Humidity	 0° C to +50 °C -40 °C to +85°C 5 % to 95 % non condensing
Standards compliance	PCI Rev. 2.1 P1386.1 / Draft 2.4a

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NPMC-860-SIO** during its usual lifetime take the following precautions before handling the board.

CAUTION

Malfunction or damage to the board or connected components

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the board read this installation section
- Before installing or uninstalling the **NPMC-860-SIO**, read the Installation Guide and the User's Manual of the **NPMC-860-SIO** carrier board
- Before installing or uninstalling the **NPMC-860-SIO** on a carrier board or both in a VME / cPCI rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPMC-860-SIO** is connected to the carrier board via all PMC connectors and that the power is available on both PMC connectors (GND, +5V, and +3,3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted to the front panel or VME / cPCI rack
  - and shielded by closed housing.

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NPMC-860-SIO**
- a power supply

2.2.2 Power Supply

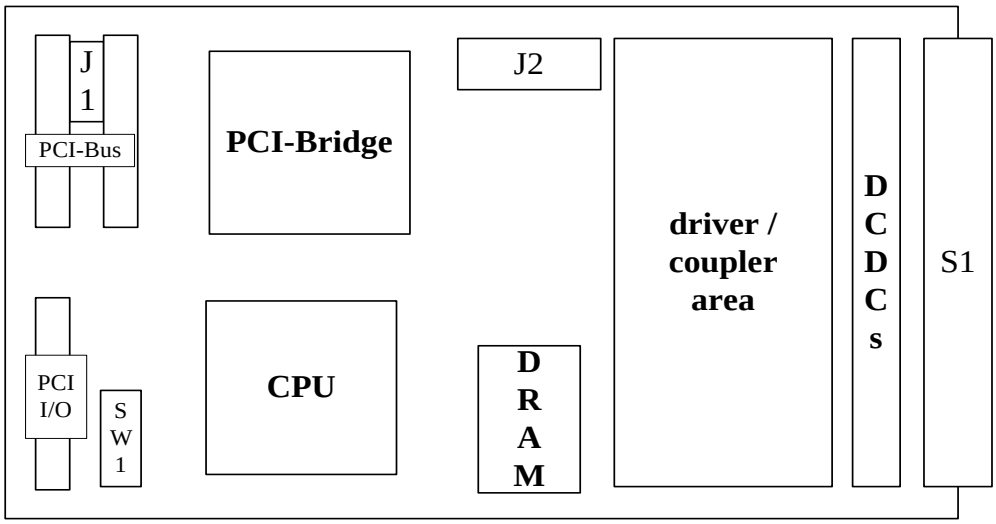
The power supply for the **NPMC-860-SIO** must meet the following specifications:

- +3,3V / 0,5 A typical
- +5,0V / 0,6 A typical

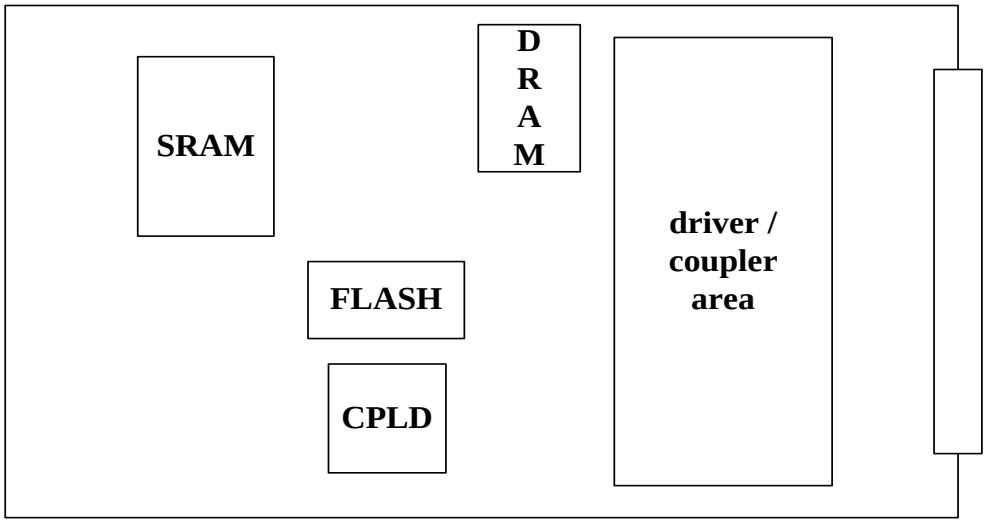
2.3 Location Overview

The figure 1 „Location Diagram of the **NPMC-860-SIO**" highlights the position of the important components. Depending on the board type it might be that your board does not include all components named in the location diagram.

Figure 3: Location Diagram of the **NPMC-860-SIO**



Top View



Bottom View

2.4 Automatic Power Up

In the following situations the **NPMC-860-SIO** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset

- when +5V voltage level drops below 4,4V *
- when +5V voltage level rises above 5,6V *
- when +3.3V voltage level drops below 2,65V *
- when +3.3V voltage level rises above 3,9V *
- or when the carrier board signals a PCI Reset

Watchdog timer

Per factory default the watchdog timer of the PowerQUICC is disabled. If the watchdog timer is enabled, it generates an non-maskable interrupt (NMI) followed by a reset when it is not retriggered by software (see the PowerQUICC users manual).

* PCI Specifications Revision 2.1, Section 4.2.1.1 and Section 4.3.2

2.5 Switch Settings

There is a 8-position DIP switch (SW1) on the **NPMC-860-SIO**, 7 bits of which can be used for customer configuration settings. Switch positions 1 – 7 are readable by software. Position 8 of the switch enables the BDM functionality, if set to “On” when the module is reset.

All options necessary for normal operation are pre-installed in the factory. By default, SW1.8 is set to “Off”.

3 Hardware Details

3.1 Memory Map

All addresses are set-up by programming the corresponding Chip-Select Decoder of the PowerQUICC. The given addresses represent only one possible configuration. This configuration is used by N.A.T. firmware.

Table 1: NPMC-860-SIO Memory Map

Device	CS Line	Default Address	Function	Notes
Flash-PPROM	CS0	$FF00 0000		2/4 MByte Flash-Prom (8 Bit wide)
DRAM	CS1	$0000 0000		4/16 MByte EDO DRAM (32 Bit wide)
Fast SRAM	CS2	$0180 0000		128/256k Fast SRAM (32 Bit wide)
QSPAN	CS3	$1000 0000	PCIbus access	window to the PCI bus (32 Bit wide) There are two PCI images available selected by the IMSEL-Signal. This signal is generated by the Port PB14. Alternately, it may be generated by Port PD15, if R4 (0Ω) is installed. In this case, PB14 has to be set to tristate. By default, R4 is not installed.
QSPAN	CS4	$0140 0000	QSPAN Registers	Qbus access to the QSPAN Registers (32 Bit wide)
I/O	CS5	$0100 0000	I/O	DIP switch (7 Bit wide, D24-30)
	CS6-7			not used

3.2 Interrupt Structure

The **NPMC-860-SIO** has the following Interrupt structure:

Table 2: NPMC-860-SIO Interrupt Mapping

Interrupt source	PowerQUICC Interrupt level
NC	IRQ-Level 0 (highest level)
NC	IRQ-Level 1
NC	IRQ-Level 2
QSPAN	IRQ-Level 3
NC	IRQ-Level 4
NC	IRQ-Level 5
NC	IRQ-Level 6
NC	IRQ-Level 7 (lower level)

3.3 PowerQUICC Port Pins Usage

Table 3: PowerQUICC Port Pin Usage (Port A)

Signal Function	PowerQUICC Port A Pin	Description
RxD_SCC1	PA15	RxD_SCC1
TxD_SCC1	PA14	TxD_SCC1
RxD_SCC2	PA13	RxD_SCC2
TxD_SCC2	PA12	TxD_SCC2
L1TxDB	PA11	TDM, only on P14
L1RxDB	PA10	TDM, only on P14
L1TxDA	PA9	TDM, only on P14
L1RxDA	PA8	TDM, only on P14
BRGO_SCC1	PA7	Clock Out SCC1
CLK2	PA6	Clock In SCC1
BRGO_SCC2	PA5	Clock Out SCC2
CLK4	PA4	Clock In SCC2
BRGO_SCC3	PA3	Clock Out SCC3
CLK6	PA2	Clock In SCC3
BRGO_SCC4	PA1	Clock Out SCC4
CLK8	PA0	Clock In SCC4

Table 4: PowerQUICC Port Pin Usage (Port B)

Signal Function	PowerQUICC Port B Pin	Description
/SPISEL	PB31	SPI, only on P14
SPICLK	PB30	SPI, only on P14
SPI_TxD	PB29	SPI, only on P14
SPI_RxD	PB28	SPI, only on P14
SDA	PB27	I^2C data
SCL	PB26	I^2C clock
TxD_SMC1	PB25	TxD SMC1
RxD_SMC1	PB24	RxD SMC1
DMAACK	PB23	DMA Ack QSpan
not used	PB22	
TxD_SMC2	PB21	TxD SMC2
RxD_SMC2	PB20	RxD SMC2
RTS_SCC1	PB19	RTS SCC1
RTS_SCC2	PB18	RTS SCC2
L1ST3	PB17	TDM, only on P14
L1ST4	PB16	TDM, only on P14
not used	PB15	
IMSEL	PB14	Image Select for QSpan

Table 5: PowerQUICC Port Pin Usage (Port C)

Signal Function	PowerQUICC Port C Pin	Description
DMAREQ	PC15	DMA Ack QSpan
not used	PC14	
not used	PC13	
not used	PC12	
CTS_SCC1	PC11	CTS SCC1
CD_SCC1	PC10	CD SCC1
CTS_SCC2	PC9	CTS SCC2
CD_SCC2	PC8	CD SCC2
CTS_SCC3	PC7	CTS SCC3
CD_SCC3	PC6	CD SCC3
CTS_SCC4	PC5	CTS SCC4
CD_SCC4	PC4	CD SCC4

Signals with asterisk (*) are described in detail below.

Table 6: PowerQUICC Port Pin Usage (Port D)

Signal Function	PowerQUICC Port D Pin	Description
L1TSYNCA/ IMSEL	PD15	TDM, only on P14, alternate Image Select for QSpan
L1RSYNCA	PD14	TDM, only on P14
L1TSYNCB	PD13	TDM, only on P14
L1RSYNCB	PD12	TDM, only on P14
RxD_SCC3	PD11	RxD SCC3
TxD_SCC3	PD10	TxD SCC3
RxD_SCC4	PD9	RxD SCC4
TxD_SCC4	PD8	TxD SCC4
RTS_SCC3	PD7	RTS SCC3
RTS_SCC4	PD6	RTS SCC4
not used	PD5	
not used	PD4	
not used	PD3	

4 Connectors

4.1 Development Port / BDM and JTAG Connector

Table 7: Development Port / BDM and JTAG Connector Pinout Options

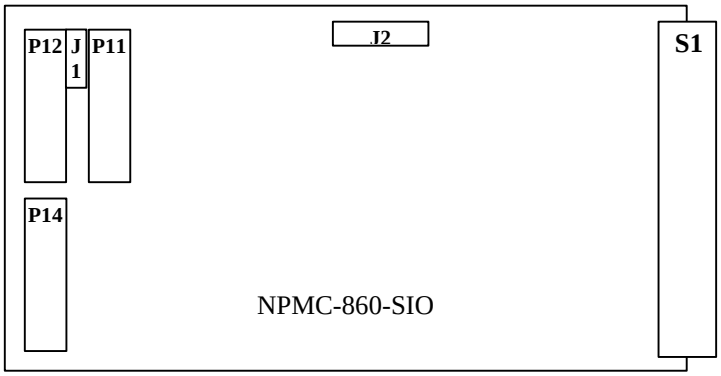
JTAG	Development Port	BDM Port	PIN					
VFLS0	VFLS0	VFLS0	1		2	/SRESET	/SRESET	/SRESET
GND	GND	GND	3		4	DSCK	DSCK	TCK
GND	GND	GND	5		6	VFLS1	VFLS1	VFLS1
/HRESET	/HRESET	/HRESET	7		8	DSDI	DSDI	TDI
+5V	+5V	+5V	9		10	DSDO	DSDO	TDO
--------	---------	---------	11		12	--------	--------	TMS

The location of the BDM port connector can be seen in figure 4 on the following page.

Position 8 of the DIP switch SW1 enables the Background Debug Mode (BDM) functionality, if set to “On” when the module is reset. If set to “Off”, the MPC860 boots normally from FLASH.

4.2 Connector Overview

Figure 4: Connectors of the **NPMC-860-SIO**



Please refer to the following table to look up the pin assignment of the NPMC-860-SIO.

4.3 PMC Connector P11

Table 8: **PMC Connector P11**

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
N.C.	1	TCK	-12V	2	N.C.
GND	3	GND	/INT A	4	/IRQ-QSPAN
N.C.	5	/INT B	/INT C	6	N.C.
N.C.	7	BUSMODE1	+5V	8	+5V
N.C.	9	/INT D	PCI_RSV1	10	N.C.
GND	11	GND	PCI_RSV2	12	N.C.
CLK	13	CLK	GND	14	N.C.
GND	15	GND	/GNT	16	/GNT
/REQ	17	/REQ	+5V	18	+5V
N.C.	19	V (I/O)	AD31	20	PCI_AD31
PCI_AD28	21	AD28	AD27	22	PCI_AD22
PCI_AD25	23	AD25	GND	24	GND
GND	25	GND	CBE3	26	/CBE3
PCI_AD22	27	AD22	AD21	28	PCI_AD21
PCI_AD19	29	AD19	+5V	30	+5V
N.C.	31	V (I/O)	AD17	32	PCI_AD17
/FRAME	33	/FRAME	GND	34	GND
GND	35	GND	/IRDY	36	/IRDY
/DEVSEL	37	/DEVSEL	+5V	38	+5V
GND	39	GND	/LOCK	40	N.C.
N.C.	41	/SDONE	/SB0	42	N.C.
PAR	43	PAR	GND	44	GND
N.C.	45	V (I/O)	AD15	46	PCI_AD15
PCI_AD12	47	AD12	AD11	48	PCI_AD11
PCI_AD09	49	AD09	+5V	50	+5V
GND	51	GND	/CBE0	52	/CBE0
PCI_AD06	53	AD06	AD05	54	PCI_AD05
PCI_AD04	55	AD04	GND	56	GND
N.C.	57	V (I/O)	AD03	58	PCI_AD03
PCI_AD02	59	AD02	AD01	60	PCI_AD01
PCI_AD00	61	AD00	+5V	62	+5V
GND	63	GND	/REQ64	64	N.C.

4.4 PMC Connector P12

Table 9: **PMC Connector P12**

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
N.C.	1	+12V	/TRST	2	N.C.
N.C.	3	TMS	TDO	4	N.C.
N.C.	5	TDI	GND	6	GND
GND	7	GND	PCI_RSV3	8	N.C.
N.C.	9	PCI_RSV	PCI_RSV4	10	N.C.
N.C.	11	BUSMODE 2	+3.3V	12	+3.3V
/RST	13	/RTS	BUSMODE 3	14	N.C.
+3.3V	15	+3.3V	BUSMODE 4	16	N.C.
N.C.	17	PCI_RSV	GND	18	GND
PCI_AD30	19	AD30	AD29	20	PCI_AD29
GND	21	GND	AD26	22	PCI_AD26
PCI_AD24	23	AD24	+3.3V	24	+3.3V
/IDSEL	25	IDSEL	AD23	26	PCI_AD23
+3.3V	27	+3.3V	AD20	28	PCI_AD20
PCI_AD18	29	AD18	GND	30	GND
PCI_AD16	31	AD16	/CBE2	32	/CBE2
GND	33	GND	PCI_RESVD	34	N.C.
/TRDY	35	/TRDY	+3.3V	36	+3.3V
GND	37	GND	/STOP	38	/STOP
/PERR	39	/PERR	GND	40	GND
+3.3V	41	+3.3V	/SERR	42	/SERR
/CBE1	43	/CBE1	GND	44	GND
PCI_AD14	45	AD14	AD13	46	PCI_AD13
GND	47	GND	AD10	48	PCI_AD10
PCI_AD08	49	AD08	+3.3V	50	+3.3V
PCI_AD07	51	AD07	PCI_RESV	52	N.C.
+3.3V	53	+3.3V	PCI_RESV	54	N.C.
N.C.	55	PCI_RESV	GND	56	GND
N.C.	57	PCI_RESV	PCI_RESV	58	N.C.
GND	59	GND	PCI_RESV	60	N.C.
N.C.	61	ACK64	+3.3V	62	+3.3V
GND	63	GND	PCI_RESV	64	N.C.

4.5 PMC Connector P14 (PMC I/O)

Table 10: PMC Connector P14

Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
RxD_SCC1	1	I/O	I/O	2	RxD_SCC2
TxD_SCC1	3	I/O	I/O	4	TxD_SCC2
CTS_SCC1	5	I/O	I/O	6	CTS_SCC2
RTS_SCC1	7	I/O	I/O	8	RTS_SCC2
CD_SCC1	9	I/O	I/O	10	CD_SCC2
BRGO_SCC1	11	I/O	I/O	12	BRGO_SCC2
CLK2	13	I/O	I/O	14	CLK4
L1TSYNCA	15	I/O	I/O	16	L1TSYNCB
L1RSYNCA	17	I/O	I/O	18	L1RSYNCB
L1ST3	19	I/O	I/O	20	L1ST4
L1RxDA	21	I/O	I/O	22	L1RxDB
L1TxDA	23	I/O	I/O	24	L1TxDB
nc	25	I/O	I/O	26	nc
RxD_SCC3	27	I/O	I/O	28	RxD_SCC4
TxD_SCC3	29	I/O	I/O	30	TxD_SCC4
CTS_SCC3	31	I/O	I/O	32	CTS_SCC4
RTS_SCC3	33	I/O	I/O	34	RTS_SCC4
CD_SCC3	35	I/O	I/O	36	CD_SCC4
BRGO_SCC3	37	I/O	I/O	38	BRGO_SCC4
CLK6	39	I/O	I/O	40	CLK8
nc	41	I/O	I/O	42	nc
nc	43	I/O	I/O	44	nc
nc	45	I/O	I/O	46	nc
nc	47	I/O	I/O	48	nc
nc	49	I/O	I/O	50	nc
nc	51	I/O	I/O	52	SDA_I2C
nc	53	I/O	I/O	54	SCL_I2C
RxD_SMC1	55	I/O	I/O	56	nc
TxD_SMC1	57	I/O	I/O	58	RxD_SPI
nc	59	I/O	I/O	60	TxD_SPI
RxD_SMC2	61	I/O	I/O	62	SPICLK
TxD_SMC2	63	I/O	I/O	64	SPISEL

4.6 The Front Panel Connector (S1)

The front panel connector is a micro SCSI-II connector (68 pins). The serial interfaces (RS232, RS422, RS485) are available on the pins of the front panel connector.
The pin assignment shows all possible configurations.
If optical isolation is not required, the GNDEXTx signals are connected to internal GND. SMC ports are always RS232, no optical isolation.

Table 11: General Pin Assignment of the Front-panel Connector

Pin	RS232	RS422	RS485	Pin	RS232	RS422	RS485
1	GNDEXT1	GNDEXT1	GNDEXT1	35	RTS3	RTS3-	
2	GNDEXT1	GNDEXT1	GNDEXT1	36		RTS3+	
3	RxD1	RxD1-	R/T1-	37	CTS3	CTS3-	
4		RxD1+	R/T1+	38		CTS3+	
5	TxD1	TxD1-		39		RxC3-	
6		TxD1+		40		RxC3+	
7	RTS1	RTS1-		41		TxC3-	
8		RTS1+		42		TxC3+	
9	CTS1	CTS1-		43	GNDEXT4	GNDEXT4	GNDEXT4
10		CTS1+		44	GNDEXT4	GNDEXT4	GNDEXT4
11		RxC1-		45	RxD4	RxD4-	R/T4-
12		RxC1+		46		RxD4+	R/T4+
13		TxC1-		47	TxD4	TxD4-	
14		TxC1+		48		TxD4+	
15	GNDEXT2	GNDEXT2	GNDEXT2	49	RTS4	RTS4-	
16	GNDEXT2	GNDEXT2	GNDEXT2	50		RTS4+	
17	RxD2	RxD2-	R/T2-	51	CTS4	CTS4-	
18		RxD2+	R/T2+	52		CTS4+	
19	TxD2	TxD2-		53		RxC4-	
20		TxD2+		54		RxC4+	
21	RTS2	RTS2-		55		TxC4-	
22		RTS2+		56		TxC4+	
23	CTS2	CTS2-		57	nc	nc	nc
24		CTS2+		58	nc	nc	nc
25		RxC2-		59	nc	nc	nc
26		RxC2+		60	nc	nc	nc
27		TxC2-		61	nc	nc	nc
28		TxC2+		62	nc	nc	nc
29	GNDEXT3	GNDEXT3	GNDEXT3	63	RxD_SMC1	RxD_SMC1	RxD_SMC1
30	GNDEXT3	GNDEXT3	GNDEXT3	64	TxD_SMC1	TxD_SMC1	TxD_SMC1
31	RxD3	RxD3-	R/T3-	65	RxD_SMC2	RxD_SMC2	RxD_SMC2
32		RxD3+	R/T3+	66	TxD_SMC2	TxD_SMC2	TxD_SMC2
33	TxD3	TxD3-		67	GND	GND	GND
34		TxD3+		68	GND	GND	GND

5 Programmer's Reference

5.1 QSPAN

5.1.1 Host Setup of the QSpan PCI Bridge

In order to configure the **NPMC-860-SIO** to work on the PCI-bus, the following steps must be taken:

1. Look up the address of the PCI-bus controller of the **NPMC-860-SIO** in the ***Configuration Space*** of the PCI-bus of the carrier board (please refer to the manual for the carrier board).
The PCI-bus controller of the **NPMC-860-SIO** occupies 256 Bytes in the ***Configuration Space*** and you should see the following address map (first 64 bytes according to PCI specification 2.1):

Table 12: NPMC-860-SIO Memory Map in the Configuration Space

Offset	QSpan register	Description of register
0x0000	PCI_ID	ID, start address configuration space
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
...	...	...
0x003c	PCI_MISC1	miscellaneous 1

For more details regarding the QSpan registers of the **NPMC-860-SIO**, please refer to the QSpan manual's register map (Table A.1, App. A-2).

2. Now write - to the offset address 0x0010 (QSpan register PCI_BSM, 32 bit) - the start address of the **NPMC-860-SIO** where it should appear in the ***memory space*** of the carrier board's PCI-bus. Please note, that all PCI register accesses have to be done in little endian format.
The register image of the QSpan should now be visible in the PCI memory space.

Table 13: NPMC-860-SIO Memory Map in the PCI Memory Space

Offset	QSpan register	Description of register
0x0000	PCI_ID	ID, start address QSpan register
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	Class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
0x0014	-	QSpan unimplemented
...	...	...
0x003c	PCI_MISC1	miscellaneous 1
...	...	...
0x800	MISC_CTL	miscellaneous control
0x804	EEPROM_CS	EEPROM control
...	...	...
0x0ffc	-	QSpan reserved

3. Initialize the register PBTI0_CTL for target image 0 and set the necessary parameters: The longword read/write access must be enabled by writing the PBTI0_CTL at offset 0x0100 (image enable, block size BS[3:0] = 0110 = 4 MB, or BS[3:0] = 1000 = 16 MB, Q-bus destination port size DSIZE[1:0] = 00 = 32 bit).

4. Set address translation decoding on register PBTI0_ADD at offset 0x0104 (host system dependent):
Write the start address where the memory of the NPMC-860-SIO module should appear in the ***Memory Space*** of the PCI bus.

5. Make certain that there are no address conflicts in your systems (set/check the amount of the memory occupied by the **NPMC-860-SIO** in the PCI memory space).

5.1.2 Q-Bus Configuration

Through the MISC_CTL register parameters for configurating the local bus (Q-Bus) are set. The settings to be performed are system dependant. But, the following aspect has to be taken into account in any case:

Setting of bit 0 (SW-RST) will cause a RESET on the Q-Bus, if the Q-BUS HRESET signal is connected to the RESETO pin of the QSPAN (like for this module). The RESETO signal follows the programming of the SW-RST bit directly, i.e. without any delay in time. Therefore, if the MPC860 is to be reset by this means, the minimum time period necessary to perform an orderly hardware reset of the MPC860 has to be strictly obeyed. Otherwise the MPC860 may enter an undefined state. A time period of 100ms is recommended between the setting and resetting of this bit. In time-critical applications this period may be reduced. Any value longer than 1ms should be suuficient. 100ms is a period of time which is suitable and safe for resetting the Q-Bus in all cases and for all CPU operating frequencies.

5.1.3 EEPROM Configuration

By means of register EEPROM_CS the Configuration-EEPROM may be read and reprogrammed, which the QSPAN uses for Power-Up – initialialisation. Please be aware of the fact that programming the EEPROM with unsuitable values may cause the PCI-Bus to hang completely.

NOTE: For more information, please refer to the QSpan manual. Please make certain that you use the correct endian format when writing into the QSpan registers.

5.2 On-board Firmware

5.2.1 Boot Software

After a power-up or reset, the on-board firmware starts automatically with the basic memory and I/O tests.

5.2.1 The Board Support Packages

If the NPMC-860-SIO is delivered with a vxWorks BSP, please refer to the vxWorks BSP Readme file for the implementation details of this BSP.

5.2.2 No on-board Operating System, nor Application Software

If the NPMC-860-SIO is delivered without operating system or protocol software, please take the following steps:

- Refer to the MPC860 manual for information on how to generate your boot code
- Configure the local memory map (see Figure 7), the interrupt registers of the MPC860, ...
- Load your boot code into the FlashPROM of the NPMC-860-SIO while the MPC860 is in RESET-mode, and start the code.

Appendix A PowerQUICC CPU

Introduction

The MPC860 PowerPC™ Quad Integrated Communications Controller (PowerQUICC) is a versatile one-chip integrated microprocessor and peripheral controller combination that can be used in a variety of applications. It particularly excels in both communications and networking systems.

The MPC860 is a PowerPC-based derivative of Motorola's MC68360 (Quad Integrated Communications Controller(QUICC™). The CPU on the MPC860 is a 32-bit PowerPC implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) of the MC68360 QUICC has been enhanced with the addition of the interprocessor-integrated-controller (I^2C) channel. Moderate to high digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high performance memories and newer dynamic random access memories (DRAMs). Overall systems functionality is completed with the addition of a PCMCIA socket controller supporting up to two sockets and a real time clock.

For further information please consult the MPC860 User's Manual supplied by Motorola.

Appendix B QSpan™ Bus Bridge

Introduction

The QSpan™ chip is a member of Tundra Semiconductor Corporation's family of PCI bus-bridging devices. The QSpan™ is designed to gluelessly bridge the QUICC™ (MC68360), the PowerQUICC™ as well as the MPC801 embedded controllers to PCI.

Features

The QSpan™ has the following features:

- A direct connect interface to the PCI bus for Motorola's QUICC (MC68360), PowerQUICC(MPC860), M68040, the PMC821 and the MPC861 embedded controllers;
- 32-bit PCI interface compliant with PCI Revision 2.1;
- Decoupled transfer technology: three 16-entry deep FIFOs buffer multiple transaction in both directions, allowing zero wait state bursting on the PCI and Motorola buses;
- IDMA peripheral support for QUICC and PowerQUICC;
- Flexible address space mapping and translation between the PCI and Motorola buses;
- Programmable endian byte ordering;
- Two user-programmable slave images available for PCI access to the Motorola buses;
- QSpan™ control and status registers accessible from both PCI and Motorola buses;
- PCI bus and Motorola buses can be operated at different clock frequencies;

Appendix C RAM/ROM

DRAM

The **NPMC-860-SIO** provides an on-board DRAM (EDO-DRAM). This memory is accessible from the PowerQUICC or the QSPAN PCI-bridge chip. The memory controller of the PowerQUICC is responsible for controlling the DRAM. This flexible memory controller allows the implementation of memory systems with very specific timing requirements.

The user is allowed to define different timing patters for the control signals that govern a memory device. This patterns define how the external control signals behave in a read-access request, write-access request, burst read-access request, or burst write-access request. The user defines how the external control signals toggle when the periodic timers reach the maximum programmed value for refresh operation.

The memory capacity is 4 MByte (optionally 16 MByte), the memory is 32 bit wide. The access time of the EDO DRAM is 60 nsec for new accesses, the access time within a row is 30 nsec (bursting)

For different operating frequency of the MPC860 the user need to define different timing patters.

The User Programmable Machine A (UPM A) controls the PowerQUICC and the PCI accesses to the DRAM memory.

In the PowerQUICC Reset-state accesses to the DRAM will be inhibited.

Parity generation and check will not supported by the module

SRAM

The **NPMC-860-SIO** provides optionally an on board high speed SRAM. This memory is accessible from the PowerQUICC or the QSPAN PCI-bridge chip. The memory controller of the PowerQUICC is responsible for controlling the SRAM. This flexible memory controller allows the implementation of memory systems with very specific timing requirements

The memory capacity is 128 kByte (optionally 256 kByte), the memory is 32 bit wide. The access time of the SRAM is 10 nsec for every access type.

There is no restriction on accessing the SRAM.

Boot Flash

The flash memory area is located on the PowerQUICC bus so that the reset vector table in the boot flash is visible to the CPU after power on reset. The boot flash memory has a size of 2 MByte (optionally 4 Mbyte) and can directly be accessed by the CPU. The flash memory area is 8-bit wide organised.

The flash memory is a 5V only device. For programming the Flash is no extra programming voltage necessary.
Programming the flash memory is possible in two ways:
- Programming the entire flash memory from the PCI-bus. The module must be in the RESET-State.
- Programming the flash memory in the run state of the PowerQUICC.

Appendix D Documentation reference

PCI Interface chip

Company: TUNDRA
Title: QSPAN (CA91CC860)
PCI to Motorola Processor Bridge Manual

MPC860 PowerQUICC

Company: Motorola Inc.
Title: MPC860 PowerQUICC
User's Manual

PCI Specification

Company: PCI Special Interest Group
Title: Peripherial Component Interconnect (PCI)
Interface Data Book
Revision 2.1

Appendix E Document's History

Revision	Date	Description	Name
0.9	1998	initial revision	ga
1.0	01.03.1999	Layout adaptation	mz
1.1	22.07.1999	Layout improvement	as
	02.11.2000	- improved Diagram espec. concering optical Isolation - Pin Assignment of connector S1 corrected (pin65-66)	mz
1.2	22.03.2001	Memory layout map corrected (description of IMSEL). Also minor changes in signal names.	ga
1.3	30.10.2001	minor amendments in various chapters	ga
1.4	22.11.2001	Programmer's Reference added, some corrections concerning address map and interrupts	ga
1.5	24.01.2002	Chapter 2.4 adapted to NW Rev. 1.0	ga
1.6	25.08.2003	Chapters 3ff new organized, port pin description added, figure 4 corrected	ga
1.7	25.10.2005	Figure 1 updated, serial transfer rate info added	ga