VersaMax Nano PLC and Micro PLC CPUs

October 4, 2004 GFK-2068D

Important Product Information

This document contains important information about the following VersaMax Nano PLC and Micro PLC models:

IC200NAL110-BC	IC200UAR014-BE	IC200UDR010-BE
IC200NAL211-BC	IC200UAR028-BE	IC200UEX209-B
IC200NDD010-CE	IC200UDD104-BE	IC200UEX210- B
IC200NDD101-CE	IC200UDD110-BE	IC200UEX211- B
IC200NDR001-CE	IC200UDD112-BE	IC200UEX212- B
IC200NDR010-CE	IC200UDD120-BE	IC200UEX213- B
IC200UAA003-BE	IC200UDD212-BE	IC200UEX214- B
IC200UAA007-BE	IC200UDR001-BE	IC200UEX215- B
IC200UAL004-BE	IC200UDR002-BE	IC200UEX222- B
IC200UAL005-BE	IC200UDR003-BE	IC200UEX616- B
IC200UAL006-CF	IC200UDR005-BE	IC200UEX626- B
	IC200UDR006-BE	IC200UEX636- B

The suffix letters following CPU part numbers indicate the hardware version followed by the firmware version. Expansion units do not have firmware, so only the hardware version is indicated.

Downloadable Firmware Upgrade Kits

44A752236-G02	R2.02 for all 14pt Micro CPUs
44A752237-G02	R2.02 for all 23/28pt Micro CPUs except IC200UDD120
44A752238-G02	R2.02 for 28pt Micro CPU with ESCP, IC200UDD120
44A752239-G02	R2.02 for all Nano CPUs except IC200NAL110/211
44A752240-G02	R2.02 for Analog Nano CPUs IC200NAL110/211

Electronic Documentation Available

All VersaMax Nano/Micro PLC user documentation, specifications and CAD drawings are available for download from the GE Fanuc website, http://www.gefanuc.com/support. Printed user manuals are available as part number GFK-1645C.

New Features

1. An optional filter for the Derivative Term has been added. This filter improves PID control loop stability by limiting the contributions of random variations and step input changes in the Set Point and Process Variable inputs. See *the VersaMax Micro PLC User's Manual*, GFK-1645Dfor details
2. Port 2 now supports Modbus RTU. Please see GFK-2220, *Modbus RTU Master Communications* for information about Modbus RTU. Installing RTU Master requires a port setup COMMREQ c from the application program to SYSID 0, TASK 20.

Fixed for this Version

1. A type B-type counter configured for single shot operation now changes its outputs correctly after hitting a high or low limit.
2. When the High-speed Counter (HSC) is configured for A quad B in continuous mode and is counting down, it now wraps to the high limit when reaching the low limit after a COMREQ loads the accumulator.
3. The Nano/Micro PLC now correctly rejects an RTU query that is more than 265 bytes in length.
4. When a channel on the HSC is configured with a high limit less than 32767 and the application uses a COMMREQ to change the count direction, the value in the count register is not forced to the maximum or minimum when the direction changes.
5. An optional filter for the Derivative Term has been added that improves PID control loop stability by limiting the contributions of random variations and step input changes in the Set Point and Process Variable inputs. Details are on the next page.
6. Changing the Integral Rate (Ki) parameter value of a PID function block from 2 to 1 (that is, from 0.002 to 0.001 Repeats/Sec.) or from 1 to 2 will not cause a step change to the Integral Term and the Control Variable.

   Changing the Integral Rate parameter value from 1 to 0 or from 0 to 1 causes a step change in both the Integral Term and the Control Variable. This result is expected. An Integral Rate value of zero specifies that the Integral Term contribution to the Control Variable is zero, while a non-zero value specifies a non-zero contribution.

Operating Notes/Restrictions

Password Protection:

In prior versions of VersaPro software, password protection for Micro and Nano CPUs was *Disabled* by default. With VersaPro 2.03, the default has been changed to *Enabled*. Attempting to download a new hardware configuration with password enabled (the new default) to a PLC whose current configuration is set for password disabled (the previous default) will result in a password configuration mismatch error. To avoid this situation, either change the new configuration to passwords disabled, or short the PLC's super-capacitor to clear the PLC's memory, and then download the new configuration.

Addition of Modules versus Extra Modules:

If an Expansion Unit that is part of the system configuration is powered up after the CPU, an "addition of module" fault is logged in the I/O Fault Table. Unless a fault exists, the fault table shows the module's reference address. The module is included in the I/O scan.

If an Expansion Unit that is NOT part of the system configuration is powered up after the CPU, an "extra module" fault is logged in the I/O Fault Table. The module has no reference address and its I/O is not scanned.

Expansion Units must be properly configured and properly connected. Make sure no Analog Expansion Unit error exists.

Analog Expansion Units:

- When an Analog Expansion Unit (IC200UEX616, IC200UEX626, IC200UEX636) fails, it drives a signal low, which in turn causes the loss of all other Analog Expansion Units in the system. Discrete expansion units cabled after the first analog expansion unit will also be lost. Such a failure can also subsequently affect the operation of any discrete expansion units, should any of them later be powered down. Consult the user's manual, GFK-1645C, for detailed troubleshooting instructions to be used in isolating expansion unit failures.
- For a Discrete Expansion Unit, the PWR LED is on ONLY when that expansion unit is powered up.

For all expansion units other than analog expansion (IC200UEX616, IC200UEX626, IC200UEX636). the PWR LED is also on if any other expansion unit or the CPU, to which it is connected is powered up. In addition, the PWR LED on an Analog Expansion Unit remains on (lit dimly) when the unit is powered down separately from the CPU. This is due to current leakage in the expansion cable.DIP Switch SW6 on an analog expansion unit controls the maximum value for the unit's analog inputs and analog outputs as follows:

SW6: OFF $\Rightarrow$ 4096 (32767 counts = 10V)

ON $\Rightarrow$ 4000 (32000 counts = 10V, 32767 counts = 10.23V)

By default, DIP Switch SW6 should be set in the OFF position (32726 counts = 10V).

Hardware configuration settings to default:

When VersaPro 2.03 is used to open a hardware configuration for a Nano/Micro PLC system that was constructed with an earlier

VersaPro version, it prompts to convert the files into a new format. During this process, any high speed counter parameters may be replaced with the original default settings. Verify all the CPU configuration settings following the folder upgrade.

VersaPro errors:

- When opening multiple monitoring windows in VersaPro while connected to a Micro or Nano CPU, one of the following error messages may be infrequently observed: "0x010D : Lost communication with COM server", or: "Too many windows open." If this happens, close the error window; exit the VersaPro application, and then reopen VersaPro to resume monitoring.
- On rare occasions Versapro may display the error message: "This action cannot be completed because the other program is busy. Choose 'Switch To' to activate the busy program & correct the problem." If this message appears, the VersaPro application becomes unstable and a shutdown of the application is required using the task manager. After this is completed, reopen VersaPro to resume operation.

Serial Communications:

- RTU communications: RTU communications on port 2 are not reliable with scan times above 140 milliseconds.
- For a Micro PLC Serial Port 2 SNP master using modems for communications, using an Attach requesting piggyback status returns zeros instead of the status information.

  Recommendation: the same piggyback status can be obtained by using the PLC Short Status command.
- For a Micro PLC Serial Port 2 SNP master, a communications request occasionally returns error code 0E05 when it should return 0E06.
- For a Micro PLC Serial Port 2 SNP Master, a communications request occasionally returns error code 070C when it should return 0C08.

High-speed Counter:

- Input references %I489 - %I493 are overwritten by the HSC function, and are not available to the application program.

  Recommendation: Avoid using references %I489 - %I493 (which are located immediately before the rest of the HSC input references) in the application program.
- When sending data commands to the High-speed Counter using the COMMREQ function, the CPU ignores the data type and start location parameters. These parameters specify where the command and data words are located in CPU memory. The CPU expects these three parameters to be located immediately after the command block.

  Recommendation: Be sure the command word and data words are located contiguously in memory, with the rest of the COMMREQ command block. They should immediately follow the "Start Location of Command Word" in the COMMREQ command block.
- If HSC Enable is On while in Stop mode and the High-speed Counter is configured for its output to be Off when placed in Run mode, the output will momentarily turn on when the PLC state changes from Stop to Run.

  Recommendations:

  1. Avoid setting the HSC/PWM/PT Output Enable bits to 1 (outputs enabled) during a Stop to Run transition. Be sure no programmer, HMI, or other device enables these bits while the PLC is in either Stop/No I/O mode or Stop/ I/O Scan mode.
  2. Never set the HSC/PWM/PT Output Enable bits to 1 using stored reference table values. These bits should always be enabled from the application program. programmer, HMI, or other source.
  3. The application program should always set the HSC/PWN/PT Output Enable bits to 0 (disable outputs) on the last scan of the PLC. The last scan can be detected using the LST_SCN system status reference, %S0002. See the User Manual for additional information about system status references.

PID Filter for the Derivative Term

In the Micro PLC User's Manual, GFK-1645C, Chapter 19, "The PID Function", the table in the Parameter Block for the PID Function section should be modified as shown below:

For Address +12, the **Config Word**, the **Low Biit Units** are changed to "Low 6 Bits used.

Description: The low 6 bits of this word are used to modify six default PID settings. The 10 high-order bits should be set to 0.

Set the low bit (bit 0) to 1 to modify the standard PID Error Term from the normal (SP – PV) to (PV – SP), reversing the sign of the feedback term. This is for Reverse Acting controls where the CV must go down when the PV goes up.

Set the second bit (bit 1) to 1 to invert the Output Polarity so that CV is the negative of the PID output rather than the normal positive value.

Set the third bit (bit 2) to 1 to modify the Derivative Action from using the normal change in the Error term to the change in the PV feedback term.

Set the fourth bit (bit 3) to activate deadband processing.

Set the fifth bit (bit 4) to activate anti-reset-windup action.

Set the sixth bit (bit 5) to activate derivative filtering.

Bit 0: Error Term +/-	When bit 0 is 0, Error Term = SP - PV. When bit 0 is 1, Error Term = PV - SP.
Bit 1: Output Polarity	When bit 1 is 0, the CV output represents the output of the PID calculation. When bit 1 is set to 1, the CV output represents the negative of output of the PID calculation.
Bit 2: Derivative action on PV	When bit 2 is 0, the derivative action is applied to the error term. When bit 2 is 1, the derivative action is applied to PV.
Bit 3: Deadband action	When bit 3 is 0, no deadband action occurs. If the error is within the deadband limits, then the error term is set to zero. Otherwise the error term is not affected by the deadband limits. If bit 3 is 1, deadband action occurs. If the error term is within the deadband limits, then the error is forced to zero. If, however, the error term is outside the deadband limits, then the error term is reduced by the deadband limit: Error Term = Error Term - deadband limit. A similar adjustment occurs when the error term is less than the lower deadband limit.
Bit 4: Anti-reset-windup action	When bit 4 is 0, the anti-reset- windup action uses a reset back-calculation. When the output is clamped, this replaces the accumulated Y remainder value with whatever value is necessary to produce the clamped output exactly. When bit 4 is 1, the accumulated Y term is replaced by the value of the Y term at the start of the calculation. In this way, the pre-clamp Y value is held as long as the output is clamped.
Bit 5: Derivative Term filter	When bit 5 is 0, no derivative term filtering occurs. When bit 5 is 1, the rate of change of the Derivative Term is limited. This improves PID loop stability by reducing the effects of random variations (noise) and step changes in the Set Point and Process Variable inputs.
Bit 0 – Bit 5:	Remember that the bits are set in powers of 2. To set bit 0, add 1 to the Config Word parameter value. To set bit 1, add 2. To set bit 2, add 4. To set bit 3, add 8. To set bit 4, add 16. To set bit 5, add 32. For example, set Config Word to 0 for default PID configuration. Add 1 to change the Error Term from SP - PV to PV - SP, add 2 to change the Output Polarity from CV = PID Output to CV = – PID Output, or add 4 to change Derivative Action from Error rate of change to PV rate of change, etc.