VR Series Catalog 2000

64-bit MIPS Processors

NEC

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February 2000

Dear NEC VR Series™ Customer:

Welcome to the February 2000 edition of the VR Series Development Tools Catalog. In this issue, we have included 18 new tools vendors and 62 products. NEC Electronics is continuing to make sure that you are provided with a broad and highly efficient tools environment. Our alliance with many of the most popular vendors has assured you of multiple options for compilers, real-time operating systems, reference boards, and software support, among others.

We know today that time-to-market pressures and “getting it right—the first time” can mean the difference in marketing a competitive product to specification and within ever-shrinking market windows. Our approach is to provide comprehensive solutions: a full range of feature-rich processors, companion chipsets, vertical market expertise, and a seamless development environment to aid your design programs.

Please review the leading-edge tools described in the following sections. Our tools partners have worked hard to anticipate your needs, not just for today but for well into the future. From the low-power VR41xx™ to the mid-range VR43xx™ to the high-end VR5432™, NEC’s VR Series offers a wide selection of 64-bit processors today.

We would appreciate your suggestions as to how we may continue to improve our service to you and that of our tools partners.

Sincerely,

NEC Electronics Europe GmbH
Marketing Europe

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VR-Series Microprocessors

Be Smart!

64-bit VR MIPS RISC Microprocessor Family

Product families with a name you can trust; that's how we like to present our microprocessors.

NEC's wide product range, from the low power VR41xx to the mid-range VR43xx family, up to the high end VR5xxx series supported by a highly efficient tools environment by well known companies like Green Hills Software, Microsoft and Wind River Systems, represent a strong alliance to provide a comprehensive solution for your application.

The following pages will give you a brief introduction of NEC's processors so that you can easily identify the right product for your application. More detailed description of all microprocessors, companion chips, tools and reference boards you will find hereafter.

The VR41xx concept

Applications

- Smart phones
- Car computing
- Industrial terminals
- General embedded equipment

Features

- VR4120 CPU core with MIPS I, II, III and MIPS 16 instruction set
- On chip peripheral functions ideal for handheld terminals
- Low Power consumption
- High speed processing by advanced process rule
- VxWorks & Windows CE support

VR43xx

Applications

- High end PC peripherals such as printers and scanner
- 3D graphic consoles for infotainment and games
- Powerful digital STBs
- Node computers in networks, LAN/WAN bridges, protocol converters

Features

- Excellent price/performance ratio
- Wide performance range
- Floating point and multiplier, MAC instruction
- MIPS 16 compressed instruction set
- VxWorks & Windows CE support

VR5xxx

Applications

- High-end embedded equipment
- Networking for multi-protocol routers
- 3D graphic units

Features

- High-speed system clock with support for slow system bus and PCI
- Superscalar architecture
- Large on-chip primary cache
- Integrated controller for secondary cache
- Enhanced floating point unit
- Enhanced system bus with over 400 Mbytes/s throughput

NEC's VR43xx and VR5xxx Family - Offering Wide Performance
If your application is more concerned with CPU performance than power consumption you should take a look at two of our product families that meet your performance requirement while staying within your budget: VR43xx and VR5xxx.

Excellent price/performance ratio
For highly cost-sensitive but high performance-embedded applications, we recommend our VR43xx family. Various speed versions and internal cache memory sizes guarantee seamless transition within the family. NEC's VR43xx microprocessors offer one of the best performance/die size solutions including Windows CE and VxWorks support.

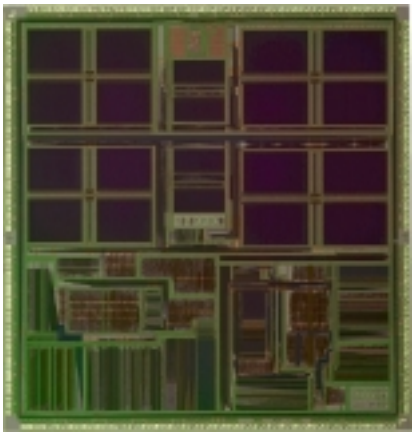
Enhanced floating point unit
Next in line behind the VR43xx family is the VR5xxx core which offers even greater performance with superscalar architecture. Beside an expanded MIPS IV instruction set it offers outstanding floating point field. A generously dimensioned primary cache (32 Kbytes instruction and data cache) and a controller for secondary cache are already integrated in this still affordable solution. The VR5000 processor offering a performance of 352 Dhrystone MIPS at 250 MHz has been a well accepted CPU for mid range to high end workstations but is also targeting applications like networking devices, office automation and computer peripherals.

High end solution
A new level of high end performance has been achieved by NEC's VR5432 processor by supporting a dual-issue superscalar pipeline and MIPS IV instruction set. If you are looking for the right product for high end office automation, network, multimedia or industrial control applications, the VR5432 is the right product for you!

Support chips and tools
Companion chips are available for all processors. Here, the interface with memory and PCI bus comes with a number of fully integrated peripheral functions. Together, Processor and Companion chip deliver a fully functional system.
Finally, to make things easier, existing development boards eliminates the need to develop prototypes for testing.

VR5000 - Evolution

VR5000-200 MHz



9.1 x 9.8 mm
0.35 µm 9 W@200 MHz

VR5000 250 MHz V 4.0

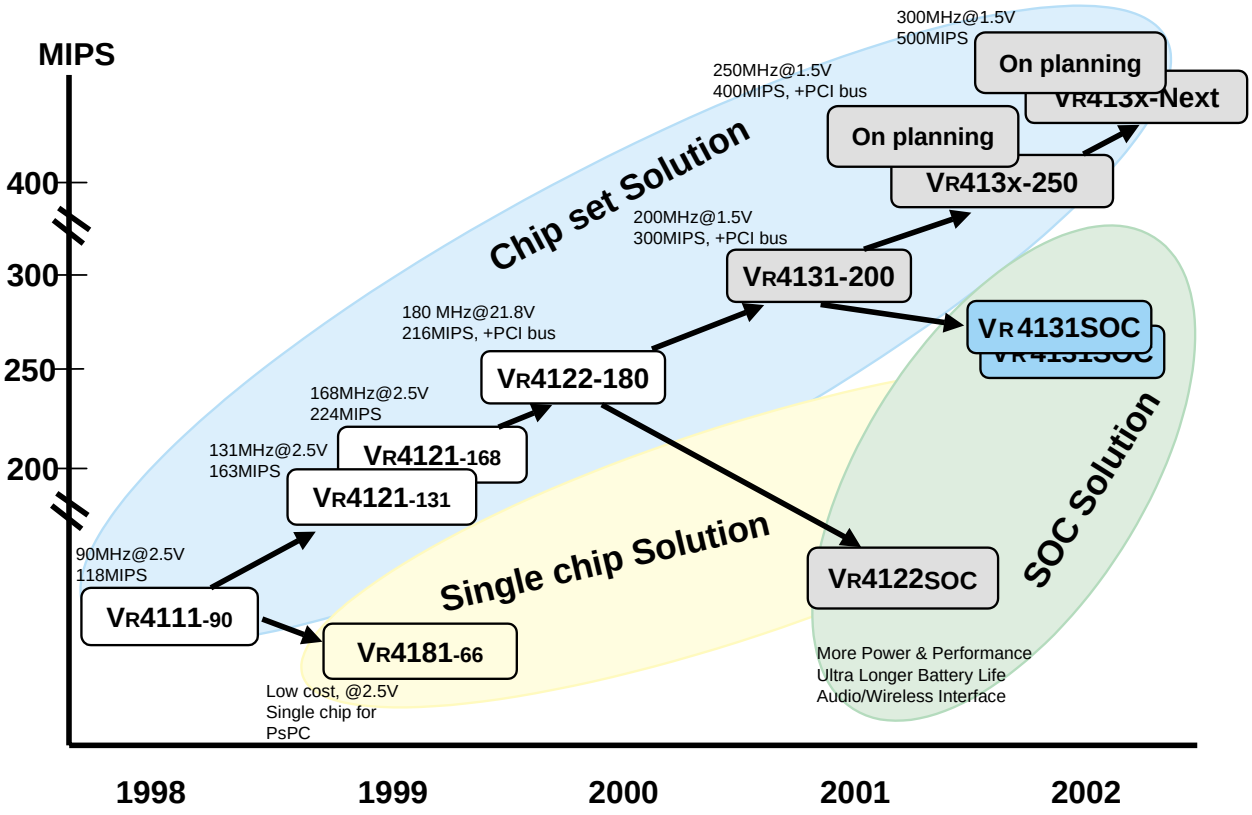
8.4 x 8.4 mm
0.25 µm 5.0 W@250 MHz

VR5000B-300 MHz

5.5 x 5.5 mm
0.15 µm 3.5 W@300 MHz

NEC's VR41xx Family - A Smart Solution

VR41xx Series™ MIPS® RISC Microprocessor Roadmap



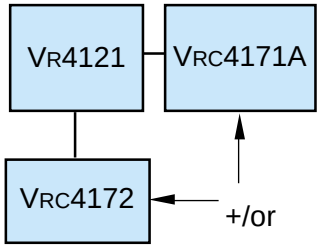
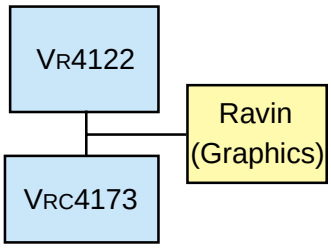
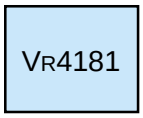
On-chip peripheral functions
Handheld products and stationary applications such as PDAs, smart or web phones, mobile multimedia, car computing and industrial terminals require high performance based on a very low power consumption. NEC's VR41xx 64-bit RISC processor family is a highly integrated solution for your application running major Operating Systems such as Windows CE or VxWorks.

Low cost system
The VR4121 microprocessor offers high speed and compact size (224-pin FPBGA / 16 mm x 16 mm) in 0.25 µm technology. With a performance up to 224 Mips at 168 MHz it is the right low-cost system on chip solution for you.

High integration
NEC's VR4122 is based on 0.18 µm technology and supports a 1.8 V core voltage. With a performance of 216 Mips at 180 MHz and an integrated PCI bus it is highly attractive for general embedded space. For automotive or demanding industrial applications we support a temperature range of –40°C to 85°C.

Single chip solution
Another system on a chip is the 64-bit VR4181 microprocessor. High speed, low power consumption and low cost are the key characteristics of our device, targeting low cost consumer devices like PDAs, Smart or web phones, GPS receivers or industrial handheld devices. Offering key features such as display controller, SDRAM interface and touch-panel interface controller this device offers you an excel-lent performance a small footprint and the lowest system cost.

VR41xx Series CPU List

	VR4121	VR4122	VR4181
Chip Set			
Performance	131/168 MHz	180 MHz 167 MHz (Superscalar) 129 MHz (-40˚C to + 85˚C)	66 MHz
CPU	VR4120 core, 16 KB / 8 KB	VR4120 core, 32 KB / 16 KB	VR4110 core, 8 KB / 4 KB
Additional Peripherals	Keyboard controller, Softmodem I/F	Additional SIU	LCD cntr, USB (client), Compact Flash I/F
A/D, D/A	10-bit, 10-bit	No	12-bit, 10-bit
Package	224-pin FPBGA	224-pin FPBGA	160-pin LQFP
Bus I/F	ISA	PCI	CSI, ISA

Microsoft® Windows® CE

TORNADO™

Green Hills SOFTWARE, INC.

All VR41XX CPUs have the following basic peripheral:

- Interrupt Control Unit (ICU)
- Real Time Clock (RTC)
- Power Management Unit (PMU)
- Serial Interface Unit (SIU)
- Infrared Controller (IR)
- LED Interface Controller (LED)
- General Purpose I/O Unit (GPIO)

VR4121 64-bit MIPS RISC Microprocessor

Description

The 64-bit VR4121™ microprocessor is a member of NEC's VR series devices created for Windows®CE and VxWorks based industrial and consumer applications. Designed around the popular MIPS®RISC architecture, the VR4121 offers excellent performance in a high-integration, low-cost system on a chip. It is the first processor that uses the ultra-low power consumption VR4120™ CPU core based on advanced 0.25 µm technology.

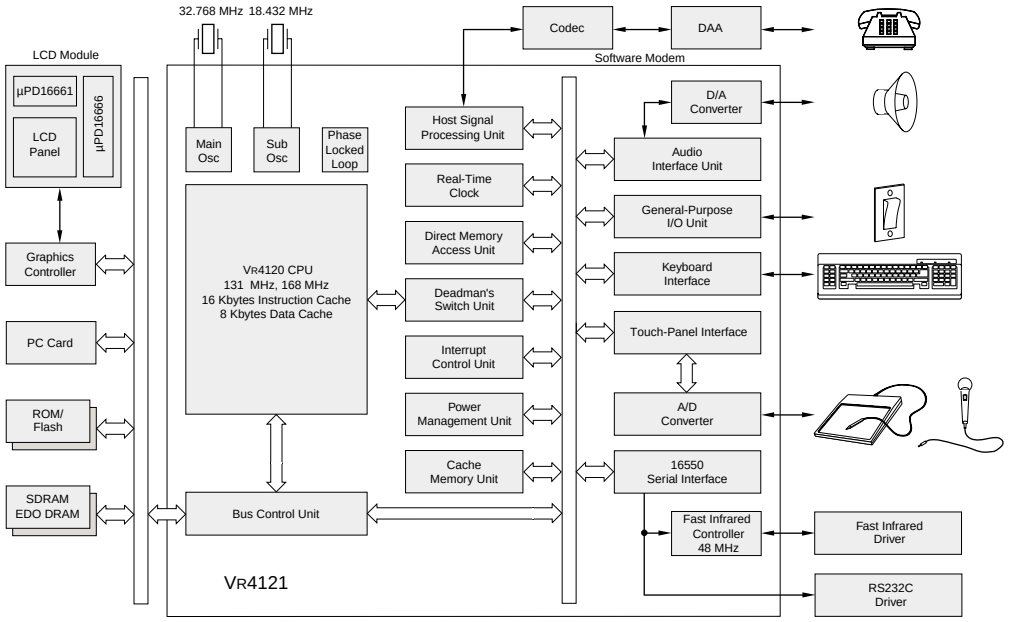
Applications

The VR4121 microprocessor's high speed, compact size, and low power consumption make it ideal for use in embedded handheld or stationary applications such as wallet PCs, PDAs, smart or web phones, mobile multimedia, in-car computing and industrial terminals. Windows® CE as well as VxWorks provide exactly the operating system features required by these applications. Both support packages are available on an evaluation and development board, along with several real-time operating systems.

Features

- VR4120 MIPS RISC CPU core
- MIPS I, II, III and MIPS 16 instruction set
- Performance up to 224 Mips at 168 MHz
- Fast single-cycle MAC instructions (DSP)
- Memory management unit
- SDRAM interface
- Cache memory: 16K instruction, 8K data
- Power management unit with 3 power-down modes
- Interrupt control unit
- 3-channel DMA controller
- Real Time clock with 4 timers
- 16550 compliant serial interface
- Infrared interface (max. 4 Mbps)
- Second serial interface
- Keyboard, touch-panel and LED interface controller
- 10-bit A/D converter
- 10-bit D/A converter
- 385 mW power consumption at 168 MHz
- Operating voltage: 2.5 V core, 3.3 V I/O
- 224-pin FPBGA package
- Windows® CE available
- VxWorks available

Block Diagram



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Ordering Information

Devices

Part Number	Package	Operating Frequency
µPD30121F1-131-GA	224-pin FPBGA	131 MHz
µPD30121F1-168-GA	224-pin FPBGA	168 MHz

Companion chips

Part Number	Package	Comment
VRC4172	208-pin FBGA	I/O Controller (USB, IEEE1284, UART)
Ravin	208-pin QFP	168 MHz

Documentation

Part Number	Devices	Type
SUD-T-4652	VR4121	Data Sheet
U13569EJ3V0UM00	VR4121	User's Manual

Tools

Order Number	Vendor	Description
DDB-VR4121S-1	NEC	Evaluation Board w/TFT
DDB-VR4121SE-1	NEC	Evaluation Board w/o TFT
See www.amc.com	Applied Microsystems*	NetROM/ROM Emulator
CPDW9X/NT-CDR-MIPS	Green Hills Software	Embedded MIPS Development Envir.
See www.algor.co.uk	Algorithmics*	Source Development Environment SDE
See www.microsoft.com	Microsoft*	Windows®CE Development Package
See www.wrs.com	WindRiver Systems*	VxWorks/Operating System
See www.atinucleus.com	Accelerated Technologies*	Nucleus Plus/Operating System

* Contact Vendor directly

For further information on NEC's VR family or other NEC products visit our European website at **www.nec.de**

VR4122 64-bit MIPS RISC Microprocessor

Description

The 64-bit VR4122 (µPD30122) microprocessor, a member of NEC's VR Series microprocessors, uses the ultra-low-power-consuming VR4120 CPU core based on advanced 0.18 µm technology. The VR4120 CPU offers excellent performance in a compact, low-cost system on a chip. The VR4122 is also available in extended temperature range (-40°C to +85°C).

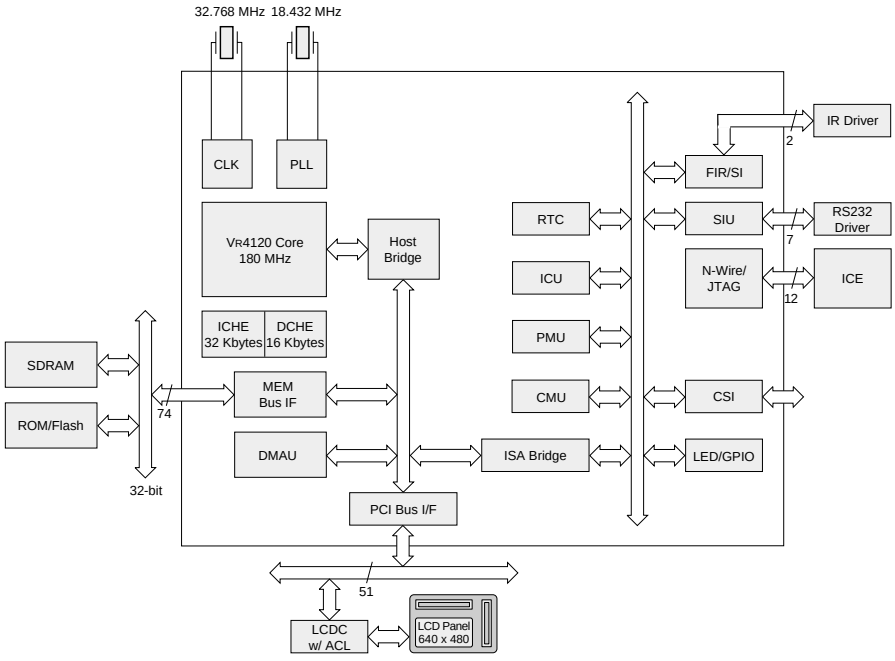
Applications

The 64-bit VR4122 microprocessor is designed especially for high-performance handheld portable computing devices and PCI-based systems such as network terminals, car information systems, webphones, digital cameras and other embedded systems. It uses the MIPS® RISC architecture developed by MIPS Technologies and offers excellent power consumption and performance in a highly integrated, low-cost system on a chip.

Features

- VR4120 CPU CORE
- MIPS I, II, III and MIPS 16 instruction set
- Performance up to 216 Mips at 180 MHz
- Fast single cycle MAC instruction (DSP)
- Memory management unit
- SDRAM interface
- Cache memory: 32 Kbytes instruction, 16 Kbytes data
- Power management unit with 4 power down modes
- Interrupt control unit
- 3-channel DMA controller
- Real time clock with 4 timers
- 16550 compliant serial interface
- Infrared interface (max. 4 Mbps)
- Second serial interface
- PCI bus interface controller
- LED interface controller
- 210 mW power consumption at 180 MHz
- Operating voltage: 1.8 V core, 3.3 V (I/O) operation
- 224-pin FPBGA package
- Windows CE available
- VxWorks available

Block Diagram



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Ordering Information

Devices

Part Number	Package	Operating Frequency
µPD30122F1-180-GA1	224-pin FPBGA	180 (-10°C to +70°C)
Please contact NEC	224-pin FPBGA	129 (-40°C to +85°C)

Companion chips

Part Number	Package	Comment
VRC4173	304-pin FPBGA	PCI Bus, USB, PC Card
Ravin	208-pin QFP	Graphic Controller

Documentation

Part Number	Devices	Type
Please contact NEC	VR4122	Data Sheet
U14327EJ1V0UM00	VR4122	User's Manual

VR4100 Family Comparison

Features	VR4121	VR4122
CPU Core	VR4120	VR4120A
Max. Pipeline Clock	168 MHz	180 MHz
Cache Size (Kbytes)	Instruction: 16; Data: 8	Instruction: 32; Data: 16
Performance	210 Dhrystone MIPS	216 Dhrystone MIPS
Instruction Set	MIPS 16, MIPS I, II, III	MIPS 16, MIPS I, II, III
MAC Instruction	Single-cycle, 32-bit	Single-cycle, 32-bit
Operating Voltage	2.5 V (core); 3.3 V (I/O)	1.8 V (core); 3.3 V (I/O)
Bus Supported	Subset of ISA	PCI, subset of ISA
Memory Interface	128 MB DRAM; 128 MB ROM	128 MB DRAM; 128 MB ROM
Power Consumption	350 mW	210 mW
Package	224-pin FPBGA	224-pin FPBGA
Temperature Range	-10°C to +70°C	-10°C to +70°C/-40°C to +85°C
Process Technology	0.25-micron UR2 process	0.18-micron UC3 process

For further information on NEC's VR family or other NEC products visit our European website at **www.nec.de**

VR4181 64-bit MIPS RISC Microprocessor

Description

The 64-bit VR4181™ microprocessor is a member of NEC's VR series devices created for embedded industrial and consumer applications. Designed around the popular MIPS RISC architecture, the VR4181 offers excellent performance in a high-integration, low-cost system on a chip. The chip features integrated peripherals for miniaturized, palm-sized terminals and systems and ultra-low power consumption, based on advanced 0.25 µm technology.

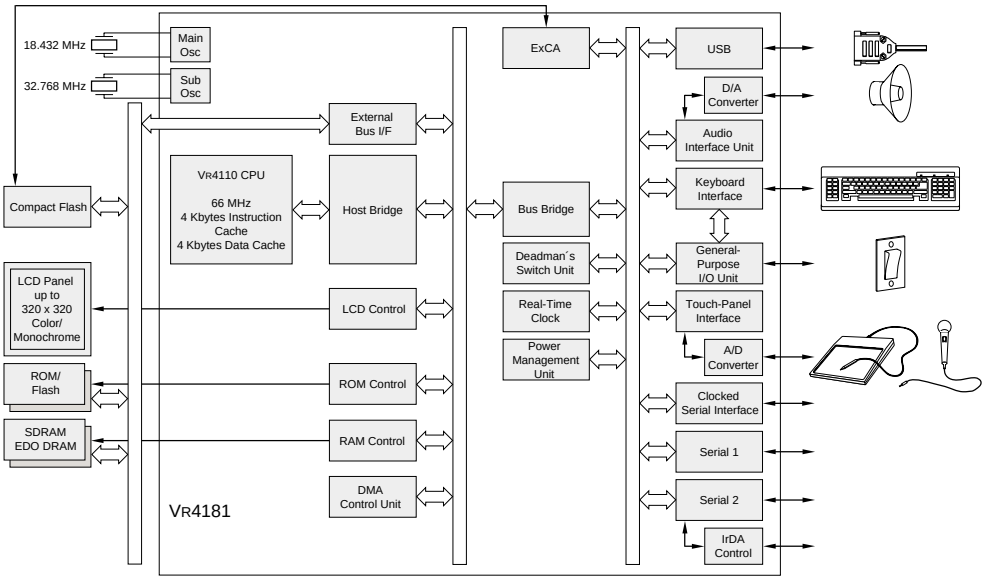
Applications

The speed, compact size, low power consumption and high integration level of the VR4181 are ideal for embedded handheld applications such as PDAs, smart or web phones, mobile communicators and GPS receivers. Windows® CE, available as a demo and reference system, provides the operating system functionality required by these applications. An outstanding feature is the ease with which industrial terminals with sophisticated man-machine interfaces can be designed using the VR4181 and Windows® CE or any other operating system already ported to the VR4100 family.

Features

- VR4110 MIPS RISC CPU core
- MIPS I, II, III and MIPS 16 instruction set
- Fast single-cycle MAC instructions (DSP)
- Memory management unit
- SDRAM/EDO RAM and ROM interface
- Cache memory: 4 K instruction, 4 K data
- Power management unit with 3 power-saving modes, down to 17 µA
- Interrupt control unit
- 4-channel DMA controller
- Timer, counter, RT clock
- Separate debug port
- 2 x 16550 compliant serial interface and clocked serial interface (CSI)
- Chip selects and general purpose I/O ports
- Infrared interface
- 8 x 8 keyboard, touch-panel and LED interface controller
- 12-bit A/D converter with 8 input channels
- 10-bit D/A converter
- 250 mW power consumption at 66 MHz
- Operating voltage: 2.5 V core, 3.3 V I/O
- 160-pin LQFP package
- Windows® CE available

Block Diagram



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Ordering Information

Devices

Part Number	Package	Operating Frequency
µPD30181GM-66-SED	160-pin LQFP	66 MHz

Documentation

Doc Number	Devices	Type
U14273EJ1V0DS00	VR4181	Data Sheet
U14272EJ1V0UM00	VR4181	User's Manual

Tools

Order Number	Vendor	Description
DDB-VR4181	Applied Microsystems	NetROM/ROM Emulator
CPDW9X/NT-CDR-MIPS	Green Hills	Embedded MIPS Development Environment
See www.algor.co.uk	Algorithmics	Source Development Environment SDE
See www.microsoft.com	Microsoft	Windows®CE Development Package
See www.wrs.com	WindRiver	VxWorks/Operating System
See www.atinucleus.com	Accelerated Technologies	Nucleus Plus/Operating System

* Contact vendor directly

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VR43xx 64-bit MIPS RISC Microprocessor

Description

The 64-bit VR43xx microprocessors are members of NEC's VR Series devices created for high-performance embedded applications. Based on the popular RISC architecture developed by MIPS™, the VR4300™ family offers one of the best performance/die size solutions on the market. In 1997 the California based magazine Microprocessor Report acknowledged this by awarding its prestigious "Embedded microprocessor of the year" citation to the VR4300 for its combination of price, performance, and flexibility.

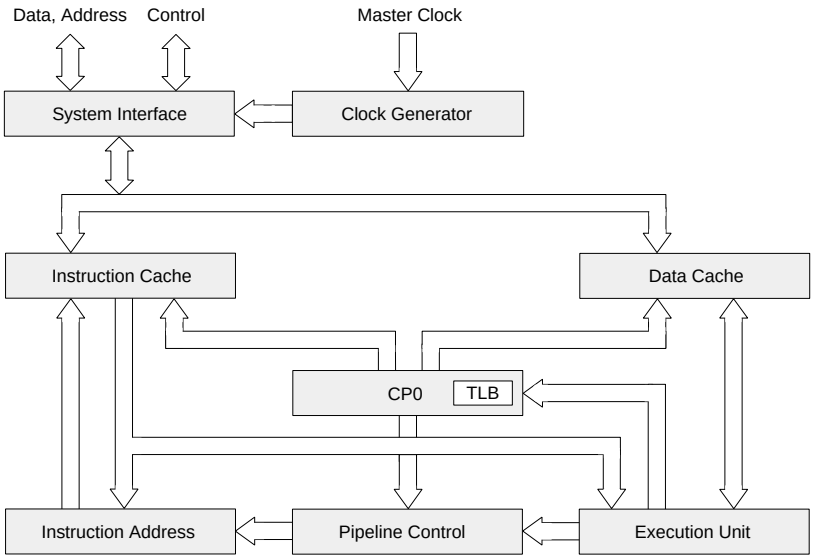
Applications

Offering superior performance at an affordable price the VR43xx microprocessors are perfect for high-performance embedded applications where cost is a primary consideration. Whereas the VR4310 offers the highest performance at 167 MHz, the VR4305 is a true low-price product that nevertheless sports an 80 MHz clock. VR43xx devices are also among the most powerful processors available to support Windows®CE.

Features

- 64-bit MIPS RISC architecture
- MIPS I, II and III instruction set
- High-speed execution of integer and floating-point operations
- 5-stage pipeline processing
- Floating-point unit
- Memory management unit
- Cache memory: 16K instruction, 8K data
- Multiplexed 32-bit address/data bus
- 64-bit or 32-bit mode
- 3 operating modes: User, Supervisor and Kernel
- Power management with 2 power-down modes
- Exception processing unit
- JTAG interface for boundary scan
- Single clock supply
- 1.4 W typical power consumption, VR4310 @ 100 MHz
- Performance up to 221 Mips, VR4310 @ 167 MHz
- Operating voltage: 3.3 V ±10%
- 120-pin plastic QFP package

Block Diagram



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Ordering Information

Devices

Part Number	Product Name	Operating Frequency	Performance	Power Consumption
µPD30200GD-80-LBB	VR4305	80 MHz	106 Mips	1.5 W
µPD30200GD-100-MBB	VR4300	100 MHz	131 Mips	1.8 W
µPD30200GD-133-MBB	VR4300	133 MHz	173 Mips	2.4 W
µPD30210GD-100-MBB	VR4310	100 MHz	133 Mips	1.4 W
µPD30210GD-133-MBB	VR4310	133 MHz	176 Mips	1.9 W
µPD30210GD-167-MBB	VR4310	167 MHz	221 Mips	2.4 W

Companion chips

Part Number	Package	Comment
VRC4372	208-pin QFP	I/O Controller
VRC4373	304-pin QFP	PCI Interface and Memory Controller

Documen-tation

Doc Number	Devices	Type
U10504EJ7V0UM00	VR43xx	User's Manual
U10116EJ6V0DS00	VR43xx	Data Sheet

Tools

Order Number	Vendor	Description
P-5032*	Algorithmics	Evaluation Board
NetROM*	Applied Microsystems	ROM Emulator
CPDW9X/NT-CDR-MIPS	Green Hills	Embedded MIPS Development Enviroment
See www.algor.co.uk	Algorithmics	Source Development Enviroment SDE
See www.microsoft.com	Microsoft	Windows® CE Development Package
See www.wrs.com	WindRiver	Operating System
See www.atinucleus.com	Accelerated Technologies	Operating System

* Contact vendor directly

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VR5000 64-bit MIPS RISC Microprocessor

Description

The VR5000 (µPD30500) is NEC's implementation of the MIPS™ RISC R5000. The VR5000 is a 64-bit dual-issue super scalar processor that offers enhanced floating-point computing capabilities. Different packaging and speed options are available now, see page 3.

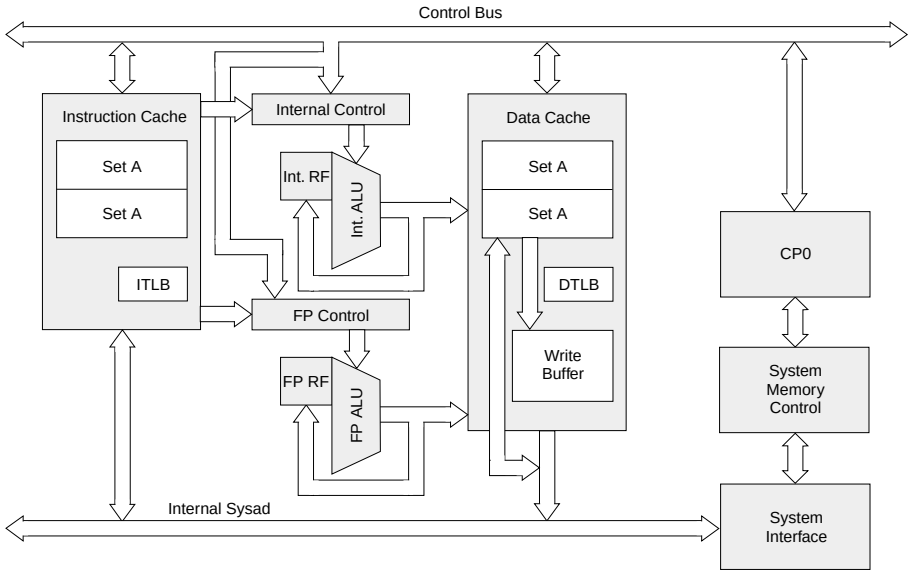
Applications

Applications for the VR5000 include internetworking devices such as routers and bridges, office automation equipment including photocopiers, image processing systems such as laser printers and other computer peripherals, digital set-up boxes, high-performance embedded systems such as arcade game machines, entry class and graphical workstations.
The processor interfaces directly without additional glue logic, using the VRC5074 companion chip, to external DRAM, local I/O bus and standard PCI bus (without buffers).

Features

- 64-bit RISC core
- 64-bit SysAD external interface
- 2-way super scalar 5-stage pipeline
- 5.2M transistors
- 6.6 SpecInt95, 6.6 SpecFP95 @ 250 MHz
- 352 Dhrystone MIPS @ 250 MHz
- Large on-chip primary caches: 32Kbytes data/32 Kbytes instruction (both 2-way)
- L2 cache support 256 Kbytes up to 2 Mbytes, write-through
- On-chip MMU support: 48-entry TLB
- MIPS-IV instruction set
- IEEE-754 compliant enhanced single/double precision floating-point for high speed 2D/3D graphics
- Binary compatibility with existing MIPS software
- Scaleable for multiple processors
- Easy interfacing with VRC5074 companion chip
- Supply voltage:
  (µPD30500) 3.3V
  (µPD30500A) 2.5V (Core), 3.3 V (I/O)
  (µPD30500B) 1.8V (Core), 3.3 V (I/O)
- 7.5 W (max) power dissipation @ 250 MHz

Block Diagram



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Ordering Information

Devices

Part Number	Package	Max. Frequency (MHz)
µPD30500S2-180	272-pin plastic BGA	180
µPD30500S2-200	272-pin plastic BGA	200
µPD30500AS2-250	272-pin plastic BGA	250
µPD30500BS2-300	272-pin plastic BGA	300

Documentation

Part Number	Package	Comment
VRC5074	208-pin FBGA	I/O Controller (USB, IEEE1284, UART)

Companion chips

Part Number	Devices	Type
U11761EJ3V0UM00	VR5000	User's Manual - Device
U12754EJ1V0UM00	VR5000	User's Manual - Instruction Set
U12031EJ3V0DS00*	VR5000	Data Sheet
U13290EU1V0DS00	VRC5074	Data Sheet

* Preliminary document

Main Differences between VR5000, VR5000A, VR5000B

Parameter	VR5000	VR5000A	VR5000B
Maximum internal operating frequency	150/180/200 MHz	200/250 MHz	250/300 MHz
Internal multiplication ratio for clock interface input	2, 3, 4, 5, 6, 7, 8	2, 2.5*, 3, 4, 5, 6, 7, 8	
Supply voltage	3.3 V ± 5%	Core: 2.5 V ± 5% I/O: 3.3 V ± 5%	Core: 2.5 V ± 0.1 V I/O: 3.3 V ± 5%
Package	223-pin ceramic PGA 272-pin plastic BGA	272-pin ceramic BGA	

* Selectable only when SysClock = 100 MHz

For further information on NEC's VR family or other NEC products visit our European website at **www.nec.de**

VR5432 64-bit MIPS RISC Microprocessor

Description

The VR5432 brings a new level of high-end performance to embedded applications. Featuring 64-bit architecture, a dual-issue superscalar pipeline and MIPS® IV instruction set support, this device is ideally suited to high-end applications.

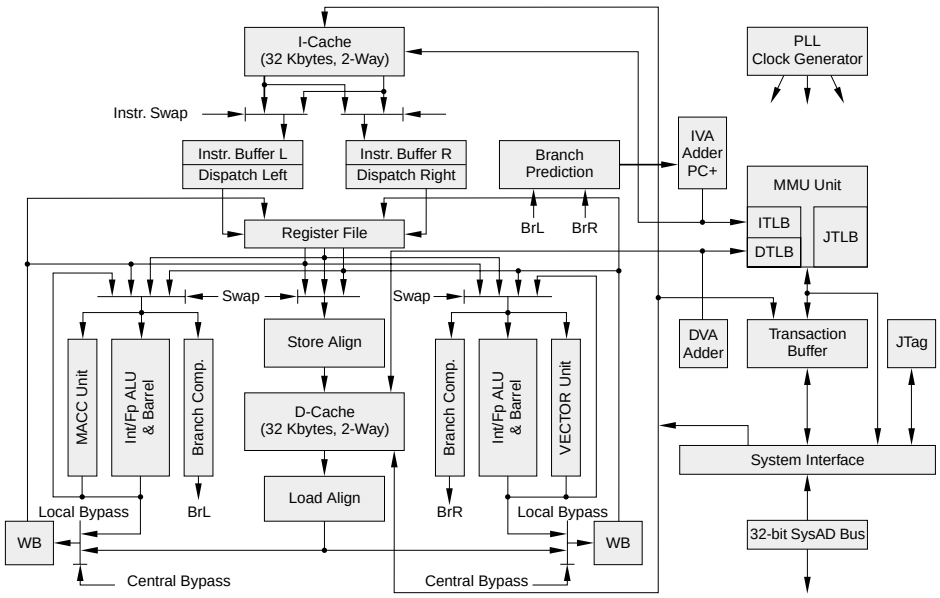
Applications

The VR5432 processor complies with the MIPS® IV instruction set, IEEE-754 floating-point and IEEE-1149.1/1149.1a JTAG specifications, and also extends these standards with many enhancements vital to high-end office automation, network, communication, multimedia and industrial control applications.

Features

- Performance up to 256 Dhrystone Mips at 167 MHz
- Superscalar pipeline
- Instruction set extensions
- Cache memory: 32 Kbyte Instruction and 32 Kbyte data
- 4 Kbyte-entry branch prediction table
- Memory and exception management
- Floating-point operation (coprocessor 1)
- Enhanced system interface
- On-chip debugging
- Low power consumption: 2.5 W (max) at 167 MHz
- Operating voltage: 2.5 V core, 3.3 V I/O
- Package: 208-pin plastic QFP

Block Diagram



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Ordering Information

Devices

Part Number	Package	Max. Frequency
µPD30541GD-167-SML	208-pin PQFP	167 MHz

Companion Chips

Part Number	Package	Comment
Bonito	352-pin BGA	SDRAM interface, PCI bus, local bus

Documentation

Doc Number	Devices	Type
U14011EJ2V0UM00	VR5432	User's Manual
Please contact NEC	VR5432	Data Sheet

Tools

Order Number	Vendor	Description
P-5032	Algorithmics*	Evaluation Board w/ various options**
See www.algor.co.uk	Algorithmics*	Source Development Environment SDE
CPDW9X/NT-CDR-MIPS	Green Hills Software*	Embedded MIPS Development Envir.
See www.wrs.com	Wind River Systems*	Vx Works Operating System
See www.microsoft.com	Microsoft*	Windows®CE Development Package
See www.linux.org	Linux*	Linux Operating System

* Contact Vendor directly

** Under development

For further information on NEC's VR family or other NEC products visit our European website at **www.nec.de**

Chipsets

VRC4172 Companion Chip for VR4121 Microprocessor

Description

The VRC4172 companion chip to NEC's VR4121 TM MIPS ® RISC microprocessor is designed for high-end Windows®CE Handheld PC Professional applications. The VR4121 microprocessor functions as the host CPU, while the VRC4172 supplies the SDRAM interface, USB interface, host- and peripheral-selectable IEEE-1284 parallel interface, 16550-compliant serial interface, PS/2 interface, general-purpose I/O ports, general-purpose chip select signal, and pulse-width modulation for the LCD back light.

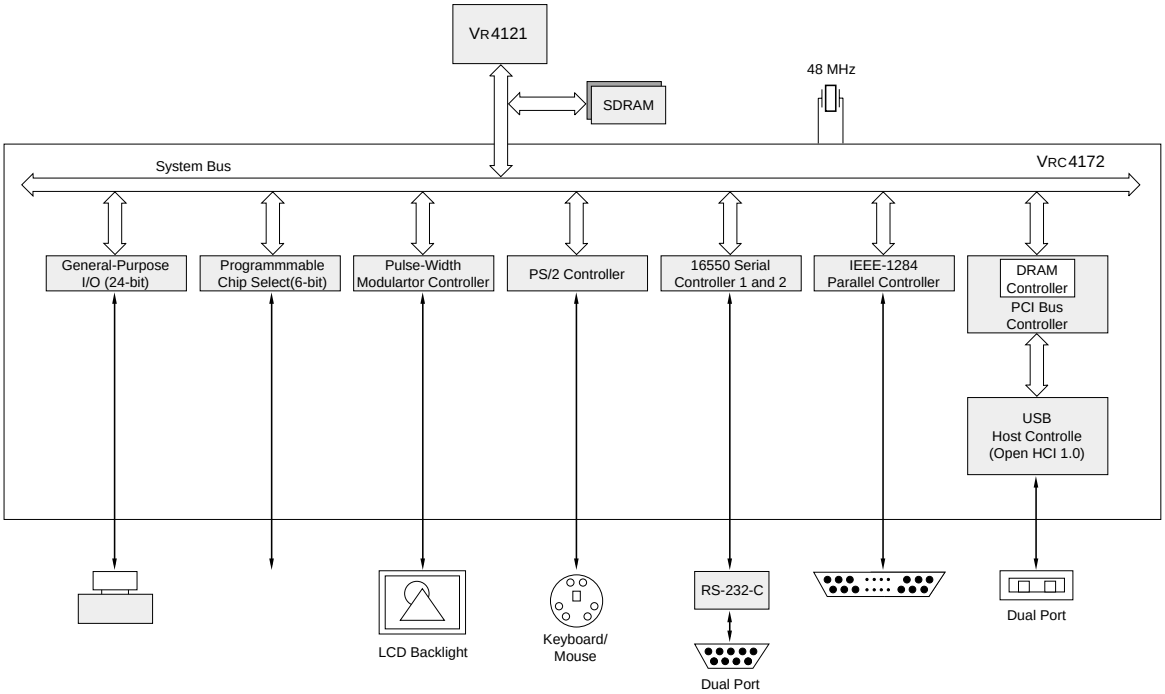
Applications

In combination, the VR4121 and VRC4172 offer an excellent performance/cost solution for next-generation Windows®CE applications, forming a superior engine for most, if not all, high-performance Windows® CE-based and VxWorks-based handheld products.

Features

- 32-bit LCD interface
- 16-bit mini-ISA bus interface
- SDRAM controller
- USB Host controller
- IEEE1284 parallel port interface
- Two 16550-compatible serial interfaces
- Programmable chip select and general purpose I/O
- PS/2 interface
- Pulse width modulation (PWM) for LCD backlight
- Glueless interface to VR4121
- Operation voltage: 3.3 V ± 10%
- 208-pin FBGA package

Block Diagram



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Package	Operation Frequency
Vrc4172	208-pin FBGA	168 MHz

Supported Devices

Part Number	Package	Operation Frequency
VR4121	224-pin FBGA	168 MHz

Documentation

Part Number	Devices	Type
Please contact NEC	VRC4172	Data Sheet

For further information on NEC's VR family or other NEC products visit our European website at **www.nec.de**

VRC4173 Companion Chip

Description

The VRC4173 is a companion chip designed to be used with NEC's VR4122 64-bit MIPS® RISC microprocessor. The VRC4173 incorporates the I/O macros necessary for a handheld PC running Windows® CE and can also access design resources on a personal computer by means of the PCI bus interface. With the VR4122 acting as the host CPU, the VRC4173 functions include PCI bus interface, USB host controller, two-slot PC Card™ controller, AC97 interface, keyboard controller, 10-bit D/A converter, 12-bit A/D audio controller, touch panel controller, general-purpose I/O pins, and built-in 48-MHz oscillator.

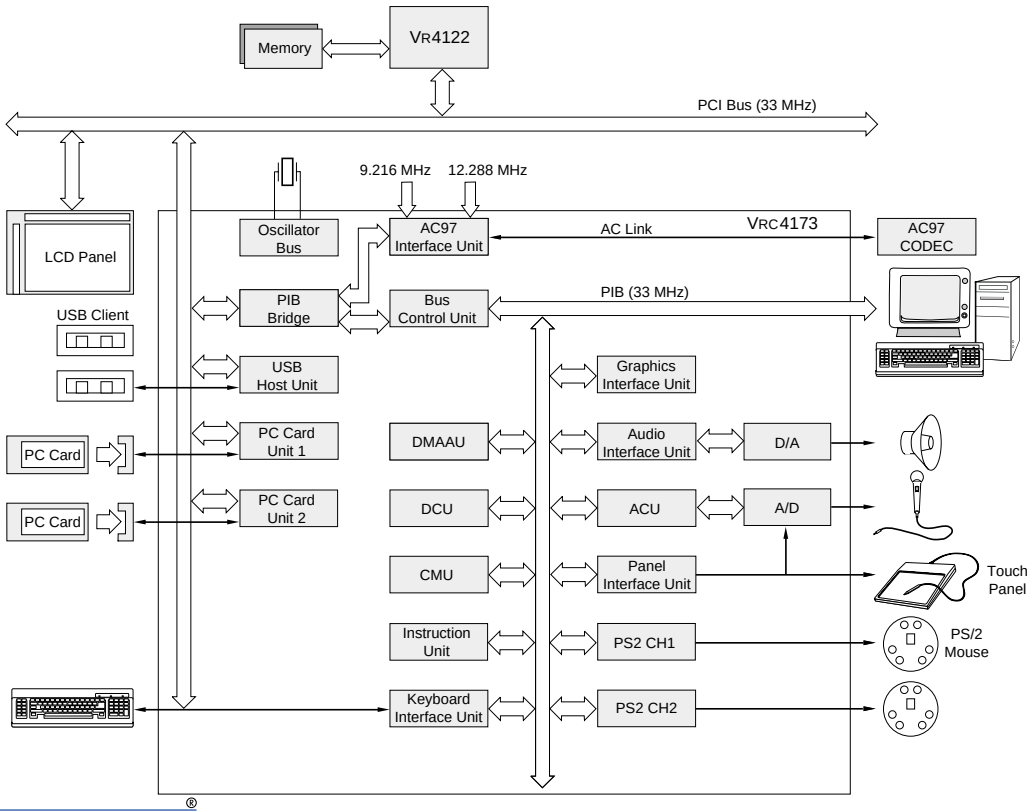
Applications

The VR4122 and VRC4173 provide an excellent performance/cost solution for Windows® CE H/PC Pro applications. They also form an ideal engine for most high-performance Windows® CE-based and VxWorks-based handheld products.

Features

- PCI bus processor interface
- USB Host controller
- Two PC card controllers
- AC link interface
- Keyboard, touch-panel and LED interface controller
- 10-bit D/A converter
- Graphic interface unit
- 12-bit A/D converter
- PS/2 interface
- Glueless interface to VR4122
- Operation voltage: 3.3 V ± 10%
- 304-pin FBGA package

Block Diagram



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Package	Comment
µPD31173F1-33-HN	304-pin FPBGA	PCI Bus, USB, PC-Card

Supported Devices

Part Number	Package	Operation Frequency
VR4122	224-pin FPBGA	150 MHz
VR4122	224-pin FPBGA	180 MHz

Documentation

Part Number	Devices	Type
Please contact NEC	VRC4173	Data Sheet
Please contact NEC	VRC4173	User's Manual

For further information on NEC's VR family or other NEC products visit our European website at **www.nec.de**

RAVIN

Description

RAVIN is a member of NEC's graphic controller series µPD7225x for image data processing. In addition to display control functions, RAVIN provides integrated high-speed rendering functions based on a high-performance PC graphic accelerator, enables input and display of external video signals and possesses a built-in D/A converter. Screen resolutions supported by µPD72254 range from ¼ VGA (320 x 240) up to SVGA (800 x 600).

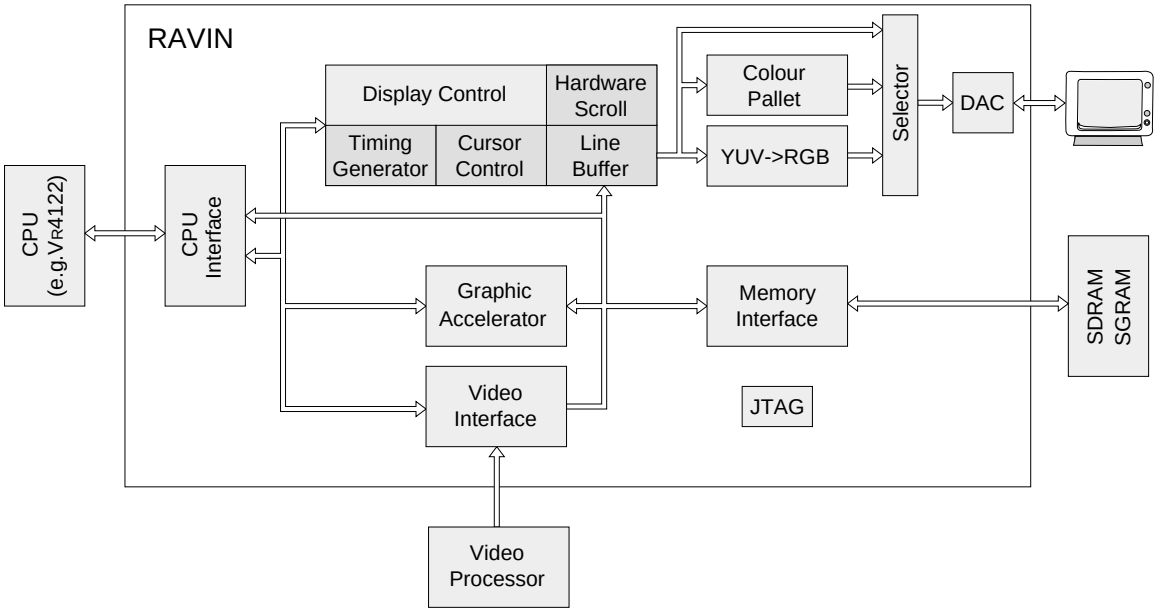
Applications

RAVIN is the ideal partner to support a MIPS-RISC processor CPU in the data handling of fine resolution, high information content images in today's multimedia applications - i.e. car navigation, dashboard displays, GPS systems, webphones, measuring instruments, game machines or industrial terminals.

Features

- Fast rendering based on PC graphic accelerator
- Extended drawing function set
- Basic set of 3D graphic functions
- Display resolution from ¼ VGA up to SVGA
- Transparent mode: 4 bitmap layers with transparency function, video layer and cursor
- Window mode: Bitmap layer, video layer, three hardware windows and cursor
- Colour mode 16 bit per pixel
- Colour mode 8 bit per pixel out of 256k colour palette
- Hardware cursor for 64 x 64 dots, 2 bit per pixel
- 32-bit CPU interface, DC to 33 MHz
- 32-bit SG/SDRAM interface, 66 MHz, up to 16 Mbyte
- 64-bit internal data path, 33 MHz internal clock speed
- External video input, scaling and display
- Soft scrolling in each direction
- Command list execution function
- Power management function
- Digital and analogue video output
- Temperature range -40 to +85° C
- Operating voltage: 3.3 V ± 10 %
- 208-pin QFP package

Block Diagram



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Package
PD72254YGD-001-LML	208-pin QFP

Partner Chips

Part Number	Package	Comment
VR4121	224-pin FPBGA	Micro Processor Unit
VR4122	224-pin FPBGA	Micro Processor Unit

Documentation

Doc.-Number	Devices	Type
To be determined	µPD72254Y	Data Sheet

Tools

Order Number	Vendor	Description
To be determined	NEC	Evaluation Board
To be determined	NEC	Function Library

For further information on NEC's display IC or other NEC products visit our European website at **www.nec.de**

Bonito
System controller for MIPS CPU's with 32-bit SysAD bus

Description

The 'Bonito' is a system controller especially designed for MIPS®RISC microprocessors with a 32-bit SysAD bus. 'Bonito' incorporates a simple and fast memory interface for PC-100 compliant SDRAMs, a Rev 2.1 compliant 33 MHz/32-bit PCI interface and last but not least a 16-bit local bus with IDE support. It has a built-in, flexible interrupt controller and numerous general purpose I/Os. In applications using the 32-bit SysAD bus (e.g. VR43xx and VR5432 based systems) it reduces the number of required parts significantly. 'Bonito' comes in a compact 352-pin plastic BGA package.

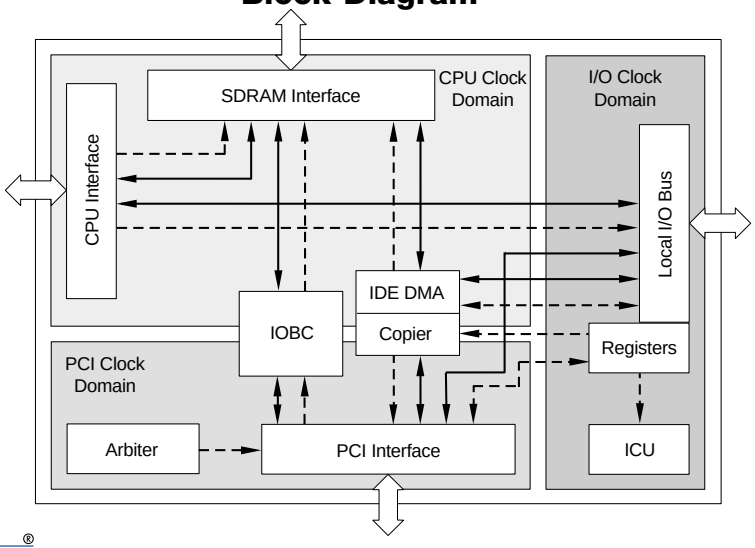
Applications

'Bonito' is designed as system controller for MIPS® RISC CPU based systems. The combination of 'Bonito' with a MIPS® RISC microprocessor gives you an excellent performance/cost ratio for computing or data traffic intensive applications like high resolution printers, scanners, networking equipment, high end Set-Top-Boxes or PC-Peripherals.

Features

- Direct connection to any MIPS R4x00 CPU with a 32-bit SysAD bus
- Direct connection to 32-bit 33 MHz PCI bus, conforming to Rev. 2.1
- Integrated PCI arbiter acting as PCI master or target
- Independent CPU and PCI input blocks
- Internal 'cache' for local memory locations provides greatly enhanced PCI transfer performance for device controllers which are PCI bus initiators
- PCI/local-memory copier for applications requiring bulk data transport
- 16-bit local I/O bus for local ROM and 'slow' peripherals
- High performance SDRAM memory interface using standard PC-100 parts in either 32- or 64-bit arrays, including 100-, 144- or 168-pin DIMMs
- DMA support for faster devices on the local I/O bus, including 'UDMA´ transfers as defined in the ATA-4 standard for PC disk drives
- Configurable debug mode
- Glueless support of CPU reset sequence
- Includes useful generic interrupt controller
- Configurable from ROM, pins or PCI bus
- Supports all VR43xx and VR5432 bus modes
- Operating voltage: 3.3 V, 5 V tolerant I/O
- Compact 352-pin 1,27 mm pitch BGA package

Block Diagram



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Package	Operating Frequency
µPD65949S1-P100-F6	352-pin PBGA	100 MHz on SysAD bus (target)

Target CPUs

Part Number	Package	Comment
µPD30200GD-80-LBB	120-pin QFP	VR4305
µPD30200GD-100-MBB	120-pin QFP	VR4300, 100 MHz
µPD30200GD-133-MBB	120-pin QFP	VR4300, 100 MHz
µPD30210GD-133-MBB	120-pin QFP	VR4310, 133 MHz
µPD30210GD-167-MBB	120-pin QFP	VR4310, 167 MHz
µPD30541GD-167-SML	120-pin QFP	VR5432, 167 MHz

Documentation

Doc Number	Device	Type
Please contact NEC	'Bonito'	Data Sheet

Tools

Order Number	Vendor	Description
P-5032	Algorithmics*	Evaluation Board with various CPU options**
CPDW9X/NT-CDR-MIPS	Green Hills*	Embedded MIPS Development Environment
See www.algor.co.uk	Algorithmics*	Source Development Environment SDE
See www.algor.co.uk	Algorithmics*	BSP for Windows®CE (on request)
See www.algor.co.uk	Algorithmics*	BSP for VxWorks Operating System**
See www.algor.co.uk	Algorithmics*	BPP for pSOS Operating System**

* Contact vendor directly

** Under development

For further information on NEC's VR series or other NEC products visit our European website at **www.nec.de**

VRC5074 Interface Controller for the VR5000 Microprocessor

Description

The VRC5074 is a single-chip device that provides a glueless interface between a VR5000 processor and a DRAM memory system, local I/O bus, and standard PCI bus. The VRC5074 interface controller connects directly to the VR5000 microprocessor and PCI bus with no buffering required. The DRAM memory interface connecting to local memory contains the logic required to directly drive several types and speeds of SDRAM. The interface control logic is highly configurable by software and can be used with minimal hardware configuration in many different types of systems. The local bus interface connecting to local I/O contains the interface logic necessary to directly drive several types and speeds of peripheral devices.

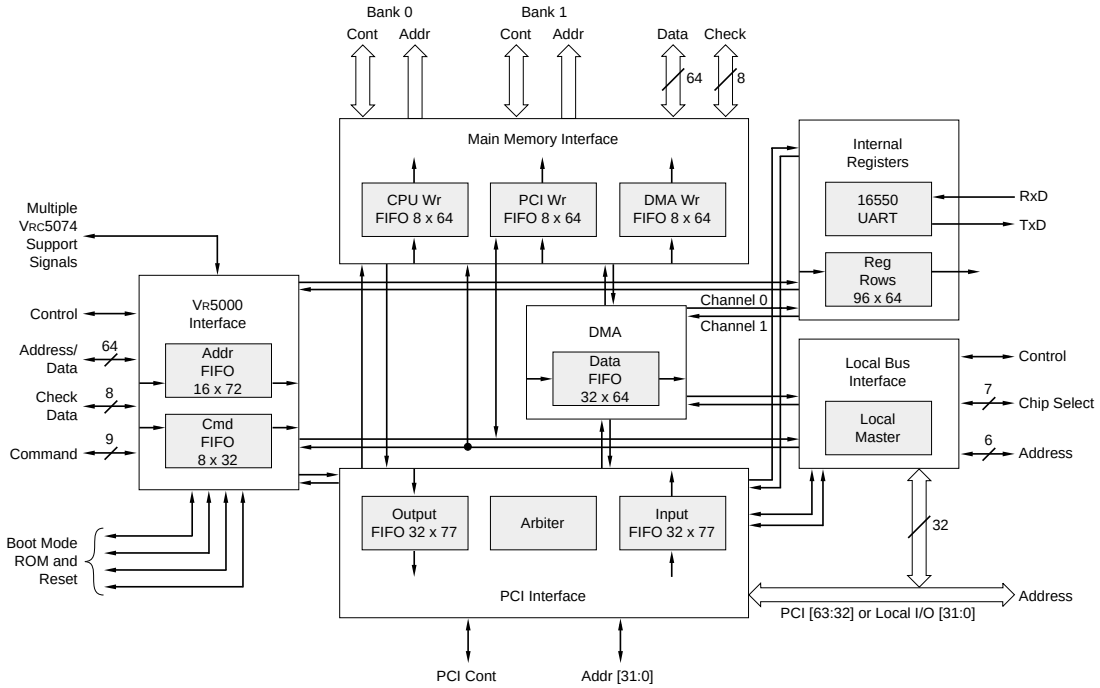
Applications

The VR5000 together with the VRC5074 offers you an excellent high-performance solution for your application like internet working devices such as routers and bridges, image processing systems like laser printers, digital set top boxes or high-end embedded equipment such as game machines or entry class and graphical workstations.

Features

- Glueless interface to VR5000 microprocessor
- SDRAM interface
- PCI bus interface controller
- Local I/O Interface
- DMA controller
- 16550 compliant serial interface
- Three timer channels
- Operation voltage: 3.3 V ± 10%
- 500-pin BGA package

Block Diagram



RISC by NEC: Know-how²

NEC

Ordering Information

Devices

Part Number	Package	Comment
Vrc5074	500-pin FBGA	Memory interface, PCI, local bus

Supported Devices

Part Number	Package	Operation Frequency
VR5000	272-pin plastic FBGA	180 MHz
VR5000	272-pin plastic FBGA	200 MHz
VR5000	272-pin plastic FBGA	250 MHz
VR5000	272-pin plastic FBGA	300 MHz

Documen-tation

Doc Number	Devices	Type
Please contact NEC	VRC5074	Data Sheet
Please contact NEC	VRC5074	User's Manual

For further information on NEC's VR family or other NEC products visit our European website at **www.nec.de**

Compilers/Debuggers/Linkers

Nucleus EDE Embedded Development Environment

Features

- Embedded Development Environment
- Based on Microsoft Developer Studio™
- Build your system using any commercial development tools
- Errors appear in window for quick editing
- Pre-configured when shipped to you
- Easy access of cross debuggers

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

PC

Product Overview

Built on the firm foundation laid by Microsoft Developer Studio™, we have constructed an Embedded Development Environment (EDE), Nucleus EDE. We began with the concept that Developer Studio™ is one of the most complete IDE's available, so we extended its capabilities to compile, link, and debug embedded applications using cross-development tools. The result is an environment that is easy to support, uses the latest technology, and is adaptable to any cross development tool. In addition to the edit, build, and debug features of Microsoft Developer Studio™, it offers project management, the class manager, and browser features. Also, you can add other tools, such as a code management system or any tool that supports code development within Microsoft Developer Studio™.

One of the greatest benefits of Microsoft Developer Studio™ is the ability to build and have any errors appear in a window so you can vector to any file that may need to be edited. We provide tools with Nucleus EDE so that you can use those same facilities for cross compilers. You build your system using cross-development tools; if any errors occur, they appear in the error window. Double click on the error, and you are immediately placed in the edit window at the line where the error occurred. After editing and repairing the error, you can rebuild your system. Also, Microsoft Developer Studio™ will ensure that the edited file has been properly saved before the build starts.

When we ship Nucleus EDE to you, it is pre-configured to include the common Nucleus directories and default paths for the tool set that you are using. Also, it contains Wizards to support the compiler, assembler, librarian, linker, and locator command-lines and switches that we use when building the target Nucleus application.

Accelerated Technology
INCORPORATED

Nucleus MNT Windows NT-based Prototyping Environment

Features

- Executes as a native Windows NT™ or Windows 95™ application
- Designed and developed with Microsoft's Visual C++™ tool set
- PC hosted development and run-time environments
- Prototype most C code that will be used in target system
- Provided with a pre-built project file

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

PC

Product Overview

Nucleus MNT utilizes three modules ported to the Windows NT (or Windows 95) threads environment to perform initialization, scheduling, and timer management functions. The initialization module sets up interrupt vectors for the timer and the terminal interface. The scheduling module employs the Windows thread model to manage the switching of tasks, while the timer module processes a timer tick to facilitate the Nucleus PLUS task sleep, time-slicing, time-out, and timer-thread capabilities.

Development and Debugging:

Nucleus MNT was designed and developed to work with Microsoft's Visual C++ tool set. The complete Microsoft Visual C++ Integrated Development Environment is available, including the editor, make/project capabilities, compiler, librarian, assembler, linker, and debugger.

By using the project file supplied with Nucleus MNT, you can be up and running almost immediately. The release files shipped with Nucleus MNT are loaded into a directory. You add the project to your Microsoft Visual C++ environment and the "Build" menu selection is invoked to produce a Windows NT console application. The Executable contains a demonstration program that exercises almost all Nucleus PLUS capabilities. You can modify this program or replace it with tasks you create when you begin development of your project.

Because Nucleus MNT and the programs developed with it are true Windows NT applications, they can be debugged using the standard Microsoft Visual C++ debugger. Other debugging aids supplied with Microsoft Visual C++ (e.g., Spy) also can be used in the debugging process.

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Nucleus DBUG+ Multitasking Debugger

Features

- Displays task information
- Displays queue information
- Displays resource information
- Displays event group information
- Displays memory partition information
- Modify/display memory capability
- Invoke all Nucleus PLUS services from command line
- Documented source code provided
- Integrated with popular source debuggers

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

PC

Product Overview

Nucleus DBUG+ was developed to assist users of Nucleus PLUS in debugging their multitasking applications. It installs as a task in any Nucleus PLUS system and provides a number of features not normally available within traditional debugging environments.

Because Nucleus DBUG+ is installed as a task, it can freely interact with the rest of the tasking environment. Additionally, tasking information can be viewed in both overview and detailed form. All user interaction with Nucleus DBUG+ is performed through a command line prompt.

The user invokes Nucleus DBUG+ by either entering a status command or invoking Nucleus PLUS services by entering the C interface calls. Status commands have optional parameters which can indicate the specifics associated with the status (e.g., ts 1 -- displays status of task number 1). C interface calls are entered and the user is prompted for the appropriate parameters.

As well as being delivered with complete source code and without royalties, Nucleus PLUS is provided with six months free technical support. This includes phone, fax, email and new releases. For more information, contact Accelerated Technology today.

Accelerated Technology
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Nucleus UDB
Portable Source Level Debugger

Features

- Automatic tracing feature
- Kernel aware debugging
- Configurable display windows for source, memory, variables, registers, etc
- Intuitive button bar interface provides a quick learning curve
- Complex breakpoints
- Console window capture-to-file capability
- Universal file viewer
- Stopwatch for timing functionality
- Improved source file tracking
- Advanced Dynamic Data Exchange
- Advanced DLL interface

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

PC

Product Overview

The price/performance ratios among microprocessors are constantly changing. Processors appropriate for today's projects may not be suitable for tomorrow's application. For the embedded systems developer, this often means readjusting to a new set of development tools. To relieve some of the burden and speed development time, Nucleus UDB offers a consistence interface across various processor platforms. This enables developers to quickly adapt to new challenges and meet the demands of changing applications.

Nucleus UDB was designed from the ground up to take advantage of the facilities contained within the Windows operating system. Nucleus UDB offers an intuitive button driven interface, as well as an event driven sequencer system. In addition, UDB provides both task specific and general breakpoint capabilities to help accelerate embedded system development. Combined, these features offer faster performance, as well as the ability to run other applications while a debugging session is active.

Source Level Debugging:
Nucleus UDB is a powerful, GUI-based source-level debugger for embedded applications. Its three component configurations include the debugger front-end, host communications module, and target monitor. These components combine for a powerful and portable debugging environment. Since the front end is standard across all target CPU platforms, developers need learn only one debugging environment.

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Nucleus FILE
MS-DOS Compatible File System

Features

- No royalties
- C source code provided
- Support for FAT32, including long filenames
- ROMable
- MS-DOS 4.0 and higher compatible
- Re-entrant file access
- Supports multiple floppy formats and fixed disks
- File system format facilities provided
- RAM disk available
- Transparent to CPU byte ordering
- Simple device driver interface
- Two entry points for date/time management
- Integrated with Nucleus PLUS

NEC CPUs Supported

VR4111, other on request

Host Platforms Supported

PC

Product Overview

The need for mass storage takes many forms, including collecting data for later analysis and continued operation of the system. In both cases, it is helpful to be able to address the data outside the embedded environment. To support these requirements, Accelerated Technology provides Nucleus FILE.

Nucleus FILE is a robust, well-integrated tool for managing MS-DOS-compatible file formats which require that a driver only needs to be fully functional on the target system. Accelerated Technology supports drivers for a number of industry standard devices. This support increases as new device drivers continue to be developed. In addition to supporting various device drivers, a RAM disk driver also is available. A limited version of this driver is provided in object form for testing on your target system, which allows you to quickly see Nucleus FILE in operation after building and downloading.

Essential Capabilities
Nucleus FILE is written entirely in C and provides all necessary functions to manage MS-DOS-compatible disks. This includes the boot block, File Allocation Table (FAT), directory, file, and device driver management. Other than standard MS-DOS capabilities, Nucleus FILE allows multiple tasks to access the file system simultaneously by requiring all tasks to register as users of the file system.

Accelerated Technology provides demonstration programs that exercise the primary functions of the file system. With the demonstration program and a complete set of documentation, building a system with MS-DOS-compatible off-line storage facilities is simple and straight forward. Standard device drivers are available for floppy disks, IDE hard drives, and SCSI devices. PCMCIA support also is available for ATA compatible drives.

Accelerated Technology
INCORPORATED

Nucleus GRAFIX
Portable Graphical User Interface

Features

- First portable Graphical User Interface (GUI)
- Scalable development across multiple CPUs
- Full use of Windows features
- Pull-down menus, dialog boxes, radio buttons, scroll windows, icons, file views, and more
- Understands PCX and BMP file formats
- Other capabilities being developed for GIF, JPEG, and TIFF formats
- Accessible with Microsoft AppStudio™

NEC CPUs Supported

VR4111, other on request

Host Platforms Supported

PC

Product Overview

In designing Nucleus GRAFIX, our goal was to create a GUI with the features that everyone needs. Other than portability, Nucleus GRAFIX includes pull-down menus, dialog boxes, radio buttons, scroll windows, icons, file views, and much more. Not only are these features powerful, but also they're exceptionally fast. That's why we especially have designed our software to combine multitasking technology with a detailed understanding of graphics hardware and how its capability can be harnessed.

Nucleus GRAFIX is highly portable due to its intelligently engineered and layered modules. We can take advantage of the varying capabilities of graphics devices so the processor can be relieved of computer-intensive tasks whenever possible. Nucleus GRAFIX is proven, its design is sound, and it provides all of the features you would expect from a full-featured windowing package. By combining the portability of Nucleus GRAFIX with the capabilities of Nucleus EDE, you can develop your GUI using the best tools available.

Nucleus EDE gives you an integrated environment and access to Microsoft AppStudio™ where you can design your GUI. It will produce an "RC" script that contains all the components you need to build a GUI for your target. The "RC" file is read and converted to a C source file that can be compiled and linked with your Nucleus GRAFIX application and executed on your target.

Nucleus GRAFIX supplies a full set of features for associating input to windows. When the mouse is clicked or dragged, or a key is pressed, the action is associated with a window so that your application is informed.

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SDE-MIPS 3.0: embedded toolkit for 32- and 64-bit MIPS

Features

- Comprehensive: all the software you need to use C and C++, even on a "bare" target. Source level "visual" debug, libc/libm, timing, profiling, soft floating-point and FP emulation. Ready-to-build sources for favourite eval boards include a simple ROM.
- A toolkit from a MIPS specialist: adds vital MIPS folklore and runtime, as well as bug-fixes and enhancements to the whole toolchain
- Fast, compact code generation, on level terms with the respected, but Unix-targeted, SGI/MIPS compiler
- 64-bit & MIPS IV support: use 64-bit power, access to 64-bit speed without requiring to re-write whole system
- Affordable:£ 1200/$2000 for a single-seat license including 12 months support and upgrades, with substantial per-seat discounts for larger sites. No-quibble money back guarantee
- Reliable and easy to port to: *gcc* is refreshingly free from bugs and surprises
- Up to date: library functions conform to ANSI and POSIX standards. The default object format is SGI-compatible ELF/ stabs (DWARF option), with ECOFF interlinking.

NEC CPUs Supported

All VR-series CPUs, including VR41xx, VR43xx, VR54xx, VR5000

Host Platforms Supported

PC: Windows 95/NT, Sun Sparc, Linux/x86

Target Systems Supported

SDE-MIPS supports all MIPS CPU variants and a large range of manufacturer-supplied evaluation boards. In particular, of course, it supports Algorithmics' own P-4032 and P-5064 prototyping boards.

Product Overview

All current MIPS CPU types supported: from 32-bit "MIPS I" to 64-bit "MIPS V" with MIPS16 and "MDMX" operations too, we support every MIPS CPU in production and every major feature set. The compiler exploits floating point and integer multiply-add instructions where available.

- 64-bit extensions: many MIPS CPUs are 64-bit machines which are 32-bit compatible. 64-bit pointers are rarely useful outside big Unix systems, but using 64-bit data can be worthwhile. SDE-MIPS generates 64-bit instructions for "long long" data, while keeping a valuable degree of compatibility with the 32-bit calling convention.
- Assembler: built for MIPS/SGI compatibility, accepts legacy sources. Accurate pipeline hazard detection, hides branch and load delays if you want it to.
- Object code: SDE-MIPS has always use ELF. The default "stabs" debug format provides source level C++ debug, but DWARF 1.1 is a fully-supported option for C.
- Conversion tools to common download formats, with sources of the conversion tool in case you need to adapt it.
- Debugger: the gdb debugger provides symbolic, source-level debug of programs on the target machine in conjunction with a simple target monitor. tkgdb adds a visual multi-window front end. Connect your target via serial port or ethernet. There's a target machine "monitor" you can link with your program, but SDE-MIPS also works with the PMON PROM monitor, or IDT's IDT/sim. Facilities extend to debugging multiple threads, single-step through ROM, break-points in flash, interruption of execution from the host, and integration with a custom I/O system.
- Debug/edit environment: at last, Windows programmers get a decent visual debugger. It works on Unix too, but we still recommend Unix-hosted programmers to learn GNU Emacs and run the debugger from an editor window; with Emacs, you're three years ahead of the best commercial "IDE".
- Profiling: The gprof profiler uses information collected by the SDE-MIPS run-time system during the actual execution of your program.
- Libraries: the package includes full POSIX- and ANSI-compliant "C" and "maths" libraries, with no license restrictions. The C library is reentrant and thread-safe.

algorithmics

◆ Floating point support: the compiler will generate MIPS FPA instructions or calls to emulation subroutines at choice. We include an IEEE754-compliant FPA instruction emulator - essential for non-trivial floating point on a MIPS CPU.
◆ Embedded system kit: a collection of sources and library functions (including power-on initialisation and cache/TLB functions); you need only write target-specific initialisation and UART "putc/getc" functions to get simple programs up and running on a new target. We bundle device code for evaluation boards as we meet them. We currently support about 20 boards - from semiconductor and support chip vendors, as well as Algorithmics' own.
◆ Example programs: we provide a selection of complete example programs, from "hello world", to complex exception handlers. Each will build straight out of the box into a running program on any supported target.
◆ C++: now works properly, including source level debug.
Slightly less perfect but useful features include a simple software emulator for some CPUs, allowing users to test low-level software before the hardware exists.

Coming in v3.x (1998 sometime)

Big advances in the underlying technologies in v3.0 means we expect to offer significant further advances with the next minor releases. In particular we hope to enhance profiling, adding basic-block counting and other relatively non-invasive compiled-in trace facilities. We'll be keen to support viable standards emerging from the MIPS EABI working group; and of course will continue to be among the first to ship a compiler for any new CPUs.

Other software from Algorithmics

◆ PMON monitor: this excellent, freely re-usable, PROM package runs on a variety of eval boards. Sources are available on our internet node, and we can help you get it ported to your hardware.
◆ AlgPOST generic power-on test suite: if you need power-on tests on your hardware, AlgPOST can save you a lot of time and trouble. Ask Algorithmics about license terms.
◆ OS packages: we develop OALs for Windows CE, and BSPs for popular real-time OS'. We have support for our own boards, and can license or develop code for your hardware.
◆ AlgRTX multithreading extension: builds on SDE-MIPS to provide a largely POSIX-compliant multitasking run-time system. AlgRTX is supplied in source form for a modest one-time fee with various support options.
◆ Support by experts: by internet email to "sde@algor.co.uk", or fax. Your query will be handled by experienced, working MIPS programmers. We'll let you ask existing customers how they feel about us.
◆ Online access: our internet node "www.algor.co.uk" contains printable SDE-MIPS documentation, and free sources such as PMON.

If it's GNU why isn't it free?

You're paying for support, installation, Algorithmics' own assembler; and most importantly, vital run-time code. All GNU-derived sources including our fixes and improvements are freely available. Our entry price is less than some GNU distributors will charge for one year's support. But if you and your organisation really can't afford our prices, let us know and we'll try to help out.

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AlgRTX: POSIX Threads Microkernel for MIPS Applications

Features

- Example-based kit: we provide a number of working mini-applications with complete source code you can build out of the box. These provide a model for "makefiles" and software building, worked examples of the use of the threads and interrupt API, and a set of basic tests for a new board support package
- Low-pain interrupts: interrupts may be handled with a natural extension to POSIX "conditions", avoiding all assembly-level programming and insulating your application completely from the MIPS architecture
- Toolkit integration: AlgRTX has grown up with SDE-MIPS, and builds on its unequalled GNU C compiler. Host/target communications can be via ethernet or serial port; the debugger is threads-aware
- Reference platform integration: Working AlgRTX implementations are available with Algorithmics' P-5064 and P-4032 reference platforms; between them these allow you to prototype with a very wide range of MIPS CPUs, including NEC VR43x0, VR54xx, VR5000

NEC CPUs Supported

VR41xx, VR43xx, VR54xx, VR5000

Host Platforms Supported

PC: Windows 95/NT, Sun Sparc, Linux/x86

Target Systems Supported

SDE-MIPS supports all MIPS CPU variants and a large range of manufacturer-supplied evaluation boards. In particular, of course, it supports Algorithmics' own P-4032 and P-5064 prototyping boards.

Product Overview

AlgRTX is a multithreading run-time system for any MIPS RISC target, available as an extension to Algorithmics' SDE-MIPS compiler toolkit. The POSIX "Threads" standard (IEEE standard 1003.1c) represents a brave attempt to write a generic API for multitasking applications, and presents an opportunity for customers who don't want to buy into a complete operating system to achieve a useful measure of code portability. AlgRTX is not a substitute for a full-blown real-time OS - if you need task/task protection, virtual memory or a third-party software market you should look elsewhere. But if you considered a do-it-yourself scheduler and other RTOS vendors want you to buy more than suits you, read on. AlgRTX provides a good working multithreading implementation optimised to the MIPS architecture.

- POSIX for portability: this is not the only OS component you'll ever need, so adherence to a widely respected API protects your software investment. With AlgRTX you need write no assembler code at all, and your application will be highly architecture- independent
- Good quality scheduler: OS theory and practice have come quite a long way in the last few years, leaving many older systems trapped in a dilemma between compatibility and modernisation. With no history to carry, AlgRTX can offer a well-mannered modern scheduler with features like priority inheritance
- No per-target or per-project royalties: your one-time payment gets you source code and an unfettered right to redeploy it - no per- project licenses
- Supportable and maintainable: AlgRTX source code is clean and well- written, and you are welcome to support it yourself. But we want to make money on support and upgrade services, and to do that we'll provide the same standard of support as we do for SDE-MIPS
- Transputer customers: the first reason we invented AlgRTX was so we could build special-purpose environments. One of those emulates the de-facto C-language scheduler API used by many Transputer applications, where the scheduler was built into the CPU microcode; using our library you can port your software from Transputer onto a modern, faster CPU without an extensive re-write
- From a MIPS specialist: Algorithmics know MIPS like nobody else. Multi-platform OS specialists can't equal our in-depth knowledge, or provide quite such good support. You also benefit from integration with our GNU-based toolkit and excellent reference boards.

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Drivers and BSPs

The AlgRTX kernel needs a timer and an interrupt controller. Most MIPS CPUs have a suitable interval timer, and have simple building- blocks for interrupt functions; but most workable systems will need an external interrupt controller of some kind. Apart from any interrupt connection, drivers are no more special to the kernel than any other software module - though if you're using POSIX threads you'll probably be looking for a POSIX-style generalised file system interface to drivers. SDE-MIPS kit drivers are suitable, are typically available for at least serial port and ethernet on supported boards. Creating a basic support package for a new board is equivalent to the process for SDE-MIPS, which is described in its excellent user manual.

Customisation

AlgRTX can be extended to your requirements; we'll consider doing that at low cost where we expect to be able to re-use the code.

What's Next?

There are two extensions we definitely intend to build into AlgRTX over the next months; any customer buying support can rely on obtaining:

- Ultra-fast low-level interrupt handlers: one underused virtue of MIPS CPUs is their very low inherent interrupt latency - in a RISC CPU, the hardware does very little interrupt processing and takes almost no time about it. Sub-s interrupt response time is quite realistic; but not if your OS is always going around disabling interrupts. AlgRTX already uses some special MIPS tricks - the "load linked/store conditional" instructions - to implement semaphores without disabling interrupts. To allow users to take advantage of that we're adding the facility to invoke simple assembler-language interrupt routines directly from the interrupt vector, and with minimum OS overhead, and providing them with a way to signal higher-level software events when necessary.
- TCP/IP stack: everyone offers this; since we already bundle some of it to provide debug communications for PMON, we're porting the whole BSD4.4 stack with its "sockets" interface to AlgRTX.

More about POSIX Threads

The IEEE's "Portable Application Standards Committee" (PASC) look after the 1003.1c "threads" standard. Several good books are available about programming to this interface (though we don't imply that their authors endorse our software!). You may like to look at:

- Kleiman, Shah & Smaalders: Programming With Threads (from Amazon) (published Prentice Hall), ISBN 0131723898. This book has been around for a while and has been our guiding light during implementation, but the next two are newer.
- David Butenhof: Programming With Posix Threads (from Amazon) (published Addison-Wesley).
- Lewis & Berg: Multithreaded Programming With Pthreads (from Amazon) (published Prentice Hall), ISBN 0136807291.

AlgRTX vs other OS'

Here's our summary of how we stand up against some well-known alternatives:

- Windows CE: is new, but has immense potential in creating an RTOS backed up by a huge mass of vertical-application software from Microsoft, and a thriving third-party software market. Windows CE is not very real-time, and has a pretty large footprint; but those are big virtues and Algorithmics are signed up as Systems Integrators.
- Linux: is in many ways the ideal OS for applications which are not real-time, but want to build software for a unix-like system and take advantage of the biggest pool of high-quality free software.
- Tornado/VxWorks: extensive tools, a simple run-time system and a fair amount of run-time software make up Wind River's offering. Its big virtue is that the low-level and relatively small run-time does give you genuine portability across different CPU architectures. "Traditional RTOS" vendors do take away some portability headaches - but of course you have to pay them to do that.

The closest things to AlgRTX are source-code-supplied RTOS' like Accelerated Technologies' "Nucleus". The difference here is down to customer preference, and perhaps our MIPS orientation.

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CodeTEST® Embedded Software Test and Analysis Tools

A Member of the CodeOPTIX™ Family of Embedded Software Visibility Tools

Features

◆ Performance Analysis
- Measures function and task execution times
- Counts call-pair linkages to identify thrashing
- Non-sampled measurements of 32,000 functions at one time

◆ Coverage Analysis
- Displays coverage at program, function, or source levels
- Plots coverage over time
- Completely interactive measurements simplify test creation and refinement

◆ Memory Allocation Analysis
- Dynamic display shows memory leaks in progress before the system crashes
- Pinpoints memory allocation and free errors to offending source line
- Measures true worse case allocation

◆ Trace Analysis
- Traces embedded programs at source, control-flow, or high level
- Deep trace captures over 100 thousand source lines of execution
- Powerful triggering and trace display options zero in on problems
- Designed for software engineers

NEC CPUs Supported

Call for supported processors

Host Platforms Supported

PC: Windows 95/98/NT

Product Overview

Designed especially for embedded developers, the CodeOPTIX family of test and analysis tools includes three NEW CodeTEST products: CodeTEST Native™, CodeTEST Software-In-Circuit™, and CodeTEST Hardware-In-Circuit™. Each represents a different phase in the embedded software development lifecycle: development, debugging, and testing.

CodeTEST Visibility Modules

Trace Analysis provides an unmatched depth of software execution trace, in three levels of detail, for processors with or without internal caches.

Performance Analysis boosts productivity by providing accurate visibility of code performance, making verification and performance problem area identification straightforward.

Memory Analysis saves time and money by proactively watching the memory usage of your application, often revealing memory leaks and other memory errors in embedded code.

Coverage Analysis improves product quality through identifying high-risk areas of code by showing exactly what functions, blocks, or statements have, or have not been executed.

Advanced Coverage Tools (ACT) qualify for the highest of regulated test standards (such as RTCA/DO-178B, Level A) for measuring and documenting statement coverage (SC), decision coverage (DC), and modified condition decision coverage (MCDC).

CodeTEST Hardware

Universal Probe provides a flexible hardware interface adaptable to a wide variety of target systems. Even under difficult space constraints the Universal Probe can connect to headers, busses, processors, and other devices.

CodeTEST-VME gives you a variety of selectable views of code behavior. Instead of “surfing” the VME backplane hunting for specific events with a bus analyzer, you can drill down and focus on individual processor code. Or move up to a higher level of abstraction and monitor System Level Trace to see the interactions among the various subsystem CPU board activities

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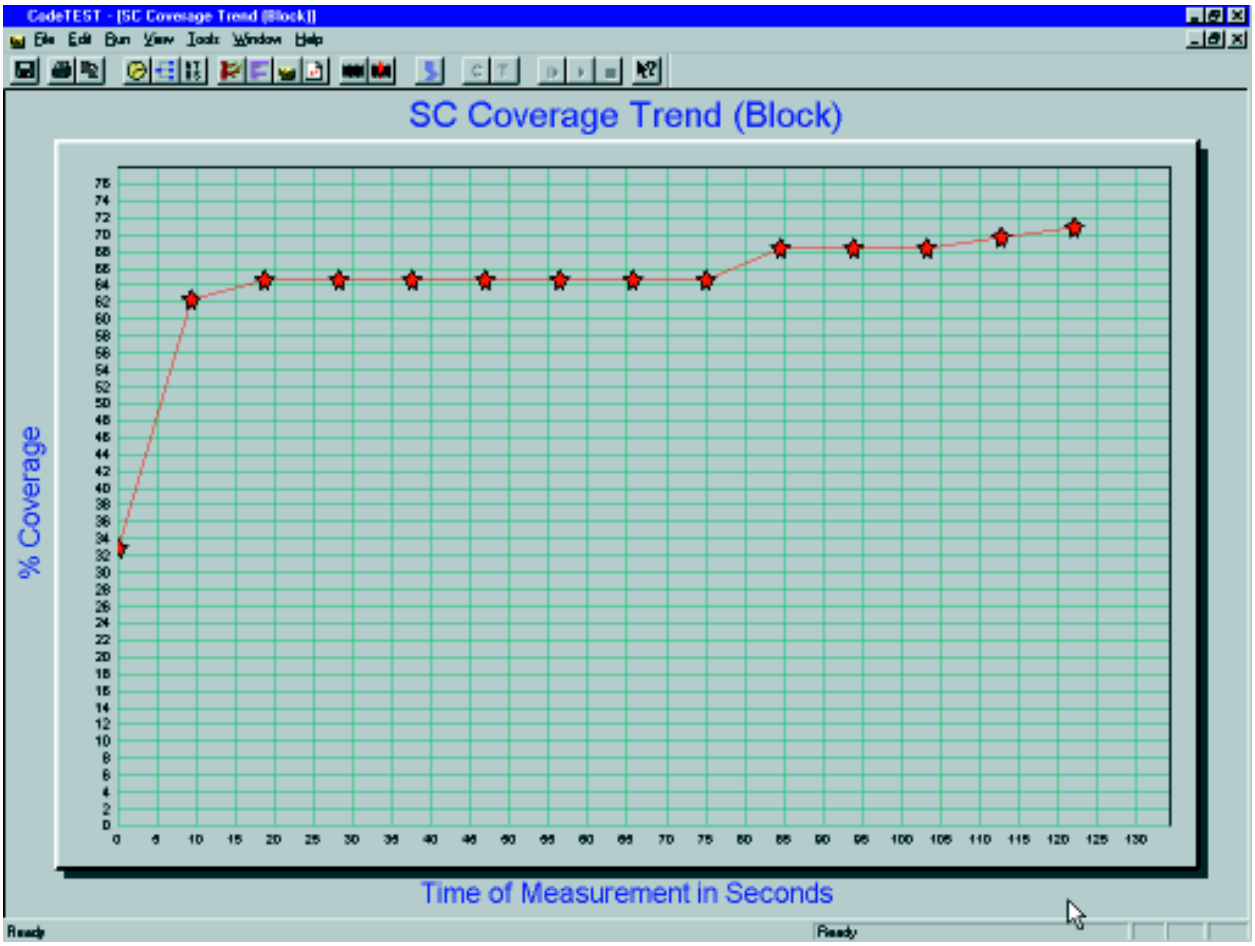
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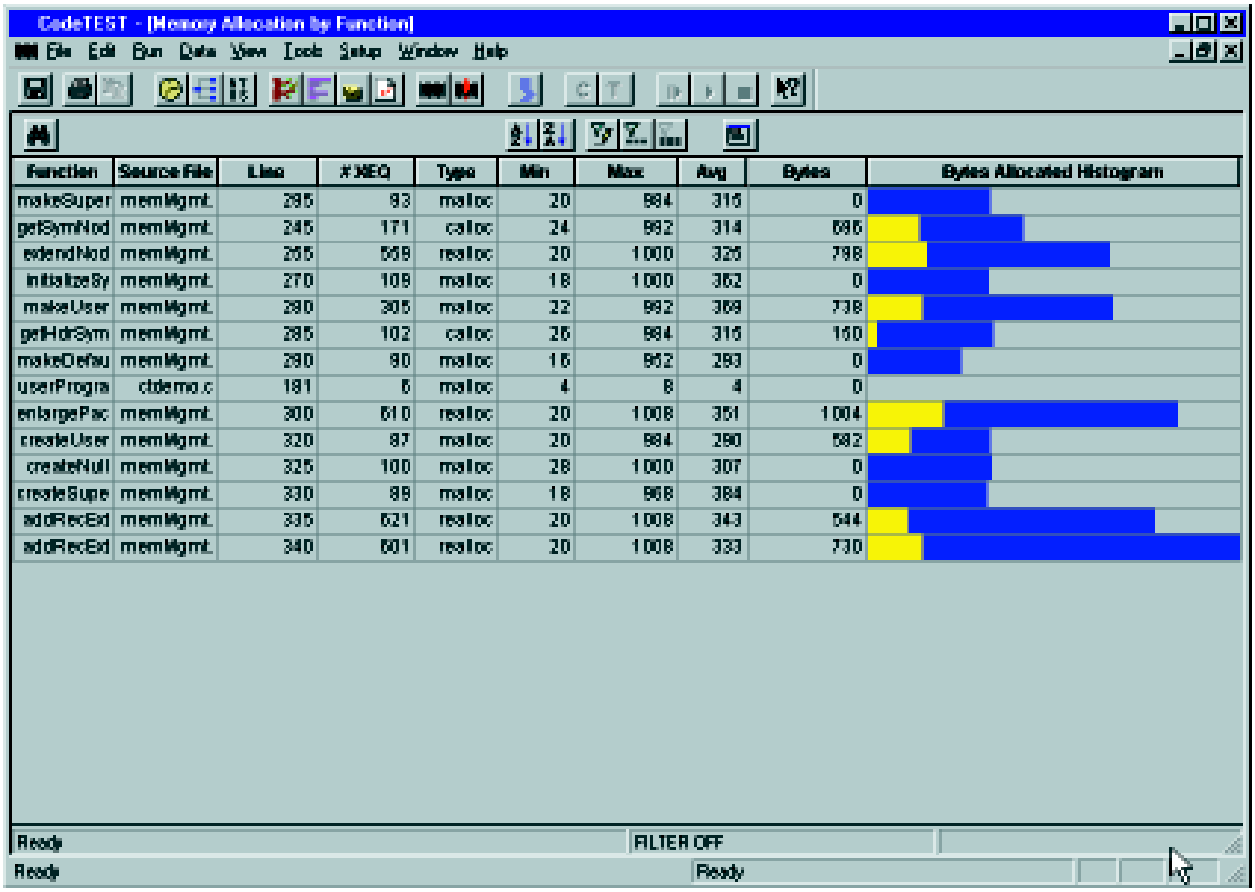
Ready
Ready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Function
Source File
Line
REQ
Type
Min
Max
Avg
Bytes
Bytes Allocated Histogram
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getSymNod memMgmt. 245 171 calloc 24 992 314 696
extendNod memMgmt. 255 559 realloc 20 1000 325 798
initializeSy memMgmt. 270 109 malloc 18 1000 362 0
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enlargePac memMgmt. 300 610 realloc 20 1008 351 1004
createUser memMgmt. 320 87 malloc 20 984 290 582
createNull memMgmt. 325 100 malloc 28 1000 307 0
createSupe memMgmt. 330 99 malloc 18 968 384 0
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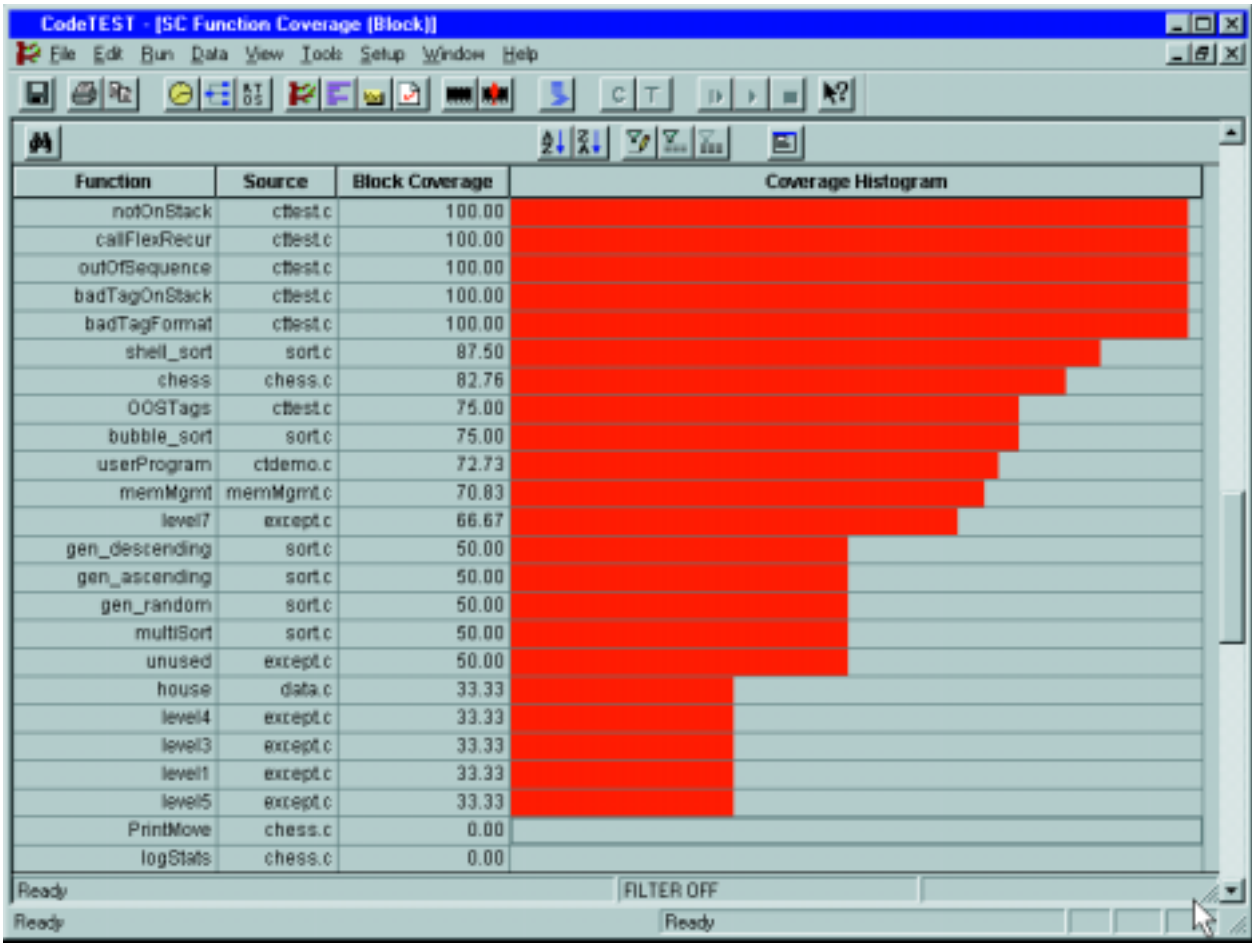

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Carole Griffiths

NetROM

Features

◆ Target Communication
- High-speed Ethernet connection between target and host
- Rapid code download over Ethernet using standard protocols such as TFTP and TCP
- Four dual-port memory channels provide four LAN channels for multiple user sessions with NetROM or the target

◆ Target Control
- Eight user-asserted target command signals
- Eight status signals from the target that can be polled at will

◆ Memory Emulation
- Offers emulation memory of 1 or 4 MB
- Supports 8-, 16-, and 32-bit words
- Support for 64-bit words and over 4 MB emulation memory through multiple NetROM units
- Automatically supports both 5 V and 3.3 V memory devices

◆ Debugger Integration
- Integrated with industry-leading source-level debuggers
- Supports task-aware and system-level debugging
- Provides writeable memory for breakpoints in ROM space

◆ Cost-Effectiveness
- Reusable tool lowers development and debugging costs

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

PC: Windows 95/98/NT

Product Overview

NetROM™ is a revolutionary product for embedded software developers. It provides a flexible debugging platform that combines high-speed target communication and debugging capabilties. NetROM requires almost no target resources and can be rapidly moved from project to project and from processor to processor.

NetROM supports a variety of debuggers and monitors from vendors including GreenHills, Integrated Systems Inc., Microtec Research, Microware, Software Development Systems, and WindRiver.

Linking your preferred debugger and target monitor, NetROM accelerates the development cycle through faster downloads and target communications, remote target control, and emulation of ROM memory devices. Using NetROM, developers can realize download and debug communications gains of approximately 20%. NetROM accomplishes this improvement by:
- Adding network connectivity to your target without requiring Ethernet hardware or software on the target;
- Eliminating the need to burn EPROMs or program FLASH devices;
- Replacing slow serial downloads with fast Ethernet downloads;
- Allowing target debugging to occur from any network host rather than a dedicated workstation;
- Reducing the time-penalty for software debug experiments.

NetROM offers emulation memory of 1 or 4 MB; supports 8-, 16-, 32-, and 64-bit words; and over 4 MB emulation memory through multiple NetROM units. Also automatically supports both 5 V and 3.3 V memory devices.

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DIAB-SDS

Optimizing C, C++, Java™ Compilers, Run-Time Analysis Tools, and SingleStep Debug Solutions

Features

- Highly optimizing compiler suites for C, C++, and Java™
- Fast, compact, high quality code for NEC MIPS CPUs
- Application specific (profile-driven) optimizations for increased performance
- Run-Time Analysis tools, including Run-Time Error Checker and Profiler, for improved code quality, performance, memory usage
- FastJ™ compiles Java to native machine code for applications without a JVM
- Powerful SingleStep GUI debugger for advanced C, C++, Java and ASM debugging
- Task/kernel aware debug
- Exceptional flexibility and reliability for embedded applications
- Proven with leading RTOS and kernel packages

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

Windows 95/98/NT, Solaris, HP/UX

Target Connections Supported

Simulators, ROM monitors, OCD/JTAG, HP logic analysis systems

Product Overview

DIAB-SDS is the embedded development tools leader and is widely known for its highly-optimizing compilers, award-winning Run-Time Analysis tools, and powerful SingleStep debug solutions. DIAB-SDS is a wholly owned, independent operating subsidiary of ISI.

Highly Optimizing Compilers

DIAB-SDS compiler suites are the expert's choice for demanding NEC MIPS-based designs. DIAB-SDS compilers feature the industry's most advanced compiler optimization techniques and offer superior performance, flexibility, and reliability. In addition to providing robust, standards compliant compilers for C, C++, and Java, DIAB-SDS tools offer many features specific to embedded development. These features include: generating ROMable code and data; ability to mix assembler with C/C++, and Java code; ROMable reentrant code and libraries; options to pack or byte swap structures to match existing data types; and complete control of code and data memory allocation and placement. For developers who want to program in Java but cannot afford the performance and size costs of a JVM, DIAB-SDS offers the FastJ compiler suite. FastJ compiles Java source code directly to native machine code and offers code size and performance comparable to C++. FastJ also supports mixed language programming so you can mix native C and ASM code with Java code. The SingleStep debugger features Java-specific capabilities that allow you to debug Java and mixed language applications. FastJ interfaces to an RTOS using Pthreads calls (a subset of POSIX). Check with DIAB-SDS to see if your RTOS/kernel is supported.

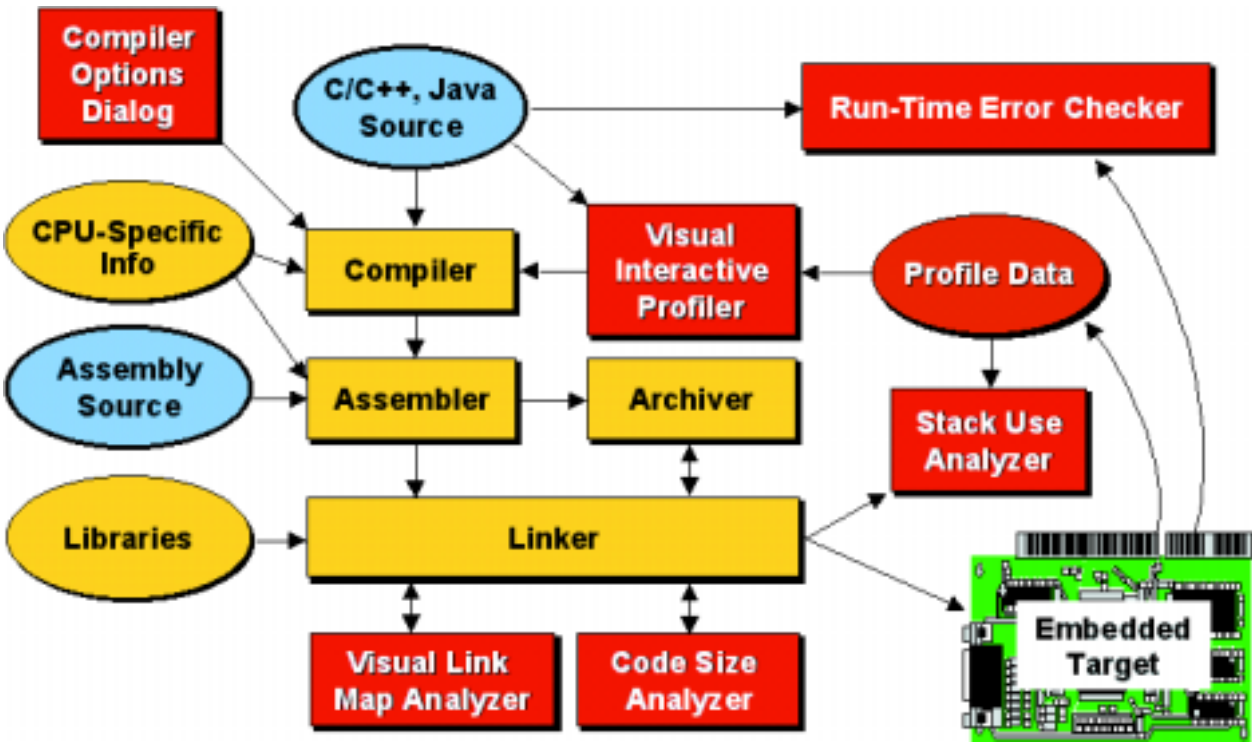
Run-Time Analysis (RTA) Tools

DIAB-SDS award-winning RTA Suite provides an integrated set of Run-Time Analysis tools to help you develop higher quality, higher performance code in less time. The RTA Suite includes a powerful Run-Time Error Checker, Visual Interactive Profiler, Stack Use Analyzer, Visual Link Map Analyzer, Code Size Analyzer and other tools to help you improve program reliability, performance and memory usage. In particular, the Run-Time Error Checker detects hard-to-find pointer errors and memory leaks while the profiler identifies true program hot spots for optimization purposes. DIAB-SDS compilers can also generate application specific optimizations based on run-time profile data.

diab·sds
An ISI Company
The Embedded Tools Leader

SingleStep Debug Solutions
The SingleStep debugger is a powerful debug environment for embedded development. Graphical source-level and assembler-level debug features are combined with a wide array of tools to provide a rich environment for debugging and developing NEC MIPS-based designs. Target connections include simulators, ROM-Monitors (PMON), OCD/JTAG connections, and logic analysis solutions to provide a complete range of debugging capabilities.
SingleStep also features advanced RTOS/kernel aware debug capabilities. These features allow you to debug applications in the context of your RTOS or kernel. Several leading RTOS packages are supported, including ISI pSOSystem, ATI Nucleus PLUS, Enea OSE, and others.

DIAB-SDS tools are available integrated with ISI's pRISM+ development environment and with other third party tools offerings. Contact your DIAB-SDS representative for more information.



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Model CCES-MIPS Software Cross Development Tools

Features

- Complete Development Tool Kit
- C/C++ compiler generates high performance code
- Fast, flexible, locating linker handles large files, arbitrarily named sections
- Source-level debug for ICE, JTAG emulators, target resident debug kernel, and instruction-set simulator
- Fast Instruction Set Simulator
- Sample processor initialization and exception handler code
- Fast floating point emulation library
- Automatic ROM image building

NEC CPUs Supported

VR4300, VR4310, VR5000, VR5432

Host Platforms Supported

Sun-4: SunOS, Solaris
PC: Windows 95/NT
HP 9000: HP-UX

Product Overview

The CCE-MIPS Software Tool kit offers a complete solution to developers using any of NEC R4000/5000 based RISC processors. The tool kit consists of tightly integrated programs to generate code and to debug your embedded application.
The tool kit includes an optimizing C/C++ compiler, a macro assembler, a locating linker, a librarian, a C source-level debugger, a symbolic assembly level debugger, an instruction set simulator, and RSS. RSS is a small powerful target resident debug kernel. In-circuit emulators from EPI are fully compatible with the code generated by this tool kit and with the debuggers provided.

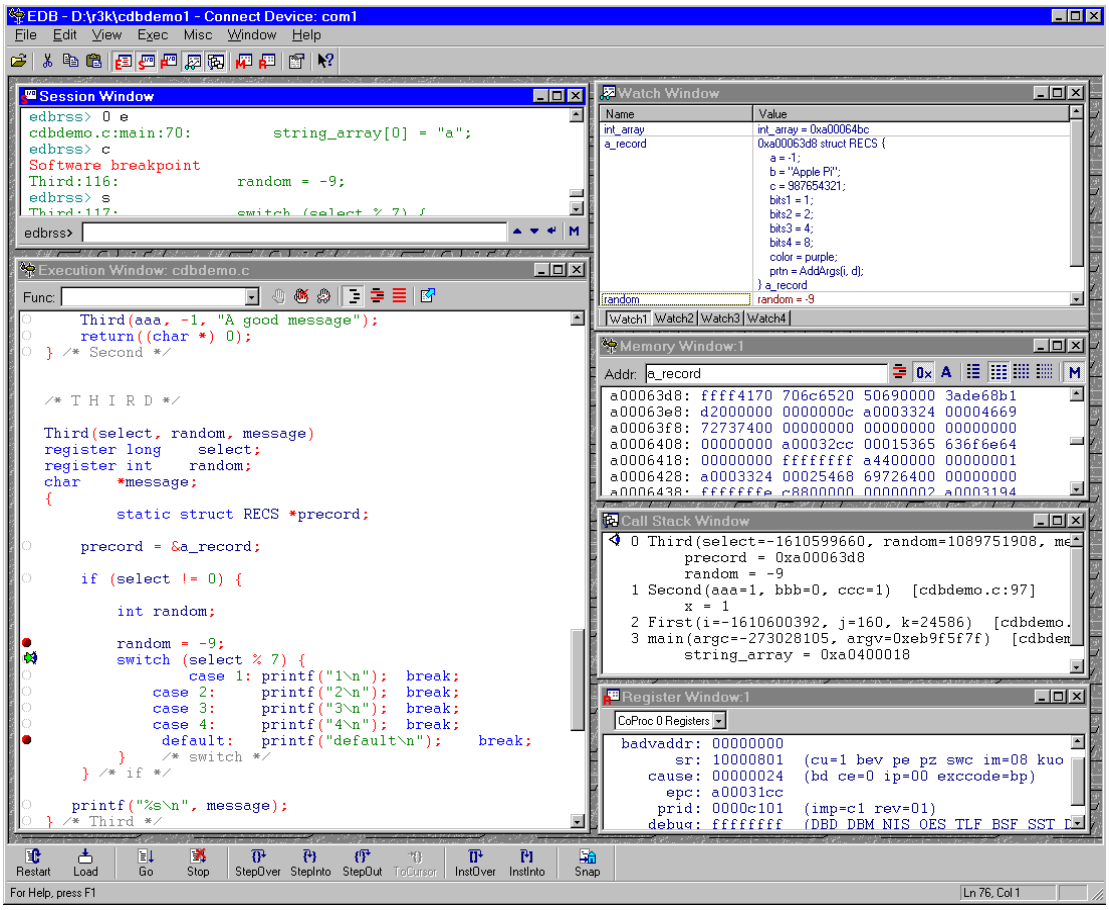
Compiler
The EPI compiler is a globally optimizing C/C++ cross-compiler that supports MIPS R3000, R4000, and R5000 processor variants. The compiler generates quality code tuned to these processors using the most effective optimization techniques available.

Assembler
The EPI assembler is fully compatible with the language requirements of the MIPS assembler. And adds built-in macro and conditional assembly capability.

Linker
The EPI linker handles very large applications quickly while making efficient use of memory. It offers full control over the placement of code and data sections. In addition to handling multiple text and data sections will generate ROM images complete with code to copy instructions and initialized data into RAM.

Debugger
EDB is an exceptional source level debugger for C. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window.
“Point and click” entry of common commands gives fast, flexible control over the behavior of your application. EDB also accepts a rich set of command line directives.
EDB displays variables in their declared type. It displays C structures in the same format you might code them yet allows custom formatting.
The debugger is compatible with the RSS target resident debug kernel, with the ISS instruction-set simulator, with the SYS4K in-circuit emulator, and with MAJIC EJTAG emulator.

Instruction Set Simulator
ISS is a feature-rich simulator and is highly configurable at run time. Every run of the simulator may be different, and as your requirements change you may enable and disable features as needed for a particular run, thus gaining the benefit of reduced simulation time.



Example of EDB Source-level Debugger Display

Target-Resident Debug Kernel

RSS is a target resident kernel that communicates with the EPI debuggers through a serial interface. Easily configured to your target board, it turns your product into a low cost and highly capable software debug station.

Utilities

The CCE-MIPS software tool kit includes an array of utilities to streamline the task of software development for embedded RISC applications.

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Model ISS-MIPS
Instruction Set Simulator

Features

- Low cost, source level debug environment
- High speed simulation
- Cache simulation with breakpoints
- TLB simulation
- User selectable simulation features
- Supports MIPS ISA I, II, III, IV

NEC CPUs Supported

VR43xx, VR5432

Host Platforms Supported

Sun-4: SunOS, Solaris
PC: Windows 95/98/NT

Product Overview

EPI's instruction set simulator, ISS, runs on personal computers as easily as on UNIX workstations, and simulates big- and little-endian targets. ISS is a feature-rich simulator and is highly configurable at run time. Every run of the simulator may be different, and as your require-ments change you may enable and disable features as needed for a particular run, thus gaining the benefit of reduced simulation time.
The ISS memory model includes tag bits for each memory location. These are used to maintain information about which locations have been accessed and how. They are also used for setting breakpoints. Breakpoints may be set on instruction fetch, read, or write cycles, or any combination of the above.

Simulation Advantages

For embedded applications, there are a number of problems that arise for which ISS is ideally suited.
Nested exceptions: Your application must be able to handle nested interrupts and interrupt service routines properly. It is nearly impossible to produce the test conditions needed to evaluate proper interrupt processing in any other environment but simulation. With ISS, you can cause exceptions to occur on demand, allowing you to test all the possibilities.
Stack usage: With ISS, you can monitor system memory usage and see how deep memory allocation stacks actually get at run time. Making the most efficient use of often limited resource in your embedded system.
Quality Validation: With ISS, it is a simple matter to tag all locations that were executed. After a test run, you can then examine the results and see if you have achieved the desired code coverage This ensures that all the code has been exercised and prevents untested code from being executed for the first time "in the field."
Performance analysis: ISS lets you tune your application for performance and get immediate feedback as to how many hits and misses occurred in both instruction and data caches. Take advantage of on-chip cache and achieve significant performance improvements by properly tuning how the code is allocated at link time.
Trace: With ISS you can use the built-in trace capability to solve "How did I get here?" problems when debugging embedded system software. Trace data may be collected to a file for post-run analysis, or collected in a buffer for immediate viewing. The trace data is annotated with register contents for all instructions that use register operands as well as symbolic and source information.
Another powerful feature is cache simulation. While some simulators do not even model cache, ISS accurately reflects the behavior of the actual cache systems.
The behavior of on-chip memory management, for those processors that include such facilities, is also modeled. This simulation supports mapping of virtual to physical addresses, and because it also indicates whether a mapped physical address is cached or uncached, the me-mory model and cache model are tightly integrated.

Debuggers

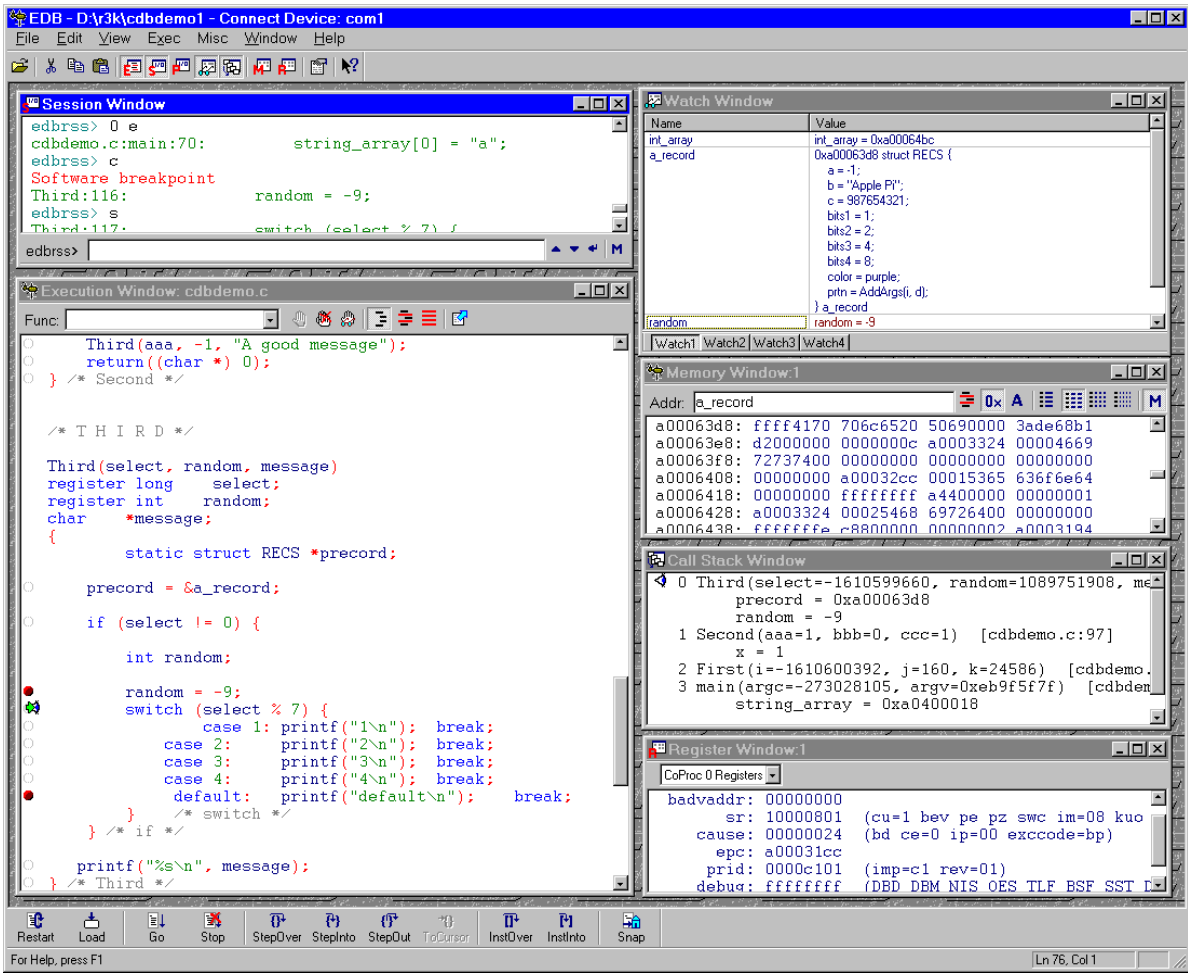
There are two debuggers that communicate with RSS. Both debuggers utilize the host computer to manage the user interface, symbol tables, file systems, etc. The RSS-MIPS serves as a target resident server kernel for the debuggers. These debuggers work with the RSS-MIPS target resident debug kernel to provide very low cost debug stations. The same debuggers work with the EPI Instruction Set Simulator and the In-Circuit Emulators for those more difficult debugging situations.

Symbolic Assembly Level Debugger

MON, a symbolic assembly-level debugger, offers features especially useful to hardware engineers for prototype debug, automated testing, and manufacturing test. It is source-language independent making it equally useful debugging code written in assembly, C, ADA, or other language.

Source Level Debugger

EDB is an exceptional source level debugger for C/C++. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window. EDB also accepts a rich set of command line directives while “Point and click” entry of common commands gives fast, flexible control over the behavior of your application. EDB displays variables in their declared type. It displays C structures in the same format you might code them yet allows custom formatting.



Example of EDB Source-level Debugger Display

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Model RSS-MIPS Target Resident Debug Kernel

Features

- Low cost, source level debug environment
- Fast binary communications interface
- Pre-configured ROMs for NEC evaluation boards
- High speed serial or optional ethernet communications driver
- Uses minimal target resources
- Callout interface for FLASH EPROM breakpoints
- Sample start-up and exception handler code

NEC CPUs Supported

VR4300, VR5432

Host Platforms Supported

Sun-4: SunOS 4.x, Solaris
PC: Windows 95/NT
HP 9000: HP-UX

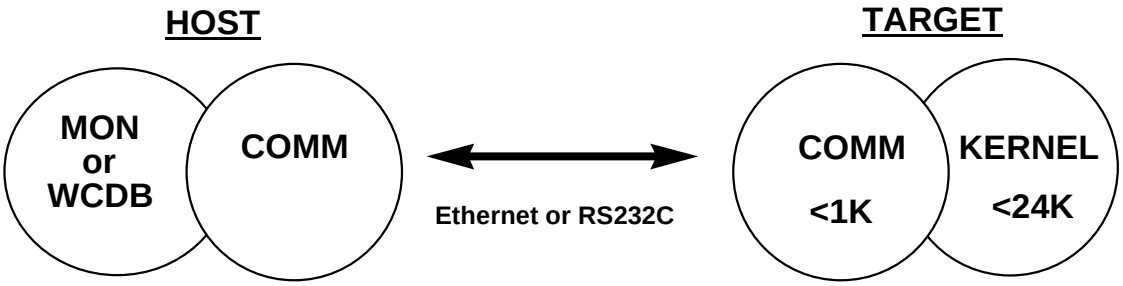
Product Overview

RSS is a target resident kernel which supports all NEC MIPS processors. It implements the functions that enable host-resident debuggers to download application programs, read and write memory and registers, set and clear software breakpoints and perform processor control, such as start and stop execution and single stepping.
RSS communicates with the host computer using a standardized packet protocol and can be configured for serial or Ethernet communications interface. The target resident portion of RSS is a debug “kernel” that is supplied in linkable object form. It is designed to use minimal target resources, needing only 25K bytes of memory, and is structured for easy porting to new target designs. Sample source code is provided for processor initialization and startup, exception handling and for the host communications interface. Binary ROM images for NEC evaluation boards are included.
RSS features a powerful background mode that allows you to interactively debug your application program while it is still running. This is especially important for real-time designs where stopping the processor invalidates a particular test.
Full source for RSS is available at low cost for customization purposes. The standard RSS product is licensed for unlimited use and production distribution for a single project. You can ship RSS embedded into your final product for field testing or remote debugging.
RSS turns your product into a low cost and highly capable software debug station.

Debuggers

There are two debuggers that communicate with RSS.
Both debuggers utilize the host computer to manage the user interface, symbol tables, file systems, etc. The RSS serves as a target resident server kernel for the debuggers.
These debuggers work with the RSS target resident debug kernel to provide very low cost debug stations. The same debuggers work with the EPI Instruction Set Simulator and the In-Circuit Emulators for those more difficult debugging situations.

Target Resident Debug Kernel



Source-Level Debugger
EDB is an exceptional source level debugger for C. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window. “Point and click” entry of common commands gives fast, flexible control over the behavior of your application. EDB also accepts a rich set of command line directives.
EDB displays variables in their declared type. It displays C structures in the same format you might code them yet allows custom formatting. The debugger is also compatible with ISS, the instruction set simulator, and with EPI’s in-circuit emulators.

Symbolic Assembly-Level Debugger
MON-MIPS, a symbolic assembly-level debugger, offers features especially useful for testing board level resources, automated testing, and manufacturing test. It is source-language independent making it equally useful debugging code written in assembly, C, ADA, or other languages.

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Model EDB-MIPS Source Level Debugger

Features

- Windowing GUI user's interface
- Command line or mouse control
- Supports command files and command aliases
- Assembly level subsystem
- Hyperlink to align source display to traced data or memory windows
- Quality technical support
- Supports MIPS ISA I, II, III, IV

NEC CPUs Supported

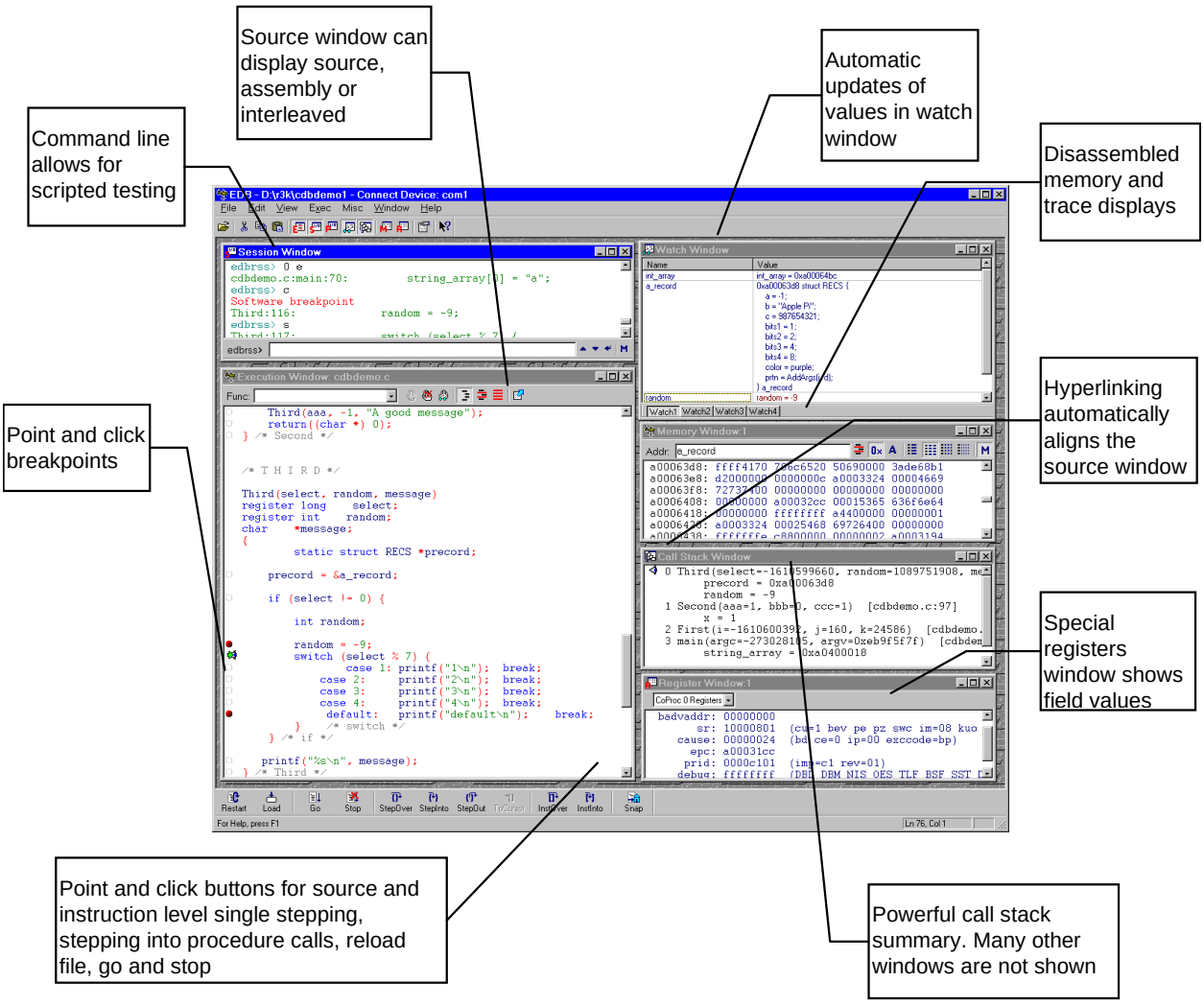
VR4300, VR4310, VR5000, VR5432

Host Platforms Supported

Sun-4: SunOS, Solaris
PC: Windows 95/NT
HP 9000: HP-UX

Product Overview

EDB is an exceptional windowed source-level debugger for C and assembly language programs. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window.
"Point and click" entry of common commands gives fast, flexible control over the behavior of your application. EDB also accepts a rich set of command line directives.
The value watch window can EDB displays variables in their declared type. It displays C structures in the same format you might code them yet allows custom formatting.
The debugger offers convenient windows to display the general registers and the coprocessor registers too.
The debugger provides a common user interface whether debugging using the ISS instruction-set simulator, the RSS target resident debug kernel, or the Models SYS4K or MAJIC emulators.



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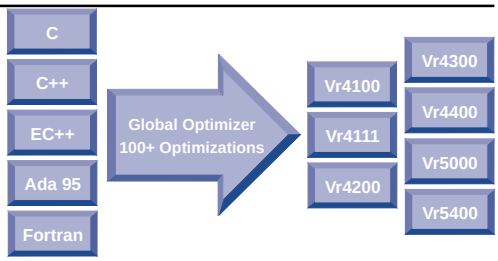
Green Hills™ Optimizing Compilers and MULTI® Development Environment



Features

- Additional Components are seamlessly integrated for enhanced functionality:
- Source-Level Debugger
- Program Builder
- Execution Profiler
- Class/Program Browser
- Version Control System
- Run-Time Error Checker
- Text Editor
- Includes Green Hills' Optimizing Compilers for C, C++/EC++, Ada 95, and FORTRAN
- Supports MIPS 16
- CodeBalance Optimizing Profiler
- User-friendly GUI
- A complete solution for both embedded and native development
- Supports UNIX and Windows 95/98/NT
- Contact us for a FREE demo CD!!

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

Windows 95/98/NT, SPARC/Solaris, PA-RISC/HP-UX

RTOSs Supported

ThreadX, VxWorks/Tornado, Nucleus PLUS, and Custom RTOSs

Target Systems Supported

Simulators, ROM Monitors, CPU Boards, In-Circuit Emulators, Processor Probes, OCD / BDM / JTAG

Green Hills
• SOFTWARE, INC. •

Product Overview

Green Hills Optimizing Compilers
Green Hills Software, the leading supplier of highly optimizing compilers for 32-/64-bit microprocessors, has been providing software tools for embedded development since 1982. Green Hills C, C++, EC++, Ada 95 and FORTRAN compilers generate fast, compact code for even your toughest applications.

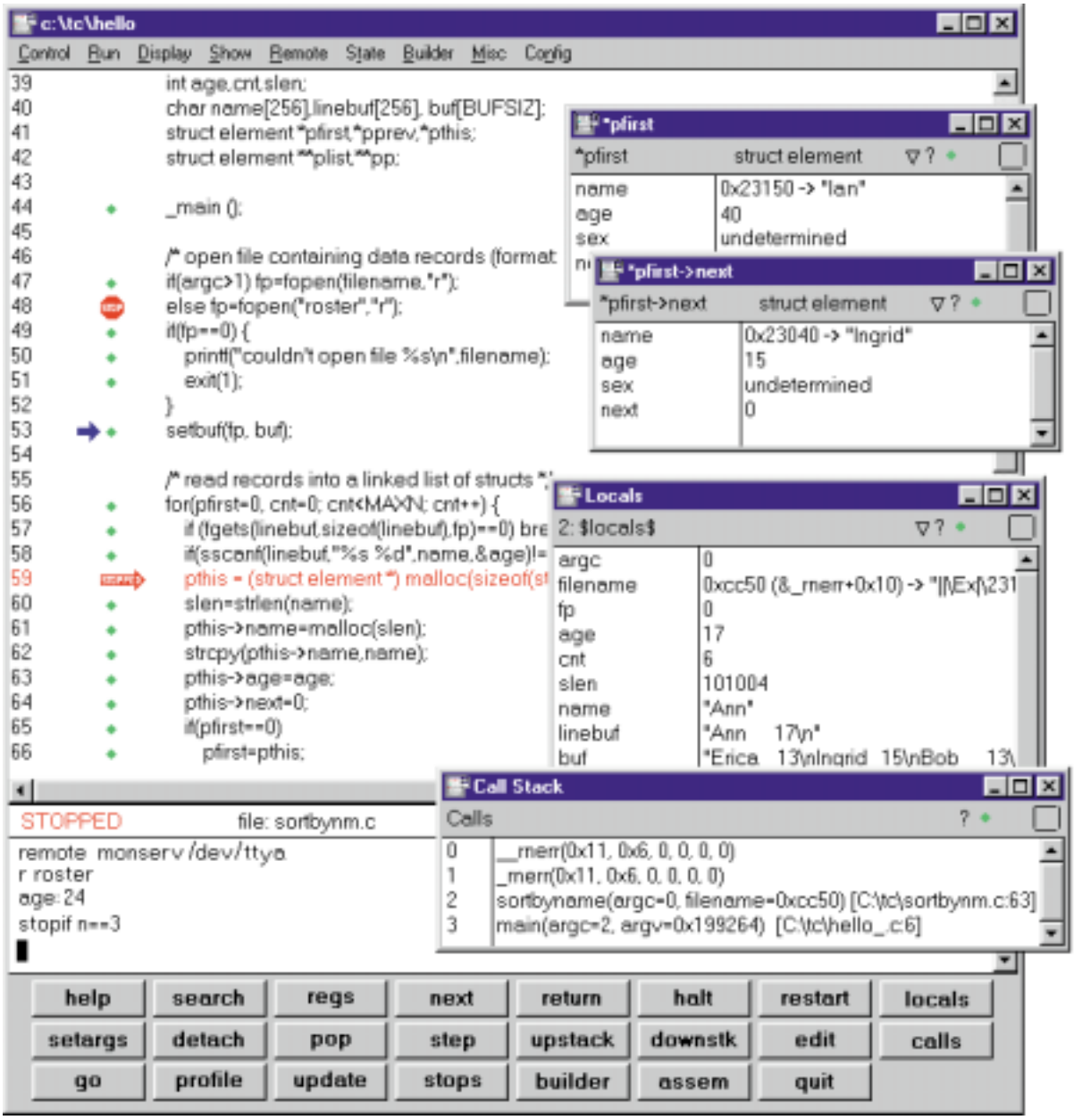
Mixed Language Programming
All five languages have compatible calling and linkage conventions, so you can mix code from multiple languages into a single executable. A two pass inliner allows functions defined in one module to be inlined into another, even if the inline code was written in a different language. Inlining can be performed either manually or automatically; automatic inlining uses built-in heuristics to determine which functions should be inlined.

Multiple sections allow you to place program, constants, variables and strings wherever required in memory. Object and debug formats include ELF/DWARF, COFF, BSD and more.

Powerful and Efficient IDE:
MULTI's components are seamlessly integrated allowing each component to communicate with the others as appropriate to provide a seamless integration throughout compilation, debugging, performance profiling, and version control. MULTI includes a project builder, source-level debugger, performance profiler, run-time error checking, graphical browser, text editor, and version control system. MULTI supports program development in C, C++, EC++, Ada 95, FORTRAN, and assembly language. Source code from these languages can be mixed together in almost any combination to create a single executable.

The MULTI Integrated Development Environment provides a direct graphical interface with all Green Hills Optimizing Compilers, and supports multi-language development and debugging. In addition, MULTI includes a powerful utility program called the CodeBalance™ Optimizing Profiler.

MIPS 16 Support:
CodeBalance enables the user to make critical performance/code-size trade-offs. By analyzing the performance profile on a function by function basis, CodeBalance performs recompilation in 16-bit mode starting with the functions that take the least amount of execution time. This achieves code-size reduction with minimal increase in execution time. This is an extremely powerful utility in developing high-performance MIPS 16-based applications, in particular.



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Microsoft® Windows® CE Platform Builder

Features

- Integrated Development Environment
- Platform SDK Export Generator
- Catalog based repositary of components
- Dynamically add/delete components to the platform
- Configures the whole system from core to complex WIndowsCE devices

NEC CPUs Supported

VR41xx, VR43xx,
(MIPS 16: VR4121A, VR4111A)

Host Platforms Supported

Windows NT/95/98, Windows CE

Product Overview

Platform Builder is the next-generation set of tools and APIs that enable you to develop the software for your next embedded system project using Windows CE. Platform Builder includes all of the components of the Windows CE operating system in binary form, along with sample code for NDIS and USB device drivers that make development easier.
Platform Builder includes eight pre-built configurations of the Windows CE operating system. These configurations range from only core kernel functionality to a complete system with a rich graphical user interface and preloaded applications.
The Integrated Development Environment (IDE) makes your embedded system development easier.
Configuring the Windows CE operating system for your custom device in Platform Builder is very similar to building an application in the Microsoft Visual Studio® development environment. The Platform Builder IDE, like the Visual Studio IDE, enables you to configure, build and debug your software all within this consistent environment.
The Platform Builder Export SDK feature allows you to create an SDK for your custom device.
Application developers can import your Software Development Kit (SDK) into the Windows CE Toolkit for Visual C++® or the Windows CE Toolkit for Visual Basic® and develop the application-level software for your platform. The SDK consists of the APIs, header files, etc., that comprise the operating system environment for your custom device.
The extensible “Catalog” allows you to easily incorporate third-party components into the Platform Builder IDE.
Platform Builder Catalog is a repository of Windows CE components. Using drag and drop you can add components from the catalog to your Platform. You can extend the catalog by adding your own components, or components developed by third parties.
Platform Builder enables you to target the processor families supported by Windows CE.

Microsoft®

For the latest list of supported processors, please visit:
http://www.microsoft.com/windowsce/embedded/resources/proc212.asp

For more information on Windows CE and Platform Builder, visit:
http://www.microsoft.com/windowsce/embedded

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Microsoft® Windows® CE Toolkit for Visual Basic®

Features

- Same development environment as known from traditional Windows based toolkit
- Visual Basic Form designer
- Direct access to Windows CE system functionality
- Full communication module support of Windows CE, like TCP/IP, infrared or serial port

NEC CPUs Supported

VR41xx, VR43xx,
(MIPS 16: VR4121A, VR4111A)

Host Platforms Supported

Windows NT/95/98, Windows CE

Product Overview

To help you take advantage of new business opportunities, Microsoft has created the Windows CE Toolkit for Visual Basic 6.0. This toolkit, which integrates with the Microsoft Visual Basic 6.0 development environment, is the most productive way to build applications for Windows CE-based devices. It supports familiar Visual Basic features, including visual design and IntelliSense® technology, making it easy to apply your knowledge of Visual Basic to Windows CE-based devices.
Familiar environment gets you up and running fast
* Use your existing knowledge and training to quickly create Windows CE-based solutions within the same development environment you use for traditional Windows-based applications.
* Use Visual Basic 6.0's IntelliSense® technology to increase your productivity with on-the-fly programming assistance, including statement completion, parameter information, and syntax error checking.
* Build applications for Windows CE efficiently by dragging Windows CE-specific components from the toolbox and dropping them onto the Visual Basic Form Designer.
Comprehensive access to Windows CE platform increases productivity.
* Save time by using COM/OLE-the world's most successful and powerful component model to build reusable solutions for Windows CE-based devices.
* Develop compelling, commercial-quality applications by using the DECLARE statement to gain direct access to custom Dynamic Link Libraries (DLLs) and Windows CE operating system functionality.
* Build compelling mobile applications by accessing communication protocols such as TCP/IP via an infrared or serial port.
* Save time and eliminate duplication of effort by reusing ActiveX® code modules.

Microsoft®

For more information on the toolkits, please visit:
http://msdn.microsoft.com/cetools

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Microsoft® Windows® CE Toolkit for Visual C++®

Features

- Visual C++ Studio enhancement
- MFC framework support
- ActiveX support for fast apllication development
- Pluggable SDK's for all WindowsCE-based devices, like Palmsize PC, Handheld PC, Auto pC, etc.

NEC CPUs Supported

VR41xx, VR43xx,
(MIPS 16: VR4121A, VR4111A)

Host Platforms Supported

Windows NT/95/98, Windows CE

Product Overview

With its power, familiarity, and flexibility, the Windows CE Toolkit for Visual C++ offers developers easy entrée into the emerging portable-PC industry. If you're a Win32 developer today, you can use the Windows CE Toolkit and your existing Visual C++ knowledge to access the entire Windows CE operating system. The toolkit supports features such as visual design and IntelliSense technology, making it the most efficient way to build Windows CE-based applications. Plus, it's readily extensible, so you can develop for all of today's Windows CE-based PC Companions, as well as tomorrow's devices.
Use Windows-based development tools to create full-featured portable applications
* You can use the Microsoft Foundation Classes (MFC) framework for Windows CE to create stand-alone executables or DLLs. With MFC for Windows CE, you can build anything from a simple dialog-box-based program to a sophisticated application that employs the full MFC document/view architecture.
* With the Active Template Library (ATL) for Windows CE, you can create small, fast Microsoft ActiveX® components and COM objects, and cut development time by using the ATL to create Composite Controls that host multiple Microsoft ActiveX or Windows-based controls.
* The Windows CE Toolkit enables you to build business applications that take advantage of the ActiveX Data Objects Control (ADOC) for Windows CE. ADOCE-a subset of ADO-includes an internal database provider, so Windows CE-based applications can access databases that are stored locally on a device.
* Free, Pluggable SDKs let you build for all Windows CE-based devices: Palm-size PCs, Handheld PCs, Handheld PC Pros, and Auto PCs. Use Pluggable SDKs to keep the toolkit up-to-date and be the first to develop for newly released devices.

Microsoft®

For more information on the toolkits, please visit:
http://msdn.microsoft.com/cetools

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Real-Time Operating Systems

Nucleus PLUS
Real-Time Operating System

Features

- No royalties
- C source code provided
- Scaleable: 4 KB - 45 KB, depending on necessary functionality
- Written in ANSI C
- Deterministic, low interrupt latencies
- Extensible: make new services by combining existing services
- Configurable: easily exclude services not used
- Dynamic creation of all Nucleus PLUS tasks
- Intertask communication: mailboxes, variable queues, pipes
- Task synchronization: counting semaphores, events, UNIX-like signals
- One-shot and multiple-shot task timers
- Memory management: fixed partitions, variable length (malloc)
- Place any Nucleus PLUS component in any area of memory
- Advanced Interrupt Management Mechanism (AIMM)

NEC CPUs Supported

VR41xx, VR4300, VR5000

Host Platforms Supported

PC

Product Overview

Real-time services that are available in the basic Nucleus PLUS product are more full-featured and capable than virtually any real-time kernel on the market today. Accelerated Technology performed an evaluation of the most prominent real-time kernels currently on the market. From this analysis, Nucleus PLUS was developed. Nucleus PLUS has been developed with a "micro-kernel" structure in mind. That is, the essential services of the real-time, embedded environment are provided in such a way that additional operating-system-oriented features can be easily added.

Nucleus PLUS is a real-time, pre-emptive, multitasking kernel designed for time-critical embedded applications.
Nucleus PLUS is extremely portable and is currently available for use with most microprocessor families.

Accelerated Technology
INCORPORATED

Nucleus PC+ Prototyping Environment for Use with Windows 3.1/95

Features

- Interface Identical to Nucleus PLUS
- Test Software Using PC Software Tools (Borland C/C++™ and Microsoft C/C++™)
- Recompile With Intel i960 Dependent Files for Target System
- Use DOS Services for I/O
- Executes as a native Windows 3.1 or Windows 95 application

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

PC

Product Overview

Nucleus PC+ is the version of Accelerated Technology's Nucleus PLUS kernel that can be used in an MS-DOS environment. This environment is ideal for embedded applications requiring the responsiveness of multitasking while taking advantage of low cost PC hardware. Further, all of your C code can be developed in the friendly PC environment.

Development Tools

The real mode version of Nucleus PC+ has been prepared for use with the Borland and Microsoft C compilers and assemblers. Accelerated Technology provides libraries that can be linked with your application to build a Nucleus PLUS-based application that is an MS-DOS executable. A special version of Borland's Turbo debugger that has been enhanced with Nucleus PLUS awareness has been developed by Paradigm Systems. This product, Paradigm DEBUG™, is ideal for debugging Nucleus PC+ applications that have been developed with either the Borland or Microsoft compilers.

For programs exceeding the 640 Kbyte boundary or those requiring the advantage of a 4 Gbyte address space, the protected mode version of Nucleus PC+ can be used. It's been prepared for use with the MetaWare High C™ and Watcom C™ compilers in combination with the PharLap DOS Extender™ and the PharLap™, Turbo™, or Microsoft assemblers.

Interrupt Management

Nucleus PC+ provides access to the PC's interrupt structure, allowing you to invoke a task thread from an interrupt. By doing this, executing threads can be preempted by an interrupt service routine. Nucleus PC+ also permits the processing of interrupts without kernel involvement. In this case, you perform the necessary register saving and restoring, or you can employ the INTERRUPT pragma.

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Nucleus NET
TCP/IP Protocol Stack

Features

- TCP/IP Protocol stack
- Protocols supported: TCP, UDP, IP, BOOTP, IGMP, ICMP, ARP, RARP, DNS, DHCP
- Optional protocols: RIP/RIPII, PPP, POP3, and SMTP
- Socket User Interface
- Full Integration with Nucleus PLUS for optimal performance.
- Blocking and Non-Blocking Services Supported
- Standard Interface to Physical Layer Devices
- Send/receive ping requests
- Compact and scalable

NEC CPUs Supported

VR4111, other on request

Host Platforms Supported

PC

Product Overview

Nucleus NET is a set of networking protocols to provide interoperability between Nucleus PLUS-based systems and other TCP/IP or UDP/IP based systems.

A socket interface is provided to maintain a similar programming environment to those familiar with the UNIX socket programming model.

Nucleus NET provides a well defined driver interface for user supplied drivers, and can support various MAC layer drivers. There is less wasted memory space, due to a more efficient packet-buffering scheme, and support is available for Raw IP, IP forwarding, IP reassembly, IP fragmentation, and IP multicasting, IGMP, and DHCP services. Network-centric applications, such as routers, switches, and bridges are also supported. Nucleus NET is also the foundation for ATI's latest Web-related products, including Nucleus WebServ.

As with all Accelerated Technology products, Nucleus NET is delivered in source code form and no royalties are charged for the inclusion of binary copies in a single product line. Nucleus is also provided with six months free technical support. This includes phone, fax, email and new releases. For more information, contact Accelerated Technology today.

Accelerated Technology
INCORPORATED

Nucleus VNET
Virtual Networking Support for Nucleus PLUS

Features

- Supports virtual networking between multiple Nucleus PLUS based TCP/IP, WinSock, and remote node applications
- Hosted on Windows NT or remote nodes on network
- Access to full Visual C++ features
- Depends on Nucleus MNT and Nucleus NET
- Can build and test multiple TCP/IP applications on same target
- Two levels of device driver support

NEC CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

PC

Product Overview

TCP/IP services are provided for Windows NT™ in the Nucleus MNT environment through a virtual networking facility. Nucleus VNET is a version of Nucleus NET that has been ported to the Windows NT environment. Nucleus VNET allows Nucleus MNT processes to communicate with each other via a shared memory area. That means multiple versions of Nucleus MNT can be executed on an NT machine, each with its own IP address. Developers who use this technology have the ability to simulate a network on an NT machine. The same shared memory area can be used to communicate with Windows NT applications via a virtual NDIS driver and nodes on the physical network using Windows NT routing facilities.

Initialization

Nucleus VNET's Virtual NDIS driver, which is responsible for allocating the global memory area, is started when the NT workstation is booted. The VNET driver then is started manually by the user. This driver must be started after the NDIS driver because it depends on the NDIS to allocate and initialize the common memory. After both drivers have been started, one or more Nucleus MNT/Nucleus VNET applications can be executed.

Communication

Nucleus VNET applications communicate with the VNET driver via NT's Device I/O Control call. Because Nucleus VNET requires Windows NT device drivers, it will execute only on a Windows NT workstation.

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CE Interface Composer

Features

- Build unique user interfaces with new SKINS support
- Any bitmap image can become a desktop interface, providing absolute control over interface appearance
- Supports Windows CE 2.11 and 2.12
- New plug-in for IE 4.0 browser control* adds Internet browsing support
- Completely COM-based for improved modularity and extensibility
- Minimize memory footprint by including only the modules you need
- Create your own COM objects that fully integrate with CE Interface Composer
- Rapid interface development with our simple configuration language
- Supports multiple user configurations on the same device
- Full control over all user options with password security and administration mode
- Includes full featured default desktop, SKINS samples, tutorials, reference manual and support
- Requires Windows CE 2.12 operating system

NEC CPUs Supported

VR4300

Host Platforms Supported

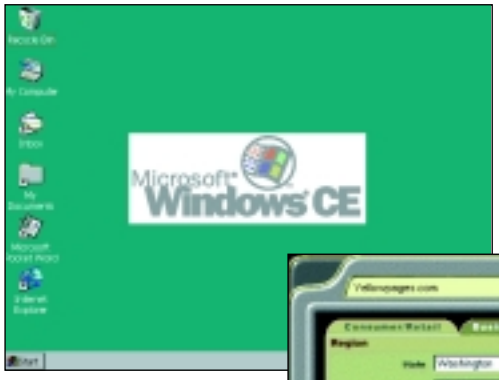
PC: Windows 95/98/NT

Product Overview

Custom Interface Builder for Windows CE
BSQUARE® CE Interface Composer** delivers an innovative user interface design solution for embedded system development and information appliance deployment. A powerful and easy-to-use tool for Windows CE-based devices, CE Interface Composer gives you unprecedented control over the look, feel, and functionality presented to the end user.

With password and access control features similar to Windows NT, developers can design a multiple-user system. CE Interface Composer includes all of the necessary features to rapidly develop a high-quality custom interface for any Windows CE-based device.

Endless Possibilities - Defining the User Experience
CE Interface Composer sets you free from the restrictions of using a general-purpose shell provided by Windows CE. With the latest version of CE Interface Composer you are bound only by the limits of your imagination. Use any bitmap image or standard Windows icon art to create your interface—the choice is yours. CE Interface Composer's flexibility and plug-in architecture allows you to build unique interfaces that are tailored to your user needs, whether you're building an interface for a field data collection device, kiosk, screenphone, or other information appliance.



Standard shell that ships with Microsoft Platform Builder.

Whether you need a standard Windows look and feel or a highly targeted interface design, CE Interface Composer provides the flexibility you need.

With CE Interface Composer, you can build interfaces that are specific for next-generation information appliances such as the sample SKIN of this screenphone.

**Formerly CE EmbeddedDesktop

bSQUARE

Complete Flexibility and Security
CE Interface Composer's flexibility is made possible by BSQUARE's innovative COM object model approach to configurable interface technology. Loosely coupled components offer the maximum level of design flexibility while minimizing system requirements. In addition you can create different "personalities" for the same device and alternate between them, according to user requirements. For example, you can create a Windows CE tablet that has one interface, a set of applications, and access rights for a doctor and a completely different interface, set of applications, and user rights for a nurse – all on the same device. CE Interface Composer provides fine-grained administrative control over the interface you design and present to the end-user. Password protect every command, including access to the file manager, control panel and start button and choose from three levels of password permissions.

Easy to Use
Designing a custom interface with CE Interface Composer requires simple scripting and is remarkably easy and fast. To get you started, a default desktop and several sample configurations are included. With a simple configuration script, you can rapidly develop your interface. The plain text file is then compiled into a form that CE Interface Composer can read, and the shell configures its components (button bar, command menu, filestore etc.) according to your instructions. There is no limit to the unique design configurations that can be created.

System Requirements
CE Interface Composer works with Microsoft Windows CE version 2.11 and 2.12 and can be used in conjunction with Microsoft Platform Builder for Windows CE (recommended). The full version of Windows CE is required (Maxall) on the target Windows CE device for CE Interface Composer to work. Configuration data is compiled on a Windows NT host machine. The finished CE Interface Composer product image runs on any hardware platform supported by Windows CE Platform Builder or any of BSQUARE's CE Xpress ™ Kits designed for Windows CE 2.11 or 2.12.

• Client (Windows CE device)
— Windows CE 2.11 or 2.12
— Any processor supported under Windows CE
— 4MB of RAM

• Desktop
— Windows NT 4.0 or higher with SP3 installed
— Pentium or faster processor 32 MB of RAM or higher
— 50 MB of available HD space for installation
— Microsoft Platform Builder 2.11 or 2.12

About BSQUARE
BSQUARE is a dynamic software company working with Fortune 500 companies to enable the age of intelligent computing devices. Specializing in Windows Embedded, BSQUARE is a supplier of software products and services for PC Companions, Internet appliances, industrial automation devices, Windows-based Terminals, and other intelligent computing devices. BSQUARE's expertise in embedded Windows is derived from years of contributing to the development of the Windows CE operating system, from serving as a Microsoft preferred provider of Visual Tools for Windows CE, and from in-depth experience with Windows NT. BSQUARE is a Microsoft-sanctioned systems integrator and distributor.

For more information on BSQUARE's CE Interface Composer or other BSQUARE products and services, visit **www.bsquare.com**, or e-mail **sales@bsquare.com**.

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CE Xpress™ Kits

Features

- Support Windows CE 2.1x
- Extend the capabilities of the Microsoft Platform Builder for a fast implementation of Windows CE on a target platform
- Separate kits available for each Windows CE-supported CPU architecture and development environment
- Feature the CE Portability Layer for complete architecture and platform portability
- Flexible BSQUARE Loader for downloading and booting Windows CE
- Platform-specific OEM Adaptation Layer (OAL)
- No BIOS or DOS required on x86 platforms
- Production-quality device drivers for on-board peripherals
- Installation utility, host tools, debug services, complete documentation, technical support
- All kits tested using BSQUARE CEValidator ™ technology

NEC CPUs Supported

VR4300

Host Platforms Supported

PC: Windows 95/98/NT

Product Overview

The Quickest Way to Develop Intelligent Computing Devices

BSQUARE ® CE Xpress ™ Kits provide tools and technology that enable complete and timely software solutions for the development of intelligent computing devices. Each processor-specific kit provides the tools and components necessary to adapt Windows CE to a specific target device. Several versions are available for a wide range of evaluation boards, reference platforms, single-board computers, and custom hardware devices.

Save Time and Expense

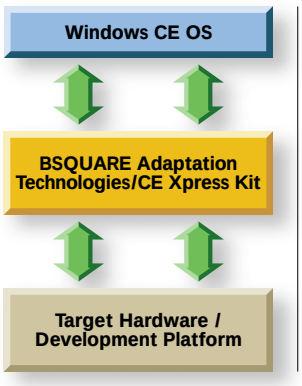
Complex and time-consuming tasks are required to bring up Windows CE on a target platform. Save valuable engineering resources by utilizing the investments already made by BSQUARE. CE Xpress Kits provide a time-to-market advantage by allowing you to spend time concentrating on the features which will make your embedded device successful in the marketplace.

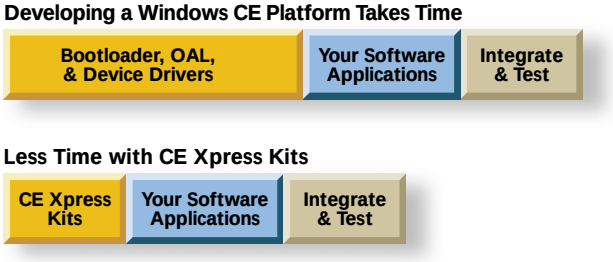
Make the Smart, Flexible Choice

CE Xpress Kits deliver the software tools needed to develop an embedded system now, and are flexible to meet future development platform requirements. BSQUARE supports the most popular development platforms within every Windows CE-supported architecture (SHx, MIPS, PPC, ARM, x86) and is continuously developing new kits for additional platforms. BSQUARE's growing library of hardware device drivers, along with BSQUARE's CE Portability Layer (CEPL) technology, support the ongoing changes any Windows CE project encounters.

Device Drivers

Each BSQUARE CE Xpress Kit includes production-quality device drivers tailored to the on-chip and on-board capabilities of the target platform. Each kit is also compatible with BSQUARE's Portable Driver Library—an extensive collection of additional device drivers that work across all Windows CE-supported platforms because they incorporate BSQUARE's CEPL technology. Access to the Portable Driver Library is available on a subscription basis through BSQUARE's CE Xpress ™ OnDemand web site, ensuring timely access to our latest driver technology.





bSQUARE

BSQUARE Loader
This platform-specific bootloader downloads the Windows CE images and boots the OS using a variety of methods (Serial, Parallel, Ethernet, Flash, PCMCIA). Some Xpress kits also include BSQUARE technology for additional booting options using BIOS.

OEM Adaptation Layer (OAL)
To quickly bring up Windows CE, start with a fully developed and thor-oughly tested OEM Adaptation Layer for any Windows CE-supported CPU. Depending on the kit, this may be in source or binary form.

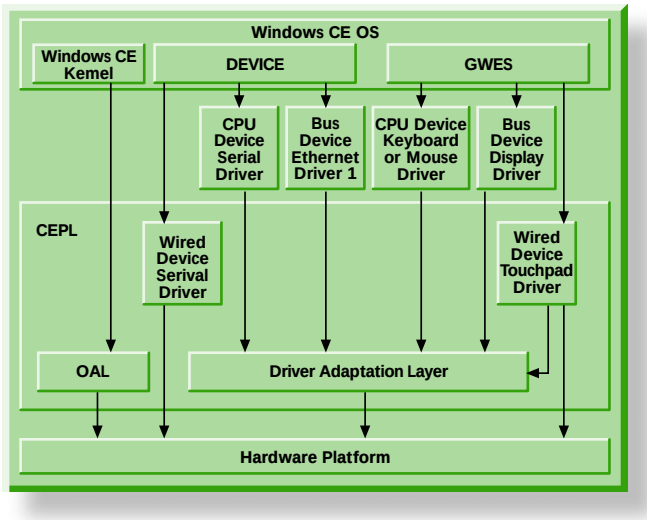
Debug Support
Debug services (CE Term, CESH, WinDbg) are supported with a variety of connection options (Ethernet, Serial, Parallel). Precise combinations vary by kit.

Tested with CEValidator
BSQUARE's longstanding commitment to quality assurance has bred a unique solution to one of the most time consuming phases of the product development cycle. CEValidator™ , the first of its kind, is a fully automated design verification environment for Windows CE. This technology is used within BSQUARE for assuring the highest quality for the CE Xpress Kits.

The CE Portability Layer (CEPL)
The CE Portability Layer is a software infrastructure technology that maximizes quality and enables portability across platforms. With the CEPL, device drivers written for one hardware platform can be easily ported to a new platform when the project advances to a next-generation CPU, when it changes hardware direction, or when it expands to include multiple platforms or architectures.

Benefits of the CE Portability Layer
- Enables portability of device drivers across all Windows CE-supported architectures using CEPL APIs and recompilation
- Enables portability of device drivers among CPUs sharing an instruction set, without recompilation
- Availability of BSQUARE's production-quality Portable Driver Library
- Delivers the highest quality, thoroughly tested common code base
- Ensures a time-to-market advantage by having to write and test less custom code for any new adaptation or device driver.

About BSQUARE
BSQUARE is a dynamic software company working with Fortune 500 companies to enable the age of intelligent computing devices. Specializing in Windows Embedded, BSQUARE is a supplier of software products and services for PC Companions, Internet appliances, industrial automation devices, Windows-based Terminals, and other intelligent computing devices. BSQUARE's expertise in embedded Windows is derived from years of contributing to the development of the Windows CE operating system, from serving as a Microsoft preferred provider of Visual Tools for Windows CE, and from in-depth experience with Windows NT. BSQUARE is a Microsoft-sanctioned systems integrator distributor.



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For more information on BSQUARE's CE Xpress Kits or other BSQUARE products and services, visit **www.bsquare.com**, or e-mail **sales@bsquare.com**.

Microsoft® Windows CE Operating System

Features

- Module based OS with RTOS capabilities
- Serial I/O
- Fully featured networking support (TCP/IP, RAS, NDIS)
- Wireless support
- Optional Products as there are Pocket Word, Excel and Powerpoint
- Internet explorer

NEC CPUs Supported

VR41xx, VR43xx,
(MIPS 16: VR4121A, VR4111A)

Host Platforms Supported

Windows NT/95/98, Windows CE

Product Overview

Microsoft® Windows® CE is a compact, highly efficient, modular operating system designed for a wide range of embedded systems-such as industrial controllers, kiosks, data terminals, set-top boxes, and hand-held computers. Since Windows CE supports a large subset of the Win32® API, you can use your existing Windows programming skills or come up to speed quickly by taking advantage of the numerous books and training courses on Win32 and developing with Windows CE. Then use that knowledge to develop applications for a whole new category of connected devices. The Microsoft Internet Explorer for Windows CE class browser control enables you to develop full-featured branded browsers for your Windows CE-based devices. You can use tables, cascading style sheets, JavaScript, DHTML, JPEG, and animated GIF and WAV files to create full-featured browsers for your device. The updated desktop applications for Windows CE make your devices more appealing to your customers. You can easily integrate the Pocket versions of Word and Microsoft Internet Explorer, along with Inbox and Handheld PC Pro-style shell into your devices. With Pocket Word, you can create documents on your Windows CE-based device that are compatible with their desktop counterparts. With Internet Explorer for Windows CE, you can surf the web, save favorite sites and view local HTML files. With Inbox you can create, send, receive and reply to e-mails from your devices. And with the Handheld PC Pro-style shell, you can provide the familiar Windows 9X-style user interface including a start button, TaskBar, desktop icons, and the Recycle Bin.

Windows CE supports a large range of communication options and application program interfaces. You can now create connected devices with the communications component in Windows CE. This component provides support for the following communications hardware and data protocols: Serial I/O support, Remote Access Service (RAS), Transmission Control Protocol/Internet Protocol (TCP/IP), Network Directory Interface Specification (NDIS) for Local Area Network (LAN), Telephony API (TAPI), Wireless Services for Windows CE.

Cryptography tools in Windows CE enable you to digitally sign files and prevent unsigned applications from loading. With the Cryptography Service Provider developer kit, you can create your own cryptography service providers, and add extra protection to your data using custom crypto algorithms.

The Dial-Up Bootloader allows you to dynamically update your OS image over the Network. The Dial-Up Bootloader makes upgrading for bug fixes or new services very easy for remotely installed devices.

Microsoft®

For the latest list of supported processors, please visit:
http://www.microsoft.com/embedded/resources/proc212.asp

For the latest Windows CE product updates and technical information,
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QNX® Realtime OS

Features

- Scalable microkernel architecture: Use one OS and one API for everything from handheld appliances to high-end SMP clusters
- Provides full memory protection for all drivers, applications, and OS components
- Recovers from software faults—even in drivers and other system services—without rebooting
- Supports hot-swapping for drivers and OS modules
- Most drivers source-code identical across processor platforms
- Fits POSIX RTOS plus full-featured GUI into less than 1MB of ROM
- Connects seamlessly to Windows desktops (control Windows from QNX, or QNX from Windows)
- Supports multiple filesystems—embedded, POSIX, CIFS, CD-ROM—simultaneously
- Full Internet technology suite (including embedded browser, email client, and web server)

NEC CPUs Supported

R4000 (including VR41xx, VR43xx series), R5000

Host Platforms Supported

Windows NT, Windows 95/98, QNX 4

Product Overview

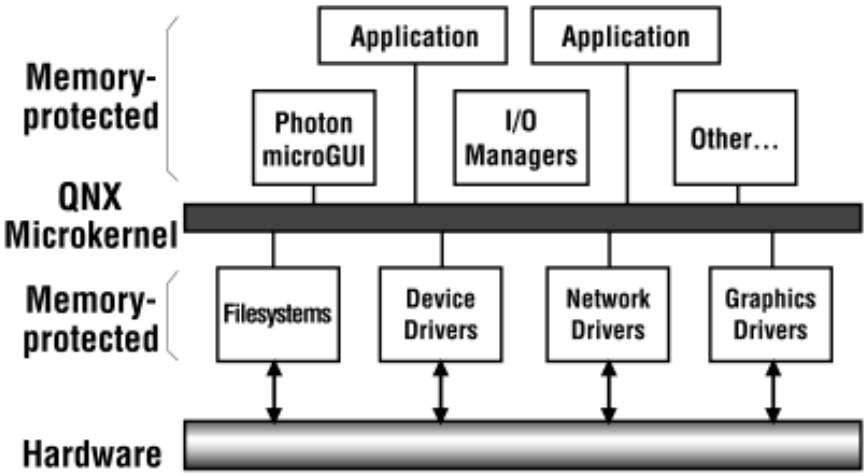
Microkernel Architecture for Massive Scalability

QNX's microkernel architecture offers unprecedented scalability. Link your application code directly against the kernel to create a single multi-threaded image for small embedded systems—as you would with a realtime executive. Or run the QNX Process Manager for all the advantages of a full process model and the ability to add thousands of applications—all running in MMU-protected memory.
Or take QNX to the extreme and run your applications over a distributed network of SMP clusters for the ultimate in large-scale configurations! Whatever your configuration—tiny, medium, massive, or distributed—recoding is never an issue since the QNX API remains consistent throughout.

Superior Memory Protection

Conventional operating systems use a single flat memory architecture where hard-to-detect programming errors like corrupt C pointers can cause programs to overwrite each other (bad) or the kernel (worse). The inevitable result: system failure. A QNX-based system, however, can intelligently recover from software faults, even in drivers and other critical programs—without rebooting—because every OS component runs in its own MMU-protected address space.

QNX's full MMU support also simplifies testing since it identifies which module tried to perform an invalid memory access—at the exact instruction. What can often take weeks or months to identify in a conventional RTOS takes virtually no time with QNX.



QNX provides memory protection for all applications, OS components, and drivers.

Build a more reliable world™

Portable POSIX APIs

QNX is the world's first microkernel with a POSIX personality. Unlike realtime executives and OS implementations that have proprietary APIs, QNX is engineered from the ground up for the latest POSIX 1003.1 standards and drafts, including realtime and thread options. QNX's POSIX implementation means portability—not only of your application code, but also of your software developers. In fact, programmers familiar with UNIX won't need any training to feel right at home in this POSIX environment. What's more, this built-in POSIX compatibility comes without the penalty of extra code. Even after the Process Manager is added to include services like process creation, pathname-space management, and memory protection, a QNX-based system is extremely small and efficient—crucial for ROMable systems.

Minimize Hardware Costs

Unlike some OSs that try to squeeze monolithic designs or bulky windowing systems into embedded environments, QNX was designed from the ground up to reduce the cost and component count of your products. For example, QNX supports execute-in-place (XIP), which allows applications to run directly out of ROM or flash. And, since its system image is actually a simple read-only filesystem, it allows applications to start without a separate filesystem manager or command interpreter.

Integrated Development Environment

QNX development is supported under the award-winning CodeWarrior Integrated Development Environment (IDE). Command-line GNU-compatible tools.

Dynamically Loadable Functionality

No other realtime OS scales so easily—just plug in the modules or drivers you need. Like other operating systems, QNX supports shared objects (also known as DLLs). But unlike other operating systems, QNX lets you add or remove entirely new OS functionality (via software modules) on the fly without rebooting your system.

Embeddable Photon microGUI®

Running in an extremely small memory footprint, Photon offers a highly functional windowing system that connects seamlessly to QNX's message-passing architecture. Photon also gives you exceptional connectivity between windowing systems. With Photon's remote user interface (RUI) technology you can view—and control—the GUI of a QNX embedded system from a window on a Windows NT/95/98 or UNIX desktop. RUIs are baud-rate aware and can run across a serial or network link. For embedded systems, this can give you a graphical interface into your consoleless black box. With the optional Citrix ICA Client for Photon, reverse connectivity is also available: Run a Windows NT/95/98 session from within a window on the Photon desktop.

Embeddable Web Server

With our tiny TCP/IP manager and embedded web server, you can control your embedded device—be it a printer, photocopier, router, or PLC—from any web browser. Retrieve statistics, configure system parameters, or troubleshoot problems, without leaving your desktop PC.

Platform-independent Device Drivers

From the beginning, drivers for QNX were designed to be source-code identical across CPUs and boards. In fact, the same binaries for a CPU can run on different boards—no more BSP nightmares. To reduce the time required to write your own device drivers, QNX provides a resource manager framework and C functions that handle the default behaviors common to most devices; all you need worry about are the low-level details specific to your device. And because each QNX driver runs as a standard process (rather than as part of the kernel itself), you can test changes in driver code without having to go through the time-consuming task of rebuilding the kernel. Simply recompile and restart the driver.

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LEO
A Development Toolchain for OSEK

Features

- Microkernel for Automotive Industry
- Fully complies to OSEK 2.0 standard
- Designed for portability and distributed systems
- Optional MMU support
- “Virtual ECU“ Real-Time Simulation for Rapid Prototyping
- Integration with CASE-Tools from ATTOL, MathWorks and Verilog

NEC CPUs Supported

VR5000 Family

Host Platforms Supported

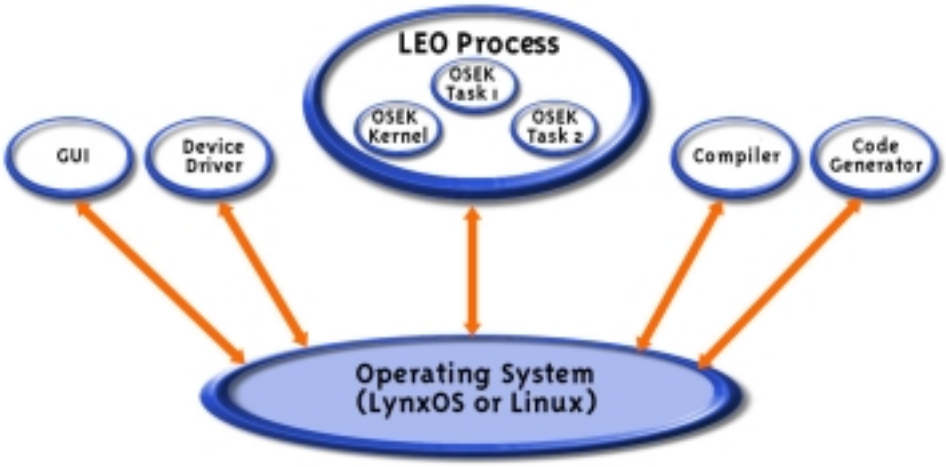
Linux, LynxOS, WinNT

Product Overview

OSEK is the evolving standard for software running on electronic control units (“ECU”) in cars. SYSGO’s LEO provides a seamless development toolchain for OSEK applications: While LEO/posix provides a “Virtual ECU” under Linux and LynxOS® for Rapid System Prototyping, LEO/p4 runs on the ECU itself. As the OSEK part is exactly the same in both versions, the code generated and tested in the prototyping phase only needs to be recompiled for the microkernel version running on the target. The message-based microkernel technology also provides an easy distribution of tasks over multiple platforms.

SYSGO Real-Time Solutions GmbH

LEO/posix for Rapid System Prototyping
During development LEO/posix runs an OSEK application and the OSEK kernel inside the host environment. The OSEK application itself can be generated by CASE-tools from MathWorks or Verilog. As the OSEK process can communicate with any other process or device driver, the OSEK tasks can access external hardware easily. Due to the real-time capabilities of the host operating system, the LynxOS version allows not only the emulation, but the real-life simulation of a complete ECU in the running car – long before the hardware is even available.



LEO/p4 microkernel on the target
Complementary to the simulation/emulation tools stands LEO/p4, the OSEK kernel to run on the ECU itself. The code generated and tested under LEO/posix can easily be ported to the target by simply recompiling it. The modular approach based on microkernel technology provides portability and is open for distributed systems. The MMU support allows to run multiple OSEK instances on the same processor, with each instance running in its own protected address space.

Ordering Information

A-LEOP-MIPS	LEO OSEK development environment for NEC VR5000
L-LEOP-MIPS	Additional License Package

Contact List:

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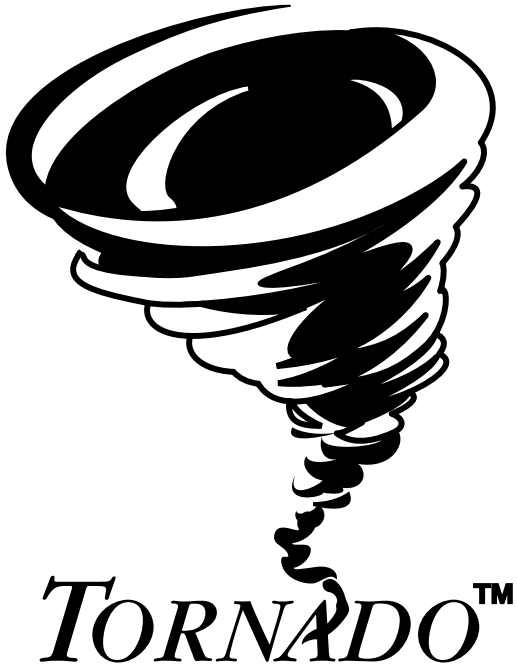
E-Mail: sales@sysgo.de
Contact: Mr. Knut Degen

Tornado II™ Development Environment

Featuring the Industry-Leading VxWorks® RTOS



Features

- The superior development platform for the embedded developer
- A complete, intuitive and integrated tools suite
- Includes C/C++ compiler, editor, browser, powerful debugger and advanced command shell
- An open, extensible and customizable environment with published API supported by over 500 third Party Wind River Partners
- Additional run-times include fully featured networking, communications, graphics, Embedded Internet, Java, multi-processing and file systems.
- Powerful optional tools including source navigator, code coverage, dynamic memory analyser, dynamic C++ object visualisation, real-time data analysis and OS analyser.
- Open target connection strategy with tools independence including serial, ethernet, ROM emulator and in-circuit emulator
- GUI driven configurator for VxWorks® scalability across all real-time implementations
- Includes the proven, industry standard, high performance VxWorks® Operating System

NEC CPUs Supported

VR41xx, VR4300, VR5000, VR5400

Host Platforms Supported

UNIX workstations, Windows 95/98/NT

WindRiver® SYSTEMS

An ISO 9001 Registered Company

Product Overview

Available for both UNIX- and Microsoft Windows-based hosts, the revolutionary Tornado development environment consists of the Tornado tools suite, the VxWorks RTOS, and a full range of communications options connecting host and target. All Tornado tools can be utilised at any stage of application development, with any level of target system resources. All are fully integrated and have sophisticated GUIs, and all are available regardless of target connection strategy (Ethernet, serial, ICE, ROM monitor or custom).

The Tornado APIs are published, from the GUI interfaces down to the debug agent interface, to facilitate customisation and third-party integration. In addition, developers can take advantage of a variety of productivity-enhancing WindPower Tools, including the VxSim simulator, the WindView system visualizer, Look! C++ dynamic visualisation debugger, CodeTest code coverage, CodeTest dynamic memory allocation analyser and the Stetho Scope data monitor.

VxWorks provides fast multitasking, preemptive scheduling (with optional round-robin scheduling for same-priority tasks) and fast interrupt response. To these microkernel features, VxWorks adds intertask communications and synchronisa-tion facilities, efficient memory management, multiprocessing support, a fast I/O system, IDE and SCSI support and MS-DOS, FLASH and RT-11-compatible file systems.

Tornado networking includes 4.4 BSD UNIX TCP/IP, sockets, SNMP, DHCP, NFS, RPC, ftp, rlogin, telnet and optional support for the X Window System. A wide range of integrated third-party networking products are available through WindRiver's WindNet Partners program, including ATM, OSI, SS7, Frame Relay, STREAMS, CORBA, ISDN, X.25, CMIP/GDMO, V.2, Iv6, XTP, Internet Protocols, and distributed network management.

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Evaluation Boards and Supported Hardware

Algorithmics P-4032: embedding 64-bit MIPS

Features

- Low cost R4x00 CPUs: uses any R4x00 32-bit CPU, including NEC VR4300 100 MHz+ 64-bit power in a low-cost, low-power package with a 32-bit bus
- High performance through simplicity: P-4032 uses high clock rates and simple, low-latency data paths, but avoids features which add cost and complexity
- PCI expansion: standard 32-bit 33MHz PCI bus, with 3.3V compatible slots available
- PC-world devices for low cost, rich I/O: includes a big choice of cheap I/O to solve interfacing problems
- Hardware featured for development support: centronics interface for fast download from PC; flash PROM for easy reprogramming; onboard ethernet for download/debug from Unix hosts; customisable interrupt controller
- Modular re-usable design. Schematics and logic listings are available to customers; you can license the complete design; or you can obtain permission to reuse chunks of logic for a modest one-off payment
- PMON monitor and SDE-MIPS integration which is fitted to every board. You can build programs for P-4032 with Algorithmics' SDE-MIPS package, right out of the box
- Wide range of OS support, including Windows CE OAL and VxWorks BSP. OpenBSD and Linux available; ported by volunteers encouraged by Algorithmics. Sources and binaries are free, support is available.

NEC CPUs Supported

VR43xx

Host Platforms Supported

PC: Windows 95/NT, UNIX

Target Systems Supported

Windows CE OAL, VxWorks BSP, OpenBSD, Linux, ISI pSOS, POSIX-threads RTOS

Product Overview

If you're looking for Pentium-class 64-bit computing power on a tight cash and power budget, you're probably looking at VR43xx CPUs. With so much power, it's possible to re-think the way systems work - if only you had the time and tools. Algorithmics' P-4032 is a key part of a package of hardware, software tools and support which can help you through evaluation, porting and redesign with the minimum of hassle. P-4032 is designed to help you get your software running, and to form a reusable example of an efficient R4x00 system design. And it's surrounded by software (some freely reusable, all available for reasonably-priced licensing).

- CPU: NEC VR43xx at up to 67 MHz interface speed. Various configurations are jumper-selectable, including the "little-endian" mode. However, software will have to adapt appropriately.
- Main memory: • from 2 - 64 Mbytes 32-bit wide DRAM using two slots for industry-standard 32-bit SIMMs. Burst EDO memory gives the best performance, but standard EDO or fast page mode modules work too. You can even fit a DRAM-pinout flash module. This is just about as efficient a 32-bit MIPS memory as can be implemented, with access latency of 100ns at the CPU pins and burst bandwidth of 266Mbytes/s.
- PROM: 512Kx8-bit FLASH PROM, and a socket for a 512Kx8-bit EPROM or emulator. The CPU can boot from either ROM, and run cached from it.
- Ethernet interface: "thick-wire" interface using a DEC 21041 PCI- bus controller. Supports fast download and host access, essential for a good development environment.
- SCSI interface: •using a 53C810 PCI-bus controller for high performance and flexibility.
- Other I/O: dual high-speed serial ports, bidirectional centronics (can implement either a "host" or "printer" port), diskette interface, EEPROM for "environment" store, real-time clock, PC- compatible keyboard, general-purpose parallel I/O, customisable interrupt controller.
- Diagnostic display: choice of a 4-character LED display, or a larger LCD display, for diagnostic and debug messages.

- PCI bus sockets: two standard edge connector sockets and one optional slot for customer's development daughterboards (all PCI signals, plus some useful extras).
- Optional debug header/card: fits onto the board, demultiplexing and presenting address and data for your logic analyser. Includes reprogrammable trigger PAL.

Software support
Algorithmics' SDE-MIPS is a software development toolkit hosted on Windows95, Windows NT, Sun workstations, Linux and some other Unix systems. The GNU C compiler at the heart of SDE-MIPS supports modern language standards and its optimiser is state-of-the-art. SDE-MIPS supports source-level debug of software running on the P-4032 and includes comprehensive libraries and lots of sample sources. See the separate data sheet for details. Not only is SDE-MIPS probably the only 64-bit cross-development toolkit you'll find, but it is also available at an irresistible special price when ordered with P-4032.

Target software and OS
- PMON is a bootstrap/monitor program originally developed by LSI Logic Inc, but placed by them in the public domain. Algorithmics use PMON on all our MIPS products. PMON sources (including Algorithmics' enhancements) are available free - it builds under our SDE-MIPS toolkit. We can do ports to your hardware on request. P-4032's ROM has power-on test software built with AlgPOST, our re-usable test framework, available to license for customer designs.
- Windows CE is available for most CPUs; OALs for our boards are made by Algorithmics.
- Wind River System's VxWorks real-time OS runs on most of these CPUs, and Algorithmics can supply a BSP (priced according to support levels).
- Other RTOS such as Accelerated Technology's "Nucleus" are usable; enquire.
- AlgRTX, Algorithmics' lightweight POSIX-threads RTOS, is available as source code on a one-time license for applications needing a customised but standards-compliant kernel. For users considering conversion from Inmos/SGS "Transputer" processors, Algorithmics have developed an additional software layer which maps the de facto C language binding of the Transputer's hardware task support into AlgRTX calls.
- Both Linux and the OpenBSD derivative of BSD4.4 run on P-4032. They each offer a high-end multi-tasking environment for the board; appropriate for customers whose need easy porting more than real-time scheduling.

Price and Availability
P-4032 is available direct from Algorithmics in England, and has been in full production since April 1996.

Technology licensing
The P-4032 and its software are available for license. A comprehensive manufacturing license for the whole board is available for a one-time payment of $35000, with no royalties payable thereafter. Similar affordable, no-nonsense deals are available for use of chunks of logic. Call us and talk about this and other offers. Algorithmics also provide short training courses, support, and customisation services.

P-4032 history
Algorithmics are the leading supplier of R4x00 evaluation platforms; our P-4000i product is in use with about 100 customers all over the world. P-4032 was developed over the winter of 1995/96 in response to increasing customer interest in the low-cost VR4300. P-5064 launched in Q3 1997 and supports 64-bit R5000-class CPUs.

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www.algor.co.uk
Contact: Dominic Sweetman

Algorithmics P-5064: new frontiers in embedded MIPS

Features

- Prototyping board for VR5400/VR5464 CPUs. Get power up to and beyond 200 MHz PC processors but without their price, heat and power consumption
- High performance through simplicity. P-5064 uses high clock rates and simple, low-latency data paths, but avoids cost and complexity features (like memory interleaving)
- SDRAM memory system: synchronous DRAM modules provide 1 word/clock bursts of 64-bit data, with parity protection. The DRAM module keeps up with the interface clock rate, between 75-100 MHz
- PCI + ISA expansion: standard 32-bit 33 MHz PCI bus, old fashioned ISA slot
- PC-world devices for low cost, rich I/O: a vast choice of I/O to solve your interfacing problems
- Hardware featured for development support: centronics interface for fast download from PC; flash PROM for easy reprogramming; onboard ethernet for download/debug from Unix hosts; customisable interrupt controller
- Modular re-usable design: P-5064's logic design is open. Schematics and logic listings are available to customers; you can license the complete design; or you can obtain permission to reuse chunks of logic for a modest one-off payment
- PMON monitor and SDE-MIPS integration: the PMON debug monitor is fitted to every board. You can build programs for P-5064 with Algorithmics' SDE-MIPS package, right out of the box
- OS support: Windows CE OAL and VxWorks BSP ready now; "OpenBSD" running too

NEC CPUs Supported

VR5000

Host Platforms Supported

PC: Windows 95/NT, Sun Sparc, Linux/x86

Target Systems Supported

Windows CE OAL and VxWorks BSP, OpenBSD, Linux

Product Overview

If your embedded application requires all the CPU power you can reasonably get in 1997/98 but your money/power/heat budget doesn't extend to a PC-type CPU, 64-bit MIPS CPUs are the best deal in town. You're going to need a high-end I/O system and first-class tools to support your MIPS CPU. Some of the biggest names in embedded applications rely on Algorithmics' packages of hardware, software tools and support. We can help you through evaluation, porting and redesign with the minimum of hassle. P-5064 will help you get your software running soon and fast, and is a reusable example of an efficient MIPS system design. And it's surrounded by software (some freely reusable, all available for reasonably-priced licensing).

- CPU: NEC R5000; NEC VR5464 or other 64-bit MIPS CPU at 75-100 MHz interface speed. All the above run the MIPS-4 instruction set, compatible with software from all earlier MIPS CPUs. All have big onchip caches. Some have onchip controllers for external cache - 1-2 Mbyte of external cache is a build-time option. Most usable configurations are customer-selectable, including the "little-endian" mode.
- Main memory: from 16 - 256 Mbytes 72-bit wide synchronous DRAM in DIMM modules. R5xxx CPUs need fast, low-latency memory, and this is just about the best that can be done at low cost; access latency is 100ns at the CPU pins and the burst bandwidth hits 800Mbytes/s.
- PROM: 1Mx8-bit FLASH PROM, and a socket for a 512Kx8-bit EPROM or emulator. The CPU can boot from either ROM, and run cached from it.
- PCI bus sockets: three standard edge connector sockets.
- ISA bus socket: for those low-cost peripherals.
- PC card (PCMCIA) dual socket: when you've got to prototype something which will be small.
- 10/100 Mb/s ethernet: transceiver or twisted-pair connection using a DEC 21143 PCI-bus controller. Supports fast download and host access, essential for a good development environment.
- SCSI interface: using a 53C810 PCI-bus controller for high performance and flexibility.
- IDE interface: two channels, PCI-bus DMA.

algorithmics

◆ Other I/O: dual high-speed serial ports, bidirectional centronics (has both a “host” and “printer” port), diskette interface, real-time clock, USB sockets, PS/2 keyboard + mouse, general- purpose parallel I/O.
◆ Customisable interrupt controller: can be reconfigured to group devices onto different CPU interrupt pins, to provide efficient support for a variety of different operating systems.
◆ Diagnostic display: choice of a 4-character LED display, or a larger LCD display, for diagnostic and debug messages.
◆ Debug header/card: available as an option, demultiplexes and presents address and data for your logic analyser. Includes reprogrammable trigger PAL.

Software support

Algorithmics’ SDE-MIPS is a software development toolkit hosted on Windows95, Windows/NT, SPARC station, HP/UX, SGI Irix, BSD/OS, Linux and some other Unix systems. The GNU C compiler at the heart of SDE-MIPS supports modern language standards and its optimiser is state-of-the-art. The toolkit has full support for R5000’s “MIPS- IV” instruction set. SDE-MIPS supports source-level debug of software running on the P-5064 and includes comprehensive libraries and lots of sample sources. See the separate data sheet for details. SDE-MIPS is available at an irresistible special price when ordered with P-5064.

Target software and OS

Customers can choose runtime software for P-5064 from:
◆ PMON is a bootstrap/monitor program originally developed by LSI Logic Inc, but placed by them in the public domain. Algorithmics use PMON on all our MIPS products. PMON sources (including Algorithmics’ enhancements) are available free - it builds under our SDE-MIPS toolkit. We can do ports to your hardware on request. P-5064’s ROM has power-on test software built with AlgPOST, our re- usable test framework, available to license for customer designs.
◆ Windows CE is available for most CPUs; OALs for our boards are made by Algorithmics.
◆ We support BSPs for Wind River System’s VxWorks RTOS other OS’, priced according to support levels.
◆ AlgRTX, Algorithmics’ lightweight POSIX-threads RTOS, is available as source code on a one-time license for applications needing a customised but standards-compliant kernel.
◆ OpenBSD (a free derivative of Unix 4.4BSD) runs on P-5064. This offers a reliable and freely reusable multitasking environment for the board; appropriate for customers whose requirements are ease of implementation and porting, rather than real-time scheduling.
◆ Linux is under discussion; ask us if it’s important to you.

Price and Availability

P-5064 is available direct from Algorithmics in England, and first customer shipments were in September 1997.

Technology Access

The P-5064 and its software are open to customers. Schematics and logic programs are available to any customer on request. We encourage customers to re-use logic from the design and can offer transfer and support packages. Algorithmics also provide short training courses, support, and customisation services.

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www.algor.co.uk
Contact: Dominic Sweetman

DDB-VR4121S
Evaluation Board

Description

The DDB-VR4121S is an evaluation board for NEC´s VR4121 microprocessor and it's companion chips. The board provides a working example of a high-performance/low-cost engine for many Windows CE-based products. This hardware is designed to evaluate VR4121 and it's companion chips capabilities and to serve as a reference design for customers. It is also used as a platform to develop and test peripheral hardware, device drivers and software applications. The DDB-VR4121S is pre-loaded with Windows CE OS in Flash ROM so that application level software development can be started right away.

Applications

As the DDB-VR4121S is intended for an easy development of Windows ® CE applications, it provides a variety of ready to use peripherals. Some of these peripherals are integrated into the VR4121 (LCD I/F, Keyboard I/F, Touch panel I/F, Modem I/F, Serial I/O) or into the VRC4171A (LCD controller, PCMCIA controller, Memory controller for external EDO DRAM). There is a parallel I/F and an ethernet I/F implemented for fast downloading and two serial I/F for debugging and communication. The touch panel is mounted on the TFT display to provide a convenient user interface. It is also possible to connect the DDB-VR4121 to a separate monitor when required. In this case both displays are active.
The DDB-VR4121S is using a very modular approach so that additional modules can be easily attached (e.g. VRC4172 module or 3rd party vendor grafic controllers for VR4121).

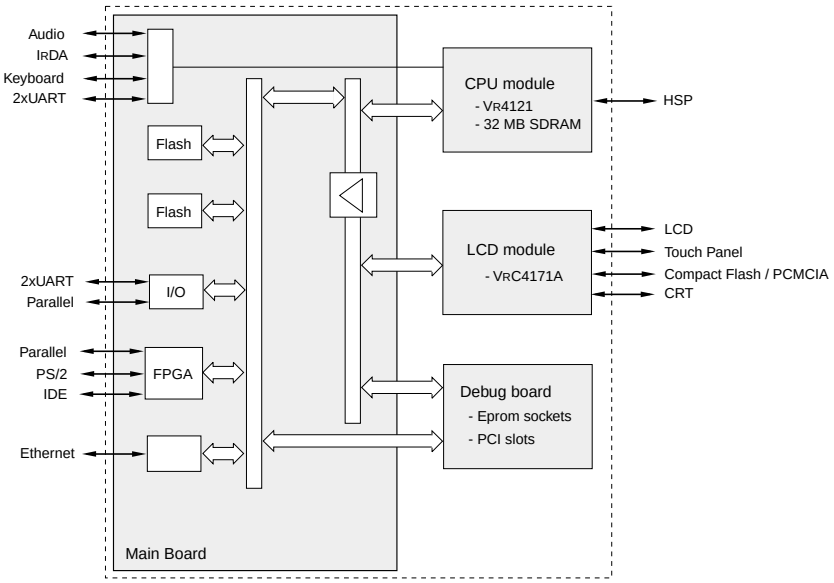
Features

- Optimized for Windows CE development:
  Comes with Windows CE (TM) operating system in Flash ROM (other OS are available); WinCE platform files included on CD
- CPU module:
  - Features NEC´s highly-integrated VR4121 MIPS processor
  - 32MB SDRAM on standard memory socket
  - HSP softmodem I/F
- Main board:
  - 4 MB of system flash (divided into 16 blocks) for boot routines
  - 32 MB of flash (on removable flash miniature cards) for OS images
  - 10/100Mb/s Ehternet LAN Controller
  - two serial, two parallel I/F
  - IDE I/F
  - IDE & PS/2 I/F
  - provides circuitry for VR4121's UARTs, audio I/F, IrDA I/F, keyboard I/F
- LCD controller module:
  - features VRC4171A
  - one compact flash and one PCMCIA connector
  - CRT video output (for direct monitor connection)
- Debug board:
  - provides standard EPROM sockets
  - logic analizer connectors
  - three PCI slots
- One or two PCMCIA card slots, three ISA slots
- NEC's 10,4" VGA colour TFT display included (only for DDB-VR4121S-1)
- Full size matrix keyboard for VR4121
- Convenient ATX standard power supply

RISC by NEC®: Know-how²

NEC

Block Diagram



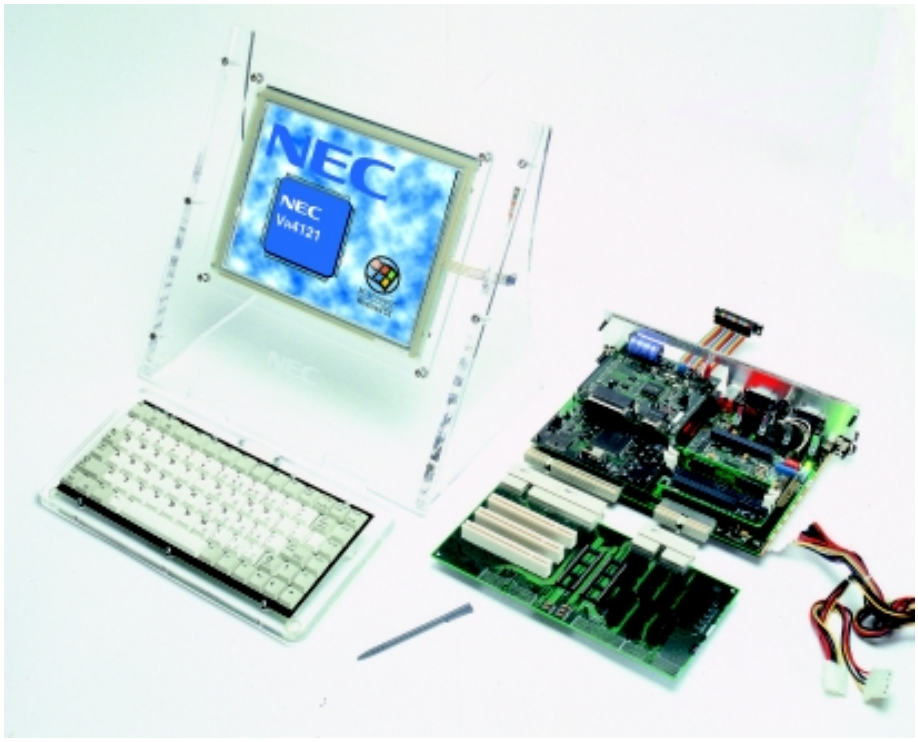
Software Support

Available operting systems for this platforms are Microsoft's Windows CE and Wind River's VxWorks. Please check with your NEC contact for other supported operating systems.
For OS-independant software development a complete toolchain for Green Hills Multi environment is available for this evalutation board.

Ordering Information

DDB-VR4121S-1	Complete Set as described above
DDB-VR4121SE-1	As described above but without NEC's 10,4" TFT display

Contact NEC for newly available other modules.



EB-VR4122-MMI Evaluation Board

Description

The EB-VR4122-MMI is an evaluation board for NEC's VR4122 microprocessor, it's companion chip VRC4173 and the advanced display controller RAVIN (µPD72254). The hardware is designed to evaluate each featured device as well as the complete system solution provided by this reference design. As support packages for both Microsoft's Windows CE and Wind River's VxWorks are provided, application level software development can be started right away.

Applications

The EB-VR4122 is intended to allow an easy development of high-performance handheld portable computing devices, PCI-based embedded systems and man-machine interfaces. The advanced features of the RAVIN display controller contribute especially to automotive applications like navigation system or driver information systems. As the board design is based on a PCI bus it allows an easy extension of funcitionality by various other PCI devices. Additionally this evaluation board features NEC's SPX DSP that take care of a great deal of middleware tasks.

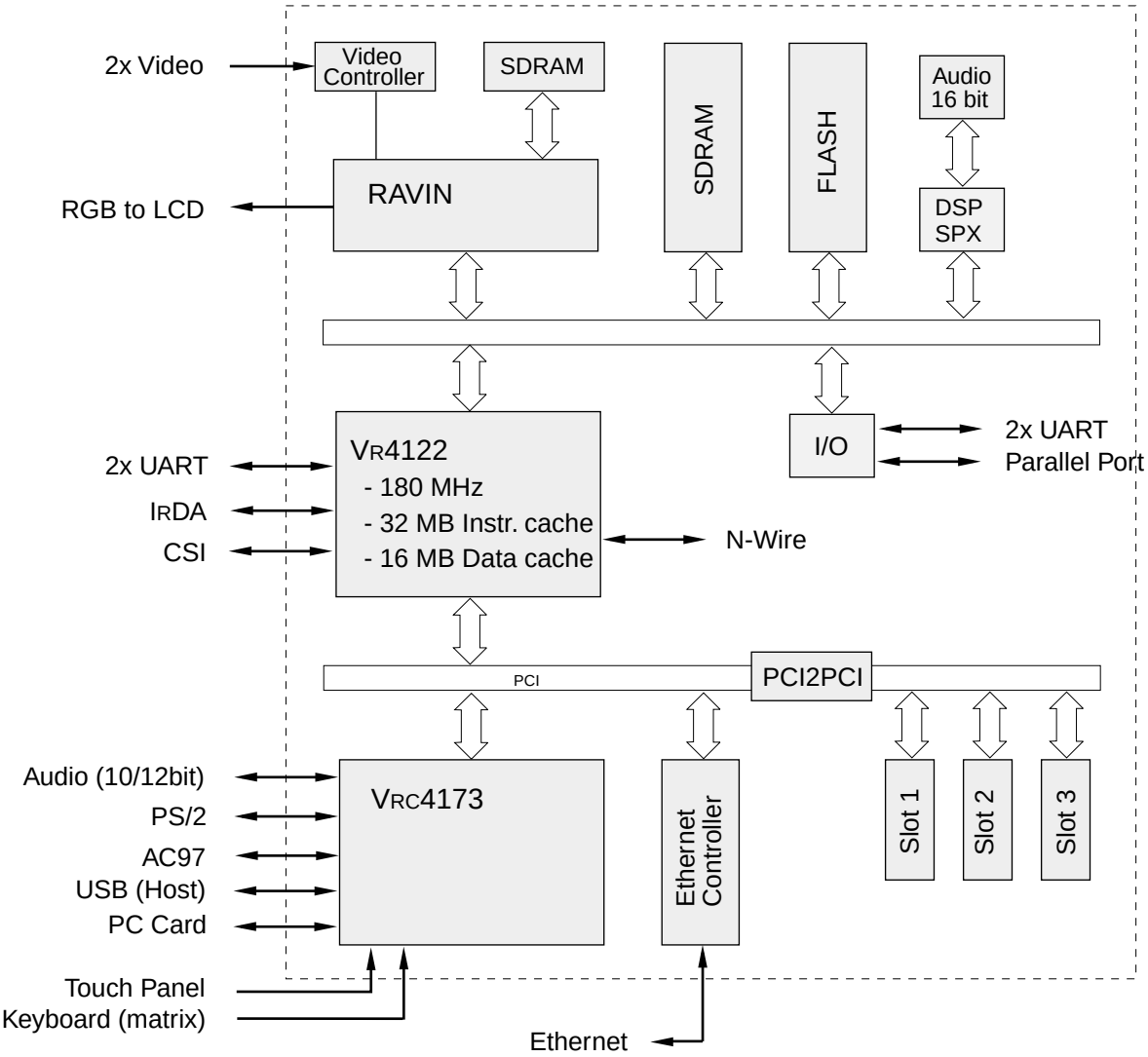
Features

- High performance/ low power CPU VR4122
  - 180 MHz pipeline frequency
  - 16 KB data and 32 KB instruction cache
  - two 16550 compatible serial ports, one CSI, IrDA
  - PCI Host Controller
  - 64 MB SDRAM / 32 MB flash on board
- Highly integrated peripheral chipset VRC4173
  - USB host controller
  - Dual PC card controller
  - matrix keyboard I/F
  - PS/2 controller
  - Touch panel I/F
  - Audio I/F
  - AC97 I/F
- Display Controller RAVIN
  - 2 Video Inputs
  - RGB output
  - 16 MB frame buffer memory on-board
- Other components
  - NEC µPD77110/14 SPX-core based DSP
  - Ethernet controller (100 Mb/s)
  - 16-bit audio I/F
  - Parallel port controller

RISC by NEC®: Know-how²

NEC

Block Diagram



Bonito Evaluation Board

Features

- Choice of CPUs: NEC VR43xx, VR5432; and most other MIPS CPUs with a 32-bit SysAD bus interface. The CPU is fitted on a small daughterboard (compatible with Algorithmics' P-4032 board).
- Good model of a MIPS 32-bit system: P-5032 models the kind of design likely to be found in many applications, with PCI I/O expansion. Moreover, its high usable clock rates and simple, low-latency data paths deliver good performance without too much cost.
- SDRAM memory system: synchronous DRAM modules provide 1 word/clock bursts of 32-bit data at the CPU interface clock rate, between 66-100 MHz.
- PC-world devices for low cost, rich I/O: a whole lot of onboard I/O to solve most interfacing problems.
- PCI expansion: four standard 32-bit 33 MHz PCI bus slots extend the range of devices which can be prototyped.
- Hardware featured for development support: flash ROM for easy reprogramming; onboard ethernet for download/debug from Unix hosts; PC "ATX" power supply and enclosure compatible.
- Dedicated debug port: a feature of BONITO is the debug port. A plug-in board makes all CPU and PCI-memory transactions instantly visible on a logic analyser.
- Modular re-usable design: P-5032's logic design is open. Schematics are available to any customer free of charge; you can license the complete design; or you can obtain permission to reuse chunks of logic for a modest one-off payment.
- PMON monitor and SDE-MIPS integration: the PMON debug monitor is fitted to every board. You can build programs for P-5032 with Algorithmics' SDE-MIPS package, right out of the box.

NEC CPUs Supported

VR4300, VR4305, VR4310 and VR5432

Host Platforms Supported

PC: Windows 9x/NT/2000, Sun Sparc, PC Linux, PC BSD/OS Unix and other Unix systems

Target Systems Supported

Linux, VxWorks/Tornado, OpenBSD and Windows CE support available

Product Overview

Algorithmics' boards are well-known in MIPS circles for quality, reliability, performance - and for the wide range of software support. The new P-5032 will help you get your software running soon and fast. The software and the BONITO design are all available for reasonably-priced licensing.

Detailed Hardware Features

- CPU: your choice: daughterboard options include NEC's VR43x0, VR5432 and other MIPS CPUs with 32-bit SysAD bus. All the above run the MIPS-3 or MIPS-4 instruction sets, compatible with software from all earlier MIPS CPUs. All have substantial onchip caches.
- Most usable CPU configurations are customer-selectable, including the "little-endian" mode.
- BONITO system controller with 100 MHz SysAD and SDRAM interfaces and 33 MHz PCI bus
- Main memory: from 32 - 256 Mbytes synchronous DRAM in PC-type 168-pin DIMM modules. MIPS CPUs need fast, low-latency memory; access latency can be 120 ns or so at the CPU pins and the burst bandwidth 400 Mbytes/s.
- ROM: 1 M x 16-bit reprogrammable FLASH PROM for power-on self-test, PMON boot monitor or other startup code.

RISC by NEC®: Know-how²

NEC

- A 32-pin 8-bit ROM socket is also provided, and meets three different requirements:
  - Holds a 512 Kbyte socketed flash ROM for an alternative bootstrap.
  - Supports an M-systems "Disk-on-Chip™" or compatible high-capacity flash module.
  - Supports an AMC "NetROM™" ROM emulator, for customers who like that way of developing start-up code.
- PCI bus sockets: four standard edge connector sockets. Algorithmics will recommend, re-sell and provide software support for suitable cards for superVGA graphics and SCSI interfaces.
- 10/100 Mb/s Ethernet: using an AMD AM79C973 PCI-bus controller. Supports fast download and host access, essential for a good development environment.
- IDE interface: three DMA-supported channels. Two are implemented by the (Intel) south bridge chip, and will be easily accessed with standard software. The third is local to the BONITO controller and is most useful if the system you're prototyping uses BONITO.
- Other I/O: dual high-speed serial ports, bidirectional centronics (has both a "host" and "printer" port), diskette interface, real-time clock, USB host support, PS/2 keyboard + mouse, general-purpose parallel I/O
- Interrupt control: facilities in both the south bridge and BONITO combined. You can group devices onto different CPU interrupt pins, to provide efficient support for a variety of different operating systems.
- Diagnostic display: a 4-character LED display for diagnostic and debug messages.
- BONITO debug header/card: available as an option, demultiplexes and presents address and data for your logic analyser.

Software support
Algorithmics' SDE-MIPS is a software development toolkit hosted on Windows 9x/NT/2000, Sun SPARC, PC Linux, PC BSD/OS unix and some other Unix systems. The GNU C compiler at the heart of SDE-MIPS supports modern language standards and its optimiser is state-of-the-art. The toolkit has full support for all P-5032's CPU options. SDE-MIPS supports source-level debug of software running on the P-5032 and includes comprehensive libraries and lots of sample sources. See the separate data sheet for details. SDE-MIPS - with 12 months' support/upgrade service - is available at an irresistible special price when ordered with P-5032.

Target software and OS
Algorithmics provide:
- PMON is a bootstrap/monitor program originally developed by LSI Logic Inc, but placed by them in the public domain (Algorithmics use PMON on all our MIPS products).
- PMON sources (including Algorithmics' enhancements) are available free - it builds under our SDE-MIPS toolkit. We can do ports to your hardware on request.
- P-5032's ROM has power-on test software built with AlgPOST, our re-usable test framework, available to license for customer designs.
- Windows CE is available for most CPUs; OALs for our boards are developed and supported by Algorithmics.
- Wind River System's VxWorks/Tornado RTOS is supported - BSPs are available.
- AlgRTX, Algorithmics' lightweight POSIX-threads RTOS, is available as source code on a one-time license for applications needing a customised but standards-compliant kernel.
- Linux is available (Algorithmics supply and can support a pre-configured kernel and compiler, other files from the public archives).
- OpenBSD (a free derivative of Unix 4.4BSD) runs, too.

Technology Access
The P-5032, the BONITO controller and its software are open to customers. Schematics are available to any customer on request. We encourage customers to re-use logic from the design and can offer transfer and support packages. Design IP is incomplete without simulation models and harnesses - we can do those too.

Algorithmics also provide short training courses, support, and customisation services.

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Contact: Dominic Sweetman

DDB-VRC5074 Evaluation Board

Features

- High-performance NEC CPU and ASIC support chips
- 512K onboard secondary cache
- Fast SDRAM memory system
- Three PCI 2.1-compliant expansion slots
- Onboard standard IEEE 802.3 100/10-Base Ethernet interface
- Real-time clock with 32K NVRAM
- Two multiprotocol serial interface ports
- PMON PROM monitor with extensive diagnostics
- VxWorks/Tornado real-time operating system available

NEC CPUs Supported

VR5000

Host Platforms Supported

PC: Windows 95/98/NT, UNIX

Product Overview

The DDB-VRC5074™ evaluation board is designed as a test bed for all the features of the VRC5074 interface controller, as well as the VR5000 microprocessor. It offers the processing power and interfacing capability of a PCI-based evaluation computer.

Hardware Features

- CPU: NEC 64-bit VR5000 at 200 MHz two-way superscalar processor, 32K on-chip instruction cache and 32K on-chip data cache, 64-bit data path, MIPS IV instruction set architecture
- Support chip: NEC's highly integrated VRC5074 interface controller features a glueless interface to the VR5000 processor. A memory controller supports two SDRAM banks and one FLASH memory bank, a PCI 2.1-compliant PCI bus controller, a DMA controller able to transfer data blocks from/to any physical address, an I/O controller with seven programmable device selects, a UART, and timers.
- I/O chip: Acer M1543 super I/O
- Secondary cache: 256 K/512 K
- System bus: 64-bit at 100 MHz
- Memory system: 64 MB onboard SDRAM main memory implemented in one memory bank
- PCI expansion: Three PCI edge connector sockets onboard, standard 64-bit PCI bus running at 33 MHz
- Ethernet: A DEC 21140A 100/10-Base PCI-based Ethernet controller is used to accomplish fast and efficient flow of information between a LAN interface and the PCI bus.
- I/O: Two serial ports implementing the EIA 232 electrical interface for software development and debugging, a bidirectional Centronics-compatible parallel port, connections for a PS/2 keyboard and mouse, a USB port and an RJ-45 connector for Ethernet, a real-time clock, 32K non-volatile memory, a watchdog timer, a bus read timeout timer, and counters and timers with interrupt capability
- Diagnostic display: One 7-segment display for diagnostic and debug messages

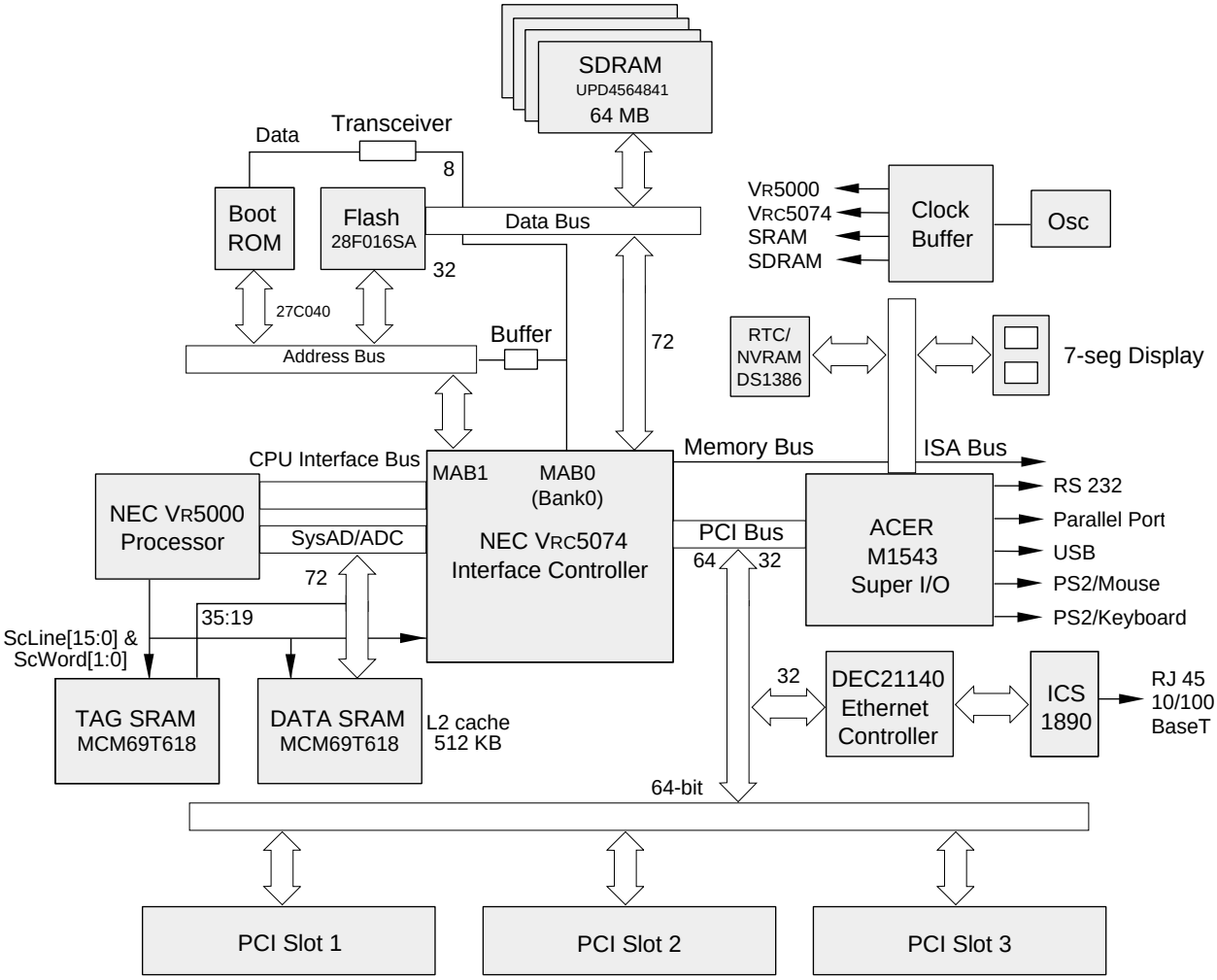
Software Support

- Supports PMON PROM monitor which, provides a flexible environment for users to perform debugging, and users can incorporate any of the code from the PMON source package into their own products with no redistribution or royalty fees
- Capable of running VxWorks/Tornado real-time operating system
- Extensive diagnostic programs for self-test
- Operates in bi-endian mode.

RISC by NEC: Know-how²

NEC

Block Diagram



DDB-VR4181
Evaluation Board (Preliminary)

Description

The DDB-VR4181 is an evaluation board for NEC's VR4181 microprocessor for Palmsize PC-style applications. With its unique combination of peripherals the VR4181 is the one-chip solution for battery operated, compact information equipment with MMI functions. The DDB-VR4181 hardware is made up from two boards: a compact VR4181 mainboard that serves as a reference design for VR4181 based systems, and a debug board providing extra interfaces connections and functions. It comes with a color LCD display of 320 x 240 pixels and Microsoft's Windows CE pre-installed. The mainboard can be operated as a stand-alone system for demonstrations or together with the debug board in the lab. Other operating systems than Windows CE can be supported on demand.

Applications

The DDB-VR4181 is intended to allow an easy development of highly compact handheld portable computing devices and man-machine interfaces. It supports a display, touchpanel a limited number of pushbuttons for easy function control and numerous interfaces. Customers can easily develop their application and driver code on this platform, because the VR4181 reference board represents an average of 80% of the final hardware.

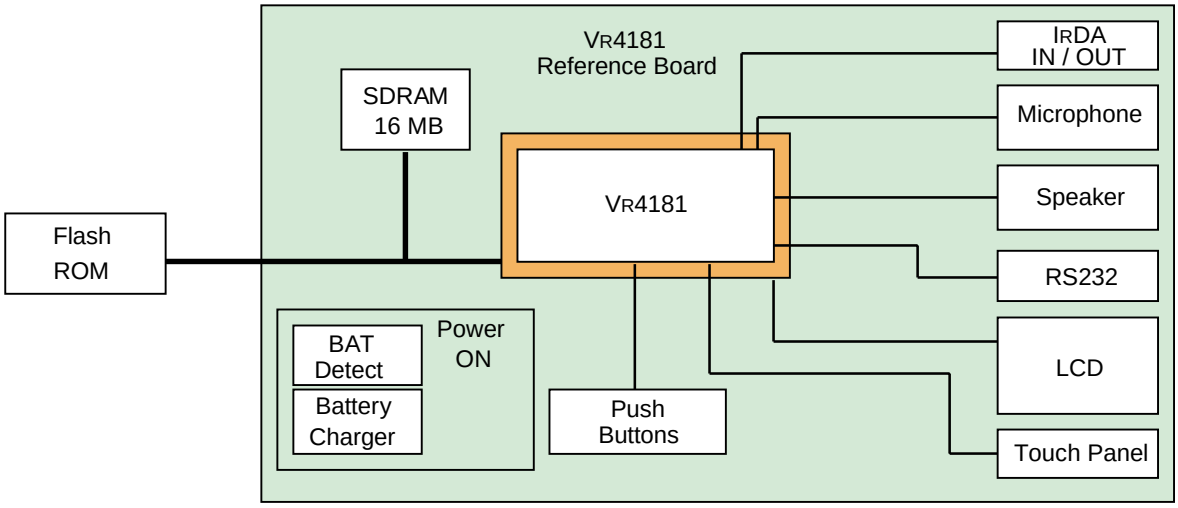
Features

- High performance/ low power CPU VR4181 with
  - 66 MHz pipeline frequency
  - 4 KB data and 4 KB instruction cache
  - external SDRAM/EDO DRAM supported
  - on-chip UMA-based LCD controller
  - 2 serial ports
  - clock synchronous serial interface (CSI)
  - (slow) IrDA
  - USB function interface
  - AD/DA converters
  - compact flash interface
- VR4181 reference board with
  - high-quality 320 x 240 D-STN color LCD with backlight
  - 16 MByte SDRAM on board
  - 16/32 MByte Flash on daughter card
  - touchpanel
  - speaker and microphone
  - IrDA transmitter/receiver
  - compact flash slot
  - pushbuttons
- VR4181 debug board with
  - Ethernet interface
  - additional serial and parallel interfaces
  - boot monitor in EPROM
  - USB connector
  - 4-digit diagnostic display
  - logic analyzer pods

RISC by NEC®: Know-how²

NEC

Block Diagram

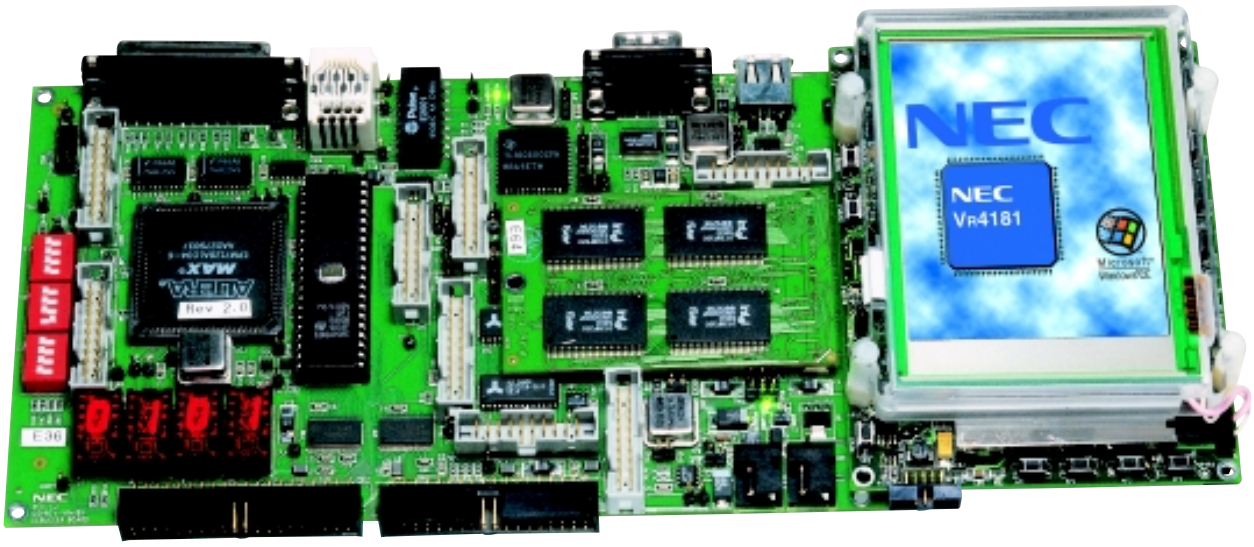


Ordering Information

DDB-VR4181

Software Support

The operating system for this platform is Microsoft's Windows CE. Please check with your NEC contact for other supported operating systems.
For OS-independent software development a complete toolchain for Green Hills Multi environment is available for this evaluation board.



Embedded V90 SoftModem With integrated DAA

Features

- 90dB dynamic range TX/RX paths
- 2-4 –wire hybrid
- Integrated ring detector
- High Voltage Isolation (Up to 4KV for International version)
- Support for “Caller ID”
- Integrated analog front end (AFE)
- Compliant with FCC Part 68, CTR21
- Low power standby
- Low profile SOIC package
- SOIC 16 pins 10x3x1.55mm
- Low power consumption (50mW operating @3.3V)

NEC CPUs Supported

VR41xx

Host Platforms Supported

Windows CE, VxWorks, pSOS

Product Overview

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating within the VR41xx, HSP becomes part of the host computer’s system software. This results in the HSP solution requiring less power to operate and less real estate on the modem board. It is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future. The PCT303W chip set allows for an even higher level of overall modem integration. The highly integrated DAA provides a digital, low-cost, solid-state interface to the telephone line. This eliminates the need for an analog front end (AFE) and attendant isolation transformer, relays and opto-isolators, dramatically reducing the number of passive components by up to 50%.

Advantages

- Lower Cost
- Smaller space requirement
- Longer battery life
- Availability
- Flexibility
- High S/N performance

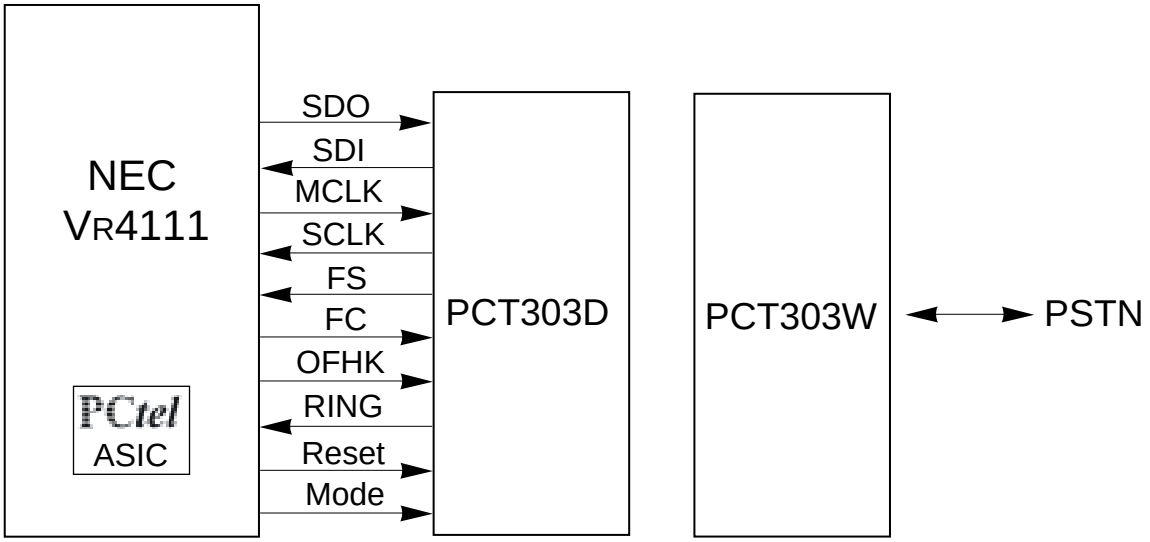
Why PC-Tel?

1. The world leader in HSP Modem technologies.
2. Proven technologies - V.32, V.34, V.90, MIPS and other RISC platforms.
3. Fully tested by huge customer base - 10 million customers in Pentium PCs.
4. Provide a complete solution including hardware/software support from the initial design to final product release.

PCtel

System Block Diagram

Highly integrated VR41xx with embedded AFE (Analog Front End) interface and PC-Tel Codec + DAA (PCT303W Chip Set). See Block Diagram below.
Additional information available: *PCT303W Data Sheet, DAA Reference Design and BOM*.

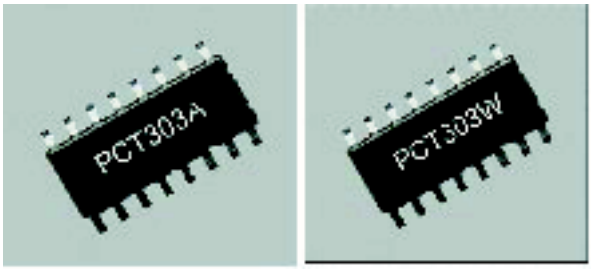


Data Modulation Standards

- ITU-T V.90
- V.34, V.32bis, V.32, V.22bis, V.22 V.21, V.23
  Bell 212A, Bell 103
- Data Compression
  ITU-T V.42bis
  MNP Class 5
- Error Correction
  ITU-T V.42 LAPM
  MNP 2-4

Fax Modulation or Protocol Standards

- ITU-T V. 17, V.29, V.27ter, V.21 Channel 2
  Group 3
  EIA Class I



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Preprocessors/Logic Analyzers/Logic Scope

Agilent Technologies 16700A Series Logic Analysis System

Integrated debugging and analysis tools covering signals to source code

Features

- Intuitive, easy-to-use multi-window interface
- Multiple time-correlated views of data for analog signal to source code execution
- Integral emulation modules coupled with debuggers and real-time analysis help bring hardware and software together
- Inverse assembler for MIPS processors helps debug code execution in real time
- Available state, timing, oscilloscope, pattern generation and emulation modules for correlating measurements to discover cause/effect relation-ships
- Support for over 200 microprocessors, microcontrollers and embedded core processors

NEC CPUs Supported

VR41xx, VR4300

Please visit our web site for more current information on new NEC processors supported.

Host Platforms Supported

Windows 95/NT

Product Overview

The Agilent Technologies 16700A series logic analysis systems offer the power of combined logic analysis and emulation in a simple, cost-effective package. With a large color display, on-screen setup assistant and intuitive user interface, your design team can finally work together to find and solve the toughest problems. In addition, an emulator module and scope or pattern generator may be added. For a fully modular solution with up to 10 measurement modules supporting over 1000 channels and 4 emulation modules you can use the 16700A logic analysis system with the 16701A expansion module.

Key Features

The Agilent Technologies 16700A series logic analysis systems share an intuitive, easy-to-use multi-window interface and common capabilities. A large display with multiple sizeable windows allows you to see at a glance more of your target system's operation. Color lets you highlight critical information so you can find it quickly. Web enable logic analysis make it easy to work remotely. Multiple time-correlated views of data let you examine target operation from different perspectives, to confirm both signal integrity and software execution flow with one tool. This is invaluable in solving cross-domain problems. On-chip emulation for many popular microprocessors together with links to debuggers help you bring hardware and software together into a working system more quickly than with conventional digital debug tools.

Solutions for Digital System Debug

Configure a System with the Modules You Need

Most Agilent Technologies 16500 measurement modules are also compatible with the 16700 mainframes. All mainframes support the following acquisition modules.

Oscilloscope

Agilent Technologies offers a 500 MHz/2 gigasample per second (GSa/s) module and a 250 MHz/1 GSa/s module. Both have two channels and a 32K memory depth. You can use the logic analyzer to trigger the scope at the precise moment necessary to identify a possible ground bounce, metastability, or cross-talk problem.

State/Timing

Agilent Technologies offers a wide variety of state/ timing modules to help you match your tools to your specific measurement needs.

Agilent Technologies
Innovating the HP Way

High-Speed Timing
To help you verify even the most demanding timing requirements, you can get up to 4 GSa/s and 128 K with built-in setup and hold time violation triggering.
Pattern Generation
Agilent Technologies' 200-Mvectors/sec, 40-channel module with 256 K of memory for stimulus can substitute for missing system components or provide a stimulus-response test environment.
Post-Processing Tool Sets Help You Integrate Hardware and Software
When you want to really understand what your target is doing and why, you need to be able to view software execution results in the context of specific hardware events. Agilent Technologies' optional tool sets are available to assist in the processing of captured analysis data.
Source Correlation Tool Set
You can correlate a logic analyzer trace with the source code that produced it and set up the logic analyzer trigger by simply pointing and clicking on a source line. This tool helps you debug your code when you cannot or choose not to halt the microprocessor.
System Performance Analysis Tool Set
You can profile and analyze system performance to uncover bottlenecks in the software or hardware elements within your target.
Serial Analysis Tool Set
This tool lets you acquire and analyze serial data streams to debug problems in peripheral communications.
On-Chip Emulation Tools Make Fixing Bugs Easier
For specific microprocessor families that feature on-chip emulation, you can add a processor emulation module to connect the on-board debugging resources of the microprocessor to the logic analyzer and to a high-level debugger.
Integrated Debugger Support
Agilent Technologies offers you unprecedented visibility into software execution for systems running software written in C and C++. You can achieve the functionality of a full-featured emulator by using a third-party debugger which drives the installed HP emulation module. This gives you active and complete microprocessor run control.
Speed Problem Solving With Off-the-Shelf Solutions for Many Common Microprocessors
Analysis probes are available for over 200 microprocessors and microcontrollers. Bus probes allow probing of popular bus architectures such as PCI, USB, VXI, SCSI, and many others.
For more information about the Agilent Technologies 16700A Series analysis systems visit our web site **http://www.agilent.com**.
For more information about Agilent Technologies test & measurement products, applications, services, and for a current sales office listing, visit our web site at **http://www.agilent.com**

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PI-R5000
Logic Analysis Probe for use with HP Logic Analyzer

Features

- Complete R5000 mnemonic disassembly
- Set-up and data storage on built-in logic analyzer disk drive
- Trace data hard copy available via RS-232 serial port
- Multi-layer, low noise PCB construction with ground and power planes
- Provides complete visibility for all address, data, status, and control lines
- Compatible with HP-16505 prototype analyzer
- Adds real-time trace to R5000 software debug for complete development solution
- Channel configuration assignment compatible with user target board

NEC CPUs Supported

VR5000

Host Platforms Supported

HP Logic Analyser Family

Product Overview

The MIPS R5000 Logic Analysis Probe provides a complete interface between any R5000 target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The MIPS R5000 configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-R5000 Logic Analysis Probe is a non-intrusive development tool and provides a powerful environment for debugging of both hardware and software real-time applications.

The PI-R5000 Logic Analysis Probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and an R5000 target system.

The PI-R5000 Logic Analysis Probe is installed directly to the target board and the R5000 processor is installed into the PGA socket on the preprocessor. The logic analyzer pods provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP Logic Analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 223-pin PGA chip package.

100/500MHz LA A | Listing 1 | Invasm | Cancel | Run

Markers Off — Acquisition Time 09 Jun 1997 15:49:56

Label> / Base>	ADDR Hex		MIPS BE 5000 Disassembly A4.2 A[7:0] Mnemonic		STAT Symbol
0	1FC1F600	00	BEQ	v00,r00,1FC1F668	8 BYTE READ
		04	SD	ra,0030(sp)	
1	1FC1F600		Wait...		8 BYTE READ
2	1FC1F600		Wait...		8 BYTE READ
3	1FC1F600		Wait...		8 BYTE READ
4	1FC1F600		Wait...		8 BYTE READ
5	1FC1F600		Wait...		8 BYTE READ
6	FFBF0030		opcode read		DATA TRANSFE
7	1FC1F668	68	LUI	at,A000	8 BYTE READ
		6C	SW	s00,1A48(at)	
8	AC301A48		opcode read		DATA TRANSFE
9	0000E050	50	Data Write	FFFFFFFF BFC1F698	8 BYTE WRITE
10	BFC1F698		data write		DATA TRANSFE
11	00001A48	48	Data Write	00000007 --------	4 BYTE WRITE
12	00000000		data write		DATA TRANSFE
13	00001A48	48	Data Write	00000007 --------	4 BYTE WRITE

Example Disassembled Trace

CORELIS

Hewlett-Packard Logic Analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

Specifications

- Logic Analyzer Required
  Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers
- Maximum Acquisition Speed
  The maximum acquisition speed is limited only by the speed of the logic analyzer.
- Signal Line Loading
  20pF @ 100K Ohms
- Number of Pods Required
  The PI-R5000 requires six sixteen-channel probes for complete state disassembly.
- Supported Package
  Supports the 223-pin PGA package
- Included
  - PI-R5000 Logic Analysis Probe
  - Disassembler and configuration software diskette
  - Operating manual.

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PI-VR4300
Logic Analysis Probe
for use with HP Logic Analyzer

Features

- Compatible with NEC VR4300 RISC embedded processor chips
- Complete VR4300 mnemonic disassembly
- Display of cycle status information including identification of memory, I/O, and burst addresses
- Quick and easy connection of Logic Analyzer pods to a VR4300 target system
- Low capacitance probing
- Set-up and data storage on built-in logic analyzer disk drive
- Trace data hard copy available via RS-232 serial port
- Multi-layer, low noise PCB construction with ground and power planes

NEC CPUs Supported

VR4300

Host Platforms Supported

HP Logic Analyser Family

Product Overview

The PI-VR4300 Logic Analysis Probe provides a complete interface between any VR4300 target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The PI-VR4300 configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-VR4300 Logic Analysis Probe is a non-intrusive development tool and provides a powerful environment for debugging of both hardware and software real-time applications.

General Overview

The PI-VR4300 Logic Analysis Probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and a VR4300 target system.

The PI-VR4300 Logic Analysis Probe is installed directly to the target board and the VR4300 processor is installed into the PGA socket on the preprocessor. The logic analyzer pods, with HP 01650-63203 termination adapters plug directly onto the mating Mictor connectors on the PI-VR4300 Logic Analysis Probe and provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP Logic Analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 120-pin PQFP chip package.

Hewlett-Packard Logic Analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

CORELIS

Specifications

- Logic Analyzer Required
  Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers

- Maximum Acquisition Speed
  The maximum acquisition speed is limited only by the speed of the logic analyzer.

- Signal Line Loading
  20pF @ 100K Ohms

- Number of Pods Required
  The PI-VR4300 requires four sixteen-channel probes for complete state disassembly.

- Supported Package
  Supports the 120-pin PQFP package

- Included
  - PI-VR4300 Logic Analysis Probe
  - Disassembler and configuration software diskette
  - Operating manual.

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PI-VR5432
Logic Analysis Probe
for use with HP Logic Analyzer

Features

- Compatible with NEC VR5432 processor chips
- Supports the 208-pin PQFP package
- Complete MIPS mnemonic disassembly
- Compatible with HP B4620B software analysis package
- Display of a complete bus cycle per line for maximum trace visibility
- Quick and easy connection of logic analyzer pods to the target system
- Low capacitance probing
- Setup and data storage on built-in logic analyzer disk drive
- Trace data hard copy available
- Multi-layer, low-noise PCB construction with ground and power planes

NEC CPUs Supported

VR5432

Host Platforms Supported

HP Logic Analyser Family

Product Overview

The PI-VR5432 Logic Analysis Probe provides a complete interface between any VR5432 target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The PI-VR5432 configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-VR5432 Logic Analysis Probe is a non-intrusive development tool and provides a powerful environment for debugging of both hardware and software real-time applications.

The PI-VR5432 Logic Analysis Probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and a VR5432 target system.

The PI-VR5432 Logic Analysis Probe is installed directly to the target board via a PQFP clip that attaches to the top of the processor. The logic analyzer pods, with HP E5436A termination adapters plug directly onto the mating Mictor connectors on the PI-VR5432 Logic Analysis Probe and provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP Logic Analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 208-pin PQFP chip package.

Hewlett-Packard Logic Analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

CORELIS

Specifications

- Logic Analyzer Required
  Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers

- Maximum Acquisition Speed
  The maximum acquisition speed is 100 MHz.

- Signal Line Loading
  20pF @ 100K Ohms

- Number of Pods Required
  The PI-VR5432 requires six sixteen-channel probes for complete state disassembly.

- Supported Package
  Supports the 208-pin PQFP package

- Included
  - PI-VR5432 Logic Analysis Probe
  - Disassembler and configuration software diskette
  - Operating manual.

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Personal Line - flexible Logic Analyzer Family for the Windows™ operating system

Features

- Disassemblers without the need of preprocessor hardware for reverse assembly of processor-code with detection and marking of jumps and non executed instructions.
- Easy-to-use graphical user interface operating under Microsoft Windows 3.1x, Windows 95 and NT
- High Level Language Manager for debugging on source code level and trigger on a source code line.
- Software interface for user written control and data display programs.
- Easy documentation through full compatibility to Windows programs like WinWord.
- 32 to 192 channels with external clock rate of 100 MHz, configurable in 16 channel steps sharing either a single clock source or two time correlated clock sources.
- 32K memory depth with full channel count, 64K at half the channels.
- Internal clock rates up to 1 GHz for 72 channels or 144 channels with 500 MHz.
- High impedance 16 channel active logic probes for easy adaptation and minimum loading.
- Powerful 15 level trigger with physical trigger outputs to trigger external devices.

NEC CPUs Supported

VR4300
Others on request.

Host Platforms Supported

PC - Windows 3.1x, Windows 95/NT

Object Formats Supported

COFF, ELF/DWARF, IEEE695, Intel OMF386

Product Overview

The Personal Line (PL) Logic Analyzer Family features up to 192 channels per mainframe, a memory depth up to 32K, external clock rate up to 100 MHz, and internal clock rate up to 1GHz. A full range of triggering capability with interactive data stimulus allows the system to work as an ideal ATE system for user specific applications. The system can be stand alone or slaved to a PC running as an application under the popular MS Windows.

Capabilities include full time-correlated dual processor tracing (expandable to 16 processors), powerful Disassemblers and High Level Language Debugging, a Software Interface to control and operate the Personal Line from user written programs and a 10 ns Time Stamp for time correlation of all busses (processors) being monitored.

Personal Line - Analyzer Family

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proLine
Microsoft-Windows based
Real Time Debug Tool

Features

- Connects to any WindowsNT or Win95/98 PC
- Easy GUI with automatic SetUp
- Supports external bus speeds up to 180 MHz
- Supports Multi-Processor systems
- Raw-Data Bus-Disassemblers support State and Timing recordings without Pre-Processor Hardware
- High Level Language Manager for debugging on Source Code Level
- Link to Software Debuggers
- Rapid Support Service for new types of NEC based ASICs and processors
- Remote control from Unix and Windows workstations using VNC
- Records up to 4 Million Events in a single shot to find even the toughest problems
- Programmable Event Search finds the most complex events within the trace
- Flexible target connection technologies

NEC CPUs Supported

VR4300, all Processors with external Address-Bus

Host Platforms Supported

PC - Microsoft Windows NT and Win95/98

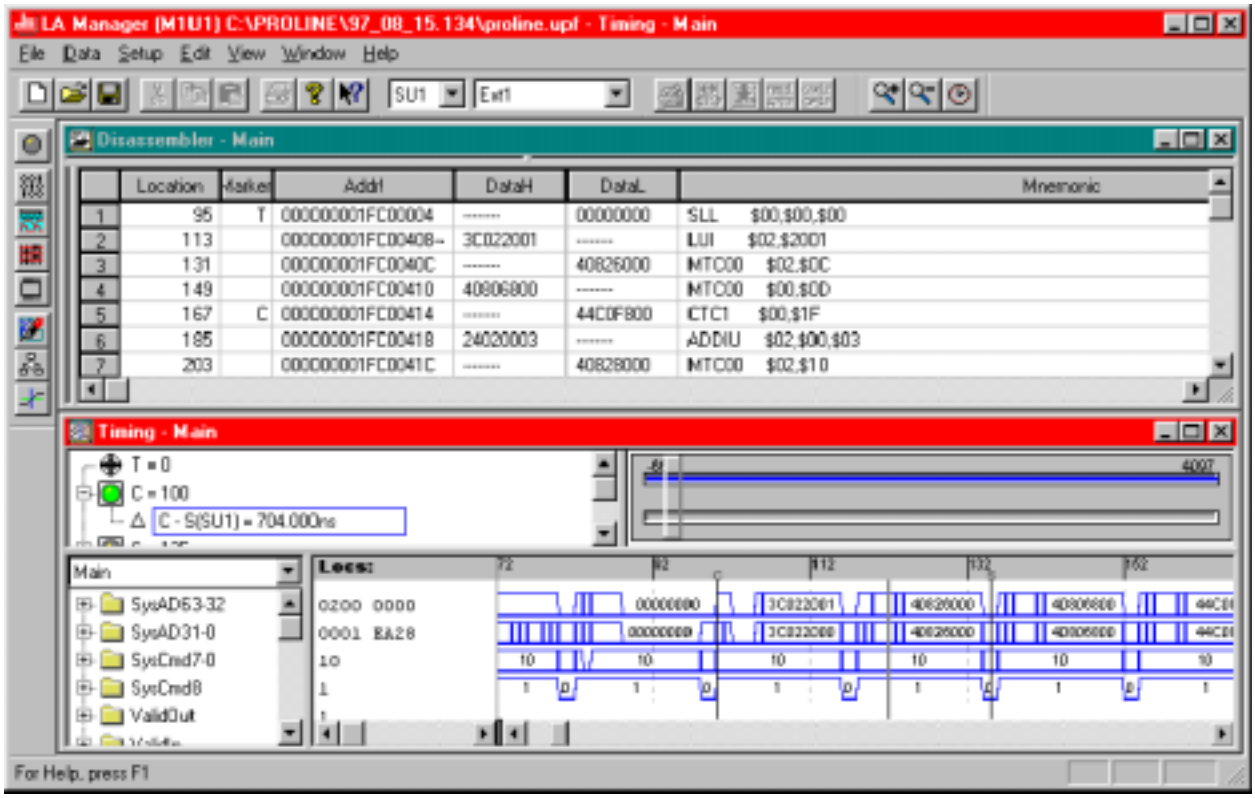
Object Formats Supported

COFF, ELF/DWARF1&2, IEEE695, UBROF

Product Overview

proLine is the latest of dli's Windows based high end logic analyzer systems.
The Hardware supports highest target speeds up to 180 MHz on the external bus, extremely deep memory for ultra long traces as well as most complex Trigger and Trace Conditions at all system speeds.
The Software allows easy handling of most complex situations, offers various time correlated data views, supports easy system SetUp and can be used on any PC even without the instrument connected (e.g. for documentation purposes).
VNC enables full remote accessibility via a local network or the Internet.
Intelligent High Level Language Support provides Source Code Debugging of application programs. including Break/Trigger-Points of the Logic Analyzer on a Source Code Line and correlating the real time trace with the Source-Code.

Member of Controlware Group



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The New TLA 700 Series for Hardware, Software and Integration

The TLA 720 is a benchtop mainframe solution with eleven-slot module expansion capability for high channel count applications.

Features

- Up to 16 Mbits per channel
- Microsoft Windows™ 98 operating system
- MagniVu ™ acquisition technology provides 2 GHz timing resolution on all channels
- 200 MHz state acquisition supports advanced processors and buses
- Simultaneous state and timing analysis through the same probes pinpoints elusive integration faults
- 500 ps timing on all channels
- Four Channel 1 GHz, 5 GS/s DSO provides high fidelity acquisition of analog signals
- Universal source code support for correlating high-level languages with real-time trace
- Performance analysis support for optimising target system performance
- Repetitive acquisition with memory comparison for automated testing
- Remote control using Microsoft COM/DCOM technology supports advanced data analysis

NEC CPUs Supported

VR41xx, VR4300, VR4310

Host Platforms Supported

Windows 98/NT

Product Overview

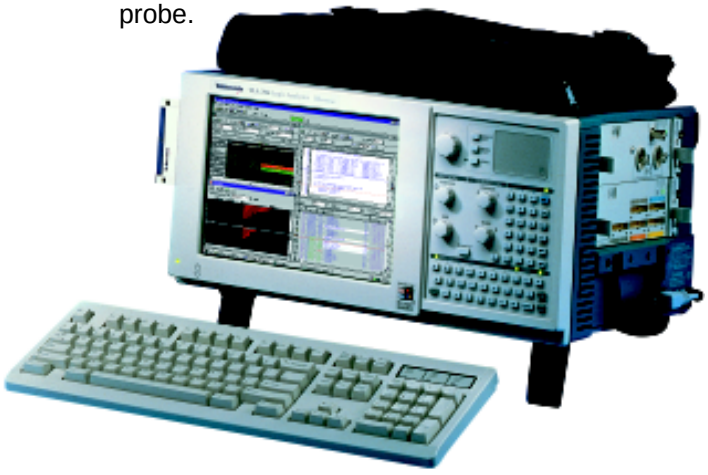
The TLA 700 Series is a new family of instruments developed specifically to address the fast-changing needs of today's digital design engineers. These products bring new technology to bear on the time and design pressures faced by digital system designers. The TLA 700 Series addresses the needs of the entire digital design team. HW developers, HW/SW integrators and embedded SW developers will all find the TLA 700 now provides solutions for those elusive problems that threaten their product development schedules ranging from analog signals to HLL source code. The family consists of portable and benchtop mainframes, logic analyzer modules, DSO modules, and a full line of complementary support products for popular microprocessors and buses.software real-time applications.

Open, industry-standard embedded PC

An open, embedded, Pentium-based PC ensures future expandability and compatibility with a wide range of PC hardware and software.

High Density Probing

The optional P6434 improves ease of connection for debugging today's high-speed microprocessor-based designs by connecting 34 channels with one probe. Both state and timing analysis, through the same probe.



TLA 714 Portable Logic Analyzer

Tektronix®

TLA 700 programmatic interface provides remote control with advanced data analysis
Extensive remote control command set based on Microsoft COM/DCOM technology interfaces seamlessly with Windows applications such as Excel or Visual Basic. Using the TLA 700 as a high-performance data acquisition device, perform advanced data analysis either directly on the TLA 700 or over the network on a remote computer.

Optional 5 GS/s, 1 GHz Digital Scope
Analog data is precisely correlated with digital data so you can see the quality of signals correlated to any problems they cause.

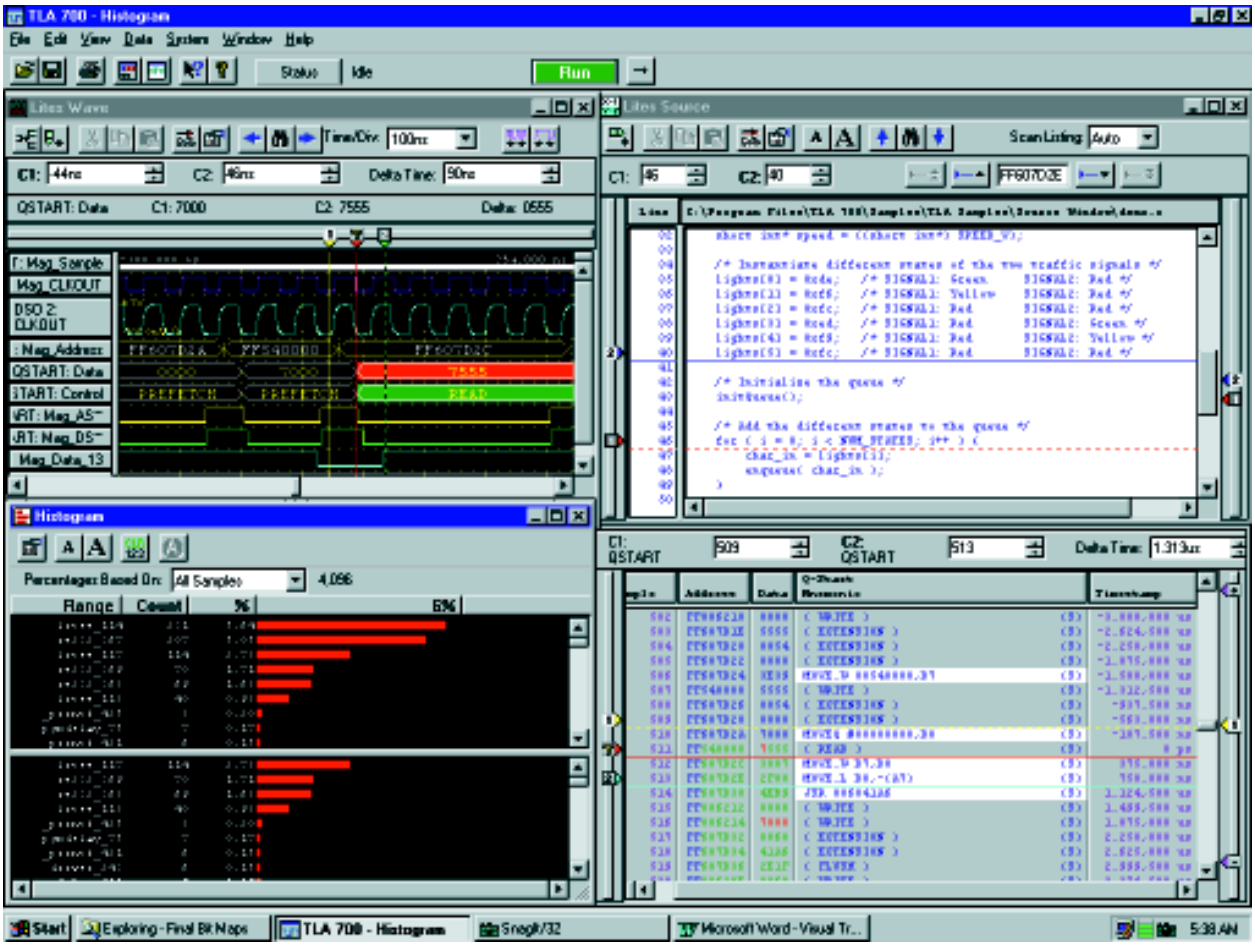
Find elusive problems quickly
Trigger directly on elusive setup/hold time violations over an entire bus. Quickly determine if the cause is intermittent timing violations.

Modular Connectivity
Both the portable and benchtop mainframe share the same modules, so moving instruments around the lab is simple.

Intuitive GUI
Based on Windows™ 98, an interface you already know how to use, so you are productive from the very first time you use the instrument.

State and timing simultaneously through the same probes
The first logic analyzer to offer both 2 GHz timing and 200 MHz state measurements at the same time, on all channels, through the same probes.

View high-level source code and processor mnemonics simultaneously
View processor trace data tightly time-correlated with high-level source code using the information in the object file from your software development environment.



Seeing the big picture from Analog signals to high-level source code:
View waveform, listing, source and histogram windows simultaneously in one large display.

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Logic Scope TLS 216

Features

- 2.5 pF, 1 megaohm Podlet Style FET Probes
- Display Modes: Analog, Timing Diagram and BusFormTM
- <±100 ps Timing Resolution
- 16 Input Channels
- 2 GS/s Simultaneous Sampling on All Channels
- 500 MHz Real-time Bandwidth
- Logic Family Presets for TTL, ECL and CMOS
- Sophisticated Time Qualified Triggering with Four Word Recognizers
- 3-Year Warranty
- Facilitates Hands-free Connection to SMTDevices
- Low Capacitance Probe for Non-intrusive Probing
- Powerful Triggering Reduces Time to Identify Problems
- Flexible Display Modes Simplify
- Recognition of Timing Faults
- High-speed Acquisitions on All Channels
- Facilitate Analysis of Complex System Interactions

NEC CPUs Supported

VR41xx, VR4300, VR4310

Host Platforms Supported

Windows 95/NT

Product Overview

The TLS 216 Logic Scope is a new class of instrument designed to simplify the task of debugging digital hardware. The Logic Scope seamlessly combines in a single instrument the analog acquisition system of a high-speed digital storage oscilloscope (DSO) with the triggering and display systems of a logic analyzer. The 500 MHz bandwidth Logic Scope samples all channels simultaneously at 2 GS/s and has sophisticated time-qualified triggering, a high resolution color display, and an integrated MS-DOS compatible 3.5 inch floppy disk drive.

Sophisticated Triggering to Identify Complex Digital Problems

In addition to edge trigger, most digital signals can be easily captured using pulse, glitch and pattern triggers. The Logic Scope provides two new trigger resources that allow the instrument to directly trigger on common digital circuit behavior. The industry's first time-interval or sequence trigger type monitors the time between two events, allowing the instrument to easily trigger on setup time violations, hold-time violations, or unexpected propagation delay. The powerful "Time-out" trigger type can be used to capture incomplete handshake sequences or to trigger the instrument when the DUT "hangs". All of these trigger types let developers identify channel-to-channel relationships, including 16-Bit patterns and time-related/time-qualified system faults. The Logic Scope's external trigger-input can be used as a "Trigger Arm" to enhance cross-triggering between two instruments, simplifying the task of using a Logic Scope with other test equipment.

2.5 pF, Low-Mass FET Probes Ensure Non-Intrusive Connection

The Logic Scope includes a set of 16 specially designed probes that have extremely low probe-tip mass (1.5 grams) and input capacitance (2.5 pF). The low probe-tip mass ensures that connections made to surface mount and fine pitch ICs will be reliable. The low input capacitance, combined with the 1 mega-ohm input resistance, decreases the effect of the probe on the DUT's operation, allowing very accurate measurements to be made with confidence.
These characteristics are made possible by using a "podlet-style" probe-tip design instead of the "pencil-style" design of traditional oscilloscope probes. Employing the de facto industry standard of 0.1 inch spacing between the signal and ground inputs, each 0.1 inch thick podlet can directly attach to the hundreds of readily available IC adapters and clips.

Applications
Hardware Performance Verification
Multi-channel Data Acquisition
Mixed Signal Analysis
A/D and D/A Analysis
Hardware Timing Analysis

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To find out more information please look at our Test and Measurement website where you can request information to be sent to you by selecting the Contact Tektronix option.

Data Generator
DG2020A * P3410/P3420 * DG2030 * DG2040

Features

DG2000 SERIES (DG2020A, DG2030)

- Output Data Rate to 400 Mbits/s Maximum (200 Mbits/s DG2020A)
- Data Length to 256 K/channel (64 K/channel DG2020A)
- Multiple Output Channels:
  DG2030: 4 or 8
  DG2020A: 12, 24 or 36
- Independent Variable Delay Output:
  DG2030: 4/8, 100 ps res., -5 ns to 18 ns
  DG2020A: 4/8/12, 20 ps res., to 20 ns
- Variable Output Level:
  DG2030: -1.5 V to +3.5 V, 5 Vp-p (50 Ohm)
  DG2020A: P3410 (TTL), P3420
  (-2 V to +7 V,9 Vp-p (open))
- Variable Rise & Fall Time Control (independent) (DG2030)
- Flexible Sequence Control and Data Jump Tri-State Control
- Powerful and Easy-To-Use Data Built-in Editor
- Data Import from Various Instrument and Other Source
- DG-LINK S/W Supports ASCII/CSV Data Import

NEC CPUs Supported

VR41xx, VR4300, VR4310

Host Platforms Supported

Windows 95/NT

Product Overview

DG2020A, DG2030 Data Generators
The Tektronix DG2020A and DG2030 digital data generators combine the high performance needed to test the latest technology devices with unprecedented ease of digital data creation and modification. The DG2020A and DG2030 are used to replicate valid, marginal and erroneous digital conditions that a design could encounter. What separates the DG2000 series from other digital pattern generators is its superior user interface combined with high performance. Everything needed to load, modify, and output
vectors is built-in. Capabilities such as advanced sequencing (looping nest), built-in encoding schemes, and flexible editors make the DG2000 Series a powerful addition to your suite of test instruments.

DATA OUTPUT
The DG2020A offers the data rate up to 200 Mbps, 64 k data words length, up to 36 output channels in 12 channel increments and 100 ps timing delay control up to 20 ns function in the portable main frame.
P3410 output pod provides TTL level signal from a grouped pin-header connector. P3420 variable output pod provides 500 mV to 9 Vpp (-3 V to 7 V), 100 mV increment that covers ECL, TTL
CMOS logic level. Output connections consist of independent SMB connectors for each channel. The P3420 is capable of >30 mA of current sourcing, enough for your most demanding applications.
The DG2030 offers the data rate up to 400 Mbps, 256 k data words length, up to 8 output channels in 4 channel increments. Output voltage is from -1.5 V to +3.5 V (250 mVp-p to 5.0 Vp-p) into 50 Ohm
that covers most popular technologies like CMOS, ECL/PECL, and TTL. Delay function supports from -5 ns to +18 ns with 20 ps increment. Tr/Tf is able to control independently from 500 ps to 8 ns.

POWERFUL AND EASY-TO-USE DATA BUILT-IN EDITOR
The powerful built-in Data creation and editing capability allows you to create and modify your data streams quickly and easily. Data can be graphically created using the built-in functions including counters, shift registers, serial data and clocks.

EXTENDED FUNCTIONARY WITH SEQUENCING
Sequencing is a capability that extends the 256 k (DG2030), 64 k (DG2020A) record length and allows external events to control data flow. Each line in the sequencer can be controlled by an external event that can cause a jump to a different block of data. The DG2000 series can have up to (2000: DG2020A, 4000: DG2030) jumps (one per line) at the full clock rate and has specified latency that can be accounted for. External, Event and Inhibit, that can control the flow and impedance of the sequence.

IMPORT THE DATA FROM OTHER SOURCES
Getting data into the DG2000 Series is simple with multiple import options from several sources. Data can be imported from several Instruments including the Tektronix TLS216 logic scope, GPX logic analyzer, 2000 Series arbitrary waveform generators, and TDS Series scopes. To import data from other sources, a comma separated variable (CSV) format is supported. DG-Link application program for the PC (Windows* 95 environment) supports ASCII file format vector import such as TLA700 Logic analyzer or logic simulation software output vector, which can be converted to DG2000 Series file format and send via GPIB or floppy disk.

Applications
Replicate Vector Data from Simulator
Characterize a Device's Timing and Amplitude Margin
Replicate Data from Unavailable Part of the System
Inject Infrequent Faults to Test Fault Tolerance
Semiconductor (ASIC/FPGA/DAC)
Storage Media Write Data (HDD/FDD/MO/DVD)
CCD (Area, Liner) Image sensor
Printer, Copy (Color/Laser) Digital Graphic Data
LCD (STN/TFT/MIM) Display Device Drive/Control
Logic Board/Bus Simulation

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www.tek.com/Measurement/

In-Circuit-Emulators

NetICE™-5432
LAN-based JTAG/ROM Emulator

Features

- Real-time non-intrusive emulation of the VR5432 MIPS processor
- Optional support of VR5432 real-time trace via the JTAG port
- Integrates the power of a local area network into the entire development process
- Powerful C/C++ source-level and assembler debugger
- Intuitive Windows™95/98/NT GUI
- Supports maximum processor clock speeds with zero wait-states
- Requires no hardware or software resources from the target system
- Program download to target RAM
- Debug code in ROM, Flash, and RAM
- Up to 8 Mbytes ROM or RAM emulation option for very fast code downloads
- Compatible with Corelis SCANTEST™ family of boundary-scan test tools

NEC CPUs Supported

VR5432

Host Platforms Supported

Windows 95/98/NT

Product Overview

The NetICE-VR5432 is an innovative LAN-based in-circuit emulator that provides a real-time, non-intrusive development environment for the NEC VR5400 MIPS processor. The NetICE-5432 connects any VR5432 processor-based target into a network node that is accessible from any Windows 95/98/NT-based PC for all development and debug activities. This capability is enabled by the NetICE-5400 full TCP/IP protocol stack. Downloading code from the host to the target through its JTAG interface is fast and is accomplished over the Ethernet using TCP/IP protocol that is available on most PCs that are connected to a LAN.

An optional ROM emulator allows very fast Ethernet code download to the target via its ROM sockets. It also allows the insertion of multiple software breakpoints into the ROM address space.

An optional real-time trace feature is available that allows a user to retrieve trace information via additional processor pins.

The Corelis NetICE-5432 emulator utilizes the industry standard IEEE-1149.1 (JTAG) boundary-scan test port to access the internal debug resources available on the NEC VR5432 MIPS proces-sor. Since the boundary-scan logic of the VR5432 processor is separate from the core processor logic itself, this access mechanism allows complete, non-intrusive access to any processor resources. Thus, no interrupts, RAM, ROM, nor registers need be assigned for debug purposes and no ROM-based debugger or loader program is required. At the same time, no peripheral resources such as serial ports are needed to communicate with the emulator/debugger. The NetICE5432 allows users to debug high-speed, cached applications at the full speed of the target processor.

In addition to these benefits, use of the JTAG interface also ensures that processor access is maintained even when the processor 'hangs' or otherwise runs out of control.

WindowsTM95/98/NT-based host software provides a complete symbolic 'C' source-level debugging capability and is compatible with all popular cross-compilers that support ELF/DWARF of COFF files. The source-level debugger is a 32-bit Windows 95/98/NT applicat-ion. Interaction with the source-level debugger is through re-sizable windows, context sensitive user programmable tool-bars, menus, and dialog boxes. There is no need to learn a command-line interface for interactive usage.

Individual windows can simultaneously display source code, disassem-bled code, memory, 'C' variables, processor registers, files, and log event messages.

CORELIS

Programs and data can be down-loaded to any part of the system RAM through the JTAG port without the need for a resident loader program. The JTAG interface is a simple interface that connects to the target system via a flexible ribbon cable and does not require removing the microprocessor. The JTAG interface is controlled by a Corelis-developed, high-performance, LAN-based, boundary-scan controller that can be easily connected to a network. Due to the unique nature of the NetICE-5432 emulator, the same hardware controller can be used for many different processors that have IEEE-1149.1 compatibility. Thus, a developer using a VR5432 processor can migrate to other processors as-required and retain his investment in hardware tools by merely installing another version of the Corelis NetICE emulator software.

Supported functions include:

- Reset processor
- Start and stop program execution
- Real-time trace buffer access
- Set breakpoints in RAM
- Set breakpoints in ROM or Flash using hardware breakpoint
- Single-step source or assembly lines
- Single-step into or over function calls
- Step into, over, or out of functions
- Display and modify processor registers
- Display, modify, and fill memory
- Disassemble memory using VR5400 mnemonics
- Download code
- Powerful macro capability

The NetICE-5432 JTAG emulator lets you modify information displayed in a window by typing new values directly into it. For example, this feature allows you to directly write to or modify a memory location.

Source and Assembler Debugging
The Corelis NetICE-5432 emulator includes a powerful source-level debugger. The debugger supports multiple windows thus allowing the developer to view many different processor activities simultaneously. For example, multiple windows can be established to view source code, assembly code, variables, register locations, etc. When viewing source and assembly code for example, the debugger can display source code corresponding to a particular line of assembly code and vice-versa. Four different types of variables can be viewed:

- Variables local to a function
- Variables static to a file
- Global variables
- Individual variables or the heap (via pointers) can also be viewed.

Memory locations can be displayed in a hex or floating-point format. The current history of function calls (stack trace) can be displayed by activating a toolbar icon.

Real-Time Trace (optional)
The NetICE-5432 is available with an optional feature to take advantage of the trace capabilities in the VR5432 processor, providing non-intrusive re-construction of application code execution flow. Trace information is retrieved via the four TrcData lines and 1 TrcCLK line in real-time and then used with the contents of processor memory to re-construct program flow. Trace data is valid whether the processor is running out of memory or instruction cache. A screen is provided to allow control and management of events that can initiate the trace collection activity.

Logging
The NetICE-5432 emulator can log an entire debug session and then play it back. “Event” logging is also supported and a log file can be created whenever an asynchronous event such as a breakpoint or processor halt occurs.

Command Files
Any group of commands can be placed in a list and executed automatically. This provides the ability to run regression tests and other lengthy tests that are best done without operator intervention. Extensive command files can cause the NetICE-5432 to execute the same command more than once with different parameters or to execute a command with a non-default parameter.

User Interface
The Corelis NetICE-5432 user interface was designed for usability and as such is the most intuitive debugger available for embedded systems debugging. One of the most powerful features of the NetICE-5432 is its extensive macro capability. By using macros, the debugger can be made to look like other debuggers or editors as well as saving keystrokes. Collections of macros can be created by building a “macro table.” An unlimited number of these tables can be supported. Powerful macro sequences can be bound to toolbar buttons, keys, breakpoints, and other debugging events.

NetICE-5432-JR ROM Emulation Option
The ROM emulation option is designed for users that want to debug targets that include processors with JTAG debug functionality-such as the VR5432-but want to enhance this functionality with additional features such as ROM space breakpoints, faster code download, code download into the real ROM space, etc.
The NetICE-5432-JR emulator has all the JTAG as well as ROM emulation features. This functionality is achieved by adding a ROM emulator card option to the JTAG emulator.
The NetICE-5432-JR combines the benefits of JTAG emulation and ROM emulation into a single system. Combining the on-chip access to debug registers and the fast download of object code associated with ROM emulation, the NetICE-5432-JR provides the most powerful LAN-based debug tool available. It takes a few seconds to download 1 Mbyte of code into the target’s memory.
The combination of JTAG and ROM emulation is designed for users that want to debug targets that include processors with JTAG debug functionality but want to enhance this functionality with additional features.

The ROM emulation option adds the following capabilities to the NetICE-5432 JTAG emulator:

- Fastest code download via Ethernet
- Execution of code from the target’s real ROM address space
- Multiple breakpoints in the ROM address space.

The NetICE-5432-JR emulator does not require a ROM monitor that is typically required by traditional ROM emulators. All of the target CPU run control and debug features are accomplished via the JTAG interface.

Ordering Information

Specify:
- NetICE-5432 (without ROM emulation)
- NetICE-5432-JR (with 2, 4, or 16 Mbyte ROM emulator)

Included

- Emulation source-level debugger on 3.5” disk
- Net 1149.1 boundary-scan controller
- Emulation cable for PowerEM
- User’s manual
- Power Supply

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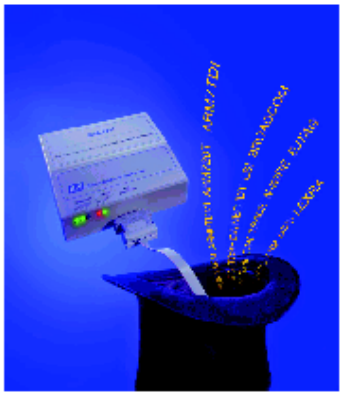
MAJIC^{PLUS}™ Multi-Processor Advanced JTAG Interface Controller



MAJIC^{PLUS}

Features

- Ideal for SoC based applications
- 32 X 512k trace memory
- Non-intrusive, uses no target resources
- Execution tracing from embedded flash, ROM, or cache
- Supports a wide choice of on-chip debug interfaces
- Supports a wide variety of CPU cores
- Supports on-chip hardware breakpoints
- Unlimited software breakpoints
- Programmable JTAG Clock (TCK = 0 to 40 MHz)
- Trigger-in and Trigger-out connections
- Ethernet and Serial I/O Ports for fast, flexible host interface
- High speed download (>200k bytes per second) of application code
- Network compatibility allows shared and remote operation
- Flash Memory for easy firmware updates to support for additional CPU cores or on-chip debug interfaces
- Sleep-mode support
- CE Marked for operation within the EC
- LED's display operation status
- Open API for debugger interface

NEC CPUs Supported

VR43xx

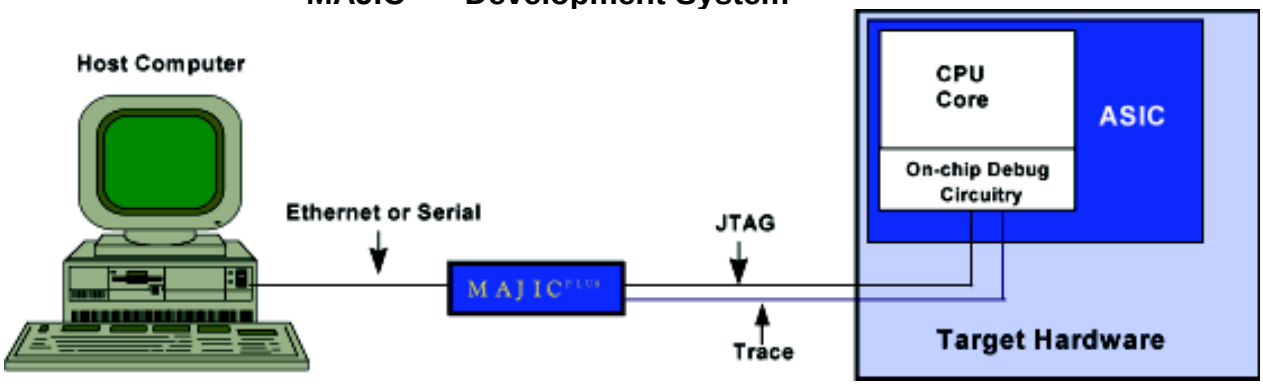
Host Platforms Supported

Sun-4: SunOS, Solaris
PC: Windows 95/NT
HP 9000: HP-UX

Product Overview

The MAJIC^{PLUS} emulator provides a high speed hardware interface between processors with an on-chip debug interface and industry standard debuggers. It is available with a choice of EPI debuggers and may be adapted for use with RT/OS aware debuggers from leading RT/OS vendors. The unit is self contained in a small case approximately 2 inches x 6 inches x 7 inches in size. Now, engineers using SoC devices can have the same level of control and visibility of the embedded CPU operations as they would with in-circuit emulators in traditional discrete CPU designs. The result is faster software integration, better testing, and improved time to market. The MAJIC's ability to expand to support additional cores, debug interfaces, or SoC devices eliminates the need to buy new emulators for each new project, thus reducing project costs. Completely non-intrusive, the MAJIC^{PLUS} communicates to the CPU core by JTAG using the existing boundary scan pins. It uses no target memory and requires no porting to the target system. Complete processor control means you can start, stop and single-step execution; read and write to registers, memory, and system I/O; and download code to target RAM – all within most industry standard debugger interfaces. Complete visibility means that you can now trace program execution on the deeply embedded CPU core. Using on-chip debug facilities such as PCTrace, N-Trace, and Real Time Debug, the emulator provides real-time visibility into the program's behavior even when the CPU is executing from cache, flash, or ROM embedded within an SoC. You may adapt the MAJICPLUS for plug and play operation with your specific processor or CPU core by selecting from a wide range of configuration kits. The kits contain the firmware and user license to match your CPU's on-chip debug facilities. Install multiple configuration kits, and the MAJIC^{PLUS} will support a variety of CPU types. The configuration kits also contain the adapters, accessories, and target interconnection cables required for the selected CPU. The MAJIC^{PLUS} is ready to run with the EPI software tools and any development board that supports a connection to the on-chip debug interface. This combination of tools will work together to provide you with a proven working environment. The MAJIC^{PLUS} is available as a stand alone unit or as a complete emulation kit. The kit comes with serial and Ethernet cables, source-level debugger, documentation, and one year of free maintenance, support, and updates. Part number: MAJIC^{PLUS}-KIT. Full development kits are also available that include a full compilation toolkit See the MAJIC Price and Configuration Guide for full details of these development kits.

MAJIC^{PLUS} Development System



Ethernet Interface
The 10base-T/100base-T Ethernet interface provides many advantages over serial or parallel interfaces to the host. Download of your application code is over ten times faster than with serial interface. This will significantly reduce the amount of time spent waiting for code changes to download to your target board. Network connection allows remote operation of the MAJIC^{PLUS}. Now you can access the lab setup directly from your desktop. This allows multiple engineers to share a common test bench.

Real-time Execution Tracing
The MAJIC^{PLUS} fully supports the instruction and data tracing of a wide selection of on-chip trace facilities. It provides 32 x 512K of configurable trace memory. Trace data from the on-chip trace interface may be synchronized with an 8-bit general purpose trace input probe. Trace capture may be enabled and disabled by external events. When combined with the EPI debuggers the system provides full real-time execution tracing of microcontrollers and SoC devices having on-chip cache, flash, or ROM.

Flash Memory
The MAJIC^{PLUS} firmware is easily upgraded without the need to replace ROMs. Install new configuration kits easily and quickly using the simple program provided. You can add support for multiple CPU types to the MAJIC^{PLUS} with a simple firmware upgrade. New firmware updates will be available on the our FTP site. Use the simple program provided to automatically program the updated firmware into the on-board flash memory. Flash memory makes it easy to program an IP address into the MAJIC^{PLUS} for point-to-point ethernet connection to a PC or workstation.

Internal RISC Processor
The use of a high performance internal RISC processor allows fast response to debugger operations such as single stepping, reading and writing memory, reading and writing registers, and downloading of application code to the target.

Choice of Configuration Kits
You may configure the MAJIC^{PLUS} to support one or more of the supported combinations of CPU core and on-chip debug interface. Each configuration kit includes the firmware, user license and interconnections necessary to support the CPU that you have chosen. Please refer to the Configuration Kit data sheet for detailed specifications on the CPUs and on-chip interfaces currently supported.

Programmable JTAG Clock
The MAJIC^{PLUS} features a programmable TCK with a 0 to 40 MHz range. This allows you to tailor the JTAG operation to match the performance of your target. It also means that you can use the MAJIC^{PLUS} with low speed ASIC emulators or with devices that feature sleep mode operation.

Status LEDs and Reset Switch
The MAJIC^{PLUS} provides five LEDs which show the operational status of the emulator. A convenient reset button is protected against accidental activation, yet is easily accessible by the user.

CE Compliant
The MAJIC^{PLUS} is compliant with applicable safety and EMC requirements. It is CE marked for use within Europe.

International Power Supply
The MAJIC^{PLUS} operates from a standard 5V power source. It comes with an external UL/CE approved AC adapter whose AC input range is compatible with all international AC voltage and frequency ranges. A standard three-wire power connector is compatible with readily available power cords through the world.

Specifications:

MAJIC ***PLUS***

Target Control:	JTAG
JTAG clock(TCK):	0 to 40 MHz Programmable
Download Speed:	>200k bytes/sec (Typical)
Trace Memory:	32 bits x 512K Configurable
Trace clock(DCK):	0 to 100MHz
Trace Control:	Trace disable BNC, TTL level
Target voltage:	2.4 to 5.0V
Serial interface:	RS232C 1900-115.2k baud
Ethernet interface:	10/100Base-T, TCP/IP
Triggers:	Trigger input Trigger output
Trigger Levels:	TTL
Indicator LEDs:	Power, Status, Run, Connect. Ethernet
Size:	2.0 H x 7.4 W x 6.5 L (inches)
Weight:	2.25 lbs
Input power:	5 VDC +/- 5%, 4.0 A
Power connector:	2.1 mm coaxial, center positive, male
Temperature:	Operating 0 - 40 degrees C
Humidity:	Operating 15% - 95% RH
Safety/EMC	CE

External AC Adapter

Output:	5 VDC, 4.0 A
Input voltage:	90 - 264 VAC
Input frequency:	47 - 63 Hz
Input power:	0.8 A
Size:	1.6 H x 2.8 W x 4.8 L (inches)
Weight:	10.3 oz
Compliance:	UL, CUL, CE, TUV
AC connector:	EN 60320/13
DC connector	2.1 mm coaxial, center positive, female

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Model SYS4K In-Circuit Emulator

Features

- Up to 50 hardware breakpoints
- Up to 8 megabytes overlay memory
- 32K deep trace memory
- Optional real-time profiler
- Three Dimensional Trace Control™
- Single step in ROM and exception handlers
- Built-in memory tests and scope loops
- Download up to 3 megabytes per minute
- 16 external Logic Inputs
- Emulate without changes to code
- Assembly level debugger
- Available source level debugger
- Ethernet and serial interface to host

NEC CPUs Supported

VR4300, VR4310

Host Platforms Supported

Sun-4: SunOS, Solaris
PC: Windows 95/NT
HP 9000: HP-UX

Product Overview

The Model SYS4K is a full featured In-Circuit Emulator for NEC's VR RISC processors. EPI meets the critical demands of the RISC development environment by combining the features of a high-performance logic-state analyzer and high speed emu-lator with a fully integrated suite of software deve-lopment tools supporting both 32-bit and 64-bit environments. This combination provides designers with an extremely powerful debugging environment that improves productivity throughout the development cycle, including bring-up of prototype hardware, debug of application software; and troubleshooting - both in development and production environments.

Debuggers — *Don't Wait to Get Your Code Working*
EPI offers two environments for debugging. EDB is a powerful windowed source-level debugger for C and assembly language programs. For rapid debug of your C code, EDB fully integrates C source level debugging with the capabilities of the emulator including synchronizing the source window with the trace display.
MONICE, a symbolic assembly-level debugger, offers features especially useful to hardware engineers for prototype debug, automated testing, and manufacturing test. It is source-language independent making it equally useful debugging code written in assembly, C, ADA, or other languages. Both debuggers employ the facilities of a host computer to manage the user interface, symbol tables, file systems, etc. This leaves the emulator free to manage and track the target system. These debuggers also work with EPI's target resident debug kernel (RSS-MIPS) to provide very low cost debug stations. Without learning a new debugging interface, developers can easily access networked emulators when their power is needed to track down the elusive bugs that can kill a development schedule.

High Speed Download — *Don't Wait to Say GO*
The SYS4K emulator can download code and data into your target at Ethernet rates or up to 600 k bytes per minute over serial RS232. Downloading at these speeds dramatically increases the number of **Debug-Fix-Download-Test** cycles a software engineer can do every day so you deliver your product sooner.

Overlay Memory — *Don't Wait to Burn PROMS*
With the overlay memory options you can map up to eight megabytes of memory into your target system. With it you can down-load code to target memory space that contains ROM. You will never have to burn a ROM again until your product is ready for final tests. When your code is executed from overlay memory you can set software breakpoints in ROM space. You can explicitly program initial accesses and block refill wait-states or match your target's performance exactly by using its acknowledge.

On-line Assembler — *Don't Wait to Test a Fix*
The debuggers' on-line assembler makes it easy to try a "fix" without waiting for a rebuild of your code. You can "patch" your code instantly, then ***Go*** to test the change. There is no need to compile and link the application.

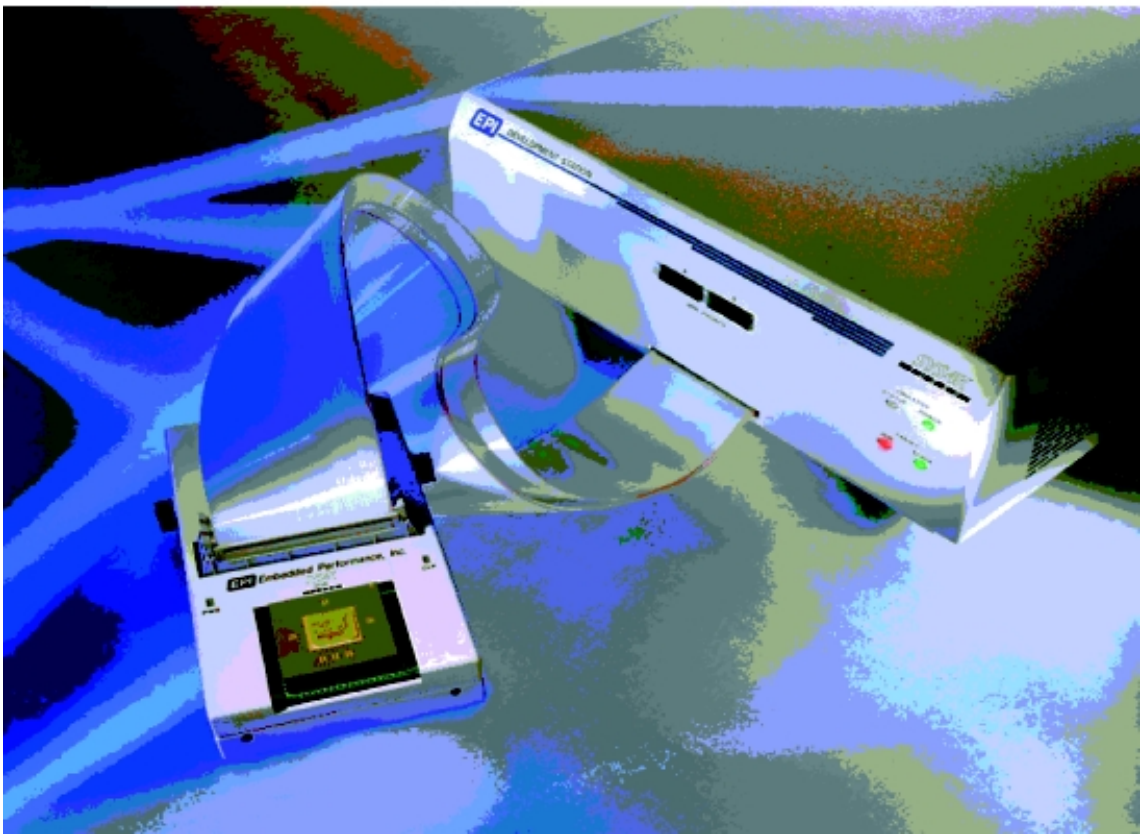
Trace and Logic Analysis — *Don't Wait to Find the Bug*
The emulators combine a fully featured logic state analyzer with full speed trace of the processor's activity. This combination means you can track the progress of your application, stop on virtually any event, and see a history of the processor's activity. With this power you can track down bugs in minutes that could take days or weeks without the emulator. The emulator can record (trace) a frame of the target's activity once each clock cycle. In addition to the processor signals, a frame includes emulator status signals, a 46 bit time stamp, plus 16 general purpose inputs. The emulator samples these signals using the same rules as the processor.

Find Complex Bugs in Real Time
The Three-Dimensional Trace and Execution Control language specifies the behavior of the trace mechanism and its controlling state machine. It directs the emulator, on a cycle-by-cycle basis, to perform actions such as *trace one frame*, *stop execution*, and *trigger* external instruments. Since the decision to trace a frame is made every cycle, you capture only the information needed thereby optimizing the use of trace memory. The application can be stopped on the occurrence of virtually any pattern or sequence of patterns. These *hardware breakpoints* do not require execution of specific instructions. For example, you can stop the processor when it writes a specified value to a specific address. This kind of breakpoint can easily find offending code when memory is being over written.

Trace Display
Once trace frames have been captured, you can display the instruction and data accesses as disassembled instructions with symbolic references or in "raw" format of 1's, 0's, and hex values. With the C source level debugger traced instructions may be displayed with the original C source code lines interleaved between the captured instruction flow. Physical addresses are translated and displayed as virtual addresses.

Host Resource Access — *Don't Wait for Hardware*
The SYS4K emulator support EPI/OS. Combined with EPI's full ANSI run time library, EPI/OS makes it possible for your application code to use host computer resources. Now your code can display status information on the host monitor and even read or write files on the host file system making it easy to simulate peripherals not yet implemented.

Target Memory Tests — *Don't Wait to Test Memory*
Not just software development tools, the TURBO emulators offer features to assist the hardware engineer as he debugs the design. The emulators offer six built-in memory tests, three 'scope loops, and the ability to trace its own accesses to target memory. Now you can thoroughly test the memory subsystem and peripherals even before the target is capable of loading and executing a program. Additionally, the emulators' trace mechanism with 16 external signal inputs and its ability to trigger a 'scope can often eliminate the need to connect a logic analyzer.



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RTE-TP series
N-Wire interface Real Time Emulator

Features

- Processor On Board emulation function. Emulation is done by using real processor that has N-Wire/JTAG interface. Therefore execution of processor is stable and could provide high transparent emulation.
- Emulation Memory is supported. ROM emulation function is supported (MAX 4MB). Several types of ROM probe are prepared (option).
- Real time trace function is supported. Trace information conforming to N-Wire specification is recorded into memory.
- High speed download
- Various host interface are prepared. PCI interface, PCMCIA interface and LAN interface are supported.
- High level language debugger. High performance and high level language debugger, MULTI (GHS Debugger) is available to use.

NEC CPUs Supported

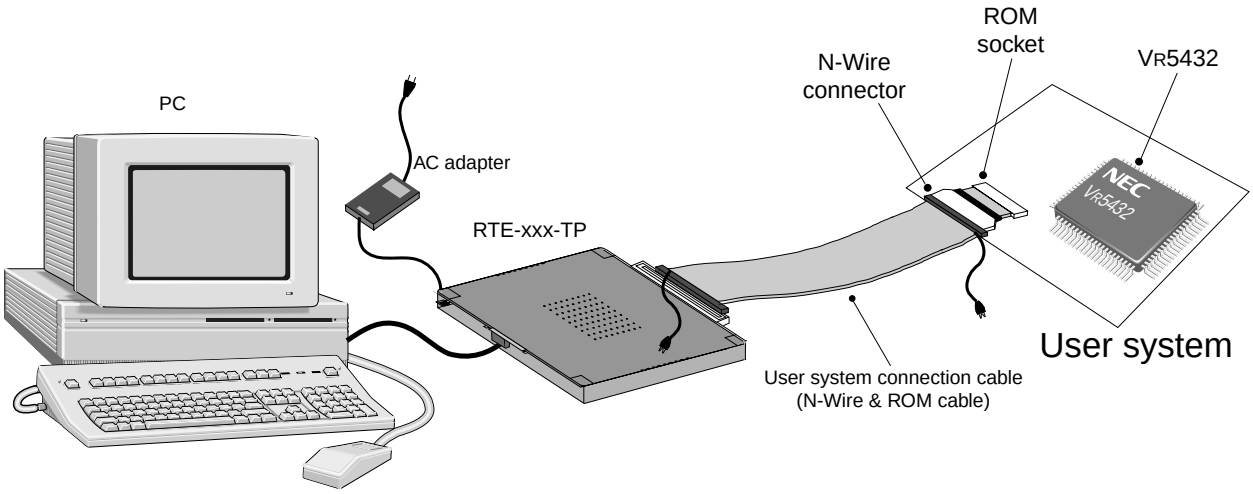
VR54xx,
VR41xx (under development)

Host Platforms Supported

Windows95/98/NT

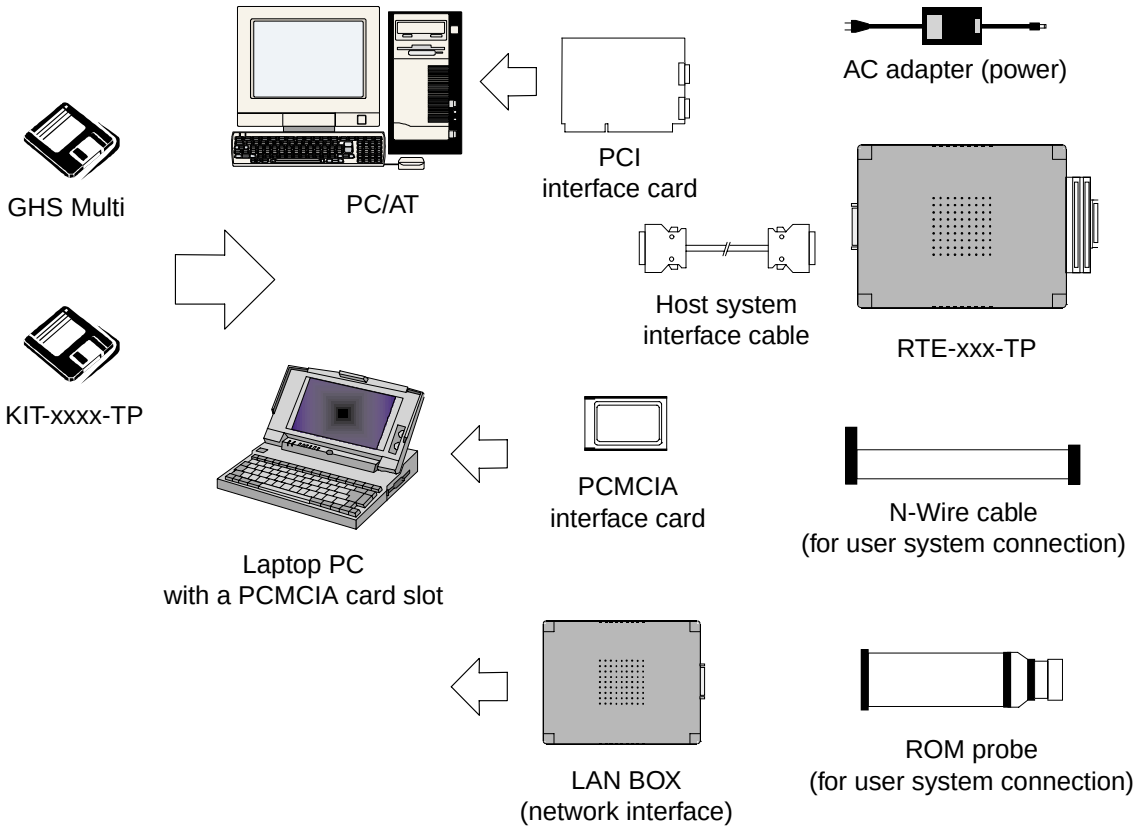
Product Overview

RTE-TP series is the emulator of NEC microcomputer which has DCU (Debug Control Unit) inside.



RISC by NEC:
Know-how²

NEC



GHS Multi:	High level language debugger for RTE-xxxx-TP
KIT-xxxx-TP:	Control software for each software
PC/AT:	PC capable of running Windows95/98/NT
PCI interface card:	PCI bus interface card
PCMCIA interface card:	TYPEII card (version 2.1 of the PCMCIA specification or later
LAN BOX:	LAN supporting PC (10 base-T)
Host system: Interface cable:	Cable for connection RTE-xxx-TP to the host card
AC adapter:	Power supply
RTE-xxx-TP:	N-Wire ICE
N-Wire cable:	Cable for connection to the user system for debugging
ROM cable:	Probe for ROM emulation

EDA & Software Modeling Tools

VirtualICE ™

The Proven Co-design and Co-verification Environment for System LSI and ASIC

Features

- Precise timing simulation of real CPU
- Applicable to multiple CPU/DSP System LSI
- Supports multi-vendor compilers including NEC's
- Supports major Verilog Simulators
- High simulation speed without sacrificing accuracy

NEC CPUs Supported

VR4100 family
VR4102 (RTL)

VR4120 ASIC CORE family
NZ4120C9, NZ4120N9 (under preparation)

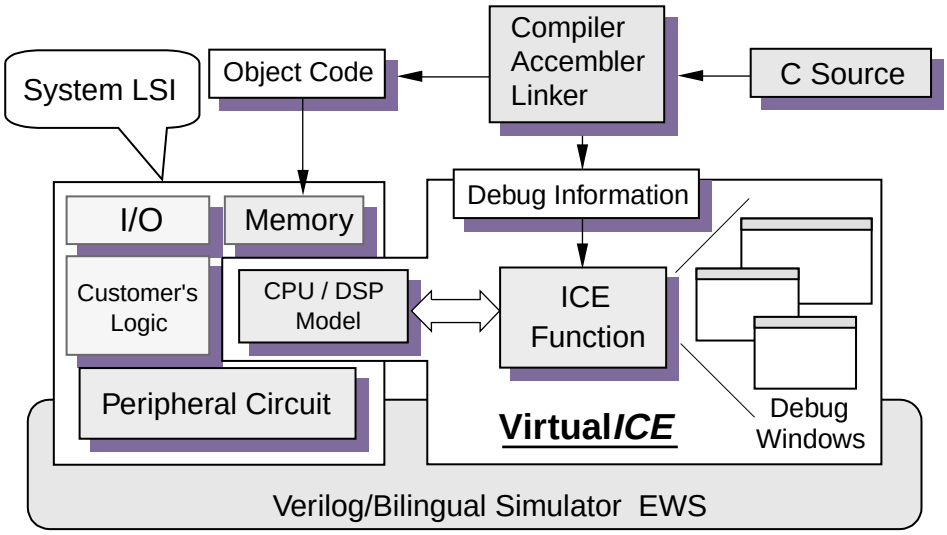
Host Platforms Supported

Sun Ultra Series or SPARC Station, Solaris 2.5.1 or later

Verilog Simulator:
Verilog-XL, VCS,
ModelSim EE/PLUS,
NC-Verilog

Product Overview

VirtualICE offers design and Verification flexibility for system-on-a-chip design. The advent of deep sub-micron technologies and the resulting system-on-a-chip capabilities have engendered new design requirements. The ability to embed programmable computing elements within a chip mandates the simultaneous development of hardware and software. Time-to-market pressures and short product lifetimes demand efforts to reduce the development cycle while simultaneously minimizing the risk of an ASIC re-spin. Current design paradigms exacerbate the situation by separating the hardware and software development. Any method of hardware/software co-design should have the full capabilities of both hardware and software debug facilities, with full function compatibility and the ability to use real object code.
Yokogawa offers solutions for hardware and/software co-design. VirtualICE for Verilog simulators facilitates hardware/software validation in all phases of development. The CPU model of VirtualICE (written in Verilog HDL) merely simulates the behaviour of hardware with accuracy timing. The CPU model fetches and executes actual instructions from memory that is generated by the actual compiler. As a natural consequence, the result of the simulation is the same as if the software were running on the actual CPU with accuracy timing. It is very simple and the best way for hardware and software co-design. VirtualICE reduces the risk of new design by testing the hardware/software interfaces early in the development cycle.



Objective

Board level simulation
Function verification and test vector extracting in the design phase of ASICs
Targetless firmware debugging
Estimation of system performance
Development of system on silicon chip

Target system

Hard disc and DVD controllers
Printers
Multi-media equipment
Cellular phone and personal digital assistants (PDA)
Car navigation systems

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Development Support Products

NEC Workshop Program 2000

Workshops '2000 NEC European Support Centre

NEC provides comprehensive workshops on a wide range of its Microproducts at the European Support Centre.

The 2-3 day courses provide participants with information on the CPU architecture of the device family, differences between family members and functionality of the on-chip peripherals.

Hands on sessions with development tools provide participants with practical experience. The workshops are targeted for technical/design engineers. All the workshops are held in English at our European Support Centre in Düsseldorf. Additional workshops at customer premises, or at local NEC sales offices, can be arranged on request.

For information on booking and detailed workshop agenda, please call +49(0)211-6503-216 or simply return the fax sheet, for further information.

Workshops	Date
75X/XL 4-bit Single Chip Microcontroller	On request
78K0 **78K0S** 8-bit Single Chip Microcontroller	15.02. 16.02.2000 09.05. 10.05.2000 12.09. 13.09.2000 05.12. 06.12.2000
78K4 16-bit Single Chip Microcontroller	28.03. 29.03.2000 05.09. 06.09.2000
V850 32-bit RISC Microcontroller	01.02. 02.02.2000 03.05. 04.05.2000 30.08. 31.08.2000 14.11. 15.11.2000
DSP/SPX	On request
VR Series 64-bit RISC Microprocessor	14.03. 16.03.2000 17.10. 19.10.2000

The latest update on our NEC Workshop can be found on our web site: **www.nec.de** in the "News" section.

RISC by NEC: Know-how²

NEC

Workshops '2000

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NEC Electronics (Europe) GmbH
Technical Product Support

Please send me further information on the following workshops:

- ☐ 75X & 75XL
  4-bit Single Chip Microcontroller
- ☐ 78K0 & 78K0S
  8-bit Single Chip Microcontroller
- ☐ 78K4
  16-bit Single Chip Microcontroller
- ☐ DSP & SPX
  Digital Signal Processor
- ☐ V850
  32-bit RISC Microcontroller
- ☐ VR Series
  64-bit RISC Microprocessor

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Appendixes

Appendix A

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Algorithmics, Ltd.

Applied Microsystems Corporation

BSQUARE Corporation

Corelis, Inc.

DIAB-SDS

Digital Logic Instruments GmbH

Embedded Performance, Inc.

Green Hills Software Inc.

Microsoft Corporation

NEC Electronics Europe GmbH

PC-TEL, Inc.

QNX Software Systems, Ltd.

Appendix A

SYSGO Real-Time Solutions GmbH

Tektronix, Inc.

Wind River Systems, Inc.

Yokogawa Electric Corporation

Company Website Locators

Accelerated Technology, Inc ..... www.atinucleus.com

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Algorithmics, Ltd. ..... www.algor.co.uk

Applied Microsystems Corporation ..... www.amc.com

BSQUARE Corporation ..... www.bsquare.com

Corelis, Inc. ..... www.corelis.com

DIAB-SDS ..... www.diabsds.com

Digital Logic Instruments GmbH ..... www.dli.de

Embedded Performance, Inc. ..... www.episupport.com

Green Hills Software Inc. ..... www.ghs.com

Microsoft Corporation ..... www.microsoft.com

NEC Electronics Europe GmbH ..... www.nec.de

PC-TEL, Inc. ..... www.pctel.com

QNX Software Systems, Ltd. ..... www.qnx.com

SYSGO Real-Time Solutions GmbH ..... www.sysgo.de

Tektronix, Inc. ..... www.tek.com/Measurement/

Wind River Systems, Inc. ..... www.windriver.com

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