FC6301
User Manual

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Revision History

Date	Revision	Revision
2010-10-05	Draft	0.1
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Table of Contents

1 Acronyms and related documents

1.1 Acronyms

ADC	Analog to Digital Converter
BLAST	Board Level Advanced Scalable Technology
DAC	Digital to Analog Converter
DCI	Digitally Controlled Impedance
DDR	Double Data Rate
DSP	Digital Signal Processing
EPROM	Erasable Programmable Read-Only Memory
FBGA	Fineline Ball Grid Array
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
JTAG	Join Test Action Group
LEB	Local Expansion Bus
LED	Light Emitting Diode
LVTTL	Low Voltage Transistor Logic level
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
MGT	Multi-Gigabit Transceiver
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
cPCI	Compact PCI
PCI-e	PCI Express
PLL	Phase Locked Loop
QDR	Quadruple Data rate
SBC	Single Board Computer
SDRAM	Synchronous Dynamic Random Access memory
SOC	System On Chip
SRAM	Synchronous Random Access memory
SSP	Synchronous Serial Port
TTL	Transistor Logic level
FMC	FPGA Mezzanine Card
HPC	High pin count

Table 1: Glossary

1.2 Related Documents

- 3U CompactPCI specifications (PICMG 2.0 R3.0)
- CompactPCI Hot Swap specifications (PICMG 2.1 R2.0)
- VITA 57.1 FPGA Mezzanine Card Standard
- Xilinx Virtex-6 documentation

2   General description

The FC6301 is a high performance CompactPCI (cPCI) card with advanced digital signal processing capabilities. The design has been targeted for customer programmable implementations of complex FPGA algorithms for Digital Signal Processing (DSP) applications. The FC6301 product is in the 3U cPCI form factor, offering various direct on-board interface options that are closely coupled to large - fast on-board memory resources of the Xilinx Virtex™-6 FPGA. The FC6301 is an excellent choice for high performance applications that require the use of accelerated frequency-domain algorithms such as with FFTs. 4DSP has many off-the-shelf Intellectual Property (IP) cores for applications that require the highest level of performance. CompactPCI (cPCI) is an adaptation of the Peripheral Component Interconnect (PCI) Specification for industrial and military embedded applications requiring a more robust mechanical form factor than a desktop PC.
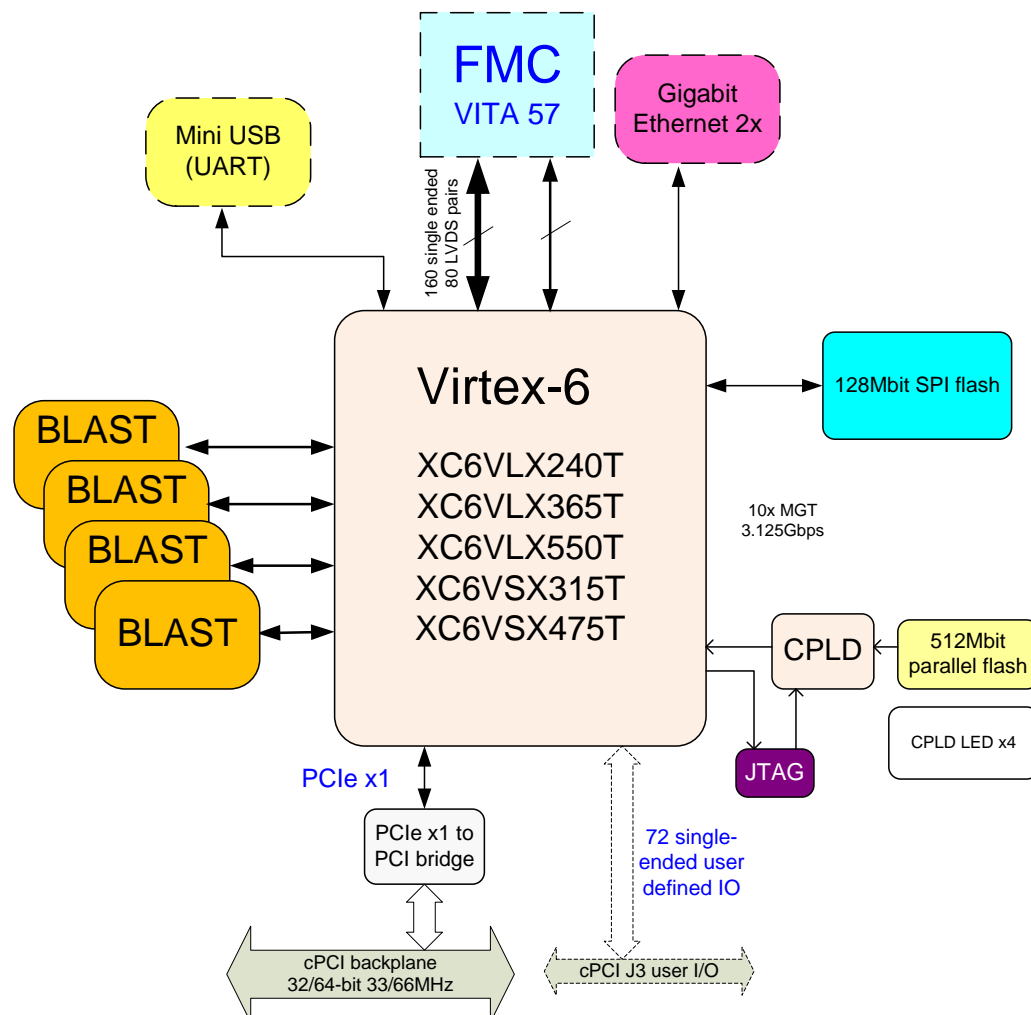

Figure 1: FMC122 block diagram

3 Installation

3.1 Requirements and handling instructions

- The FC6301 daughter card must be installed cPCI backplane compliant to the cPCI standard.
- Do not flex the board and prevent electrostatic discharges by observing ESD precautions when handling the card.

3.2 Firmware and Software

Drivers, API libraries and a program example working in combination with a pre-programmed firmware for the FPGA is provided. The FC6301 is delivered with an interface to the Xilinx PCIexpress endpoint in the Virtex-6 device and an example VHDL design so users can start performing data transfers over the PCI bus right out of the box. For more information about software installation and FPGA firmware, please refer the 4FM Get Started Guide.

4 Design

4.1 Phycisal specifications

4.1.1 Board Dimensions

The FC6301 card complies with the compact PCI standard known as PICMG 2.0 R3.0. The card is a 3U (100.00 mm by 160.00 mm) module which incorporates a 32 bits PCI bus on the P1 connector. The P2 connector is fully routed to the Virtex6 FPGA.

Figure 2 : FMC122/FMC125/FMC126 dimensions

4.1.2 Front panel

There are two front panel options. One front panel is used when an FMC board is mounted. The other front panel is used when the Ethernet IO option is chosen.
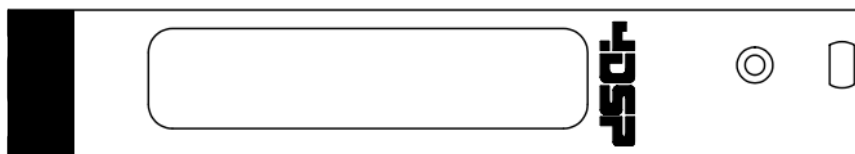

Figure 3: FMC option Bezel drawing

4.2   Front panel IO

The FC6301 offers different front panel IO options. Not all can be used simultaneously. In case an FMC is used no Ethernet connection is possible.

4.2.1   Gigabit Ethernet

Two Ethernet ports (RJ45 connectors) are available on the FC6301 in the front panel I/O area. The FPGA is connected to a 2-port Ethernet PHY (88E1121) that connects to two RJ45 connectors.

The Gigabit Ethernet ports are capable to adapt to lower Ethernet speeds (10/100) if required. This is a specific option which is not available in combination with an FMC daughter card.

4.2.2   UART

One UART connection will be available on the fontanel via a mini USB connection. The serial interface is made using a USB to UART Bridge (CP2102). The UART will connect directly to the Virtex 6 FPGA via a level translator.

4.2.3   FMC

The Virtex-6 device interfaces to an FPGA Mezzanine Card (FMC) via an High pin count (HPC) VITA 57.1 site. The FMC site provides flexibility for adding analog and/or digital IO via Customer developed, third party or 4DSP FMC boards. 4DSP offers a wide variety of FMC cards that can be used on the FC6301. These are:

- FMC103: 4-ch A/D 210 Msp/s @ 12-bits
- FMC104: 4-ch A/D 250 Msp/s @ 14-bits
- FMC107: 8-ch A/D 65 Msp/s @ 12-bits
- FMC108: 8-ch A/D 250 Msp/s @ 14-bits
- FMC110: Dual A/D. Dual D/A Channel
    - 2-ch A/D 1 Gsp/s @ 12-bits
    - 2-ch D/A 1 Gsp/s @ 16-bits
- FMC122: Single-Dual A/D Channel
    - 1-ch A/D 2.50 Gsp/s @ 8-bits
    - 2-ch A/D 1.25 Gsp/s @ 8-bits
- FMC125: Quad-Dual-Single Channel A/D
    - 1-ch A/D 5.00 Gsp/s @ 10-bits
    - 2-ch A/D 2.50 Gsp/s @ 10-bits
    - 4-ch A/D 1.25 Gsp/s @ 10-bits
- FMC126: Quad-Dual-Single Channel A/D
    - 1-ch A/D 5.00 Gsp/s @ 10-bits
    - 2-ch A/D 2.50 Gsp/s @ 10-bits
    - 4-ch A/D 1.25 Gsp/s @ 10-bits

4.2.4   LED

Four LEDs are connected to the CPLD and are available in the front panel I/O area

4.3   SPI flash

A 128 Mbits serial flash device (S25FL128P) will be available to the Virtex-6 device. This flash allows the storage of vital data like processor boot code and settings into a non volatile memory.

The flash is operated using a standard SPI interface that can run up to 104 MHz, allowing for a page programming speed up to 208 KB/s. Reading data from the flash can be done at speeds up to 13 MB/s.

The SPI programming pins will be connected to a bank that supports 1V8, whereas the serial flash will be operating at 3V3. This will not cause problems for the signals from the Virtex-6 to the flash device but the signal from the flash device to the Virtex-6 will pass through a level translator (SN74AVC4T245).

4.4   Virtex-6 FPGA device

The Virtex-6 FPGA device is the DSP processing node of the FC6301. The Virtex-6 FPGA device is from the Virtex-6 SXT and LXT family in a 1759 balls fine line ball grid array package. It can be an XC5VLX240T, XC5VLX365T, XC5VLX550T, XC5VSX315T or XC5VSX475T.

4.5   PCI interface

A one lane PCI express is connected to a bridge device (PI7C9X110) thus making the Virtex-6 FPGA available for access on the parallel PCI bus. The following performances have been recorded on the bus.

- ➢ **PCI 33 MHz: Host to FC6301 60 Mbytes/s sustained**
- ➢ **PCI 33 MHz: FC6301 to Host 110 Mbytes/s sustained**
- ➢ **PCI 66 MHz: Host to FC6301 120 Mbytes/s sustained**
- ➢ **PCI 66 MHz: FC6301 to Host 140 Mbytes/s sustained**
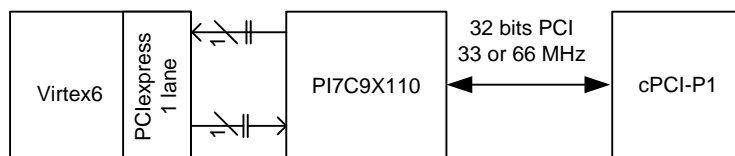
Figure 4 : PCI interface diagram

4.6   BLAST sites

Thanks to the availability of 3 BLAST sites a wide variety of memory and processing modules can be connected to the Virtex-6 device. For each BLAST site it is possible to choose from the list of available BLAST modules.

For more information about the available BLASTs on the FC6301 please consult the following page: BLAST modules http://www.4dsp.com/BLAST.htm

Due to its small form factor and ease of design, the BLAST modules enable a rapid solution for custom memory or processing requirements.

BLAST SITE	1	2	3	4
Single BLAST	YES	YES	YES	YES
Single Extended BLAST	YES	YES	YES	YES
Double BLAST	NO	NO	NO	NO
Double Extended BLAST	NO	NO	NO	NO

Table 2: BLAST Configuration Options

BLAST SITE	1	2	3	4
DDR3	YES	YES	YES	YES
DDR2	YES	YES	YES	YES
QDR	YES	YES	YES	YES
ADV212 JPEG2000	YES	YES	YES	YES
32GB NAND FLASH	YES	YES	YES	YES

Table 3: BLAST Memory/Processing Options

4.7 Clock tree

The FC6301 clock architecture offers an efficient distribution of low jitter clocks. A 100 MHz clock from a low jitter oscillator is distributed to the FPGA and the PCIexpress to PCI bridge using a PCI express jitter attenuator (ICS847003). This clock is used as the PCIexpress reference clock.

A low jitter programmable clock device (CDCE925) able to generate frequencies from 62.5MHz to 255.5MHz in steps of 0.5MHz is also available. This clock management approach ensures maximum flexibility to efficiently implement multi-clock domains algorithms and use the memory devices at different frequencies.

Further there is also a fixed 50 MHz clock is distributed to the FPGA and the CPLD.
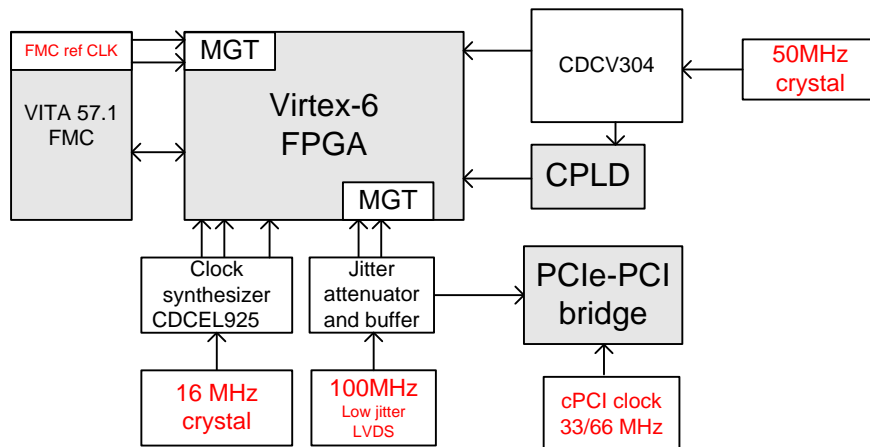

Figure 5 : Clock tree

4.8   FPGA device configuration

4.8.1   Flash storage

The FPGA firmware is stored on board in a flash device. The 512Mbit device is partly used to store the configuration for both FPGAs. In the default CPLD firmware configuration, the Virtex-6 device is directly configured from flash if a valid bitstream is stored in the flash. The flash is pre-programmed in factory with the default firmware example.
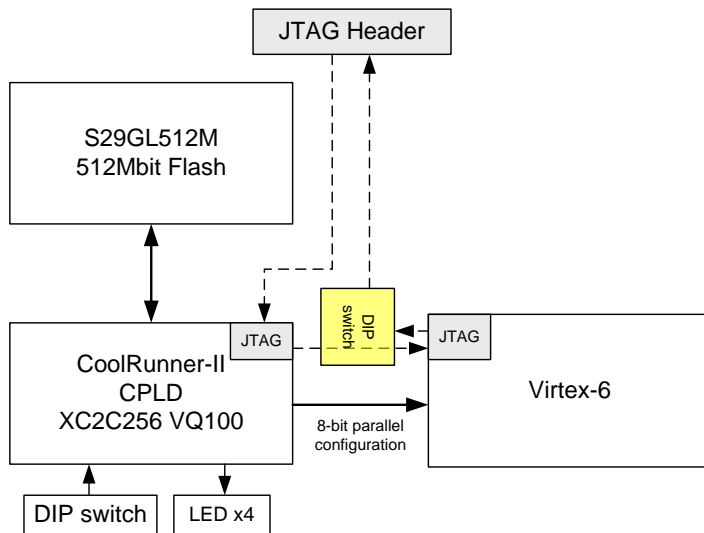

Figure 6 : Configuration circuit

4.8.2   CPLD device

As shown on Figure 4, a CPLD is present on board to interface between the flash device and the FPGA device. It is of type CoolRunner-II. The CPLD is used to program and read the flash. The data stored in the flash is transferred from the host motherboard via the PCI bus to the Virtex-6 device and then to the CPLD that writes the required bit stream to the storage device. A 50MHz clock connects to the CPLD and is used to generate the configuration clock sent to the FPGA device. At power up, if the CPLD detects that an FPGA configuration bitstream is stored in the flash, it will start programming the FPGA device in SelectMap mode.

The CPLD configuration is achieved by loading with a Xilinx download cable a bitstream from a host computer via the JTAG connector. The FPGA device configuration can also be performed using the JTAG chain.

4.8.3   DIP Switch

A switch is located next to the JTAG programming connector. The switch positions are defined as follows:

Sw1	OFF	Default setting. The Virtex-6 configuration is loaded from the flash at power up.
	ON	The Virtex-6 **safety** configuration is loaded from flash at power up. To be used only if the Virtex-6 cannot be configured from flash or does not perform properly with the switch in the OFF position.
Sw2		Reserved
Sw3		Reserved
Sw4		Reserved

Table 4: Switch description

4.8.4   CPLD LEDs and board status

Four LEDs connect to the CPLD and give information about the board status.

LED 0	**Flashing**	Virtex-6 FPGA bitstream or user_ROM_register is currently being written to the flash
	ON	Virtex-6 FPGA device not configured
	OFF	Virtex-6 FPGA device
LED 1	**ON**	Switch 1 is on position ON. The CPLD has been forced to configure the FPGA with the safety configuration
	OFF	Switch 1 is on position OFF.
LED 2	**Flashing**	The Virtex-6 has been configured with the safety configuration bitstream programmed in the flash at factory because an invalid bitstream was detected in the user configuration space. Please write a valid Virtex-6 device A bitstream to the flash.
	ON	Flash is busy writing or erasing
	OFF	Flash device is not busy
LED 3	**ON**	CRC error. Presumably a wrong or corrupted FPGA bitstream has been written to the flash. Once on this LED remains on
	OFF	No CRC error detected

Table 5: LED board status

4.8.5   JTAG

A JTAG connector footprint is available on the FC6301 for configuration purposes and the JTAG chain can be accessed using a press-fit JTAG connector. The JTAG chain is connected via a DIP switch that enables the following configurations:

- CPLD -> FPGA
- CPLD only

The JTAG connector can be placed on both sides of the PCB. The connector location seen from the top of the PCB is shown in Figure 10.
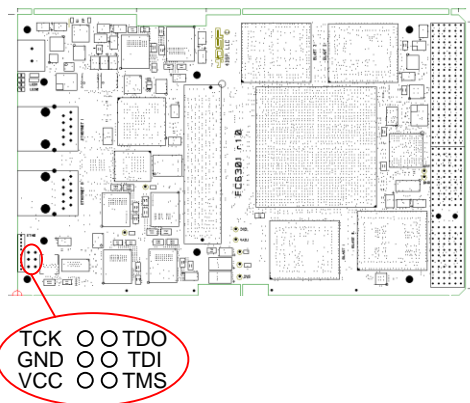

Figure 7:JTAG connector location.

4.9 Power supply

The Power is supplied to the FC6301 via the CompactPCI connectors. Several DC-DC converters generate the appropriate voltage rails for the different devices and interfaces present on board. The FC6301 power distribution is as follows:
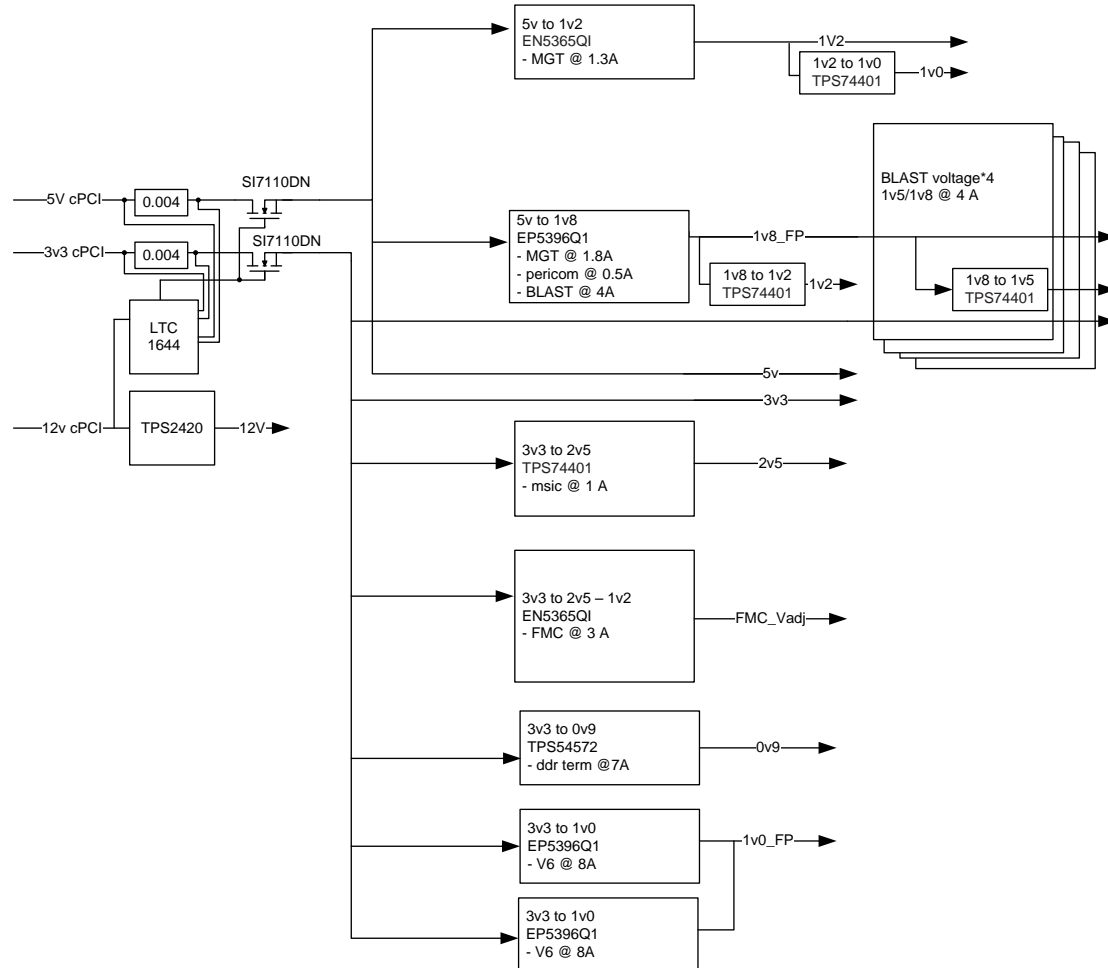

Figure 8: FC6301 power distribution

Device/Interface	Voltage	Maximum current
DCI and memory reference voltage	0.9V	6 A
Virtex-6 core	1V	16A
CPLD, BLAST sites	1.8V	8A
Virtex-6 Vccaux, Virtex-6 bank connected to A/D daughter card, EP80579	2.5V	2A
CPLD, PCI bridge, Virtex-6 bank connected to A/D daughter card, power generation	3.3V	11A
power generation	5V	12A
Front Panel IO daughter card	12V	TBD
MGT power supply	1 V, 1.2V	2A, 1.5A

Table 6 : Power supply

4.10 Hotswap

Hot Swap is the act of removal and insertion of cards into a platform while that system is operational. This process should not cause any failures on the systems power supply and system's I/O signals. Protection of the card's circuitry also needs to be taken into account in this process.

A compact PCI board can implement three different types of hot swap:

- Non Hot Swap do not have hot swap features
- Basic Hot Swap boards have the minimum features required
- Full Hot Swap have the minimum requirements plus the ability for software connection control

The Pericom bridge is a hot swap friendly device but full hot swap is not supported. A hot swap controller is required to monitor all power levels, pre-charge the cPCI signals and to switch the backend power on and off. The LTC1643A hot swap controller from linear technologies is used. For more information on hot swap refer to the hot swap specifications.

4.11 Power and temperature monitor

Two ADT7411 devices are used to monitor the power on the different voltage rails as well as the temperature. The ADT7411 data are constantly passed to the Virtex-6 device. Measurements can be accessed from the host computer via the PCI bus.

Parameter:	Device 1	Formula
On-chip temperature	ADT7411 Die Temperature	
On-chip AIN0 (V_{DD})	+3.3V	
External temperature	FPGA A temperature	
External AIN3	12V	AIN3*(1249/249)
External AIN4	1V0	AIN4
External AIN5	3V3	AIN5
External AIN6	1V2	AIN6
External AIN7	MGT1V2	AIN7
External AIN8	MGT1V0	AIN8

Table 7: Monitoring device 1 connections

Parameter:	Device 2	Formula
On-chip temperature	ADT7411 Die Temperature	
On-chip AIN0 (V_{DD})	+3.3V	
External AIN1	BLAST0_vcore	AIN1
External AIN2	BLAST2_vcore	AIN2
External AIN3	5V	AIN3*(1249/249)
External AIN4	0V9	AIN4
External AIN5	VADJ	AIN5
External AIN6	1V8	AIN6
External AIN7	12V current	Tbd
External AIN8	2V5	AIN8

Table 8: monitoring device 2 connections

5   Environment

5.1   Temperature
Operating temperature

- 0°C to +60°C (Commercial)
- -40°C to +85°C (Industrial)

Storage temperature:

- -40°C to +120°C

5.2   Convection cooling
The air flow provided by the chassis fans the FC6301 is enclosed in will dissipate the heat generated by the on board components. A minimum airflow of 300 LFM is recommended.

Optionally a low profile heat sink/fan can be glued on top of the Quad ADC. The card has a fan power connection that can be switch on and off under carrier card control (TBD).

For standalone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC and ensure that the temperature of the devices is within the allowed range. 4DSP's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

6   Safety
This module presents no hazard to the user.

7   EMC
This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

8   Warranty

	Hardware	*Software/Firmware*
Basic Warranty (included)	1 Year from Date of Shipment	90 Days from Date of Shipment
Extended Warranty (optional)	2 Years from Date of Shipment	1 Year from Date of Shipment