NEX-MCA
Users Manual

Including these Software Support packages:
MCA

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TABLE OF CONTENTS

1.0 OVERVIEW 4
1.1 General Information 4
2.0 SOFTWARE INSTALLATION 4
2.1 TLA700 4
2.2 DAS9200 5
3.0 CONFIGURING the NEX-MCA BUS ADAPTER 5
3.1 General Information 5
4.0 CONNECTING to the NEX-MCA ADAPTER 6
4.1 General 6
4.2 TLA700 6
4.3 92A96 6
5.0 CLOCK SELECTION 8
5.1 General Information 8
6.0 VIEWING DATA 8
6.1 Viewing State Data on the TLA700 8
6.2 Viewing Timing Data on the TLA700 8
6.3 Viewing State Data on the DAS9200/TLA500 9
6.4 Viewing Timing Data on the DAS9200/TLA500 9
APPENDIX A - Necessary Signals for Clocking 10
APPENDIX B - Considerations 11
B.1 MCA Loading 11
B.2 "Patch" Areas 11
APPENDIX C - Modifying the NEX-MCA Adapter 12
APPENDIX D - MCA Bus Pinout 13
APPENDIX E - References 15
APPENDIX F - Support 16

TABLE OF TABLES

Table 1- NEX-MCA TLA700 / 92A96 Wiring 7
Table 2- MCA BusOp Symbol Table 9

1.0 OVERVIEW

1.1 General Information

The NEX-MCA adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA700, a 92A96, or a 92C96 acquisition module to a MCA backplane. (The MCA designation refers to the Micro Channel Architecture specification.) In addition, the method of connection permits the use of other measurement devices such as oscilloscopes.

The included software will permit the acquisition of MCA bus cycles, and will display the data in easy-to-read symbolic form rather than raw hexadecimal or binary data.

Please note that this manual uses some terms generically. For example, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA700 apply to a TLA704/714 or TLA711/720 chassis with one or more 7L3/4 or 7M3/4 acquisition cards.

This manual assumes that the user is familiar with the MCA backplane specification and the Tektronix TLA700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA700, it is expected that the user is familiar with Windows 95/98.

For information on using a Prism 32GPX/GPD module with this support, or if 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix E for contact information.

2.0 SOFTWARE INSTALLATION

Two 3½” diskettes have been included with the NEX-MCA Bus Adapter. One is for use with the TLA700 series, the other is to be used with a DAS9200 or TLA500.

2.1 TLA700

The MCA support software is loaded in the same method as other Win95/98 programs. Place the NEX-MCA Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose MCA and click on **Okay**. Note that for either support the Logic Analyzer card must be at least 102-channels in width.

2.2 DAS9200

The included diskette should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing "MCA Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

3.0 CONFIGURING the NEX-MCA BUS ADAPTER

3.1 General Information

The number of signals defined by the Micro Channel specification exceeds the channel count of a 92A96, or 102-channel TLA. Because of this, three jumper blocks have been defined - JP2, JP3, and JP4. By placing a shorting jumper across the pair of pins next to the desired signal name, that signal can then be monitored during the acquisition. For information on physically modifying the NEX-MCA adapter to monitor signals not provided with the standard implementation, refer to Appendix C.

JP2 is used to select between SDSTRB~ and the derived signal DSDSTRB~. For proper clocking of Streaming Data activity the jumper should be set for DSDSTRB~ (connecting pins 2 and 3, the leftmost two pins). For high speed timing purposes, it may be desired to view the actual SDSTRB~ signal. In these cases, the jumper should be placed between pins 1 and 2, the rightmost two pins.

JP3 selects between CHRESET and SDCLK. To monitor CHRESET the jumper should connect pins 1 and 2 (the rightmost two). Placing the jumper between pins 2 and 3 (the leftmost pair) will permit monitoring the SDCLK signal.

JP4 is used to select which IRQ line should be monitored. Using the jumper, short the two pins adjacent to the desired IRQ signal.

4.0 CONNECTING to the NEX-MCA ADAPTER

4.1 General

Although taller than a standard Micro Channel module, the NEX-MCA adapter is designed to plug directly into any Micro Channel backplane slot. The board length and connector spacing conforms to Micro Channel specifications.

4.2 TLA700

When using NEX-MCA support with a TLA700 containing a 7L3/4 or 7M3/4 acquisition module, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. These grouped channels (8 podlets to a group) should be connected to the locations denoted for the A96. Follow the silk-screened information on the board that shows the proper relationship between the signal and reference inputs. When properly connected, the sides of the podlets that have writing on them should be visible.

Connect the four clock leads to their specified locations at J12 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the TLA700 when used with the NEX-MCA adapter.

4.3 92A96

When using a 92A96, connect the grouped pods (8 podlets to a group) to their appropriate locations by following the silkscreen information printed on the adapter board. The 92A96 pods are labeled A0-A3, D0-D3, and C0-C3. Each pod has its proper location denoted on the silkscreen of the adapter board. When attaching the pods, follow the silkscreen information on the board showing the ground and signal pin locations. When properly connected, the colored sides of the podlets should be visible.

Connect the four clock leads (one per A96 cable) to their specified locations at J16 (the only connector with 4 locations). Again, follow the silkscreened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the 92A96.

Group Name	Signal Name	MCA Pin #	TLA700 / 92A96 input	Group Name	Signal Name	MCA Pin #	TLA700 / 92A96 input
Address	A31	B86	A3:7	Data	D31	A75	D3:7
(Hex)	A30	B85	A3:6	(Hex)	D30	A74	D3:6
	A29	B84	A3:5		D29	B74	D3:5
	A28	A84	A3:4		D28	B73	D3:4
	A27	A83	A3:3		D27	B72	D3:3
	A26	A82	A3:2		D26	A72	D3:2
	A25	B82	A3:1		D25	A71	D3:1
	A24	B81	A3:0		D24	A70	D3:0
	A23	B06	A2:7		D23	B69	D2:7
	A22	B07	A2:6		D22	B68	D2:6
	A21	B08	A2:5		D21	A68	D2:5
	A20	B10	A2:4		D20	A67	D2:4
	A19	B11	A2:3		D19	A66	D2:3
	A18	B12	A2:2		D18	B66	D2:2
	A17	B14	A2:1		D17	B65	D2:1
	A16	B15	A2:0		D16	B64	D2:0
	A15	B16	A1:7		D15	B53	D1:7
	A14	B18	A1:6		D14	B52	D1:6
	A13	B19	A1:5		D13	B51	D1:5
	A12	B20	A1:4		D12	A51	D1:4
	A11	A04	A1:3		D11	A50	D1:3
	A10	A05	A1:2		D10	A49	D1:2
	A9	A06	A1:1		D9	B49	D1:1
	A8	A08	A1:0		D8	B48	D1:0
	A7	A09	A0:7		D7	A42	D0:7
	A6	A10	A0:6		D6	A41	D0:6
	A5	A12	A0:5		D5	A40	D0:5
	A4	A13	A0:4		D4	B40	D0:4
	A3	A14	A0:3		D3	B39	D0:3
	A2	A16	A0:2		D2	A38	D0:2
	A1	A17	A0:1		D1	B38	D0:1
	A0	A18	A0:0		D0	A37	D0:0
BusOp	TC~	A30	C0:1	Misc	IRQn~	- - -	C2:6
(Sym	MSDR~	B62	C3:3	(Hex)	SFDBKRT~	A64	C0:5
	SDR1~	B61	C2:3		CHCK~	B32	C3:6
	SDR0~	B44	C2:2		RST/SDCK	- - -	C3:7
	REFRESH~	A45	C2:5		MADE24	A02	C0:3
	DSDSTRB~	*	C2:0		SBHE~	A54	C3:0
	M/IO~	A34	C0:0		CHRDYRTN	B35	C2:1
	S1~	A33	C3:5		ADL~	A20	C2:4
	S0~	A32	C3:4		CMD~	B34	C2:7
BusSize	TR32	B80	C0:4	Arb	BURST~	A22	C0:2
(Hex)	DS32RTN~	A79	C0:7	(Hex)	PREEMPT~	A21	C3:2
	DS16RTN~	A44	C0:6		ARB/GNT~	- - -	C3:1
	BE3~	A78	C1:3		ARB3	A28	C1:7
	BE2~	B78	C1:2		ARB2	A26	C1:6
	BE1~	B77	C1:1		ARB1	A25	C1:5
	BE0~	B76	C1:0		ARB0	A24	C1:4
Clocks	CMD~	B34	CLK0	Clocks	SDCLK	*	CLK1
	MSDR~	B62	CLK2		unused		CLK3

Table 1- NEX-MCA TLA700 / 92A96 Wiring

* Derived signal

5.0 CLOCK SELECTION

5.1 General Information

All Micro Channel data is acquired using either both edges of CMD~ (for standard cycles) or a combination of CMD~ and the synthesized SDCLK (for Streaming Data cycles). The circuitry on the NEX-MCA Bus Adapter is used to provide the necessary clock edges at the necessary times for properly acquiring Streaming Data cycles.

6.0 VIEWING DATA

6.1 Viewing State Data on the TLA700

After making an initial acquisition, the TLA700 will display the data in the Listing (State) format.
Address and Data information are displayed as hexadecimal values; Bus Operation data is displayed using symbols; Miscellaneous, Bus Size, and the Arbitration signal groups are all displayed in hexadecimal radix.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. One symbol table (Table 2) has been provided to show the type of transaction that occurred on the MCA bus, and its filename is "MCA_BUS.TSF". This symbol table quickly shows whether the acquisition was of a memory or I/O operation, whether it was a read or a write, etc.

It is important to note that changing the group, channel, or wiring of the Bus Operation group can result in incorrect symbol information being displayed.

6.2 Viewing Timing Data on the TLA700

By default, the TLA700 will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: MCA and MCA-MagniVu. The first (MCA) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Timing format. The second selection, MCA-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA700 System User's Manual for additional information on formatting the Waveform display.

Pattern	TLA700 / 92A96 Symbol
xx0xxxx	Refresh
0x1xxxx	Reserved
101x101	StrmngDataMemRead
101x110	StrmngDataMemWrite
111xx11	Inactive
111x101	Memory Read
111x110	Memory Write
111xx00	Reserved
111x001	I/O Read
111x010	I/O Write

Table 2- MCA BusOp Symbol Table
Signals, from left to right:
TC~, MSDR~, SDR1~, SDR0~, REFRESH~, DSDSTRB~, M/IO~, S1~, S0~

6.3 Viewing State Data on the DAS9200/TLA500

After an acquisition is made the DAS9200 Logic Analyzer will display the data in State Display mode (as a default only). Address and Data information are displayed as hexadecimal values; Bus Operation data is displayed using symbols; Miscellaneous, Bus Size, and the Arbitration signal groups are all displayed in hexadecimal radix.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. One symbol table (Table 2) has been provided to show the type of transaction that occurred on the MCA bus, and its filename is "MCA_BUS". This symbol table quickly shows whether the acquisition was of a memory or I/O operation, whether it was a read or a write, etc.

It is important to note that changing the group, channel, or wiring of the Bus Operation group can result in incorrect symbol information being displayed.

6.4 Viewing Timing Data on the DAS9200/TLA500

It may be useful to display acquired information using the Timing Diagram display of the DAS9200. (Note that, unlike some other logic analyzers, with the DAS9200 there is no need to re-acquire MCA data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the DAS9200 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

APPENDIX A - Necessary Signals for Clocking

To properly acquire Micro Channel backplane activity, the following signals must be provided: CMD~, MSDR~, CHRDYRTN, SDR1~, SDR0~, and SDSTROBE~. However, SDSTROBE~ is only necessary when Streaming Data cycles are to be monitored.

For all but Streaming Data cycles, Address information is acquired on the falling edge of CMD~, and the Data bus is acquired on the rising edge of CMD~. The other signals (MSDR~, CHRDYRTN, SDR1~, and SDR0~) are used as clocking qualifiers, or as cycle type determinants.

In order to properly acquire Streaming Data bus cycles some circuitry had to be added to the NEX-MCA adapter. This circuitry generates the SDCLK and DSDSTRB~ signals used by the logic analyzer card to properly acquire these cycles. These signals DO NOT exist on the MCA backplane.

APPENDIX B - Considerations

B.1 MCA Loading

It must be noted that the NEX-MCA Bus Adapter does not provide any buffering of the MCA backplane signals. This was a conscious design decision that was made by balancing the tradeoffs of possible backplane loading versus signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-MCA adapter, to see the exact timing relationships and signal waveforms from the backplane. It is believed that the signal loading of the TLA700 or 92A96 acquisition cards is low enough so that MCA signal degradation will not occur.

The NEX-MCA Adapter Board was designed so that the run lengths for critical signals (and those with the highest activity levels, such as the address / data bus) are as short as possible. This should help greatly in retaining signal integrity.

B.2 "Patch" Areas

If signal loading or reflection does become a concern, the capability exists to add series resistors to any MCA signal. Patch areas have been provided next to each TLA700/A96 connector, consisting of two rows of plated through holes. These areas (outlined on the silk-screen and labeled as Nxx) are suitable for individual resistors or resistor networks. To add a series resistor, simply cut the trace of the desired signal on the component side of the board, and solder the resistor between the two feed-throughs.

APPENDIX C - Modifying the NEX-MCA Adapter

As previously mentioned, the Micro Channel specification has too many signals to be able to acquire them all with just one 92A96 or 102-channel TLA acquisition card. Assumptions have been made as to what signals are of interest, but these assumptions may not be appropriate for every instance. For these occasions, the NEX-MCA adapter may be easily modified to monitor any desired signals.

All MCA signals have been brought out to feed-throughs on the board, and there are three unused TLA/A96 connectors on the board (J4, J8, and J20). These connectors each have a series of holes beneath them (towards the edge connector) to provide easy solder points. Use wire wrap wire to connect the Micro Channel signals to these connectors.

When changing the signals connected to an A96 pod, the channel grouping default in the TLA700/DAS 9200 will have to be changed appropriately. Refer to the TLA70 or DAS 9200 manuals for information on this procedure. Also note that if any of the signals to the MCA BusOp group are changed then the included Symbol Table will no longer be accurate.

APPENDIX D - MCA Bus Pinout

Pin #	Row B - Solder Side	Row A - Component Side
1	AUDIO GND	CD SETUP~
2	AUDIO	MADE24
3	GND	GND
4	14.3MHz OSC	A11
5	GND	A10
6	A23	A9
7	A22	+5V
8	A21	A8
9	GND	A7
10	A20	A6
11	A19	+5V
12	A18	A5
13	GND	A4
14	A17	A3
15	A16	+5V
16	A15	A2
17	GND	A1
18	A14	A0
19	A13	+12V
20	A12	ADL~
21	GND	PREEMPT~
22	IRQ9~	BURST~
23	IRQ3~	-12V
24	IRQ4~	ARB0
25	GND	ARB1
26	IRQ5~	ARB2
27	IRQ6~	-12V
28	IRQ7~	ARB3
29	GND	ARB/GNT~
30	DPAREN~	TC~
31	DPAR0	+5V
32	CHCK~	S0~
33	GND	S1~
34	CMD~	M/IO~
35	CHRDYRTN	+12V
36	CD SFDBK~	CD CHRDY
37	GND	D0
38	D1	D2
39	D3	+5V
40	D4	D5
41	GND	D6
42	CHRESET	D7
43	SDSTROBE~	GND
44	SDR0~	DS16RTN~
45	GND	REFRESH~
46	Key	key

Pin #	Row B - Solder Side	Row A - Component Side
47	Key	key
48	D8	+5V
49	D9	D10
50	GND	D11
51	D12	D13
52	D14	+12V
53	D15	DPAR1
54	GND	SBHE~
55	IRQ10~	CD DS16~
56	IRQ11~	+5V
57	IRQ12~	IRQ14~
58	GND	IRQ15~

Pin #	Row B - Solder Side	Row A - Component Side
59	Reserved	Reserved
60	Reserved	Reserved
61	SDR1~	GND
62	MSDR~	Reserved
63	GND	Reserved
64	D16	SFDBKRTN~
65	D17	+12V
66	D18	D19
67	GND	D20
68	D22	D21
69	D23	+5V
70	DPAR2	D24
71	GND	D25
72	D27	D26
73	D28	+5V
74	D29	D30
75	GND	D31
76	BE0~	DPAR3
77	BE1~	+12V
78	BE2~	BE3~
79	GND	DS32RTN~
80	TR32	CD DS32~
81	A24	+5V
82	A25	A26
83	GND	A27
84	A29	A28
85	A30	+5V
86	A31	APAREN~
87	GND	APAR0
88	APAR2	APAR1
89	APAR3	GND

APPENDIX E - References

Tektronix TLA700 System User's Manual

Tektronix TLA700 Logic Analyzer User's Manual

Tektronix DAS9200 / TLA500 System User's Manual

Tektronix 92A96 / 92C96 Module User's Manual

"The IBM PS/2 Hardware Interface Technical Reference"
published by IBM, P/N S68X-2330-00
November 1989

"The Micro Channel Architecture Handbook"
by Chet Heath and Winn L. Rosch
published by Brady
ISBN 0-13-583493-7

APPENDIX F - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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Support Contact Information

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General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.