PCI-QUAD04

Four Channel Quadrature Encoder Input Board

User's Manual

Revision 2
October, 2000

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1.0 INTRODUCTION

The PCI-QUAD04 is a PCI plug-in board that provides inputs and decoding for up to four incremental quadrature encoders. The PCI-QUAD04 can also be used as a high speed pulse counter for general counting applications.

Incremental quadrature encoders are used to provide feedback signals from motors, that is, to count rotations and convert the physical movement into a series of electrical signals. These signals are sent to the computer which then decides whether or not to trigger signals that control the motor's movement and what those control signals should be. The PCI-QUAD04 is the link between up to four incremental quadrature encoders and the computer.

The PCI-QUAD04 is a plug-in board for PC/XT/AT computers; it uses one PCI slot and two rear panel openings for up to four channels. Each incremental quadrature encoder connects to an input channel on the board through a DB37 female connector on the board's rear panel. Channels 1 through 4 connect to the DB37 connector on the rear panel bracket.

For each channel, the signals provided at the DB37 connectors are:

- Phase A+, A–
- Phase B+, B–
- Index +/-
- +5VDC and GND (optional power for +5V encoders)

For pinout diagrams, refer to Section 3.5.

The board provides inputs for three basic signals, Phase A, Phase B, and Index. Phase A and Phase B are generated at a 90° phase shift with respect to each other. Using these signals, a computer can determine system position (counts), velocity, (counts per second), and direction of rotation.

The Index signal is used to establish an absolute reference position within one count of the encoder rotation (360°). Therefore, the Index signal is often used to reset or preset the position counter, particularly upon system startup when the incremental encoder can not determine the starting position of the motor. The Index signal can also be used to generate an interrupt signal to the computer.

The Phase A, Phase B, and Index inputs are jumper-selectable for differential or single-ended input mode. These signals, after being routed through differential receivers, offer various paths to the LS7266 inputs through the FPGA. The inputs are register-selectable for:

- Individual incremental encoder inputs to allow up to four channels.
- Cascadable counters to allow non-quadrature counting up to 96 bits.
- Routing the Index input to either the Load Counter/Load Latch input or the Reset Counter/Gate input with quarter cycle and half cycle signals supported.
- Routing the Compare or Carry/Borrow output signals to the 8259 Interrupt controller.

The heart of the PCI-QUAD04 is the LSI Computer Systems, Inc., LS7266R1 24-bit Dual-Axis Quadrature Counter IC. This component contains:

- Two 24-bit counters with associated 24-bit preset and 24-bit output latch registers;
- Integrated digital filtering with 8-bit counter prescalers,
- Programmable index functionality and programmable count modes including non-quadrature modes.

The board can also operate as a high-speed pulse and general purpose counter, cascadable to 96 bits. The 24-bit counters can count either in binary or BCD through register selection.

The board also includes an 82C59 Programmable Interrupt Controller which accepts the four Index inputs directly and the Carry/Borrow outputs from the LS7266 (counter overflow/underflow or count value match) to generate interrupts to the PC bus. The interrupt controller operates in Polled Mode and allows for masking and priority setting of the interrupt inputs.
For an overall view of PCI-QUAD04 functionality see Figure 1-1.

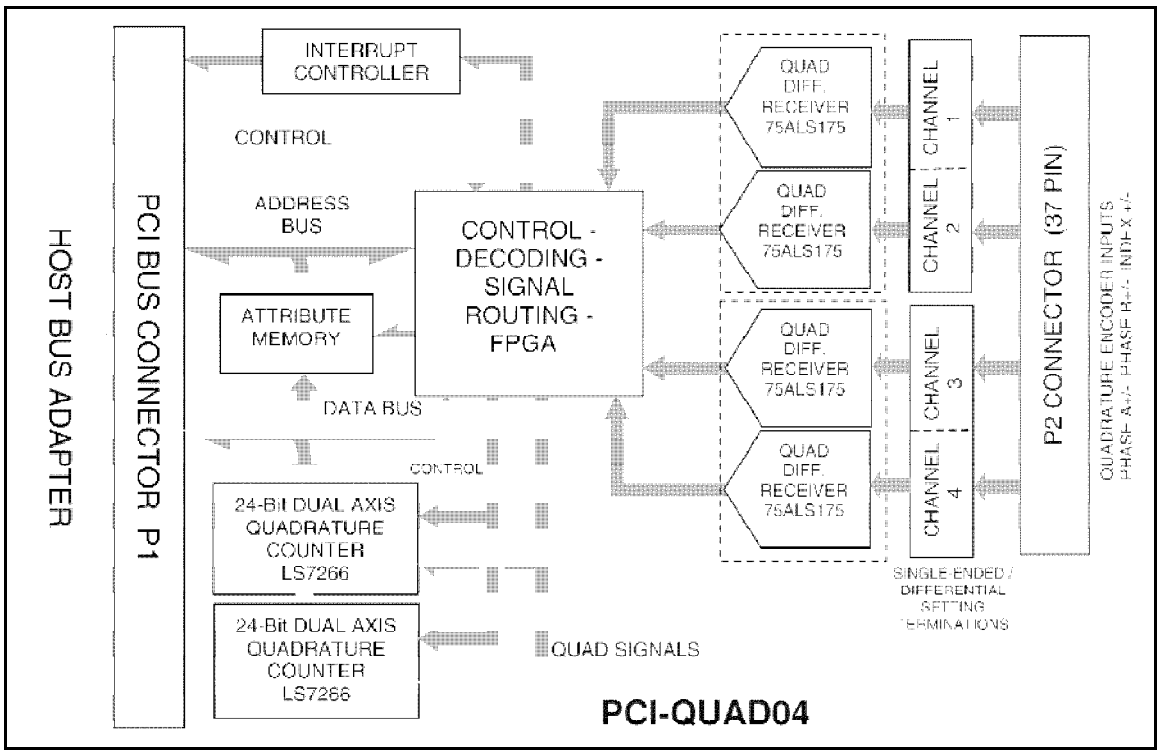

Figure 1-1. PCI-QUAD04 Functional Block Diagram

2.0 SOFTWARE INSTALLATION

Before installing your board in the computer, you should install and run *Insta*Cal™. *Insta*Cal is the installation, calibration and test software supplied with your data acquisition / IO hardware. It will guide you through the hardware settings for your board. These settings are also detailed in the following section.

The complete *Insta*Cal package is also included with the Universal Library. If you have ordered the Universal Library, use the Universal Library disk set to install *Insta*Cal. The installation will create all required files and unpack the various pieces of compressed software. To install *Insta*Cal, refer to the *Software Installation Manual* for complete instructions

3.0 HARDWARE INSTALLATION

Before installing the board, configure the channels for either SINGLE-ENDED or DIFFERENTIAL operation. The channel configuration is established with a set of jumper blocks on the board. Each jumper is labeled for its functionality. Refer to section 3.1 following for details.

3.1 SINGLE-ENDED/DIFFERENTIAL JUMPER SETTINGS

Prior to installation, set the jumpers on the PCI-QUAD04 to the positions required by your application. The PCI-QUAD04 is supplied preset for single-ended use with no termination resistors installed.

Single-Ended Configuration (Default)

Insert Jumper From pin 2 to 3 (SE)

		Input Channel		
Input	***1***	***2***	***3***	***4***
Phase A	P3	P8	P14	P11
Phase B	P4	P7	P13	P10
Index	P5	P6	P12	P9

Differential Configuration

Insert Jumper From pin 1 (DIFF) to 2

		Input Channel		
Input	***1***	***2***	***3***	***4***
Phase A	P3	P8	P14	P11
Phase B	P4	P7	P13	P10
Index	P5	P6	P12	P9

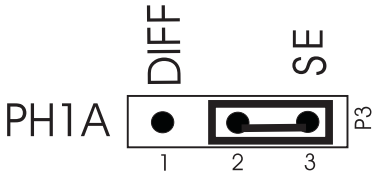

Figure 3-1. Example of Jumper Pin Numbering - SE/DIFF Jumpers

3.2 TERMINATION RESISTORS

Although termination resistors typically are not required, SMT pads on the board have been left open, and labeled to allow the user to install terminating resistors from the various inputs to ground.

Install Termination Resistors		**Channel**		
Input	**1**	**2**	**3**	**4**
Phase A+	R9	R22	R38	R30
Phase A-	R10	R23	R39	R31
Phase B+	R11	R20	R36	R28
Phase B-	R12	R21	R37	R29
Index+	R14	R19	R35	R27
Index-	R13	R18	R34	R26

3.3 BOARD INSTALLATION

1. Turn the power off.
2. Remove the cover of your computer. Be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.
3. Locate an empty PCI expansion slot in your computer.

4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the PCI-QUAD.

3.4 PCI-QUAD04 EXTERNAL CONNECTIONS & PINOUT

Pin assignments of the 37-pin connector, P2, are shown in Figure 3-2 below. ***Be sure to correctly phase the encoder according to the manufacturer's instructions.***

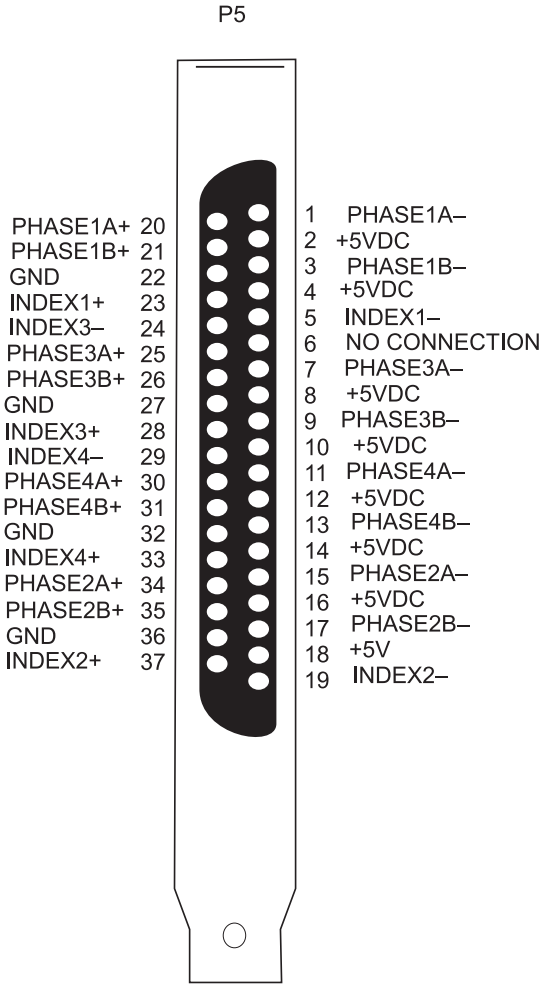

Figure 3-2. 37-Pin Connector P2 Pin-Out

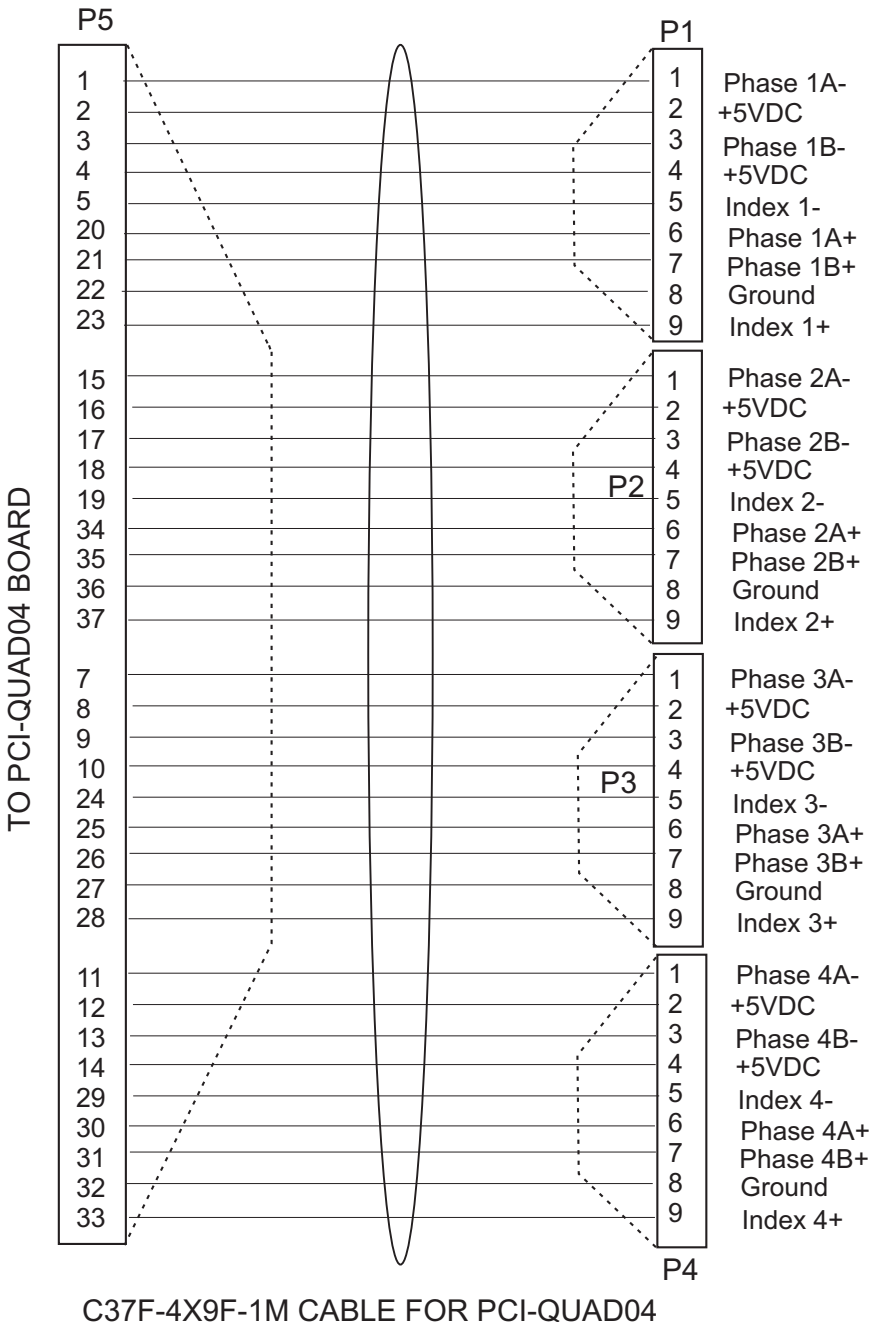

Figure 3-3. Board Connector-to-Cable C37F-4X9F-1M Pin Out

4.0 REGISTER MAP AND DESCRIPTIONS

4.1 OVERVIEW

The following section outlines the register map of the PCI-QUAD04 as well as briefly describing the commands necessary to program the PCI-QUAD04 at the register level (refer to Table 4-1 below). The heart of the PCI-QUAD04 is the LSI/CSI LS7266R1, a powerful device which is highly integrated to allow few external components to be needed. As seen in the LS7266R1 block diagram, many functions are controlled through register programming.

Table 4-1. I/O Region Register Operations

I/O Region	Function	Operations
BADR0	PCI memory-mapped configuration registers	32-bit double word
BADR1	PCI I/O-mapped config. registers	32-bit double word
BADR2	Config & control registers	8-bit byte

4.1.1 BADR0

BADR0 is reserved for the PLX-9052 configuration registers. There is no reason to access this region of I/O space for most PCI-DIO96 users. The installation procedure and Universal Library access all of the required information in this area. Unless you are writing direct register level software for the ,PCI-QUAD04 you will not need to be concerned with this address.

4.1.2 BADR1+4Ch

INTCSR CONFIGURE

32:15	14	13	12	11	10	9	8
X	X	X	X	X	INTCLR	X	LEVEL/EDGE

7	6	5	4	3	2	1	0
X	PCINT	X	X	X	INT	INTPOL	INTE

READ/WRITE

The INTCSR (Interrupt Control/Status Register) controls the interrupt features of the PLX-9052 controller. As with all of the PLX-9052 registers, it is 32-bits in length. Since the rest of the register have specific control functions, those bits must be masked off in order to access the specific interrupt control functions listed below.

- INTE is the interrupt enable (local):
  0 = disabled, 1 = enabled (default)
- INTPOL is the interrupt polarity:
  0 = active low (default), 1 = active high
- INT is the interrupt status:
  0 = interrupt not active, 1 = interrupt active
- PCINT is the PCI interrupt enable:
  0 = disabled (default), 1 = enabled
- LEVEL/EDGE is the interrupt trigger control:
  0 = level triggered mode (default), 1 = edge triggered mode
- INTCLR is the interrupt clear (edge triggered mode only):
  0 = N/A, 1 = clear interrupt

Note: For applications requiring edge triggered interrupts (LEVEL/EDGE bit 8 = 1), the user must configure the INTPOL bit for active high polarity (bit 1=1).

4.2 CHANNEL CONTROL REGISTERS (BADR2 +0 THROUGH BADR2 +7)

Table 4-1. Register Map

PCI-QUAD0x REGISTER MAP										
Register		**Data Bits**								
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**
PCIBASE2+0	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read Channel 1 OL bytesegment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write Channel 1 PR bytesegment addressed by BP
PCIBASE2+1	RD	0	IDX	U/D*	E	S	CPT	CT	BT	Read Channel 1 FLAG register
	WR	0	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 RLD register
	WR	0	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 CMR register
	WR	0	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 IOR register
	WR	0	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 IDR register
	WR	1	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 RLD register
	WR	1	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 CMR register
	WR	1	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 IOR register
	WR	1	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 IDR register
PCIBASE2+2	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read Channel 2 OL bytesegment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write Channel 2 PR bytesegment addressed by BP
PCIBASE2+3	RD	0	IDX	U/D*	E	S	CPT	CT	BT	Read Channel 2 FLAG register
	WR	0	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 2 RLD register
	WR	0	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 2 CMR register
	WR	0	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 2 IOR register
	WR	0	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 2 IDR register
	WR	1	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 RLD register
	WR	1	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 CMR register
	WR	1	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 IOR register
	WR	1	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 1 and 2 IDR register
PCIBASE2+4	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read Channel 3 OL bytesegment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write Channel 3 PR bytesegment addressed by BP
PCIBASE2+5	RD	0	IDX	U/D*	E	S	CPT	CT	BT	Read Channel 3 FLAG register
	WR	0	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 RLD register
	WR	0	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 CMR register
	WR	0	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 IOR register
	WR	0	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 IDR register
	WR	1	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 RLD register
	WR	1	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 CMR register
	WR	1	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 IOR register
	WR	1	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 IDR register
PCIBASE2+6	RD	D7	D6	D5	D4	D3	D2	D1	D0	Read Channel 4 OL bytesegment addressed by BP
	WR	D7	D6	D5	D4	D3	D2	D1	D0	Write Channel 4 PR bytesegment addressed by BP
PCIBASE2+7	RD	0	IDX	U/D*	E	S	CPT	CT	BT	Read Channel 4 FLAG register
	WR	0	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 4 RLD register
	WR	0	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 4 CMR register
	WR	0	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 4 IOR register
	WR	0	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 4 IDR register
	WR	1	0	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 RLD register
	WR	1	0	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 CMR register
	WR	1	1	0	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 IOR register
	WR	1	1	1	*----------	SEE LS7266R1 SPEC	----------			Write to Channel 3 and 4 IDR register
PCIBASE2+8	RD	CBINT4	CBINT3	CBINT2	CBINT1	IND4SEL	IND3SEL	IND2SEL	IND1SEL	Interrupt routing control register
	WR	CBINT4	CBINT3	CBINT2	CBINT1	IND4SEL	IND3SEL	IND2SEL	IND1SEL	
PCIBASE2+9	RD	N/A	PH4B1	PH4B0	PH4A	PH3B	PH3A	PH2B	PH2A	Input signal control register (for cascading counters)
	WR	N/A	PH4B1	PH4B0	PH4A	PH3B	PH3A	PH2B	PH2A	
PCIBASE2+10	RD	*----------	8259 Programmable Interrupt Controller Port A	----------						Programmable Interrupt Controller Port A
	WR	*----------	8259 Programmable Interrupt Controller Port A	----------						*----------
PCIBASE2+11	RD	*----------	8259 Programmable Interrupt Controller Port B	----------						Programmable Interrupt Controller Port B
	WR	*----------	8259 Programmable Interrupt Controller Port B	----------						*----------

The LS7266R1 contains two control registers per axis, and the configuration of each axis requires a sequence of writes to set the operating mode of the chip. The following description outlines the configuration steps for a single axis. The first axis control registers are contained at the BADR2 +0 address and at BADR2+1. The other axis perform identically.

When read, the BADR2 +0 address returns the Output Latch (OL) data. Writes to the BADR2 +0 address set the Preset Register (PR). All register access to the LS7266R1 is done through byte wide operations. However, the PR and OL registers are 24-bits wide. The LS7266R1 contains a byte pointer that is auto-incremented after each write. To set the preset register requires three byte-wide writes (outport b), starting with the least significant byte. Be sure to reset the byte pointer prior to any register writes. The BADR2+1 address accesses the status and control registers for the given axis. There are four unique registers which can be configured by writing to the BADR2+1 register. For further details please also refer to the LS7266R1 data sheet.

At the BADR2 +1 location the four registers are uniquely selected for write access by the value in bits 5 and 6. The following table indicates the bit values for each register.

Register Name	Selected for Write Access by bits 5 & 6
Reset and Load (RLD)	x00x xxxx
Count Mode (CMR)	x01x xxxx
Input/Output Control (IOR)	x10x xxxx
Index Control (IDR)	x11x xxxx

If bit 7 is one (1) then the selected operation will effect both the X and Y channels. If bit 7 is zero then the X*/Y input is used to select the target channel. The remaining bits in each register are used to configure the LS7266R1 for various operating modes.

The following sections describe how each register can be configured. It should be noted that in several instances there are bit fields that support multiple options. Obviously, only one option can be selected for each write operation, thus, it may be necessary to perform several writes to the same register to achieve the desired results. For example, to initialize the RLD register, that is, to clear all of the status flags and reset the counter, requires three separate writes to the register. Refer to the tables below for more details.

4.2.1 Counter Mode Register (CMR)

The CMR contains three user-configurable fields, count representation, count mode, and quadrature scaling. Each field consists of one or more bits in the CMR register. After you select the desired mode, the bit fields need to be assembled into a byte that can be written to the CMR register. Bits 5 and 6 are always 1 and 0, respectively, for CMR register accesses.

Data Encoding
The quadrature count can be represented in either BCD or binary. Bit 0 of the CMR register selects the desired option.

CMR Count Representation	Bit 0 Value for Count Configuration
BINARY	x01x xxx0
BCD	x01x xxx1

Count Mode
There are four different count modes that are selected by bits 1 and 2. The count modes are Normal, Range-Limit, Non-recycle, and Modulo-N.

CMR Count Mode	Bit 1 & 2 Value for Mode Selection
Normal	x01x x00x
Range-Limit	x01x x10x
Non-recycle	x01x x01x
Modulo-N	x01x x11x

Count Mode Definitions:

- Range Limit: An upper limit, set by PR, and a lower limit, set to 0, are set. The CNTR stops at CNTR = PR when counting UP and when CNTR = 0 when counting DOWN. Counting resumed only when the count direction is reversed.
- Non-Recycle: CNTR is disabled whenever overflow or underflow happens. End-of-cycle marked by Carry (UP) or Borrow (DOWN). Re-enabled by reset or load on CNTR.
- Modulo-N: Count boundary set between 0 and content of PR. When counting up, at CNTR = PR, the CNTR is reset to 0 and the up count is continued from that point. When counting down, at CNTR = 0, the CNTR is loaded with content of PR and down count is continued from that point.

Quadrature scaling
There are four different scaling values that can be applied to quadrature signals: Non-quad, X1, X2, and X4. The scaling to be applied is set in bits 3 & 4 of the CMR register. Assuming the attached encoder generates 2500 pulses per revolution in

X1 mode, then you would receive 5000 pulses in X2 mode and 10,000 pulses in X4 mode. If the board will be used to detect simple clock pulses then select Non-Quadrature mode.

CMR Quadrature Scaling	Bit 3 & 4 value for quad scaling
Non-Quadrature	x010 0xxx
X1	x010 1xxx
X2	x011 0xxx
X4	x011 1xxx

4.2.2 Reset and Load Signal Decoders (RLD)

The RLD contains three user configurable fields. This register controls all of the reset options as well as the data transfer options. The following sections describe each field in the RLD register and the various modes that can be set for operation. The RLD register is used to reset the counter and the status flags and also to provide access to the error bit E, which is the only means for resetting this flag once it is set.

RLD Reset Byte Pointer Field
This field is used to reset the byte pointer. The byte pointer is auto-incremented each time the Output Latch (OL) register is read or the Preset Register (PR) is written to. The byte pointer must be reset prior to any access to the 24-bit counter register.

RLD Byte Pointer Reset	Bit 0 value for byte pointer reset
NOP	x00x xxx0
BP Reset	x00x xxx1

RLD Reset Fields
In addition to the byte pointer there are several other fields that can be reset. This field provides the mechanism for resetting the counter and all of the status flags. The Borrow Toggle (BT), Carry Toggle (CT), Compare Toggle (CPT), and the Sign Flag (S) can all be reset through bits 1 and 2 of the RLD register. Finally, the only way to clear the Error (E) flag once it has been set is through the RLD register.

RLD Reset	Bit 1 & 2 value for reset fields
NOP	x00x x00x
CNTR	x00x x01x
BT, CT, CPT, and S	x00x x10x
E	x00x x11x

RLD Transfer Fields
The final bit field in the RLD register consists of bits 3 and 4. This field controls the data transfer operation of the LS7266 chip. There are three options that are available as listed in the table below. The contents of the Preset Register can be transferred to the Counter, the contents of the Counter can be copied to the Output Latch for reading, and the Preset Register contents can be copied to the Filter Clock Prescalar. This register provides the software mechanism for reading the current count from the encoder. First write to the RLD register to transfer the contents of the counter to the output latch, then reset the byte pointer and perform three reads of the output latch.

RLD Transfer	Bit 3 & 4 value for transfer fields
NOP	x000 0xxx
Preset to Counter	x000 1xxx
Counter to Output Latch	x001 0xxx
Preset to Filter Clock Prescalar	x001 1xxx

4.2.3 Input/Output Control Register (IOR)

The IOR register contains four user configurable fields and should be initialized prior to writing the IDR register which follows. The IOR register, in conjunction with the IDR register, configures how the A and B input signals are interpreted.

A/B configuration bit
This configuration bit controls whether or not the A and B inputs are enabled or disabled. This bit must be enabled for the counter to respond to input clock pulses.

IOR A/B enable/disable	Bit 0 value for enable/disable
Disable A and B	x10x xxx0
Enable A and B	x10x xxx1

LCNTR/LOL Pin Configuration
This register is only applicable if the IDR register bit 2 is set to 0. In this case the Index input from the external encoder is directed to the LCNTR/LOL pin. This bit then configures the operation of the LCNTR/LOL pin. The operation can be set to either load the counter with the preset value or load the output latch input. Thus, if the IDR register specifies the Load CNTR operation, then each time the Index input is asserted, the counter will be reloaded with the value stored in the preset. If the Load OL input option is selected, then each Index input will cause the current counter value to be updated to the Output Latch. In this mode you are not required to use the RLD register to force the contents of the counter to be copied to the output latch. The contents of the counter will automatically be available at the Output Latch every time the Index signal is asserted. **Note: the Index input is asserted once per revolution.**

IOR LCNTR/LOL pin configuration	Bit 1 value for CNTR/LOL select
Load CNTR	x10x xx0x
Load OL input	x10x xx1x

RCNTR/ABG Pin Configuration
This bit configures the operation of the RCNTR/ABG pin. This register in only applicable if the IDR register bit 2 is set to 1. In this mode the Index input from the encoder is directed to the RCNTR/ABG input. The operation can be configured to either reset the CNTR input or as an A/B enable gate. **Note: in non-quadrature mode this register should be set for A/B enable gate operation.**

IOR RCNTR/ABG pin configuration	Bit 2 value for RCNTR/ABG select
Reset CNTR	x10x x0xx
A/B enable gate	x10x x1xx

FLAG 1 & 2 Configuration
This bit field controls the operation of the FLG1 and FLG2 real-time counter outputs. The selected configuration will determine what signal is output on the FLG1 and FLG2 output pins. For cascading the counters this register should be set for Carry/Borrow, Up/Down operation. The FLGx output pins are also redirected to the onboard 8259 Programmable Interrupt

Controller (PIC). Depending on how the FLGx register is configured an interrupt can be generated based on the options in the following table.

IOR FLG1/FLG2 configuration	Bit 3 & 4 value for FLG1/FLG2 select
FLG1 Carry, FLG2 Borrow	x100 0xxx
FLG1 Compare, FLG2 Borrow	x100 1xxx
FLG1 Carry/Borrow, FLG2 U/D	x101 0xxx
FLG1 IDX, FLG2 is E	x101 1xxx

4.2.4 Index Control Register (IDR)

The IDR register controls how the Index input from the encoder should be treated; it contains three user-configurable fields. The polarity and Index routing selection are also made through this register. **Note: Disable indexing for non-quadrature inputs.**

Enable/Disable Index
This bit is used to select whether or not indexing is enabled for the LS7266.

IDR Index enable/disable	Bit 0 value for enable/disable select
Disable Index	x11x xxx0
Enable Index	x11x xxx1

Index Polarity Select
If your are connecting a quadrature encoder, then this bit selects the polarity for the index: 0 for negative polarity and 1 for positive polarity.

IDR Index Polarity	Bit 1 value for Index Polarity select
Negative Index Polarity	x11x xx0x
Positive Index Polarity	x11x xx1x

Index Pin Select
The final bit field in the IDR register determines where the index input will be connected. A 0 in this field will select the LCNTR/LOL pin as the connection for the encoder index output. If the field is set to 1, then the RCNTR/ABG pin is selected as the index input. Prior to configuring this field the IOR register bit 1 or 2 must be configured. See the previous section for more details on these bit fields.

IDR Index Pin Select	Bit 2 value for Index Pin select
LCNTR/LOL pin is indexed	x11x x0xx
RCNTR/ABG pin is indexed	x11x x1xx

4.3 GLOBAL CONTROL REGISTERS

Four global control registers are located at offsets 8-11 from the BADR2 address. The following sections outline these four registers and the various control functionality which they provide. Unlike the channel configuration registers, the current state of the global control registers can be obtained through reading the desired register. To help understand registers and functions, refer to Figure 4-1 below as you read the register descriptions.

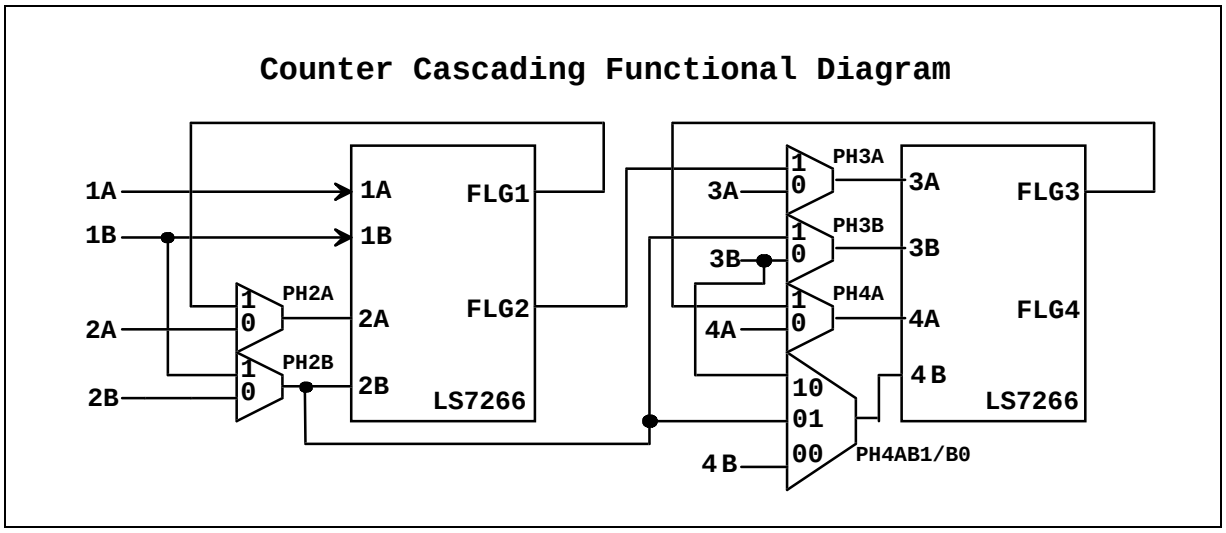

Figure 4-1. Cascade Counting Functional Diagram

4.3.1 Index & Interrupt Routing Control (BADR2 + 8)

The first four bits of this register route the index pin from the quadrature encoder to either the LCNTR/LOL input or the RCNTR/ABG input for each of the four encoder inputs. The value set in this register should be consistent with the value written in the IDR register. The most significant four bits select the interrupt source as either Compare select or Carry/Borrow select.

Interrupt Routing:

Register BADR2 + 8 D4-D7

Channel	**1**	**2**	**3**	**4**
Input	CBINT1	CBINT2	CBINT3	CBINT4
FLG1 - Carry/Compare/Index	0	0	0	0
FLG2 - Borrow/UP/Down	1	1	1	1

Index Routing: Connects the index input to the counter control input pin below.

Register BADR2 + 8 D0-D3

Channel	**1**	**2**	**3**	**4**
Input	IND1SEL	IND2SEL	IND3SEL	IND4SEL
RCNTR/ABG	0	0	0	0
LCNTR/LOL	1	1	1	1

*The FLG1 and FLG2 output pins are register programmable for Carry, Borrow, Compare and flag status functions. (See 7266 IOR register for proper functionality)

4.3.2 Input Signal Control (BADR2 + 9)

Controls Counter Cascading: (Non-quadrature mode)

Set the FLGx pin for the CARRY/BORROW function through the IOR Register bits 3 and 4 so that the cascaded direction output will be CARRY for UP counting and BORROW for DOWN counting.

Register BADR2 + 9 D0-D6

	PH2A	PH2B	PH3A	PH3B	PH4A	PH4B1/PH4B0
(4) 24-bit counters (1/2/3/4)	0	0	0	0	0	0,0
(2) 48-bit counters (1-2/3-4)	1	1	0	0	1	1,0
(1) 24-bit/1 - 72bit (1/2-3-4)	0	0	1	1	1	0,1
(1) 96-bit counter (1-2-3-4)	1	1	1	1	1	0,1

Defaults to 0x00 (no inter-counter connections).

4.3.3 Programmable Interrupt Control Port A & B (BADR2 + 10 & 11)

The PCI-QUAD04 uses an 8259A Programmable Interrupt Controller which routes up to eight interrupts from the Index inputs or Carry/Borrow outputs (due to overflow, underflow, or compare match, depending on strap setting and register programming) from the LS7266's. The interrupt output from the 8259 is routed through the FPGA and register enabled and set to IRQ 2, 3, 5, 7, 10, 11, 12, or 15 on the PC bus. Each interrupt can be masked to prevent unwanted interrupt generation through 8259 programming.

The 8259A can only be used in non-vectored x86/x88 mode, or polled mode. That is, when an interrupt is generated, the user must poll the 8259A to determine which interrupt was set. This mode is set externally by setting:

INTA* (pin 26) connected to +5VDC
SP\EN (pin 16) connected to 10kohm pullup to +5VDC
CAS0:2 (pins 12,13,15) connected to 10kohm pullup to +5VDC

For programming and further information on the 8259A interrupt controller, consult an Intel Peripheral Components 1992 data book (or Harris 8259A data sheet).

5.0 SPECIFICATIONS

All Specifications typical for 25°C unless otherwise specified.

Power consumption

(Not supplying power to external encoders)

+5V	325 mA typical, 460 mA max.

(Typical supplying 1 Dynamics Research Incremental Optical Rotary Encoder part number M21AAFOBB2E-2500)

+5V	1058 mA typical, 1479 mA max.

Input section

Receiver type	SN75ALS175 quad differential receiver
Configuration	Each channel consists of PhaseA input, PhaseB input and Index input. Each input is jumper-selectable as single-ended or differential
Differential	PhaseA, PhaseB and Index (+) inputs at user connector routed to (+) inputs of differential receiver. PhaseA, PhaseB and Index (–) inputs at user connector routed to (–) inputs of differential receiver.
Single-Ended	PhaseA, PhaseB and Index (+) inputs at user connector routed to (+) inputs of differential receiver. PhaseA, PhaseB and Index (–) inputs at user connector routed to ground. (–) inputs of differential receiver routed to +3V reference.
Number of channels	4
Common mode input voltage range	±12V max.
Differential input voltage range	±12V max.
Input sensitivity	±200mV
Input hysteresis	50mV typ.
Input impedance	12 kohm min.
Propagation delay	27 ns max. (tpLH, tpHL)
Absolute maximum input voltage	
Differential	±14V max.
Miscellaneous	Meets or exceeds ANSI EIA/TIA-422-B, EIA/TIA-423-B, RS-485. Meets ITU recommendations V.10, V.11, X.26, X.27. Designed for multipoint busses on long lines and in noisy environments.

Counter section

Counter type	LS7266R1 24-bit Dual-axis Quadrature Counter
Quadrature Mode	
Clock frequency	4.3 MHz max.
Separation	57 ns min.
Clock pulse width	115 ns min.
Index pulse width	85 ns min.
Count Mode	
Clock frequency	30 MHz max, (25 MHz max Mod-N mode)
Clock A - high pulse width	14 ns min.
Clock A - low pulse width	14 ns min.
Filter clock (FCK)	10 MHz
Digital filter rate	10 MHz, software selectable divider (1 to 256 in single steps)
Crystal oscillator (FCK source)	
Frequency	10 MHz
Frequency accuracy	100 ppm

Interrupt Controller Section

Controller type	8259 Programmable Interrupt Controller
Configuration	Polled mode only
Interrupts	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9052 INTCSR
Interrupt polarity	High or low level. Programmable through PLX9052 Rising / falling edge. Programmable through PLX-9052
Interrupt sources	All Carry/Borrow outputs from LS7266R1, all Index inputs

Environmental

Operating temerature range	0 to 70°C
Storage temerature range	–40 to 100°C
Humidity	0 to 90% non-condensing

For your notes

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

Part Number	Description
PCI-QUAD04	Four-Channel Incremental Quadrature Encoder Board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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