SOMAT

User Manual

English

SoMat eDAQ

with TCE Software

I2740-1.1 en SoMat P/N DOC 0004-01

HBM

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Safety Information

Safety Rules

The supply connection, as well as the signal and sense leads, must be installed in such a way that electromagnetic interference does not adversely affect device functionality.

Automation equipment and devices must be covered over in such a way that adequate protection or locking against unintentional actuation is provided (such as access checks, password protection, etc.).

When devices are working in a network, these networks must be designed in such a way that malfunctions in individual nodes can be detected and shut down.

Safety precautions must be taken both in terms of hardware and software, so that a line break or other interruptions to signal transmission, such as via the bus interfaces, do not cause undefined states or loss of data in the automation device.

Before connecting the device, make sure that the mains voltage and current type specified on the type plate correspond to the mains voltage and current type at the site of installation and that the current circuit used is sufficiently safe.

The maximum permissible supply voltage for the eDAQ is 55 V DC.

Appropriate use

The eDAQ and its connected transducers may be used for measurement tasks only and directly related control tasks. To ensure safe operation, the transducer may only be used as specified in the operating manual. It is also essential to follow the respective legal and safety regulations for the application concerned during use. The same applies to the use of accessories.

Each time, before starting up the equipment, you must first run a project planning and risk analysis that takes into account all the safety aspects of automation technology. This particularly concerns personal and machine protection.

Additional safety precautions must be taken in plants where malfunctions could cause major damage, loss of data or even personal injury. In the event of a fault, these precautions establish safe operating conditions.

This can be done, for example, by mechanical interlocking, error signaling, limit value switches, etc.

General dangers of failing to follow the safety instructions

The eDAQ complies with the state of the art and is safe to operate. Inappropriate use and operation by untrained personnel can give rise to remaining dangers.

Anyone responsible for installing, starting up, maintaining or repairing the equipment needs to have read and understood the operating manual and in particular the safety instructions.

Maintenance and cleaning

The eDAQ is maintenance free. Please note the following when cleaning the housing:

- Before cleaning, disconnect the equipment from the power supply.
- Clean the housing with a soft, slightly damp (not wet!) cloth. Never use solvents, since these could damage the labelling on the front panel and the display.
- When cleaning, ensure that no liquid gets into the equipment or connections.

Remaining dangers

The scope of supply and performance of the data acquisition system covers only a small area of measurement technology. In addition, equipment planners, installers and operators should plan, implement and respond to the safety engineering considerations of measurement technology in such a way as to minimize remaining dangers. Prevailing regulations must be complied with at all times. There must be reference to the remaining dangers connected with measurement technology. After making settings and carrying out activities that are password-protected, you must make sure that any controls that may be connected remain in safe condition until the switching performance of the amplifier system has been tested.

In this manual, the following symbols are used to point out remaining dangers:

DANGER

Meaning: Maximum danger level

Warns of an imminently dangerous situation in which failure to comply with safety requirements will result in death or serious bodily injury.

WARNING

Meaning: Dangerous situation

Warns of a potentially dangerous situation in which failure to comply with safety requirements can result in death or serious bodily injury.

CAUTION

Meaning: Potentially dangerous situation

Warns of a potentially dangerous situation in which failure to comply with safety requirements could result in death or serious bodily injury.

Meaning: Electrostatic sensitive devices

Devices marked with this symbol can be destroyed by electrostatic discharge. Please observe the precautions for handling electrostatic sensitive devices.

Symbols pointing out notes on use and waste disposal as well as useful information:

NOTE
Points out that important information about the product or its handling is being given.

Meaning: CE mark
The CE mark enables the manufacture to guarantee that the product complies with the requirements of the relevant CE directives (the declaration of conformity is available at http://www.hbm.com/HBMdoc).

Meaning: Statutory marking requirements for waste disposal
National and local regulations regarding the protection of the environment and recycling of raw materials require old equipment to be separated from regular domestic waste for disposal.
For more detailed information on disposal, please contact local authorities or the dealer from whom you purchased the product.

Working safely
Error messages may only be acknowledged if the cause for the error has been removed and no further danger exists.

Conversions and modifications
HBM's express consent is required for modifications affecting the SoMat eDAQ design and safety. HBM does not take responsibility for damage resulting from unauthorized modifications.
In particular, any repair or soldering work on motherboards is prohibited. When exchanging complete assemblies, it is essential to use original HBM parts only.
The product is delivered from the factory with a fixed hardware and software configuration. Changes can only be made within the possibilities documented in the manuals.

Qualified personnel
The equipment may be used by qualified personnel only; the specifications and the special safety regulations need to be followed in all cases.
This means people who meet at least one of the three following requirements:

- Knowledge of the safety concepts of automation technology is a requirement and as project personnel, you must be familiar with these concepts.
- As automation plant operating personnel, you have been instructed how to handle the machinery and are familiar with the operation of the equipment and technologies described in this documentation.
- As commissioning engineers or service engineers, you have successfully completed the training to qualify you to repair the automation systems. You are also authorized to activate, to ground and label circuits and equipment in accordance with safety engineering standards.

It is also essential to comply with the appropriate legal and safety regulations for the application concerned during use. The same applies to the use of accessories.
The term "qualified personnel" refers to staff familiar with the installation, fitting, start-up and operation of the product, and trained according to their job.

1 Getting Started

The SoMat eDAQ is a microprocessor-based data acquisition system designed for portable data collection in a variety of test environments.

1.1 Overview

The SoMat eDAQ is a sealed stand-alone data acquisition system for testing in the harshest of environments. It has leading-edge signal conditioning and a capacity to perform a broad range of on-board data processing. Engineered to be rugged and mobile, the eDAQ is tested to military standards at 10 g's from 55 to 2000 Hz. Input power for the system operates in a wide range from 10 to 55 volts DC for the ECPU-PLUS processor. Internal back-up batteries protect the eDAQ from unplanned power losses or low voltage events. Hundreds of synchronous channels are possible in a single system with virtually limitless channel counts when networking multiple systems using Ethernet communications.

1.1.1 eDAQ Layers

The eDAQ consists of one base processor layer and a number of optional add-on layers. The following table lists the available layers, including the base processor.

Name	Order Number	Description
ECPU	1-ECPU-PLUS-2	eDAQ Base Processor with Extended Voltage
	1-ECPU-PLUS-COM-2	eDAQ Base Processor with integrated ECOM layer
ECOM	1-ECOM-2	eDAQ Vehicle Network Communications Layer
EHLS	1-EHLS-B-2	eDAQ High Level Analog Layer
	1-EHLS-AO-2	eDAQ High Level Analog Layer with Analog Out
EBRG	1-EBRG-350-B-2	eDAQ Bridge Layer; 350-Ohm
	1-EBRG-350-AO-2	eDAQ Bridge Layer; 350-Ohm with Analog Out
	1-EBRG-120-B-2	eDAQ Bridge Layer; 120-Ohm
	1-EBRG-120-AO-2	eDAQ Bridge Layer; 120-Ohm with Analog Out
EDIO	1-EDIO-B-2	eDAQ Digital I/O Layer
	1-EDIO-5HZGPS-2	eDAQ Digital I/O Layer with SoMat GPS
ENTB	1-ENTB-2	eDAQ Non-Isolated Thermocouple Layer
EITB	1-EITB-K-2	eDAQ Isolated Thermocouple Layer ; K-type
	1-EITB-J-2	eDAQ Isolated Thermocouple Layer; J-type
	1-EITB-T-2	eDAQ Isolated Thermocouple Layer; T-type
	1-EITB-E-2	eDAQ Isolated Thermocouple Layer ; E-type
ELLB	N/A	eDAQ Low Level Layer (no longer in production)
EHLB	N/A	eDAQ High Level Layer (no longer in production)

1.2 Equipment

This section describes the provided equipment and the support equipment necessary to set up the eDAQ system and run a test.

1.2.1 Provided Equipment

The initial shipment of a basic eDAQ contains the hardware listed below; additional hardware may be included based on options ordered. The eDAQ also comes with SoMat Test Control Environment (TCE) software.

NOTE

If any items do not arrive as expected, contact your system supplier, nearest HBM sales representative or HBM immediately.

Item (Order No.)	Description
SoMat eDAQ	SoMat eDAQ base layer and any optional layers.
SoMat Digital I/O Transducer Cable (1-SAC-EDIGIO-2)	44-pin HDD-Sub male plug with two connector cables ending in pigtails.
SoMat Communications Cable (1-SAC-ESR9/XO-2 or 1-SAC-ESR9/HUB-2)	26-pin HDD-Sub male plug with two connector cables, one labeled “E-ETHERNET” which ends in an RJ-45 connector and the other labeled “RS232” which ends in a 9-pin D-Sub female plug. The XO cable is used for connection directly to the host computer, while the optional HUB cable is used for network operation.
SoMat Power Cable (1-SAC-EPWR15-2)	15-pin D-Sub female plug with two connector cables ending in pigtails.
SoMat TCE Installation CD	CD containing the installation files for TCE.

1.2.2 Support Equipment

In addition to the eDAQ base processor, add-on layers and included cables, set up of the eDAQ system requires an adequate power supply, a support PC and any transducers or sensors needed for testing.

Power Supply

The eDAQ is designed to always be connected to an adequate power supply for the duration of all test runs. An example of an adequate power supply is a charged nominal 12-volt vehicle battery system that reliably supplies around 13.5 volts. The ECPU-PLUS processor supports nominal 12-, 24- and 42-volt vehicle battery systems. HBM also offers an optional SoMat AC Power Supply (1-E-AC-2 or 1-E-AC/18-2).

For more information on eDAQ power, see “Power Considerations” on page 31.

Support PC

A support PC is necessary to run TCE. The PC must meet these minimum requirements for TCE to operate correctly.

- Microsoft Windows® 95/98/NT/2000/XP
- 40 MB of available hard disk space

- CD-ROM drive or Internet access (required for updating and installing software)
- 16 MB of RAM (32 MB recommended)
- Mouse or other pointing device
- An Ethernet card

Sensors
The eDAQ supports a wide variety of sensors for data acquisition, including several offered directly by HBM. Contact your sales representative or visit www.hbm.com/somat for more information.

1.3 Setting Up the System

Setting up the eDAQ data acquisition system involves installing TCE on the support PC and setting up the eDAQ hardware.

1.3.1 Installing SoMat Test Control Environment (TCE)

To install TCE:

1. Run the TCE installer found on the TCE/eDAQ distribution CD or downloaded from the www.hbm.com/somat. Follow the instructions on screen.
2. When prompted, enter the desired destination folder for the installation. By default, the TCE installation program places each new software release in a unique folder.
3. If updating to a new version of TCE, copy or move the file “TceMS.ini” from the “Work” subdirectory of the previous TCE installation folder to the “Work” subdirectory of the new TCE installation folder. This process transfers the current TCE preference settings into the new version of TCE.

Using a Common Installation Folder
Previous versions of the TCE installer used a common destination folder for all releases. To continue using a common folder, uninstall the previous TCE version before starting the new installation. Change the installation program default folder name to the common folder name (previously, “C:\Program Files\SoMat\Tce_eDAQ”) during the installation process. To keep TCE preference settings, be sure to save the “TceMS.ini” file before uninstalling the previous version of TCE.

1.3.2 Getting Familiar with the eDAQ

eDAQ Front and Back Panels
The ECPU front panel contains the power switch and status LEDs needed for eDAQ operation as well as the access door to the PC Card slot. The power and communications connectors needed to set up the eDAQ are on the ECPU back panel. The configuration of the front and back panels are shown in the following diagrams.

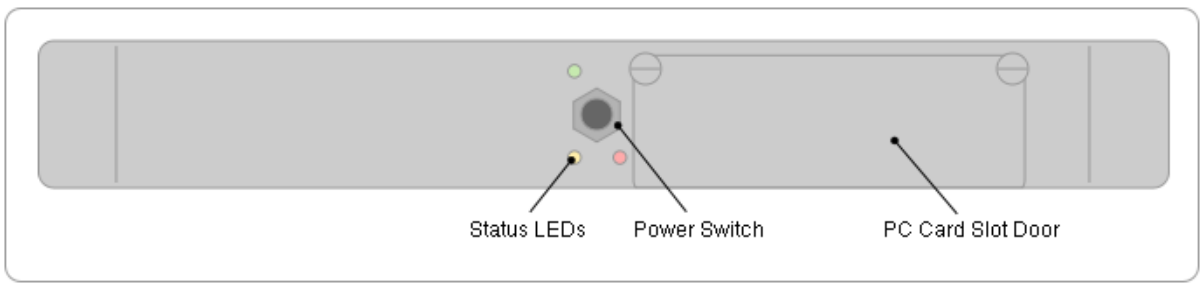


Figure 1-1: Diagram of the eDAQ front panel.

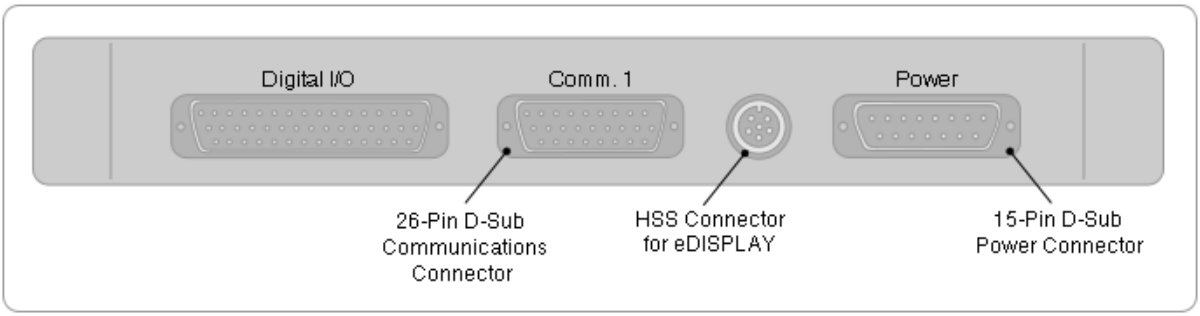


Figure 1-2: Diagram of the eDAQ back panel.

SoMat Communications Cables

The eDAQ is compatible with several different communications cables. Each cable has a 26-pin D-Sub for connection to the eDAQ Comm port. The cables may also have an Ethernet X/O connector for direct communication from the eDAQ to the PC, an Ethernet HUB connector for communication through an Ethernet hub, a 9-pin serial connector for communications through a PC serial port or a set of two LEMO sync connectors for networking eDAQ systems. A summary of the available communication cables is below.

Communications Cable	Ethernet (X/O)	Ethernet (HUB)	Serial	Sync
1-E-ETHERNET X/O-2	X			
1-E-ETHERNET HUB-2		X		
1-SAC-ESR9/XO-2	X		X	
1-SAC-ESR9/HUB-2		X	X	
1-SAC-ESYNCADAPT-2		X		X
1-SAC-ESYNCADAPT-SC-2		X	X	X

1.3.3 Setting Up the eDAQ

To power the eDAQ and establish communications with its support PC:

1. Connect the 26-pin D-Sub connector of a SoMat Communications Cable to the Comm connector on the eDAQ. For Ethernet communication, connect the RJ-45 connector either directly to the PC or to an Ethernet hub, depending on the communications table. For serial communication, connect the 9-pin D-Sub connector directly to the PC. The serial connection may be removed once the setup process is complete, but it may be helpful in network setup should difficulties arise with Ethernet communication.
2. Connect the appropriate cable(s) to the eDAQ for the desired type of transducers or sensors.
3. Make sure the power supply for the eDAQ is turned off and connect the SoMat Power Cable (1-SAC-EPWR15-2) between the eDAQ Power connector and the power supply. Use the red and black pigtails on the cable labeled “POWER” for the main power connection: black to the negative or ground terminal and red to the positive terminal. The remote cable, labeled “REMOTE POWER,” is for remote control of the eDAQ. To use remote power, connect a single-pole, single-throw

switch to the pigtails. If not using remote power, make sure the pigtail wires are well insulated as shorting the two wires together turns the eDAQ off. For more information on remote power usage see “Remote Power” on page 33.

4. Turn on the power supply. If the status LEDs do not light, press the power switch on the front panel to apply power to the eDAQ.

1.4 Test Process

There are several phases to conducting a test using the eDAQ as outlined below. For more information on using TCE to complete these phases, see “Using TCE” on page 63.

Plan Test

Before any test setup, first develop a test plan including the test objective, the physical quantities to be measured, any signal manipulation or computations to perform during the test, the desired data collection method and when and how often data should be recorded.

Prepare Hardware

After planning the test, install the various gages, sensors and cables required for the test. This includes attaching the transducers to the components being measured, connecting the transducer cables to the transducer and connecting the transducer cables to the appropriate eDAQ connectors.

Define Test

The eDAQ collects data from transducers and other input sources, manipulates the signals using computed channels and stores the data in a variety of DataModes™. Use the TCE software that comes with the eDAQ to fully define the desired test. Also during this phase, verify that the transducers and data channels are operating as expected using TCE channel display options.

Run Test

Running the test consists of several necessary steps including initializing the eDAQ, starting the test run, collecting the data, stopping the test run and ending the test session. After a test is initialized, the eDAQ allows for multiple test runs during a single test session. Use TCE or the integrated web interface to perform these tasks as well as more advanced test run options.

Upload, Display and Analyze Test Data

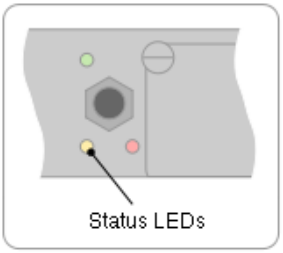
Use TCE or the web interface to upload the acquired test data. The web interface also offers simple data displays. For more advanced data display and analysis, use SoMat InField™. For more information on InField, refer to the InField User’s Manual.

2 Using the eDAQ

The following chapter describes the setup and operation of the eDAQ including the LED status indicators, updating firmware, eDAQ communications, power considerations, data storage and eDAQ networking.

2.1 eDAQ Base System

2.1.1 Status LEDs



There are three LEDs (green, yellow and red) located on the eDAQ front panel that are important indicators of eDAQ status.

Initial State
When powering on, all three LEDs turn on indicating that the main processor is starting the boot up process. However, the eDAQ displays different LED states than this on abnormal conditions as defined by the following table.

Red	Yellow	Green	Description
4 Hz	Off	Off	Bus pins misaligned.
4 Hz	4 Hz	Off	Blown fuse.
On	On	Off	Power supply failure or voltages not stabilized.
On	On	On	No problems detected, boot up starting.

NOTE
If all three LEDs stay on for more than about 10 seconds, the boot has failed at a very early stage or the boot was interrupted in the serial loader (which should not happen accidentally).

Possible States
After all three LEDs are on, the main processor boot up begins. The LED states that can exist after the boot up starts are defined as follows.

Red	Yellow	Green	Description
On	On	On	Normal for early in boot up process.
Off	On	On	Normal for later in boot up process.
Off	Off	On	Ready, no test initialized, no error/status flag.
On	Off	On	Ready, no test initialized, error/status flag.

Red	Yellow	Green	Description
Off	0.5 Hz	On	Ready, test initialized, no error/status flag.
On	0.5 Hz	On	Ready, test initialized, error/status flag.
Off	1 Hz	1 Hz	Ready, waiting for sync, no error/status flag.
On	1 Hz	1 Hz	Ready, waiting for sync, error/status flag.
Off	8 Hz	On	Ready, test running, no error/status flag.
On	8 Hz	On	Ready, test running, error/status flag.
2 Hz	On	On	Updating firmware - do not power down.
4 Hz	4 Hz	4 Hz	Power microprocessor not communicating with main processor.
On	On	2 Hz	Powering down.
Off	Off	Off	Powered down.

For more information on error and status flags, see “eDAQ Flags” on page 188.

2.1.2 eDAQ Layer Addressing

The eDAQ stack is configured at the factory with the layer address jumpers properly set. Follow the guidelines below to reconfigure an eDAQ stack.

Checking Current Layer Addresses

To check the current layer addresses, use TCE to upload the eDAQ log. Select Upload FCS Log from the FCS Diagnostics sub-menu of the FCS Setup menu. Choose to view the file in Microsoft® Notepad and then scroll to the end of the log file where there is a list of the installed hardware and their jumper address. An example list is below.

```
<** LogBook End **>

Slot Jumpers : Type      Name       Version   Serial
00       0 : MPBMS01   MPB        v5.4      MSMPB.13-1632
01       0 : MPSMS01   MPBSer                MSMPB.13-1632
02       0 : PWRMS01   Power      v2.2      MSMPB.13-1632
03       1 : BRGMS01   Brg_1      v1.2      MSBRG.02-0702
04       2 : BRGMS01   Brg_2      v1.2      MSBRG.02-1235
05       4 : DIOMS01   DIO_1      v1.7      MSDIO.02-1097
06       4 : GPSMS01   GPS_1      v1.7      MSDIO.02-1097
07       6 : HLSMS01   HLSS_1     v1.1      MSHLS.03-2378
```

Layer Address Jumpers

On all eDAQ layers except the ECPU, there is a set of three jumper locations used to assign a physical layer address. Each jumper location consists of two associated pins labeled 1-2, 3-4 or 5-6 where pins 1-2 represent the least significant digit and pins 5-6 represent the most significant in a three-digit binary number. A jumpered pair results in a logical 0. An illustration of all possible logical addresses follows.

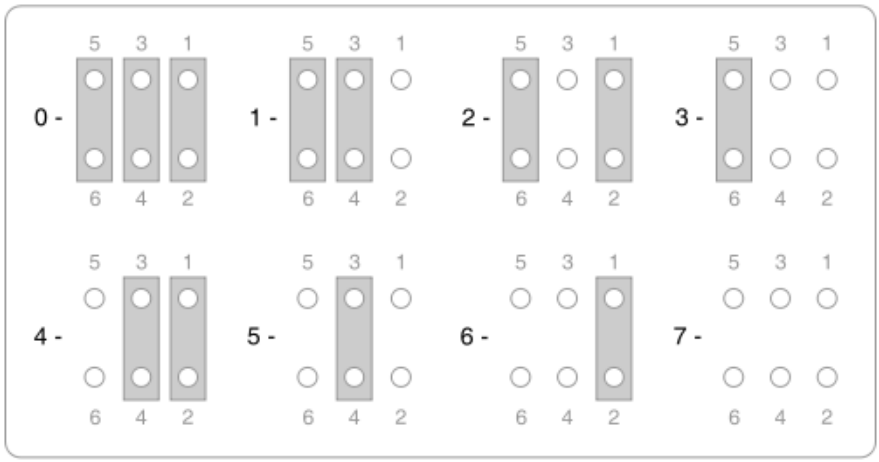


Figure 2-1: Possible jumper configurations for addressing eDAQ layers.

All layer address jumper sets are on the side of the bus connector receptacle (i.e., opposite the side with the bus connector bare pins). The jumper is labeled JP1 on all layers except the EHLB where the jumper is labeled JP2.

Valid Layer Addresses

There are two general types of layers for the eDAQ: type I layers, previously referred to as legacy boards, and type II layers, previously referred to as expansion boards. The table below defines the type of all available layers.

Type I Layers	Type II Layers
ECPU (Base Processor)	EDIO (Digital I/O Layer)
EHLB (High Level Layer)	ECOM (Vehicle Network Communications Layer)
ELLB (Low Level Layer)	EHLS (High Level Analog Layer)
	EBRG (Bridge Layer)
	ENTB (Thermocouple Layer)
	EITB (Isolated Thermocouple Layer)

From the factory, the ECPU layer is hardwired with the address 0 and is always positioned at the bottom of the stack. The stack can include any combination of additional add-on layers stacked on top of the ECPU layer. The following rules apply when addressing add-on layers in the same eDAQ stack.

- A type I and type II layer may share a layer address.
- A type I layer address must be unique among other type I layers.
- A type II layer address must be unique among other type II layers.
- A type I layer cannot have the address of 6 when type II layers are present.
- A type I layer cannot have the address of 7 under any configuration.

Taking these rules into account, an eDAQ stack configuration with all type I layers may have a maximum of five add-on layers and any other configuration may have a maximum of four type I layers and eight type II layers not accounting for power and temperature limitations.

NOTE
For eDAQ stacks with more than one EDIO layer, any EDIO layer with a GPS module must have a lower layer address than all EDIO layers without a GPS module. This rule also applies to stacks with more than one ECOM layer.

Stacking Order
There are hardware IDs associated with each layer as displayed in TCE or the web interface. For all layer types that can appear more than once in an eDAQ stack, the hardware IDs have numbered suffixes starting with 1 and are assigned starting with the layer that has the lowest layer address. For example, if there are two EBRG layers in the stack with layer addresses 3 and 4, the layer with address 3 is referenced as Brg_1, and the layer with address 4 is referenced as Brg_2.
HBM has adopted the convention of assembling the stack so that the hardware ID suffix increases as the layer is positioned further away from the ECPU. In the example above, the EBRG addressed at 3 with hardware ID of Brg_1 is closest to the ECPU. It is strongly advised to follow this convention.

2.1.3 Updating Firmware

HBM regularly releases updates to the SoMat eDAQ firmware that expand functionality and fix known bugs. To download compatible firmware and software, visit www.hbm.com/somat.

NOTE
The eDAQ firmware uses an alpha-numeric version number (e.g., 3.11.A) while TCE uses a numeric version number (e.g., 3.11.0). For compatibility, the first two numbers of the eDAQ and TCE version numbers must be identical (e.g., 3.11).

After running the installer on the support PC to copy the files to the SoMat directory, follow the steps below to upgrade the eDAQ firmware. Always update the ECPU firmware before updating any layer level firmware.

CAUTION
If updating from an earlier release version, do not attempt to perform the upgrade if the eDAQ is in need of time-critical testing. An upgrade failure of the eDAQ firmware can render the eDAQ inoperable until it is upgraded at the factory.

Updating ECPU Firmware
To update the ECPU (MPB) firmware:
1. Power cycle the eDAQ.

2. Open the eDAQ web interface to the Hardware tab and click on the Code column for the MPB. For more information on the eDAQ web interface, see “eDAQ Web Interface” on page 179.
3. Browse to the correct firmware file on the PC and click Update. Wait for the eDAQ to return to the ready state.
4. Refresh the web interface as it may change with the new firmware.

Troubleshooting the ECPU Firmware Upgrade

There are a few isolated reports of the web browser opening a window for an add-on layer when performing a firmware update for the ECPU.

If this problem occurs, do the following:

1. Copy the firmware file and rename it as “__e10-update.tar.gz.” Note that the first two characters in the new file name are underscores.
2. In the System tab of the web interface, select the option to transfer a file to the eDAQ.
3. Browse to the new file as the file to copy and enter “/” as the destination path on the eDAQ.
4. From the System tab, reset the eDAQ. The eDAQ reboots and updates the MPB firmware.

Updating Layer Level Firmware

To update layer level firmware:

1. Open the eDAQ web interface to the hardware table and click on the Code column for the desired layer. For more information on the eDAQ web interface, see “eDAQ Web Interface” on page 179.
2. Browse to the correct firmware file on the PC and click Update. Wait for the application verified message indicating a successful update.
3. If no other firmware updates are required, cycle the power on the eDAQ to complete the overall firmware update process.

NOTE

For more detailed procedures for each layer type and a listing of the current layer level firmware versions see the instructions for installing eDAQ firmware provided with the firmware installation.

2.2 Communications

2.2.1 Communications Methods

Ethernet Communications

Data transfer rates of up to 4 MB per second are possible using the 100BASE-T Ethernet connection for communications between the eDAQ and its support PC. A 100BASE-T compatible Ethernet card must be installed in the support PC.

Connect the eDAQ to its support PC directly using the provided crossover cable (1-E-Ethernet X/O-2) or through a network using the optional hub cable (1-E-Ethernet HUB-2). Using a network removes proximity restrictions on the eDAQ and support PC.

Serial Communications
The eDAQ supports an RS232 communications option. The default baud rate is 115200, configurable to lower baud rates to support serial bus modules. The serial port can also be configured as a data input port using hardware and transducer channel interfaces similar to vehicle bus inputs.

2.2.2 Changing the eDAQ IP Address and Host Name

In order to change the IP address or host name of the eDAQ, first establish communication between the eDAQ and the support PC. The following sections describe the appropriate steps to follow for each of the methods of communication.
Using an Ethernet connection:

1. Open a web browser on the support PC.
2. Enter the IP address of the eDAQ in the address field. The default IP address programmed into the eDAQ nonvolatile memory during production is noted on a tag attached to the eDAQ (typically 192.168.100.100).

NOTE
The support PC must be configured to be able to reach 192.168.100.100 from the Ethernet port on the PC. This typically requires reconfiguration of the network interface. Refer to your operating system documentation or see your network administrator for help.

3. Click the System tab to open the eDAQ system setup page.
4. Select Network Setup to open the eDAQ network setup page.
5. Make changes to the hostname, IP address, netmask, and gateway. Check with the network administrator for the appropriate settings for these fields. Use the dotted quad format (xxx.xxx.xxx.xxx) for IP address, netmask, and gateway.
6. Click Reconfigure Network to save the changes to the eDAQ.
7. Cycle the power on the eDAQ for changes to take effect. The support PC must be configured to allow continued eDAQ communications as noted in step 2 above.

For more information on the eDAQ web interface, see “eDAQ Web Interface” on page 179.
Using a serial connection:

1. Power down the eDAQ and connect the serial communications cable to a PC COM port.
2. Open the HyperTerminal application in Windows® and follow the setup, entering a name for the connection and selecting the COM port. In the Connect To property page, use the Configure button to set up the communications protocols to a 115200 baud rate, 8 data bits, 1 stop bit, no parity and no flow control. In the Settings property page, select the Auto Detect emulation mode.
3. Cycle the power on the eDAQ.
4. After some initial boot log messages, a string starting with AT is displayed. Press ENTER four times to activate the login prompt. Login as `setup` with no password.
5. The eDAQ presents four network parameters available for modification: host name, IP address, subnet mask and gateway. Each has a separate prompt with the current/default value appearing in brackets after the description. Enter the new value or press enter to accept the existing value for each of the four parameters.
6. After entering all the parameters, enter y to confirm the settings or n to cancel.

7. Reboot the eDAQ to complete the procedure and allow the modifications to take effect.

NOTE
For complete access to all system tasks, login as `root` with no password. The command line prompt character (#) is displayed. Issue Unix-based command lines to perform required tasks.

CAUTION
All system firmware files and user data files can be deleted or corrupted by misuse of commands at the root interface level. Only use the commands provided here or by customer service to solve or troubleshoot eDAQ problems.

2.3 Power Considerations

The eDAQ requires an adequate power supply for the duration of all test runs. Consult the following notes for important eDAQ power considerations.

CAUTION
If operating the equipment on a DC supply network, take additional precautions to discharge excess voltages.

2.3.1 Input Power Voltage

Maximum Input Power Voltage
The maximum input power voltage is 55 volts for the ECPU-PLUS processor. Exceeding the maximum input voltage for the eDAQ for more than a few milliseconds results in a blown user-replaceable fuse.
The ECPU-PLUS processor supports nominal 12-, 24- and 42-volt vehicle battery systems.

NOTE
The eDAQ fuses are 10-amp, 42-volt rated automotive mini-blade fuses. For the eDAQ, spare fuses are stored in a compartment under the bottom panel fuse access plate (new units are shipped with six spares in this compartment).

Minimum Input Voltage
The eDAQ requires a minimum of ten volts for boot up and a minimum of nine volts for continuous operation once booted. After boot up, the eDAQ continues to operate for a limited time at an input voltage down to six volts.

When the input power voltage drops below nine volts, which occurs during normal vehicle engine cranking, the eDAQ switches in the internal backup battery as the power source. Power continues to source from the internal battery until the input voltage returns to ten volts or more. If the input voltage drops below six volts or the eDAQ detects that the internal battery has limited remaining life, the eDAQ performs an orderly power shut down. When input power voltage is restored to ten volts or more, the eDAQ reboots and continues operation. A fully charged internal backup battery contains enough reserve capacity to power an eDAQ stack drawing 50 watts in this mode of operation for more than one minute.

NOTE
The above voltages are at the eDAQ power connector, which are always less than the voltages at the power source because of some voltage drop in the wires used to route the power supply voltage to and through the eDAQ power connector. These voltage losses are dependent on the length and gauge of the connection wiring assembly.

Power Fail Shutdown
When a power fail shutdown initiates with a test run in progress, the eDAQ immediately stops the test run and flushes all data in temporary buffers to the PC Card. This can take several seconds. It is imperative that the backup battery is sufficiently charged to keep the eDAQ running during this time. If this is not the case, data stored in the SIF format becomes corrupted.

2.3.2 Battery Power

A fully charged eDAQ backup battery has at least 100 watt-minutes of reserve power. It takes about four hours to fully recharge a completely discharged backup battery. The battery charging circuit draws four watts maximum while charging. The backup battery charger operates on an as needed basis. An intelligent charge controller monitors current into and out of the backup battery, tracking the current charge state of the battery. When the battery has discharged to about 92% of rated capacity and the eDAQ is connected to a power supply at more than ten volts, the charger turns on and runs until fully charged, normally a process of about 20 to 30 minutes.
An eDAQ that is turned off and connected to a power supply such as a vehicle battery, runs one of these 20-minute charge cycles about once every two days, or an average power drain of about 30 milliwatts (i.e., 2.5 milliamps at 12 volts).
When a battery is changed or disconnected and reconnected, the eDAQ detects the new connection and assumes the battery to be discharged. The eDAQ initiates the charge cycle upon connection to a power supply and runs until it detects a full charge.

NOTE
The eDAQ web browser interface provides a status indicator that shows the level of battery charge as either low, medium or high and indicates whether the recharging circuit is currently on or off.

2.3.3 Remote Power

The remote power switch cable from the eDAQ power connector acts as a three-way switch in conjunction with the front panel power push button. Use the remote power cable with a single pole, single throw contact switch. The two physical switches, the front panel switch and the user-installed remote power switch, act to invert the switching logic of the other. Choose to power the eDAQ with either an open or closed remote power switch by simply toggling the front panel switch.
If not using remote power, ensure that the red and black wires are either fully insulated from each other or solidly connected to each other to prevent accidentally turning the power off. If the wires are connected to each other and there is any chance of magnetic induction, do not coil the cable in a loop.

NOTE
Do not apply any voltage source to the auxiliary power switch cable. It is designed for use with a single pole, single throw contact switch only.

Application Note: Using Remote Power to Start a New Test
The remote power switch can be used to force a reboot with a test running, effectively starting a new test run. The remote power switch accomplishes this in a way that does not drain the backup battery since the main power supply is still on during the duration of the power down operations. It is recommended to avoid other methods that turn off or disconnect the power supply as this drains the backup battery and can result in SIF data corruption.

2.3.4 Powering an eDAQ from a Vehicle

The following sections illustrate the recommended power connections for using a vehicle electrical system as the eDAQ power source. The included diagrams are not intended to be complete, detailed instructions. Please read the entire section on eDAQ power supply and backup battery considerations for a better understanding on the limits and implementation of both main and remote power to an eDAQ unit.

CAUTION
Connection to the positive power terminal without proper grounding may result in a blown fuse and/or other damage to the eDAQ.

NOTE
When using additional cable length to make the connections, select an appropriate gauge wire to carry sufficient current (≥ 10 amps) and voltage (≥ 12 volts).

Non-Switching Battery Ground

The following diagram illustrates the proper method of powering an eDAQ with a direct connection to a vehicle battery that has a permanent ground connection to the vehicle chassis.

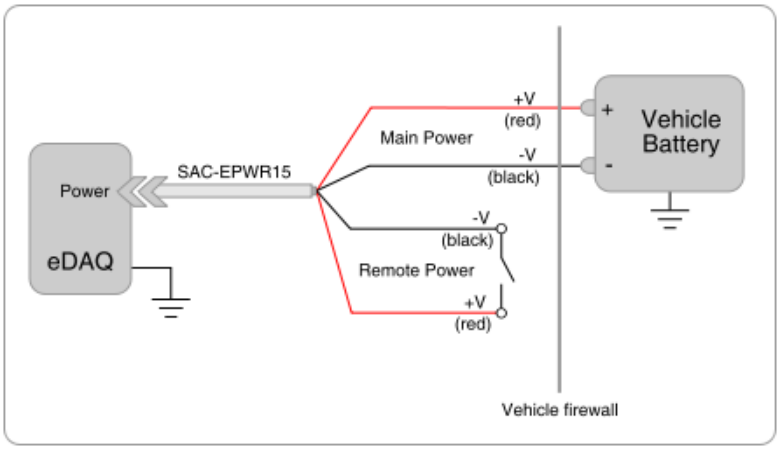


Figure 2-2: Vehicle battery connection for non-switching battery to ground.

An alternate method, shown below, uses a vehicle electrical system or harness which may be a switching supply such as an ignition or a relay-type device. This method, while feasible, is not recommended and cannot be guaranteed as safe. Results may include unwanted multiple runs of data, improper reboots, lost data due to multiple power cycles and improper charging of the internal battery pack.

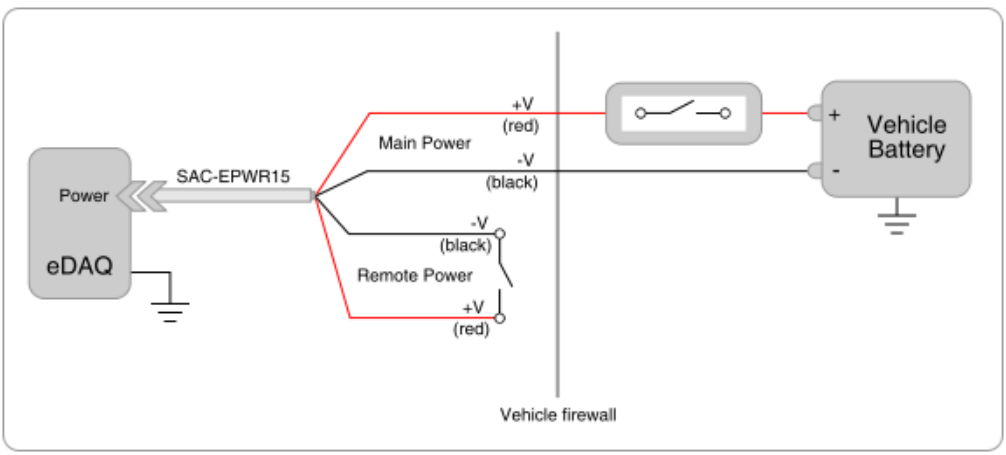


Figure 2-3: Alternate vehicle battery connection for non-switching battery to ground.

Negative Battery Terminal Switching

For a system with a switched power system that removes the negative battery terminal from the equipment chassis ground, carefully follow the illustrated recommendation below.

CAUTION

Failure to follow these suggestions may result in blown fuses and/or permanent damage to the eDAQ. Improper powering of the unit requiring repairs by HBM technicians may be deemed as non-warranty usage, resulting in service charges.

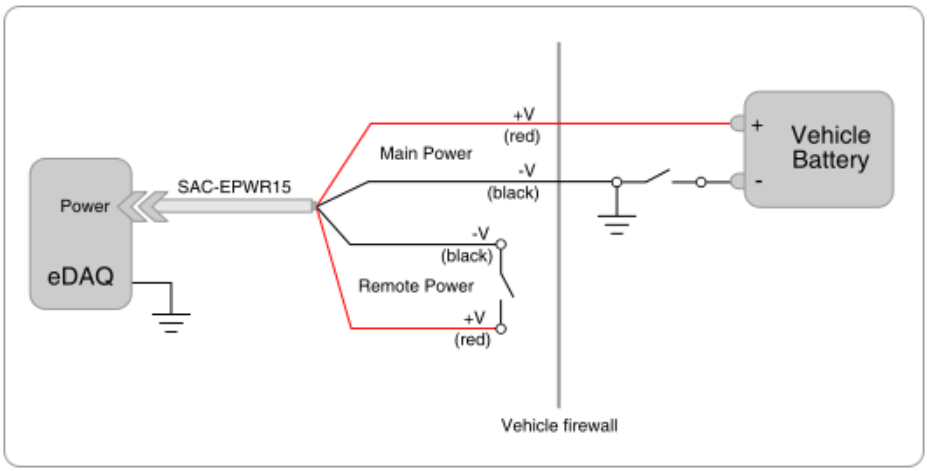


Figure 2-4: Vehicle battery connection for switching battery to ground.

The figure below shows an example of improper powering that may result in a short and damage the eDAQ.

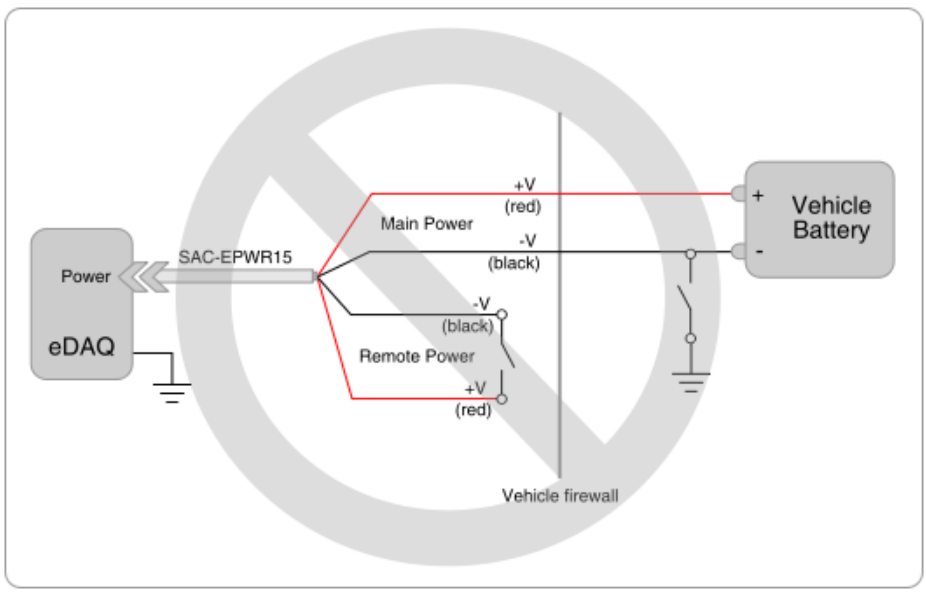


Figure 2-5: Improper vehicle battery connection for switching battery to ground.

2.4 Data Storage

2.4.1 Data Formats

The eDAQ offers two formats for storing recorded data: SIE and SIF. Select which data format to use in the TCE network setup window. A summary of the differences between the SIE and SIF data formats follow.

SIE	SIF
Unlimited file size	Files limited to slightly less than 4 GB
eDAQ can store multiple data files	eDAQ can only store one data file
Data is readable during testing	Data is readable only after test completion
No support for RAM disk data storage	RAM disk data storage available
No support for max bursts mode for the Burst History DataMode	Max bursts mode available for the Burst History DataMode
No support for accumulating histogram data across test runs	Support for accumulating histogram data across test runs

For more information on using SIE and SIF in TCE, see “Default data option” on page 54.

NOTE

For all storage media options, the eDAQ stores raw SIF test data and related information in a set of individual component files referred to as SIC files using a fixed naming convention (i.e., sif00000.sic, sif00001.sic, sif00002.sic, etc.). To view these files, use the explore eDAQ files option in the web interface to navigate to the hd/eDAQ directory. This is not recommended except under the advise of HBM support.

2.4.2 Data Storage Options

The ECPU contains several options for data storage including the RAM disk, an internal CompactFlash card and DRAM memory. In addition, the eDAQ includes an external PC Card slot.

NOTE

The external PC Card, internal CompactFlash and DRAM memory options are referred to collectively as PC Card storage. For information on selecting the actual media using the eDAQ web interface, see “Select Storage Device” on page 183.

RAM Disk

The RAM disk storage option has quite limited use in most test applications. The default 3.5-MB size is usually much too small for sequential data storage or histogram data storage of many test runs.

The RAM Disk memory is a section of the volatile DRAM memory. This section of DRAM memory is copied to the internal CompactFlash card on power downs or error resets and then copied back to DRAM on boot up.

NOTE
The SIE format does not support data collection to the RAM Disk. Regardless of the data storage setting, SIE data is saved to the storage device selected in the web interface. If the PC Card storage device is selected and there is no PC Card in the eDAQ, tests collecting SIE data cannot be initialized.

DRAM Memory
The amount of DRAM memory available for data storage is dependent on the size of the socketed DRAM. The DRAM storage media option is applicable for limited testing scenarios only. While it provides the maximum throughput compared to all other storage modes, the DRAM memory is volatile. This means that the test data is lost if the eDAQ powers down or resets for any reason, such as a power failure or error reset. In these cases when the eDAQ sets the PCMAccessError flag and begins re-initialization, use the Format RAM Disk menu option to restore normal operation.

CAUTION
DRAM memory is volatile. All test data is lost if the eDAQ powers down or resets for any reason.

Internal CompactFlash
The eDAQ can use a disk partition on the internal CompactFlash for data storage. The size of the internal Flash partition available for data storage is dependent on the size of the internal Flash card. Note that about 32 MB of the internal Flash memory is reserved for the eDAQ Linux OS.
The internal Flash storage media option provides up to five times better data throughput than the external PC Card storage media option assuming the Flash card uses DMA (as is the case for the HBM supplied cards). As such, this is the preferred storage media for test applications when uploading the data from the support PC.

External PC Card
The eDAQ has an external PC Card slot compatible with original PCMCIA cards and CompactFlash cards used with a PC Card extender. To open the door covering the PC Card slot, loosen the screws holding the door closed. When done working with the PC Card slot (e.g., swapping out a card), be sure to close the door and fasten the screws tightly to prevent dust and moisture from entering.

NOTE
Some ECPU layers include dual PC Card slots. The eDAQ can only use one of the two PC Card slots at any one time.

2.4.3 External PC Card

Usable PC Card Types
The eDAQ PC Card slot accommodates Type II and III cards in a variety of densities with hard drive or flash-based memory.

NOTE
If the eDAQ will be used where it will be subject to vibration and movement, use a flash-based memory PC Card instead of a disk drive card.

While many types of PC Cards work with the eDAQ, some do not work at all. Furthermore, different brands and models of PC cards can have significantly different data throughput characteristics. For reasons beyond the scope of this manual, older PC Cards often perform better than newer PC Cards from the same manufacturer. It is recommended to use the same types of PC Cards that HBM provides for current production shipments. After thorough testing, HBM selects cards that optimize data throughput.

Format Options
Use the eDAQ web interface or TCE to format the PC Card. In the Hardware tab, click the storage link in the MPB row for details on the PC Card media. Then select the Initialize/Format link to begin formatting.
If using a hard drive card, select either a Windows compatible MSDOS format or a Linux format. The Linux format provides somewhat higher data throughput performance and is recommended when uploading the data file from the eDAQ to the PC. The MSDOS format is required to read the data from a Windows PC after removing the card from the eDAQ.

NOTE
It is generally recommended to format the PC Cards using the eDAQ. However, formatting the cards using the support PC in either the FAT or the FAT32 format options is also acceptable.

PC Card Removal
After a test run is stopped, remove the external PC Card from the eDAQ only after it has been logically unmounted. To unmount, power down the eDAQ, wait for all LEDs to turn off and then manually eject the PC Card.

CAUTION
Ejecting the external PC Card without going through the above procedure can often corrupt the test data.

Once ejected, do not reinsert the card into the eDAQ for data upload. Instead, insert the card directly into a Windows or Linux PC Card slot. For SIE files, simply copy the file to the PC. For SIF files, transfer the SIC files to the PC and then use TCE to consolidate the SIC files into a standard SIF file.

Swapping PC Cards with a Test Initialized
The eDAQ supports the capability to swap in a new PC Card and re-initialize a test that was previously initialized, effectively storing a test run across multiple PC Cards. There is no limit to the number of swapped cards. The data file on each card is a complete file, allowing analysis independent of any other data files. When swapping cards, the eDAQ maintains contiguous test run number sequencing, prerun rezeroing offsets for applicable transducer channels, interactive trigger states and remote test run control states.

NOTE
This option is not available for a set of eDAQs.

To swap PC Cards with a test initialized, carefully follow this procedure.
1. With a test initialized and a test run either in progress or stopped, power down the eDAQ and wait for the power sequence to complete.
2. Insert the new, previously formatted PC Card. The new PC Card must be purged of all SIF data component files.
3. Power on the eDAQ. The existing test is re-initialized and the next test run starts automatically unless using the remote control mode.

NOTE
If a PC Card is swapped in without purging the SIF component files, the eDAQ does not attempt to re-initialize the test run. Instead, it sets the PCMAccessError flag, turns on the red LED and effectively goes into an idle state. In this situation, power down the eDAQ, insert a purged PC Card or the original PC Card and power on the eDAQ. Test re-initialization then proceeds normally.

2.5 Networking eDAQ Systems

Networking allows multiple eDAQ units to acquire data synchronously using a single master sample rate (MSR) clock source. The networked system can consist of any combination of eDAQ and eDAQ-lite systems. For more information on data synchronization in a network of systems, see “Networked eDAQ System Synchronization” on page 232.

2.5.1 Hardwired Network

This section describes how to set up the eDAQ hardware for networking. For information on using TCE to manage an eDAQ network, see “Networking eDAQ Systems” on page 90.

Required Hardware

For (*n*) eDAQ systems, the following hardware is required and assumes Ethernet communications mode. A hardwired network consists of one master eDAQ and (*n*-1) slave units.

- (*n*) Networking Adapter Cables (1-SAC-ESYNCADAPT-2)
- (*n*-1) Networking Sync Cables (1-SAC-ESYNC-2)
- (2) Networking Termination Connectors (1-SAC-ESYNCTERM-2)
- 1 - 100BASE-T Ethernet hub with *n*+1 ports

Hardware Connections

Referring to the diagram below, the SoMat SAC-ESYNCADAPT Networking Adapter Cable (1-SAC-ESYNCADAPT-2) is a communications cable that includes two cable stubs with LEMO connectors which provide a tee connection to the data synchronization clock. The master eDAQ supplies the clock and distributes it to each slave through the SoMat SAC-ESYNC Networking Sync Cables (1-SAC-ESYNC-2). For the each of the end units, connect one side of this tee to a SoMat SAC-ESYNCTERM Networking Termination Connector (1-SAC-ESYNCTERM-2).

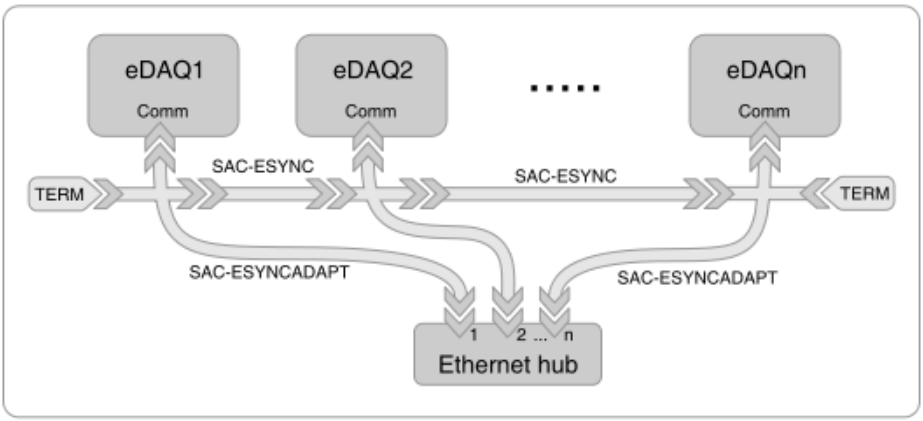


Figure 2-6: Cable connections for networking multiple eDAQs.

2.5.2 Wireless Network

With a GPS module in either an EDIO or ECOM layer, it is possible to configure the eDAQ to generate the MSR clock synchronized with the GPS timing signal. This mode of operation allows multiple eDAQ systems to wirelessly synchronize data. Use this option only when the GPS module can maintain consistent GPS lock.

To set up GPS MSR clock generation, select the network mode as GPS Stand Alone (see “Adding a Network Node” on page 63), configure the EDIO or ECOM hardware to enable GPS clock generation (see “Configuration Options” on page 97) and define at least one GPS channel in the test setup (see “Bus-Oriented Input Channels” on page 129).
The test run start time is required to align the data acquired from different eDAQ units. The eDAQ logs the start time in terms of GPS time in the data file under the global keyword `DF_GPSStartRunTime_#`, where # is the run number. The format for the date and time follows the ISO 9161 standard in the format YYYY-MM-DDThh:mm:ss.ssss±hhmm.

NOTE
Because the eDAQ writes the start time based on UTC (Universal Time Coordinates), the final ±hhmm of the start time, which is the signed offset from UTC, is always +0000.

NOTE
Use the GPS Master network mode for the ECOM layer to generate the GPS clock for itself and one or more hardwired slave eDAQ systems. Connect the slave eDAQs as described for normal hardwired networking.

3 Test Control Environment (TCE)

The SoMat Test Control Environment (TCE) software, provided with the eDAQ, is an interface between the eDAQ and the support PC. Use TCE to:

- Create test setup files that define transducer channels, computed channels and DataModes™ for online data analysis
- Perform and manage calibrations for input transducers
- Initialize, run and end tests on a single eDAQ or a network of eDAQs
- View real time test data with integrated run-time displays
- Monitor eDAQ memory status during data acquisition
- Transfer test data from the eDAQ to the support PC for analysis
- Configure the option to remotely control test runs

This chapter describes the TCE user interface and preferences. For details on using TCE to perform the listed tasks and more, see “Using TCE” on page 63.

3.1 TCE User Interface

The following sections describe the TCE user interface including the setup windows, pull-down menus, toolbar and status bar.

3.1.1 Setup Windows

Create and modify TCE files using the five setup windows. Access any of the button options in the windows using the mouse or the keyboard entry indicated by the underlined character. For example, select the Add button by either clicking on it or pressing A on the keyboard. Select multiple entries using the standard CTRL and SHIFT keystrokes.

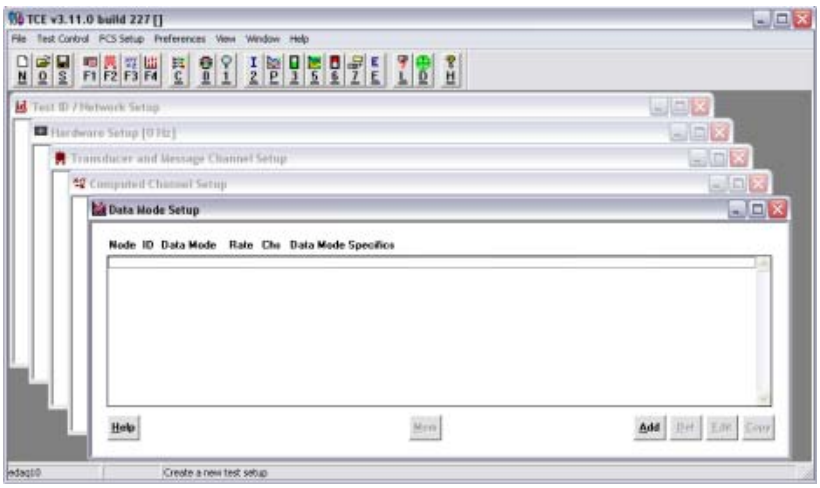


Figure 3-1: TCE setup windows for a new test setup file.

Test ID/Network Setup

The upper test identification section of the window shows the descriptive name of the test, the name of the operator, the test date and any notes or comments regarding the test or special instructions. The lower network setup portion of the window contains the eDAQ or the list of eDAQs for the test setup and their network node parameters.

Option	Description
Edit ID	Modify the test identification information shown in the upper window.
Import	Import a network node definition from an existing TCE setup file. TCE also imports all hardware modules, transducer and computed channels and DataModes associated with the network node.
Add	Add a network node to the existing TCE setup file. Specify an IP address or host name and communication parameters.
Del	Delete an existing network node from the TCE setup file. TCE also deletes all hardware modules, transducer and computed channels and DataModes associated with the network node.
Edit	Modify an existing network node definition.
Data Option	Select the desired data file format. For more information on data format options, see Default data option.
Manage SIE Files	Launch the eDAQ web interface to manage the SIE data files on the eDAQ. For more information on managing SIE files, see “SIE Test Data” on page 184.

For more information on setting up a network node, see “Adding a Network Node” on page 63.

Hardware Setup

The hardware setup window lists the hardware layers installed on the systems specified in the network setup. Each layer entry includes the front panel connector ID names, the layer serial number, the firmware (code) version number, an indication of applicable ECNs and select configuration details. Use the Query button to populate the list.

Option	Description
Query	Load the hardware setup from the systems specified as network nodes. TCE issues a prompt if the queried hardware configuration differs from the current setup.
Config	Display and/or edit the configuration details for the selected hardware layer. Configuration options are not available for all layers.

For more information on using TCE to configure hardware, see “Configuring the Hardware” on page 64. For more information on the configuration options for specific hardware, see “eDAQ Hardware” on page 93.

Transducer Channel Setup

Use the transducer channel window to define and modify the transducer configuration required for the test. This includes defining transducer identification information, user-programmable settings and calibration methods and parameters. Each transducer entry includes the transducer ID name, the connector, the transducer sample rate, the calibration date, the output data type and select configuration details.

Option	Description
Add	Add a new transducer definition to the setup. TCE adds the new transducer above the selected entry.
Del	Delete the selected transducer channels.
Edit	Modify the selected transducer channel definitions. Edit a single transducer definition or a group of transducers of the same channel type.
Copy	Copy the selected transducer definition into one or more new transducer definitions. TCE adds the new transducers below the selected entry.
Sort	Sort the transducer channels list alphabetically by connector ID.
DVM	Run a DVM display for the selected transducer channels. This option is not available when a test is initialized. For more information on the DVM display, see “DVM” on page 80.
Scope	Run the scope display for the selected transducer channel. The scope display is limited to a single channel. This option is not available when a test is initialized. For more information on the scope display, see “Scope Plot” on page 81.
Freq	Run the spectrum analyzer display for the selected transducer channel. The spectrum display is limited to a single channel. This option is not available when a test is initialized. For more information on the spectrum display, see “Spectrum Plot” on page 82.
Cal	Perform various calibration tasks on the selected transducer channels. This option is not available when a test is initialized. For more information on calibrating channels, see “Calibrating Input Channels” on page 67.
Ampl	Report the selected signal conditioner amplifier settings. This option is provided primarily for HBM development.
SMART Utils	Open the SMART module utilities window. This option is applicable for a SMART module transducer channel. For more information on SMART utilities, see “Using SMART Utilities” on page 125.

For more information on setting up an input channel, see “Creating Channels and DataModes™” on page 65. For information on specific input channel types, see “Input Channels” on page 111.

Computed Channel Setup

Use the computed channel window to define any computed channels required for the test. A computed channel is derived from one or more transducer or previously defined computed channels. Defining computed channels in a test setup is optional.

NOTE

A computed channel referencing a previously defined computed channel must be listed below the referenced channel in the setup window.

Option	Description
Add	Add a new computed channel definition to the setup. TCE adds the new computed channel above the selected entry.
Del	Delete the selected computed channels.
Edit	Modify the selected computed channel definition.
Copy	Copy the selected computed channel definition into a new computed channel. TCE adds the new channel below the selected entry.

For more information on setting up a computed channel, see “Creating Channels and DataModes™” on page 65. For information on specific computed channel types, see “Computed Channels” on page 135.

DataMode Setup

Use the DataMode window to define the DataMode configuration required for the test. A DataMode definition consists of a list of input channels, a data sampling rate, triggering mode and conditions and other DataMode specific parameters.

Option	Description
Add	Add a new DataMode definition to the setup. TCE adds the new DataMode above the selected entry.
Del	Delete the selected DataModes definitions.
Edit	Modify the selected DataMode definition.
Copy	Copy the selected DataMode definition into a new DataMode definition. TCE adds the new channel below the selected entry.
Mem	Display the SIF data raw memory allocated for the selected DataMode definition.

For more information on setting up a DataMode, see “Creating Channels and DataModes™” on page 65. For information on specific DataMode types, see “DataModes™” on page 165.

3.1.2 Pull Down Menus

The following table describes the menu options available in TCE. Where applicable, the last column provides a section number in this document for more information on the menu command.

NOTE

To perform any tasks in the FCS Setup menu, the PC must be connected to the eDAQ specified in the TCE communications preferences.

Menu	Menu Option	Description	Section
File	New Setup [CTRL+N]	Create a new setup file.	4.1
	Open Setup [CTRL+O]	Open an existing setup file.	4.1.4
	Save Setup [CTRL+S]	Save the currently open setup file.	
	Save Setup As	Save the current setup file with a new name and/or location.	
	Save Setup Listing	Generate a readable listing file containing current setup information.	
	Save Setup Tab Delimited	Generate a tab-delimited text file of current hardware setup. Provided primarily for HBM internal use.	
	Open SIE or SIF File	Extract keyword and message channel data from an existing SIE or SIF file.	4.6.3
	Consolidate SIC Files	Generate a complete SIF file from a set of SIF component files (SIC files).	
	Call Infield/EASE/DataXplorer [CTRL+D]	Start InField, EASE or DataXplorer for displaying and/or analyzing test data.	
	Exit	Quit TCE.	
	Recent Files	View a list of the five most recently opened TCE files.	

Menu	Menu Option	Description	Section
Test Control	Control Panel [CTRL+0]	Open the TCE control panel.	4.3
	Get Test Status [CTRL+1]	Check the current test status of the eDAQ.	4.4
	Initialize Test [CTRL+2]	Initialize the eDAQ in preparation for the test run.	4.3.1
	Remote Control [CTRL+R]	Suspend or resume remote control operation.	4.7
	Preview Run	Start a test run with all DataModes storage suppressed.	4.3.3
	Start Run [CTRL+3]	Start a test run.	4.3.4
	Prerun Options...	Access a variety of tasks after initialization.	4.3.2
	Transducer Checks	Perform a variety of checks on transducer channels.	
	Rezero Display [CTRL+Z]	Display and re-zero transducer channels for an initialized test.	
	Reference Shunt Checks	Check the repeatability of shunt calibrations.	
	Install Shunts	Install shunt calibration resistors during a test run.	
	Interactive Triggering [CTRL+4]	Open a dialog to control the values of the eight available interactive triggers.	4.3.5
	Run Time Display [CTRL+5]	Open the run-time display window.	4.5
	Stop Run [CTRL+6]	Stop a test run.	4.3.6
	End Test [CTRL+E]	End the current test run.	4.3.7
	Auto Range Options	Configure the option to automatically use the minimum and maximum values recorded in the last test run as the full-scale values in future test runs.	3.2.8
	Upload Test Data [CTRL+7]	Transfer all or selected test runs stored in the eDAQ to a user-specified PC disk file.	4.6
	Upload SIE Only	Transfer SIE data files stored in the eDAQ to a user-specified PC disk file.	4.6.1
	Upload SIF Only	Transfer the SIF data file stored in the eDAQ to a user-specified PC disk file.	4.6.2
	Upload Test Setup	Transfer the test setup file stored in the eDAQ to a user-specified PC disk file. This option is not available when a test is running.	
	Save AOM File	Generate a file that contains the calibration parameters required to relate analog outputs to equivalent engineering units values.	4.2.4

Menu	Menu Option	Description	Section
FCS Setup	Set Master Sample Rate	Specify the master sample rate (MSR) as either 100000 Hz, the standard MSR for the eDAQ, or 98304 Hz, provided to support power of two sample rates. Data sample and data storage rates must be integer divisors of the MSR. The eDAQ stores the MSR in nonvolatile memory for access only after an eDAQ reset. Therefore, TCE initiates a programmed reset of the eDAQ unit when the parameter changes.	
	Set Reset Options	Control options for initiating system resets. The only applicable option is the no new run on FCS error reset option which prevents the eDAQ from attempting to start a new test run when a serious error forces a reset. For normal operation, do not select this option so that the eDAQ can attempt to salvage as much of the test run as possible. This option is not available when the test is initialized.	
	Set Clock	Set the real time clock on the eDAQ unit based on the current date and time setting on the host PC.	
	Reset	Perform a programmed reset of the eDAQ unit. Use this option only if absolutely necessary, such as when the system is not responding.	
	Delete RAM Disk Files	Delete all resident test and data files from the RAM disk. Only use this option if there is no test initialized on the eDAQ and all test data has been safely uploaded from the eDAQ.	
	Format RAM Disk	Format the RAM disk on the eDAQ unit and erase all files, including some test data files, from the RAM disk. This option is available at all times even while a test is running. Because the eDAQ formats the RAM disk in the normal process of test initialization, formatting the RAM disk is not typically necessary.	10.1
	Diagnostics	Access commands for troubleshooting purposes.	10.1
	Test FTP	Perform a diagnostic test on the eDAQ file transfer process (FTP) functionality. This option is not available when a test is initialized.	
	Check RAM Disk	Check the integrity of the eDAQ RAM disk.	
	Upload Log	Save the eDAQ log, which contains messages, warnings and errors from TCE and the eDAQ, to a PC disk file.	
Preferences	Communication Preferences	Configure the Ethernet communications with the eDAQ.	3.2.1
	General Preferences	Configure TCE application preferences.	3.2.2
	FCS Specific Preferences	Configure TCE preferences specific to the target eDAQ.	3.2.3
	Remote Test Run Control	Configure the preferences for using remote control.	3.2.4
	Scope and Spectrum	Configure the settings for scope and spectrum displays.	3.2.5
	Run Time Display	Configure the settings for run-time displays.	3.2.6
	Group DVM Display	Configure the settings for group DVM displays.	3.2.7

Menu	Menu Option	Description	Section
View	Toolbar	Show/hide the TCE toolbar.	3.1.3
	Status Bar	Show/hide the TCE status bar.	3.1.4
	Test ID/Network Setup	Show/hide the test ID/network setup window.	3.1.1
	Hardware Setup	Show/hide the hardware setup window.	3.1.1
	Transducer Channels Setup	Show/hide the transducer channels setup window.	3.1.1
	Computed Channels Setup	Show/hide the computed channels setup window.	3.1.1
	DataMode Setup	Show/hide the DataMode setup window.	3.1.1
Window	Cascade	Cascade all open windows.	
	Tile	Tile all open windows.	
	Arrange Icons	Arrange all minimized windows at the bottom of TCE.	
	Close All	Close all windows.	
	Next Window	Activate next window.	
	Previous Window	Activate previous window.	
	Toggle Maximized	Maximize or restore active window.	

3.1.3 Toolbar

The TCE toolbar provides quick access to commonly used TCE functions. Each button also provides a guide to commonly used keyboard shortcuts.

Button	Command	Button	Command
	New setup. [CTRL+N]		Initialize test. [CTRL+I]
	Open setup. [CTRL+O]		Start preview run. [CTRL+P]
	Save setup. [CTRL+S]		Start test run. [CTRL+3]
	Open hardware setup window. [F1]		View run-time data. [CTRL+5]
	Open transducer channel setup window. [F2]		Stop test run. [CTRL+6]
	Open computed channel setup window. [F4]		Upload test data. [CTRL+7]
	Open DataMode setup window. [F3]		End test. [CTRL+E]

Button	Command	Button	Command
	Open control panel. [CTRL+0]		Get eDAQ log. [CTRL+L]
	Get test status. [CTRL+1]		Call Infield/EASE/DataXplorer. [CTRL+D]
	Open help. [CTRL+H]		

3.1.4 Status Bar

The status bar is at the bottom of the TCE window and displays information about the test setup status. The status bar is divided into three sections.

Communications Mode

The communications mode displays the IP address or host name of the active eDAQ. When TCE is actively communication with the eDAQ, the background color of the entire status bar changes. When communicating with the eDAQ specified in the TCE communications settings, the status bar turns red. When communicating with other eDAQs for network control or monitoring purposes, the status bar turns either blue, green, yellow or orange based on the assigned index to the network node.

Test Modified

The test modified section indicates, by displaying the word “Modified,” that the current test setup has been modified from its last saved state.

General Information

The general information indicator provides TCE status information with a brief description of the current action or the action just completed.

3.2 TCE Preferences

The TCE Preferences menu provides a variety of options to modify some aspects of TCE including dialog window displays, remote test run control configuration and TCE warning messages. TCE saves the preference settings in a file named “TceMS.ini” in the working subdirectory of the installation folder.

3.2.1 Communications

Connect Timeout Period

Specify the desired timeout period in seconds for initiating communications with the eDAQ. The default value of five seconds should work well for dedicated ethernet communications with an eDAQ that is not on a network hub. Longer timeouts may be required for communications with an eDAQ on a busy or slow network hub or on a wireless ethernet connection.

NOTE

The communications I/O timeout, used for all PC to eDAQ communications, equals the connect timeout period for periods greater than ten seconds. Otherwise, TCE sets the I/O timeout period to the minimum timeout period of ten seconds.

Socket Buffer Size
Specify the buffer size used for PC to eDAQ communications. In general, leave the default value of 61440 bytes for optimum communications data throughput. For situations where timeouts on communications occur, increasing the timeout period is recommended over decreasing the socket buffer size.

IP Address or Host Name
Specify the IP address or host name of the desired eDAQ.

3.2.2 General

Descriptions (not IDs) for data file (plot) labels
Store the TCE channel description fields in the data file for use as labels on plot windows. When selected, empty or duplicate channel descriptions prompt warnings from TCE. Modifying this option is not available after test initialization.

NOTE
Although TCE description fields allow 63 characters, data file labels are limited to 31 characters. Because the Rainflow and Peak/Valley Matrix DataModes add prefixes to the labels, it is recommended to limit the description field to 24 characters when using these DataModes.

Require user to verify test control selections
Force TCE to issue a verification prompt after every Test Control menu command.

Chain auto range options to stop test run
Require TCE to open the auto range options dialog after each test run stops. For more information on auto range options, see “Auto Range Options” on page 60.

Chain SIF frame demultiplex to upload/consolidate (SIF Only)
Force TCE to demultiplex all multiplexed SIF file data records after successful upload or SIC consolidation. This option significantly improves data analysis performance by products such as InField. Note that TCE does not perform the demultiplexing if there are any abnormalities in the upload or consolidation.

Prompt user for run descriptions on test run starts
Force TCE to issue a prompt for a test run description at the start of every test run. As this option is the only method of entering test run descriptions, deselecting it ensures blank test run description fields.

Require user to verify PC card purge during test initializations
Force TCE to issue a verification prompt in order to purge the PC Card during test initialization. If not selected, TCE purges the PC Card automatically.

NOTE
If multiple SIE files exist on the eDAQ, TCE issues the verification prompt regardless of the preference setting.

Allow test initializations with channels that are not calibrated
Allow TCE test initializations with non-calibrated transducer channels. This option is not applicable to strain transducer channel types.

Auto set current communication preference on TCE setup file open
When opening a TCE setup file, automatically set the current communication preferences. If the existing preference matches any network node defined in the opened file, the preference remains unchanged. Otherwise, TCE sets the active eDAQ to the master network node or, if no master exists, the first defined network node.

Warn user if...

Warn user if...	Description
Ratio of Calibration Span to Full-Scale Span <	Issue a warning if the calibration span is less than the specified percent of the full-scale span for a transducer channel (or vice-versa).
Difference Between Host PC and FCS Clocks >	Issue a warning if the difference between the host PC real time clock and the eDAQ real time clock exceeds the specified number of minutes.
Deviation of Shunt Calibration Volts from Ideal >	Issue a warning if the measured shunt calibration span in volts deviates from the ideal shunt calibration by at least the specified percentage.

Warn user about unused channels
Select one of three options of when TCE should issue a warning about unused channels.

Option	Description
If channel is not used in a DataMode or computed channel	Issue a warning when any defined channel is not either used a computed channel or stored in a DataMode.
If channel is not used in a DataMode	Issue a warning when any defined channel is not stored in a DataMode.
Do not issue warnings	Never issue a warning.

Analog output file format options
Select one of three options of which file format to use when generating analog output calibration files.

Option	Description
Use original file format.	Generate a Windows INI compatible file.
Use tab-delimited file format.	Generate a tab-delimited file compatible with Excel.
Ask user for desired file format on each usage.	Prompt for a file format decision for each generated file.

For more information on analog output calibration files, see “AOM Calibration File” on page 72.

3.2.3 FCS Specific

Default pipe frame rate

Select the default pipe frame rate from the provided list. The first number of each entry is the rate for an MSR of 100000 Hz and the second number is the rate for an MSR of 98304 Hz. As data samples are collected from the transducer channels, the eDAQ places them in blocks of data (data frames) and routes (pipes) them into computed channels and DataModes. In the flow of data from the transducer inputs through the DataModes, the data frames are referred to as pipe frames.
The lowest pipe frame rate is considerably more efficient from a processing point of view when there are a large number of channels defined at lower sample rates (≤ 500 Hz). Using the lowest pipe frame rate also modestly improves throughput performance for most tests with sample rates below 10000 Hz. At sample rates above 10000 Hz, a higher pipe frame rate generally results in the best throughput performance. Because TCE run-time displays run at the pipe frame rate, higher pipe frame rates may be desired.

Default data option

Select the default option for how the eDAQ stores data. For more information on the SIE and SIF data formats, see “Data Formats” on page 36.

Option	Description
SIE (delete old SIE files on test init)	Collect data in the SIE file format and limit the number of SIE files on the eDAQ to one, emulating the behavior of SIF files.
SIE	Collect data in the SIE file format and allow multiple SIE files on the eDAQ at the same time.
SIF	Collect data in the SIF file format. Only one SIF file is allowed on the eDAQ at one time.
SIE and SIF (diagnostic, delete SIE)	Collect data in both the SIE and SIF file formats and limit the number of SIE files on the eDAQ to one. This option consumes eDAQ storage twice as fast and places significantly increased demand on the eDAQ processor.
SIE and SIF (diagnostic)	Collect data in both the SIE and SIF file formats. This option consumes eDAQ storage twice as fast and places significantly increased demand on the eDAQ processor.

NOTE

The diagnostic data options are provided primarily for HBM internal usage.

Check actual full scales
Force TCE to check the actual full-scale limits for all selected channels defined in the test. Choose to check ELLB, EHLS or EBRG channels. TCE performs the check immediately after test initialization and reports if the over range protection meets the conditions below. For more information on full-scale values, see "Full-Scale Values" on page 112.

Option	Description
Low Level	Warn if over range protection on ELLB channels is less than 5% or greater than 25%.
High Level SS	Warn if over range protection on EHLS channels is less than 1% or greater than 25%.
Bridge	Warn if over range protection on EBRG channels is less than 1% or greater than 25%.

Enable min-max tracking for Time History DataModes
Track min and max values for each input channel in a Time History DataMode. This option is not recommended for optimum throughput performance, but it is required to support TCE auto range functionality. For more information on auto range options, see "Auto Range Options" on page 60.

Use PC Card memory for remote RAM disk storage
Store the static part of the RAM disk file on the PC Card. This effectively limits the size of the RAM disk file and helps prevent a situation where the RAM disk memory fills up before the PC Card memory.

NOTE
When this option is selected, the ability to upload individual test runs is disabled.

Use default sample rate/filter for all low level calibrations
Select this option to use the default sample rate and digital filter combination of a low-pass, 8-pole Butterworth filter with a 15 Hz break frequency for all ELLB channel calibrations. If unselected, TCE uses the sample rate and digital filter currently defined in the channel definition.

Shunt calibration mode options
Select the desired mode for performing ELLB channel shunt calibrations. The smart range mode is the default and the recommended mode. Both the fixed range and auto range modes are older modes maintained from previous versions of TCE.

Mode	Description
Smart Range	This is the default mode. TCE makes a coarse voltage measurement to determine the approximate the bridge output with no shunt resistor installed (i.e., the bridge imbalance). This measurement is accurate to about ±0.1 millivolts. Based on this value and the computed ideal voltage offset for an installed shunt resistor, TCE sets up the low level channel signal conditioner with an over range of either 12.5% of the ideal range or 1 millivolt, whichever is greatest. Then TCE acquires both un-shunted and shunted voltages to provide a very high resolution and fast calibrations. This mode is very general in that it supports all bridge and shunt resistance and can handle large bridge imbalances up to ±100 millivolts.
Fixed Range	This mode provides the fastest shunt calibrations. TCE sets up the low level channel signal conditioner for a fixed range of ±40 millivolts. Then TCE acquires both un-shunted and shunted voltages. This modes supports most 120-, 350- and 1000-ohm bridges using shunt resistors that provide equivalent strains in the 1000- to 4000-microstrain range. However, it does not provide optimal resolution and cannot handle bridges with large imbalances.
Auto Range	This mode provides maximum resolution for both un-shunted and shunted voltage measurements, but is also the slowest mode. TCE makes a coarse voltage measurement to determine the approximate voltage with the shunt resistor installed. TCE sets up the low level channel signal conditioner with the offset D/A converter configured to compensate for this voltage and the gains set to the maximum. TCE then acquires a highest resolution precision voltage measurement to set the shunted voltage value. TCE repeats the process with the shunt resistor removed to set the un-shunted voltage value. This mode can handle very large bridge imbalances up to ±500 millivolts.

Following are some timing benchmarks for the three modes as a function of the sample rate and digital filter used. In all cases, the values are the time in seconds required to shunt calibrate 16 channels (i.e., all eight channels on two ELLBs). Note that the time required to shunt calibrate eight channels on one ELLB or 32 channels on four ELLBs is:

Sample Rate / Digital Filter	Smart Range	Fixed Range	Auto Range
100 Hz / Butterworth 15 Hz	30 seconds	23 seconds	41 seconds
100 Hz / Linear Phase 33 Hz	27 seconds	21 seconds	38 seconds
200 Hz / Linear Phase 67 Hz	21 seconds	16 seconds	28 seconds
500 Hz / Linear Phase 167 Hz	17 seconds	13 seconds	21 seconds
1000 Hz / Linear Phase 333 Hz	14 seconds	11 seconds	17 seconds
2500 Hz / Linear Phase 1000 Hz	12 seconds	10 seconds	17 seconds

3.2.4 Remote Test Run Control

The remote control setup preferences configure the eDAQ for remote control of test runs using digital input and output lines. The eDAQ uses the digital input and output lines on the ECPU for remote control operation. After selecting Remote Test Run

Control from the Preferences menu, choose the eDAQ-Plus option to modify the following preferences. For more information remote test control, see “Using Remote Control Operation” on page 90.

NOTE
Changing these preferences after a test is initialized does not affect the remote control operation for the test currently in progress.

Modify current test setup settings only
Change the remote control parameters in the current test setup only. When this option is disabled, all parameters are saved as TCE defaults. TCE applies the default settings to all new setup files and files without defined remote control parameters. Previously defined parameters retain their values taking precedence over the application defaults.

Control mode
Select the desired remote control mode.

Option	Description
Disable	Do not use remote control.
Enable	Use remote control for all subsequent tests.
Query	Choose whether to use remote control at each test initialization.

Input bit assignment
Select the desired run/stop control bit. If the line for this bit is high (logical 1), a test run starts; when the line goes low (logical 0), the test run stops.

NOTE
With the remote control mode in use, all digital input lines for the ECPU can function as normal digital inputs.

Optional output bit assignments
There are four status outputs available; all are optional.

Output	Description
Running	Indicates the test running state. Flashing indicates running, steady on indicates starting or stopping a run and steady off indicates no test run in progress.
Alarm	Indicates a serious error or user alarm. TCE always reports the specific error or warning condition on the next interaction with the eDAQ. Note that running out of either RAM or PC Card memory sets this alarm.
RAM Low %	Indicates when the available RAM disk memory falls below the user-specified limit.
PCM Low %	Indicates when the available PC Card memory falls below the user-specified limit.

NOTE
To support remotely powered LED indicators, the eDAQ switches output lines to ground for the on state and to open circuit for the off state.

NOTE
When using any of the optional output bits for eDAQ remote control operation, the digital outputs on the ECPU are not available.

3.2.5 Scope and Spectrum Display

The scope and spectrum display options allow changes in the color schemes and other presentation parameters for both run-time displays and the original displays used when a test is not running. For more information on scope and spectrum displays, see “Viewing Channel Displays” on page 78.

Trace color
Select the desired color for drawing signal trace vectors.

Screen color
Select either black or white as the background screen color.

Auto scale mode
Automatically scale the y-axis. As spectrum displays always use auto scale, this option is only applicable to scope displays.

Show grid lines
Activate visible grid lines on the plot.

Show prerun value
Start the display showing the prerun value when present. This option is only applicable to the scope displays.

3.2.6 Run-Time Display

Use the run-time display preferences to set a default run-time display type and configure display options for the bar and strip chart display. For more information on run-time displays, see “Viewing Channel Displays” on page 78.

Display mode
Select the preferred display mode to use as the default when opening a run-time display.

NOTE
To modify the display parameters for scope and spectrum plots, use the scope and spectrum display preferences. The digital readout display has no display options.

Trace/bar color
Select the desired color for drawing the signal traces or bars.

Screen color
Select either black or white as the background screen color.

Strip chart plot mode
Select the desired behavior when the signal trace reaches the right edge of the plot.

Option	Description
Normal	The signal trace begins again at the left side of the plot.
Scroll	The signal trace scrolls continuously to the left at the rate at which data is received and with the current value at the right edge.
Mixed	The right half of the signal trace moves to the left half of the plot and the signal trace continues from the middle of the plot.

Show strip chart grid lines
Activate visible grid lines on the strip chart plot.

3.2.7 Group DVM Display

Select one of three display modes for group DVM displays.

Option	Description
Original Static	Use static control fields and limit to a maximum of 16 channels.
Scroll List	Use a scrollable list control with sizable fields: channel ID, current value and units. Limit to a maximum of 256 channels.
Scroll List Extended	Use a scrollable list control with sizable fields: network, connector ID, channel ID, current value, saturation bounds and units. Limit to a maximum of 256 channels.

3.2.8 Auto Range Options

NOTE
Access the auto range options from the Test Control menu.

NOTE
Automatically chain this task to the stop run task using TCE General Preferences.

Use the auto range options to acquire the minimum and maximum values for all channels stored in Time History DataMode in the eDAQ resident SIE or SIF file. This includes all transducer channels and all computed channels that have the full-scale values defined. The information is displayed on a run-by-run basis. The initial dialog window presents the results from the last run. Select to display other runs as desired. The channels are sorted in the order of full-scale saturation percent (i.e., how close the channel is to either of the user-defined full-scale limits). This option is available whenever the SIE or SIF data file is resident in the eDAQ.
There are also options provided to auto range the full-scale definitions based on the minimum and maximum values reported for each channel for any given run. To use this functionality, highlight the desired channels in the list box complete the following control fields.

Range Multiplier %
Use the range multiplier to set some range padding on the auto range assignments. If this parameter is set to 100%, the full-scale limits are set to the minimum and maximum values acquired for the test run. The default value of 200% sets the full-scale values so that the resulting full-scale range is double the range of the acquired data. The minimum value is 10% which might be used if the acquired data exceeds the original full-scale limits. If ensuing test runs are expected to be very consistent with the trial test run used for auto ranging, it may be desirable to use a smaller padding value (e.g., 125%).

Keep Original FS Means (kom)
Check this option to maintain the original full-scale mean values. This typically results in a loss of dynamic range, but may be required for certain applications. The range multiplier parameter is used as described above to ensure that sufficient padding is provided on both ends of the full-scale definition.

Auto Set
Select the auto set option to apply the defined auto range parameters to the selected set of channels. TCE updates the list box. This option can be used as often as necessary to assign different subsets of channels different auto range parameters.

Save TCE Setup

Select this option to compute the new full-scale settings and save them in a new TCE setup file. TCE asks for the save file name and issues a report after saving the file. The report lists the new full-scale settings for each channel that has been auto ranged.

There are two situations where TCE overrides the user-defined auto range settings.

4. The hardware imposes limitations on most full-scale settings. For example, signal conditioners that have voltage inputs are limited by the A/D converter range. TCE automatically imposes these restrictions on any auto-ranged transducer channel.
5. TCE limits auto range changes that magnify the original full-scale range to be no more than a factor of 1000. This is required to avoid numerical problems with data channels where the minimum and maximum values acquired are the same or very nearly the same.

NOTE

In some special situations, the same transducer or computed channel may be stored in more than one Time History DataMode. In this case, TCE uses the first occurrence (in relation to the definition order in the TCE setup file) of the duplicated channel for display and auto range operations.

4 Using TCE

The following chapter provides detailed information on performing the various tasks available using TCE. These include defining a test setup, calibrating transducer inputs, running a full test, monitoring eDAQ status and transducer inputs before, during and after test runs, uploading test data for analysis, configuring remote control operation and setting up a network of eDAQ systems.

4.1 Defining a Test

Use the TCE setup windows to define a new test or modify an existing test. The steps involve in defining a test include: specifying one or several eDAQ systems used in the test by creating a network node or a set of network nodes; configuring the hardware layers and modules installed on the defined nodes; and adding transducer channels, computed channels and DataModes™ to acquire, manipulate and store test data.

4.1.1 Adding a Network Node

To add an eDAQ network node and define its communications and network configuration, select Add in the test ID/network node window. For a single eDAQ test, add one network node. For a set of networked eDAQ systems add a network node for each eDAQ in the test.

NOTE
If using only a single eDAQ, this step is optional. A hardware query updates all required fields in the network node setup according to the current communications preferences.

IP Address or Host Name
Specify the IP address or host name of the desired eDAQ.

Connect Timeout Period
Specify the desired timeout period in seconds for initiating communications with the eDAQ. The default value of five seconds should work well for dedicated ethernet communications with an eDAQ that is not on a network hub. Longer timeouts may be required for communications with an eDAQ on a busy or slow network hub or on a wireless ethernet connection.

NOTE
The communications I/O timeout, used for all PC to eDAQ communications, equals the connect timeout period for periods greater than ten seconds. Otherwise, TCE sets the I/O timeout period to the minimum timeout period of ten seconds.

Socket Buffer Size
Specify the buffer size used for PC to eDAQ communications. In general, leave the default value of 61440 bytes for optimum communications data throughput. For situations where timeouts on communications occur, increasing the timeout period is recommended over decreasing the socket buffer size.

Network Mode
Select one of the available network mode options detailed in the table below. There can only be one master (Master, GPS Master, or Megadac Master) in the test setup file. There can be any number of slaves. For more information on networking using TCE, see "Networking eDAQ Systems" on page 90.

Network Mode	Description
Master	The eDAQ ECPU generates the MSR clock for itself and all other connected slaves defined in the test setup.
Slave	The eDAQ does not generate the MSR clock. A master eDAQ (or other clock source) must route the MSR clock to the eDAQ.
Stand Alone	The eDAQ ECPU generates the MSR clock for itself only.
GPS Stand Alone	The GPS on the eDAQ EDIO or ECOM layer generates the MSR clock for itself only. The EDIO or ECOM layer must be configured to generate the MSR clock.
Megadac Master	The eDAQ ECPU or EDIO layer generates the MSR clock for itself and all other slaves defined in the test setup and supplies a derived clock to drive the Megadac. The EDIO layer must be configured to generate the MSR clock.
GPS Master	The GPS on the eDAQ EDIO or ECOM layer generates the MSR clock for itself and all other slaves defined in the test setup. The EDIO or ECOM layer must be configured to generate the MSR clock.

For more information on the EDIO configuration options used for the GPS and Megadac modes, see "Configuration Options" on page 97. For more information on the ECOM configuration options used for the GPS modes, see "Configuration Options" on page 96.

4.1.2 Configuring the Hardware

Use the hardware setup window to view and configure all hardware layers and modules installed on the defined network nodes. Select Query in the hardware setup window to obtain entries for the installed hardware. If the queried configuration differs from the current hardware setup, choose to update the list or abort the query when prompted. TCE also issues an alert for any flags set by the eDAQ since the last query. Double click an entry or select Config to open the hardware configuration options. Several of the hardware layers and modules offer user-configurable settings while others only show characterization details. For information on specific configuration settings available for each layer or module, see "eDAQ Hardware" on page 93.

NOTE
The thermocouple layers (EITB and ENTB) and the power controller do not offer any configuration options.

Hardware with user-configurable settings:

- ECPU
- Serial Bus (ECPU)
- EDIO

- ECOM
- Vehicle Bus (EDIO, ECOM and EHLB)
- GPS (EDIO and ECOM)

NOTE
Serial bus configuration settings are only available when a custom module is installed using the web interface. For detailed instructions on installing several different custom modules, see the installation instructions provided with the firmware installation.

Hardware with viewable characterization details only:

- EBRG
- EHLS
- EHLB
- ELLB

4.1.3 Creating Channels and DataModes™

Adding Channels and DataModes
Transducer channels, computed channels and DataModes are all added and modified in much the same way. In the appropriate window, click add to Add a new channel or DataMode. TCE first presents a list of the types of channels or DataModes. Selecting the desired type opens the configuration window for that type of channel or DataMode. When adding a transducer, TCE presents a list of common channel configurations. Select a pre-defined or blank configuration from the list. Either option allows modification. For more information on specific parameters for each channel and DataMode see chapters “Input Channels” on page 111, “Computed Channels” on page 135, and “DataModes™” on page 165.

Copying Channels and DataModes
When creating many channels or DataModes with similar properties, use the Copy option available in each window. For computed channels and DataModes, TCE only allows the creation of one copy at a time.
For transducers, TCE allows the creation of multiple copies. The number of copies defaults to the maximum allowed. TCE automatically assigns a connector to each a new channel. Choose the default IDs mode as detailed below.

Default IDs Mode	Description
All Fields Blanked	Create the copies with blank ID names. Manually enter the ID names in the next window.
All Fields Same as Original	Create the copies with ID names identical to the original channel. Edit the ID names in the next window such that there are no duplicates.
Numeric Increment (Suffix)	Create the copies with an increasing numeric suffix in the ID name. If desired, edit the ID names in the next window.

Modifying Channels and DataModes
To modify the parameters of an existing channel or DataMode, highlight the desired definitions and select Edit or double click the definition entry. For computed channels and DataModes, TCE limits the edit operation to one definition at a time.

For transducers, TCE allows group edits for a set of channels of the same type. After selecting edit, choose which set of parameters to modify. The available parameters vary depending on the type of channel.

Deleting Channels and DataModes
Delete a single definition or a set of definitions by simply highlighting the desired channels or DataModes and selecting Del. Note that any computed channel or DataMode that uses a deleted channel as an input remains listed but is no longer a valid definition.

4.1.4 Using Existing Setup Definitions

TCE provides several methods for using the setup information from existing setup and data files. These include simply opening and modifying a previously saved test setup, extracting setup and supporting files from a SIE or SIF data file and importing defined network nodes.

Modifying an Existing Test
Opening and modifying an existing test setup file is probably the most common mode of defining test after creating an initial test from scratch. To open a previously saved file, select Open Setup from the File menu or toolbar. Modify the setup as desired using the same methods described for creating a file. To save the setup to a different file, select Save Setup As from the File menu.
To support setup files generated outside of the TCE software, TCE validates the setup file fields on every open setup command. Specifically, TCE validates all fields associated with the DataMode, computed channel, transducer channel and test ID modules. The hardware modules are not validated under the assumption that they will be updated using a hardware query. TCE generates a log file in the TCE working directory that contains a list of warnings and errors found during validation.

Notes on Using Setup Files from Previous TCE Versions
Consider the following when using setup files from previous versions of TCE.

- Serial bus channels defined in TCE setup files prior to V3.8.2 are invalid. Delete these channels from the setup file and add them from the new serial bus databases provided with later releases.
- TCE automatically updates J1708 channels created using the original J1587 version of the database. Note that TCE removes all vehicle speed, latitude, longitude and altitude channels if they exist in the TCE setup file.

Importing a Network Node
The network setup window provides an option to import previously defined network node from a saved TCE setup file into the existing setup. Select Import in the network setup window to begin the import process. Importing a network node extracts all the information associated with the node including hardware, transducer and computed channels and DataModes.
TCE does not import any channels or DataModes with ID names identical to existing channels or DataModes in the defined test. If this situation occurs, delete the newly imported node, rename the duplicate IDs in the existing setup or in the setup containing the network node and import the node again.

Extracting a Setup from a Data File
To extract a TCE setup file from a SIE or SIF data file, select Open SIE or SIF File from the File menu. After choosing the desired data file, select Keyword Extraction Options and then TCE Setup File to PC File. Save the file and open it in TCE as any other previously saved setup file.

4.2 Calibrating Input Channels

Transducer calibration for the eDAQ system is independent of a specific signal conditioner or hardware layer. The transducer calibration definition is solely in terms of the relationship between the transducer output signal (i.e., voltage for most transducer types) and the selected engineering units. Note that this relationship is dependent on the excitation settings, the use of an excitation signal and the bridge settings for applicable types of transducer channels.
For a transducer that has not been calibrated, indicated by a “No” as its calibration date, select Cal in the transducer channel setup window to begin calibration. For calibrated transducers, select Cal to perform one of several calibration control options.

NOTE
For some channel types, TCE completes the calibration date parameter when the channel is created. To calibrate these channels, first delete the calibration by selecting Cal and choosing the Delete Calibration option.

4.2.1 Calibration Modes

Modify the calibration mode on the second page of the channel definition window, accessible with the Edit option or by double clicking the channel. The two mode parameters define the two steps required to uniquely determine the calibration line which represents the linear relationship of engineering units to the input signal. Define either two calibration points (values) or one calibration point (value) and a calibration slope (span).
With the two calibration steps properly defined, select Calibrate to perform the actual calibration. Upon completion, TCE sets the calibration date to the current date and disables the parameters related to calibration.

General Calibration Modes
Select one of four available calibration modes for generic transducers.

Cal Mode	Description
External Value	Define a single point on the calibration line. When prompted during the actual calibration run, apply the transducer signal value equivalent to the specified engineering units value. The eDAQ measures the signal value.
External Span	Define the slope of the calibration line. When prompted during the actual calibration run, apply two transducer signals that differ by the specified engineering units value. The eDAQ measures the two signal values and computes the slope of the calibration line in engineering units per signal units.
Defined Value	Define a single point on the calibration line. Enter both the transducer signal value and the engineering units equivalent.
Defined Span	Define the slope of the calibration line. Enter both the transducer signal value span and the engineering units equivalent of the span.

NOTE
For EHLS, EBRG, ELLB and EHLB input channel types, TCE supports the option to perform parallel calibrations if the calibration is defined with either two external values or one external value and one defined span. If multiple channels have this calibration definition, TCE asks if the calibrations should be performed in parallel or serially.

Example Calibration
Suppose an inductive pickup is used on a flywheel with 180 pickups. To output RPM, calibrate the channel with the following definitions:

- Defined Value : Eng Units [0 RPM] == Sig Units [0 Hz].
- Defined Span : Eng Units [60 RPM] == Sig Units [180 Hz].

Shunt Span Modes
Low level signal conditioner transducers (EBRG, Strain SMART Module and ELLB) offer additional mode options. These modes are all based on an internally applied shunt resistor to simulate strain or load.

Channel	Additional Modes
ELLB	10-kilohm span, 20-kilohm span, 40-kilohm span, 80-kilohm span, 160-kilohm span, 320-kilohm span, 640-kilohm span, 1.28-megohm span
EBRG	50-kilohm span, 100-kilohm span, 200-kilohm span, 500-kilohm span
Strain SMART Module	50-kilohm span, 100-kilohm span

These options define the slope of the calibration line. Enter the engineering units equivalent for the span. The eDAQ internally applies the selected shunt resistor across one arm of the bridge and measures the preshunt and postshunt signal voltages.

Notes on Shunt Span Modes

- The eDAQ stores the precise values for each of the shunt resistors in nonvolatile memory on the hardware layer. The eDAQ performs the necessary computations to compensate for each shunt resistor's deviation from the exact values presented in the above list.
- For EBRG or Strain SMART Module channels, use the Install Shunts option in the Test Control menu to install the shunt calibration resistors during a test run or preview. Use the test run data to quickly verify that all applicable channels are nominally calibrated. While this data can also be used to verify calibration accuracy in a strict sense, this is a more complicated process that requires knowledge of actual excitation voltage and actual shunt resistor value. There is no option to remove the shunt resistors, but the eDAQ always removes shunt resistors when preparing for a new run, a channel display or any calibration task. For networked eDAQ systems, the shunt resistors are installed sequentially from one network node to the next.

NOTE
Although this task requires a fairly small amount of eDAQ processing, it can result in a DeviceOverFlow error reset for tests running at the edge of the eDAQ processing limit.

- An internal shunt resistor applied across the +Ex to -Sig leg of the bridge results in a downscale shunt. In other words, the voltage output from the bridge swings in the negative direction when the shunt is applied. Take this into consideration when setting the sign of the associated engineering value.
- If the measured voltage span and the theoretical ideal voltage span do not agree within the specified percentage found in the TCE General Preferences, TCE issues a warning message.

Preshunt Value
Specify a preshunt value to define a single point on the calibration line in conjunction with one of the shunt span modes (e.g., 40-kilohm span). Enter the engineering units equivalent. The voltage used is the preshunted voltage measured in the shunt span step. This mode is recommended to reduce the entire calibration to one step.

Shunt Tools
For a bridge channel, use the shunt tools option as a guide to indirectly select a shunt span mode (e.g., 40-kilohm span) with an associated engineering equivalent value. The two options for shunt calibration are based on a known shunt calibration or gage and bridge factors.
For a shunt calibration based on a known shunt, enter the shunt resistor and corresponding engineering value (e.g., a 33.2-kilohm shunt that produces a 2200-pound output). TCE initially highlights the shunt resistor that results in the closest engineering value. Select the desired calibration step definition based on the strain values expected in the field.
The equivalent engineering values for the shunt resistors use the following equation.

$$V_e = V_k \frac{R_g + 2R_{sk}}{R_g + 2R_{se}}$$

where, V_e is the equivalent engineering units value, V_k is the known engineering units value, R_g is the nominal gage resistance, R_{sk} is the known shunt resistance and R_{se} is the equivalent shunt resistance.

NOTE
Be careful to ensure that the known shunt calibration applies to the same leg of the bridge circuit that used in the shunt calibration; otherwise, the polarity of the computed shunt span may be inverted.

A shunt calibration based on the gage and bridge factors calculates a shunt resister using the gage factor of the active strain gage and bridge factor for the bridge configuration defined with the channel parameters. Select the desired calibration step definition based on the strain values expected in the field. The shunt tool assumes that the engineering units are microstrain. If using dimensionless strain units, divide the equivalent strain value by 1000000.
The equivalent strain uses the following equation.

$$E_s = \frac{1000000 R_g}{BG(R_g + R_s)}$$

where, E_s is the equivalent strain in microstrain units, R_g is the nominal gage resistance, G is the gage factor and B is the bridge factor.

NOTE
If the shunt target results in a downscale shunt, E_s is multiplied by -1.

NOTE
Changing the bridge type, bridge resistance, shunt target, gage factor or bridge factor invalidates the computed equivalent strain. Run the shunt tool again after changing these parameters.

Multi-Point Cal
The multi-point calibration mode is available for EBRG and EHLS channels only. When beginning a calibration with the multi-point cal mode selected, follow the instructions on the series of configuration windows to fully define the calibration. Define anywhere from 3 to 16 calibration points for TCE to acquire and least squares fit to determine the best linear fit calibration slope and offset. Once the calibration is completed, TCE creates two defined values based on the user-defined full-scale min and max.

4.2.2 Calibration Control

Access the calibration control options by selecting to calibrate an already calibrated channel. Use calibration control to perform various transducer calibration tasks including check calibration, zero adjust calibration, or delete calibration.

Check Calibration
The check calibration option performs a calibration run and displays a graph and numeric data comparing the original calibration with the one just performed. For one channel, the calibration check window shows the maximum deviation and the defined and measured calibration values. For two or more channels, the summary window shows each channel's maximum deviation in both engineering units and percentage of full-scale range. Click the More Info button to show the calibration check window for the highlighted channel.

NOTE
The calibration check does not account for zero adjustments done after the original calibrations.

Zero Adjust Calibration
The zero adjust calibration allows adjustments for small differences between the original zero setting used in calibration and the zero setting required for actual measurement. This is useful to compensate for zero drift common with many input channels.
First, enter the engineering value equivalent to the current input channel states. Next, the eDAQ measures the current input channel outputs and offsets the calibration lines as required to yield the specified engineering value. Performing a zero adjust calibration adds a tilde (~) to the end of the transducer's calibration date.

NOTE
Use the zero adjust option only when necessary and then only for very small adjustments. Because the zero setting is permanently modified, consider recalibrating the channel instead of using this option.

NOTE
For quadrature decoder channels, the eDAQ resets the internal counter value to zero before performing a zero adjust.

Delete Calibration
Delete the calibration to clear the calibration date field and modify calibration-related parameters before recalibrating the channel.

Shunt Calibration Loop
The shunt calibration option, primarily for HBM development purposes, verifies the reliability and accuracy of ELLB shunt calibrations. It is available only for ELLB channels that use shunt calibrations. This task has no affect on existing calibrations.

4.2.3 Calibration Specifications

EHLS and EBRG Channels
To measure calibration signal voltages for EHLS and EBRG channels, the eDAQ down samples the A/D converter subsystem by a factor of 1000 or 960 (depending on the MSR) to 100 or 102.4, respectively, using a Butterwoth 8-pole digital filter with a 15-Hz break frequency. The eDAQ manipulates the signal conditioner gains and offsets in an auto ranging mode to yield near maximum resolution of the input signal (i.e., the eDAQ sets the gains as high as possible). The eDAQ acquires one A/D sample to determine the signal voltage of the input channel.

High Level Channels
For most high-level input channels (i.e., high level, pulse counter, vehicle bus, serial bus and GPS input channels), the eDAQ acquires a set of data samples at the user-specified sample rate and averages these to provide a single signal value for calibration purposes. If the sample rate is 50 Hz or more, the eDAQ uses 100 data samples. Otherwise, the uses a number of data samples equal to twice the sample rate (down to the minimum of one data sample).

Thermocouple Channels
For standard and isolated thermocouple input channels, the eDAQ uses only one data sample to provide a single signal value for calibration purposes.

ELLB Channels
To measure calibration signal voltages for ELLB input channels, the eDAQ down samples the A/D converter subsystem by a factor of 1000 or 960 (depending on the MSR) to 100 or 102.4, respectively, using a Butterwoth 8-pole digital filter with a 15-Hz break frequency. The eDAQ manipulates the signal conditioner gains and offsets in an auto ranging mode to yield near maximum resolution of the input signal (i.e., the eDAQ sets the gains as high as possible). The eDAQ averages ten A/D samples to determine the signal voltage of the input channel.

NOTE
Override the defaults described above using the low level calibration options in the TCE FCS Specific Preferences.

4.2.4 AOM Calibration File

HBM offers the EHLS, EBRG and ELLB layers with an optional analog out function to provide high level analog output signals for each channel. Select Save AOM File from the Test Control menu to generate a PC file that contains the calibration parameters required to relate the high level analog outputs of the EHLS, EBRG and ELLB signal conditioners to equivalent engineering units values.
This option is available only after a test run has been started because the eDAQ does not maintain the analog signal conditioner circuitry in a fixed state after a test is initialized. For example, when a new test run starts, the eDAQ temporarily disconnects the signal input lines from the front panel connector leads and shorts them to ground to account for amplifier offsets and other sources of offset. Furthermore, if calibration

checks are performed after the test is initialized, the analog circuitry for those transducers are in a significantly different state after the checks and remain in this state until there is a requirement to change the analog circuitry setup (such as starting a test run, running the rezero display, etc.). Although the analog outputs calibration parameters are often quite consistent from test run to test run, this may not always be the case and should definitely not be presumed.
There are two file format options available to store the analog output calibration file parameters. The original file format is discussed in detail below. The second file format is a tab delimited file format that is Excel compatible. It contains the same information as the original file format, but is organized differently. It also has the ELLB channels sorted alphabetically by connector ID.
The original analog output calibration file is written in a standard Windows initialization file format (i.e., it can be read using the GetPrivateProfileString() function provided in Windows). Following is a fragment of a typical original AOM file with added comments. The numbers in brackets are the maximum string lengths - this includes the null terminator. All numeric fields are floating point.

```
[Main]
SetupFile=c:\tce\test.tce   TCE setup file path [256]
RunNumber=1                 Test run number
NumXdcrChs=4                Number of transducers

[XdcrCh_1]                  For the 1st transducer...
ID=RF_Wheel_Fz              Transducer channel ID [13]
NodeName=eDAQ05             Network Node Name [256]

Connector=LoLev_1.c01       Hardware connector ID [13]
Units=lbs                  Engineering units string [16]
Scale=984.571              Cal slope (eng units / volts)
Offset=-0.00179932         Cal intercept (eng units @ 0
volts)
Eng_FSMin=-10000           Engineering units Full-Scale
Min
Eng_FSMax=10000            Engineering units Full-Scale
Max
Volts_FSMin=-10.1567        AO voltage @ Full-Scale Min
Volts_FSMax=10.1567         AO voltage @ Full-Scale Max

[XdcrCh_2]                  For the 2nd transducer...
ID=RF_Wheel_Fy              Transducer channel ID [13]

(and so on...)
```

4.3 Running a Test

Use the controls in the Test Control menu or in the toolbar to perform test run tasks. Alternatively, use the Control Panel, opened from the Test Control menu, for quick access to common test run tasks. The Control Panel also shows the amount of RAM and PC Card memory available for data storage.

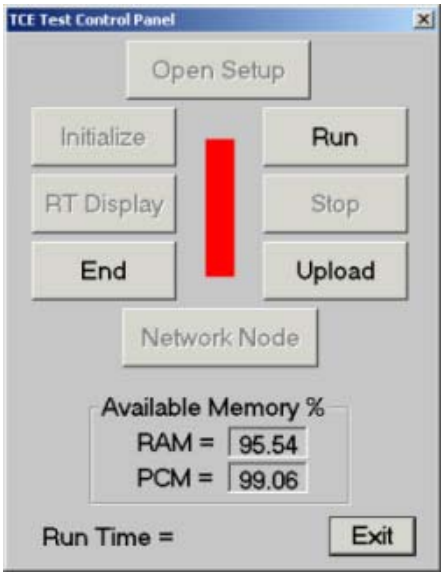


Figure 4-1: TCE Control Panel for quick access to test run tasks.

Running a test using the existing test setup definition consists of the following steps.

4.3.1 Initializing a Test

The initialization process prepares the eDAQ for a test run. Select Initialize from the Test Control menu or toolbar to begin initialization which consists of the following steps.

- Verify that the current test setup is saved to a disk file and there are no internal inconsistencies in the test setup such as uncalibrated channels or unresolved ID references.
- Check that the eDAQ real-time clock agrees with the real-time clock in the support PC within the user-specified tolerance.
- Purge the eDAQ RAM disk and PC Card, removing previous test setup and SIF data files.
- Transfer the required test setup files to the eDAQ.
- Set up the eDAQ signal conditioner excitation circuits, allowing the maximum time for the excitation circuits to stabilize before the test run starts.
- Create the data file and write some of the header fields.
- For transducer channels with programmable gains and offsets, check the actual full-scale limits to verify that the over range protection is sufficient. TCE issues a warning for any unusual situations as specified in the TCE General Preferences.

4.3.2 Prerun Options

After initialization and before starting a test run or between test runs, there are a number of prerun options available through the Prerun Options sub-menu of the Test Control menu.

Transducer Checks

The transducer checks option provides the ability to run the DVM, scope or spectrum displays or perform calibration checks. Select the desired channel or channels from the list and the preferred option using the radio buttons and then click Run to execute the option for the selected transducer or transducers.

Option	Description
Calibration Check	Run a calibration check. Note that the calibrations are the current transducer calibrations which may differ from the calibrations defined at test initialization if the transducer has been rezeroed. Check for this difference using the rezero offset option.
DVM Display	Run the DVM display.
Scope Display	Run the scope display.
Spectrum Display	Run the spectrum display.
Rezero Offset	View the differences between the current transducer calibration intercepts and those defined at test initialization. For each transducer channel, this difference is the cumulative sum of all rezero offsets in engineering units since test initialization.

Rezero Display

Use the rezero display to view and rezero the defined transducer channels. Select the desired channel or channels and click OK. TCE continuously reads and displays the current transducer signals in engineering units. Select the hold option to pause display updates or use the scroll bar at the right of the window to adjust the display update rate. The rezero display also shows the prerun rezero value defined for the transducer in the test setup and indicates in the (A) column if the transducer is to be rezeroed just prior to the next test run. To manually rezero a channel, select the transducer in the (B) column and click the rezero button or press ALT+R.

Reference Shunt Checks

Use the reference shunt checks option to perform shunt resistor checks on the low level transducer channels that are defined with the reference shunt option enabled. The shunt check information includes the transducer channel ID, the last check span in engineering units stored in the data file and the difference between the minimum and maximum shunt check spans in engineering units. Select more info to view a more detailed report of the shunt checks on the highlighted channel. To run another shunt check, select run shunt check.

NOTE

The eDAQ stores the shunt check information file in a global keyword accessible area of the SIE or SIF data file. For more information on extracting this file, see “Extracting Data from SIE or SIF Files” on page 88.

NOTE
The shunt span calculations do not correct for leadwire resistance effects or the slight deviations of the actual shunt resistances from the nominal resistances. Therefore, the stored shunt spans are not as accurate as the calibration shunt spans are more than sufficient for documenting changes in transducer response from run to run.

NOTE
If the voltage readings for any shunt check span exceeds the limit for the type of signal conditioner, TCE tags the reported span as invalid by marking it with a “-?” string.

4.3.3 Previewing a Test Run

A preview run effectively starts a test run with all DataMode storage suppressed. All of the transducer channels and computed channels run in preview mode just as they would during a data collection run. To start a preview run, select Preview Run from the Test Control menu or toolbar.

4.3.4 Starting a Test Run

To start a test run, select Start Run from the Test Control menu or toolbar. The SoMat eDAQ supports multiple test runs for an initialized test. Start a new test run anytime after a previous run stops or during a preview run. When starting a test run, TCE presents a start test run dialog window displaying the next run number and allowing the input of a short run description (up to 63 characters per run).

NOTE
Use TCE General Preferences to suppress the start test run dialog window.

The data acquired on multiple runs is stored in a single SIF data file. Each channel of acquired data is tagged with the designated run number.
Run descriptions are stored in a fixed 2048 character record of the SIF data file allocated when the test is initialized. The run descriptions can be extracted from the SIF data file using an EASE procedure file that is resident in the TCE installation directory.

4.3.5 Using Interactive Triggers

TCE interactive triggers allow user input from the software to control a computed channel or DataMode through the use of an Interactive Trigger computed channel. There are eight Boolean logic controls available which must be assigned to an Interactive Trigger computed channel. When the test is initialized, TCE sets all the triggers to FALSE. Select Interactive Triggering from the Test Control menu to control the trigger states before or during a test run. Use the check box by each trigger index and clack Apply Triggers Now to change the trigger state. A check indicates a TRUE

state. TCE grays out the triggers not defined in the test setup. To invert the trigger logic (i.e., a check for a FALSE state), use the invert trigger parameter in the Interactive Trigger computed channel. For more information on the Interactive Trigger computed channel, see “Interactive Trigger” on page 152.

NOTE
The eDAQ maintains the trigger states through power fail or error reset test run restarts.

4.3.6 Stopping a Test Run

Manually stop the current test run by selecting Stop Run from the Test Control menu or toolbar or use the Test Run Stopper computed channel to automatically stop a test run based on triggering conditions. For SIF files, certain post run tasks may be required before the test is actually stopped. If the PCM storage option is in use, the SIF post run tasks consist of ensuring that the SIF component files on the PC Card are completely flushed and closed. There are no post run tasks for SIE data files.

4.3.7 Ending a Test

To end a test run, select End Test from the Test Control menu or toolbar. Ending a test prevents starting a new test run until after re-initializing the eDAQ. This option is available when a test is initialized and no test run is in progress. Data files are still available for upload after ending a test.

4.4 Monitoring Test Status

Select Get Test Status from the Test Control menu or toolbar to display the state of the current test and eDAQ data storage. The provided indicators are described below.

Category	Indicator	Description
Test Run Status	Test Initialized	Indicates that a test is initialized on the eDAQ.
	Remote Control	If a test is initialized, indicates the status of the remote control mode as either disabled, enabled or suspended.
	Run #	If a test is initialized, indicates the current run number or the next run number if no test is running.
	Run or Preview Started	Indicates that a test run or preview is in progress.
	Run Time	If a test run or preview is in progress, indicates the elapsed time since the start of the run. The elapsed time display rolls over after 1000 hours.
	Post Run Tasks	Indicates that a test run is stopped, but the required post run tasks are not completed.
RAM Disk Files	Origin	Indicates the original TCE name of the current test setup file.
	Setup	Indicates the eDAQ reference name of the current test setup file.
	Data	Indicates the name of the current SIF data file. Note that even when using only SIE data, the eDAQ retains a very small RAM disk-based SIF file for internal purposes.

Category	Indicator	Description
RAM Disk Memory (in bytes and percent total of RAM disk memory)	Total	Indicates the total RAM disk memory on the eDAQ.
	SIF File	Indicates the current size of the resident SIF data file.
	Unused	Indicates the unused memory available for data file storage.
PC Card Disk Memory (in bytes and percent of total PC Card memory)	Total	Indicates the total memory on the PC Card.
	SIE File	Indicates the cumulative size of the SIE data files currently on the PC Card.
	SIF File	Indicates the cumulative size of the SIF component data files current on the PC Card.
	Unused	Indicates the unused memory on the PC Card available for data file storage.
	SIF File limited to	Indicates the maximum allowable size for the SIF file.
	SIF File Built on PC Card	If PC Card data storage is in use, indicates that the SIF file has been consolidated and the PC Card can be removed from the eDAQ after powering down.

4.5 Viewing Channel Displays

TCE includes a variety of integrated run-time displays to view real-time data from input channels and computed channels during a test run. TCE also offers a several signal display types to view transducer input signals when a test run is not in progress.

4.5.1 Displays Overview

Channel displays are available before initialization, as a prerun option and as run-time displays during a test run.

NOTE
When applicable, always define the excitation circuitry before displaying the transducer signal.

- *Pre-Initialization*—Before initialization, TCE can display transducer channels before or after calibration. The eDAQ uses the user-defined sample rate and digital filtering. The display types available before initialization are DVM, scope plot and spectrum plot (i.e., Freq). Access all three types in the transducer setup window. The DVM and scope plot displays are also accessible in the display control section on page two of the transducer channel definition dialog box.
- *Prerun*—The DVM, scope plot and spectrum plot display modes are available as prerun options after initialization and before the first test run or between test runs. To access the displays, select Transducer Checks from the Prerun Options sub-menu of the Test Control menu.
- *Run Time*—Run-time displays show the raw signals from input and computed channels on a real-time basis providing verification that input and computed channels are functioning properly. Run-time displays are only available while a

test is running. The available run-time display types are bar chart, strip chart, digital readout, scope plot and spectrum plot. Access the display modes from the Run-Time Displays option in the Test Control menu or toolbar.

NOTE
TCE stores the run-time display channel set and display mode in a RAM disk file. When restarting a run-time display during a test, TCE starts the display in the last used configuration.

The following table presents a summary of the displays in TCE, when they are available and the maximum number of channels each supports.

Display	Pre-Init	Prerun	Run-time	Max Chs.
DVM	yes	yes	no	16 or 256
Scope Plot	yes	yes	yes	1
Spectrum Plot	yes	yes	yes	1
Digital Readout	no	no	yes	16
Bar Chart	no	no	yes	16
Strip Chart	no	no	yes	4

NOTE
The maximum number of channels allowed for a group DVM display depends on the display mode selected in the Group DVM Display Preferences. For more information on these preferences, see “Group DVM Display” on page 59.

Notes on Run-Time Displays

Run-time data is acquired using two different methods depending on the display mode. The digital readout, bar chart and strip chart displays use the min-max data acquisition method while the scope and spectrum plots use the contiguous block data acquisition method.

Min-Max Method:

- When the run-time display starts, the eDAQ continuously monitors each channel, tracks the minimum and maximum signal values and holds those values in a buffer. Periodically, TCE polls the eDAQ to get the minimum and maximum values. After the eDAQ sends the values to TCE, it resets the min-max search so that the next read gives the minimum and maximum values since the last read.
- A min-max display runs continuously on the eDAQ while the display is opened and examines all data samples in the min-max search. Though the display was designed to minimize the overhead on the eDAQ, it does add to the eDAQ processing load and can result in a DeviceOverFlow error reset for tests running at the edge of the eDAQ processing limit.
- Minimum and maximum values are not time-stamped and the TCE polling loop results in reads that are only approximately equally spaced in time. When using PC Card data storage, the time interval between TCE polls is typically more erratic.
- The min-max display mode can only be used with one application at a given time. If a second application (e.g., InField) attempts to run a min-max display mode at the same time, the data presented in TCE becomes invalid.

Contiguous Block Method:

- When the run-time display starts, TCE requests a contiguous block of data samples from the eDAQ for the selected channel. The eDAQ responds to the request by returning the block of data samples. TCE displays the data in the specified format and then requests a new block of data samples.
- A contiguous block display adds to the eDAQ processing load and can lead to a DeviceOverFlow error reset for tests running at the edge of the eDAQ processing limit.

4.5.2 Common Display Options

Start Run (run-time only)
For run-time displays during a preview run, select Start Run to start a test run.

View
Select one of the two view modes available for each display.

View Mode	Description
Scan	Update data in the display as it is received.
Hold	Do not update the display. For some displays, the Hold mode allows access to certain display options.

Setup (run-time only)
Select setup to exit the current display and return to the run-time display setup window.

Units (pre-init and prerun only)
Select one of two units options available.

Units	Description
Signal / Volts	Display the transducer in signal units (e.g., volts). This is the only option available for uncalibrated transducers.
Engineering	Display the transducer in engineering units (e.g., microstrain). This is the default option for calibrated transducers.

Quit / Off
Select Quit (run-time) or Off (pre-init and prerun) to exit the display.

4.5.3 DVM

The DVM (digital voltmeter) display samples and displays up to 16 or 256 transducer signals in a digital format. The DVM is available pre-initialization and as a prerun option. TCE presents the DVM display window differently for a single channel and a group of channels.

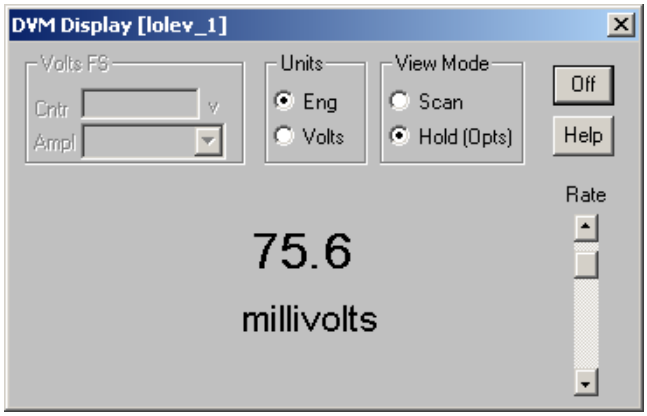


Figure 4-2: A TCE DVM signal display for a single channel.

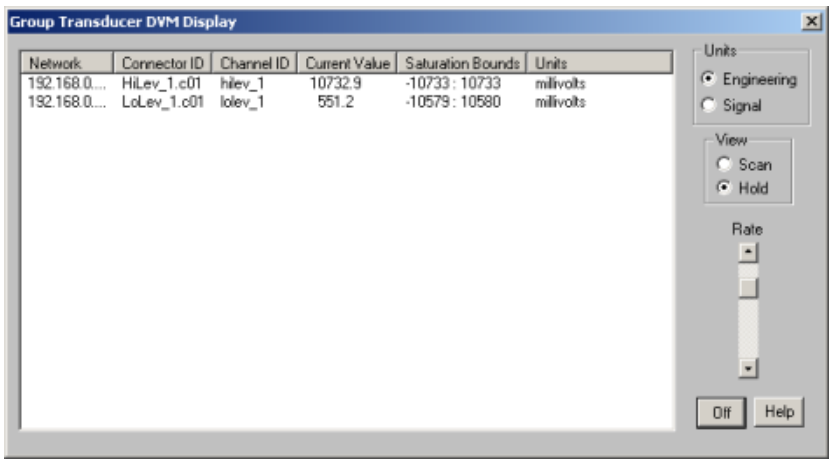


Figure 4-3: A TCE DVM signal display for a group of channels.

Rate

Adjust the rate scroll bar to change the rate at which TCE updates the display.

NOTE

A DVM for a single digital input channel offers the option to read bits. When using this option, the eDAQ reads the current state of the digital input line and TCE displays a check when the line is high (i.e., logical TRUE) or no check when the line is low (i.e., logical FALSE).

4.5.4 Scope Plot

The scope plot display is similar to that of an analog oscilloscope except that the display is not updated until the eDAQ acquires all of the data samples and transfers them to TCE which creates a delay in the data presentation. The scope plot is available for a single channel at pre-initialization, as a prerun option and as a run-time display. For more information on scope plot display preferences, see “Scope and Spectrum Display” on page 58.

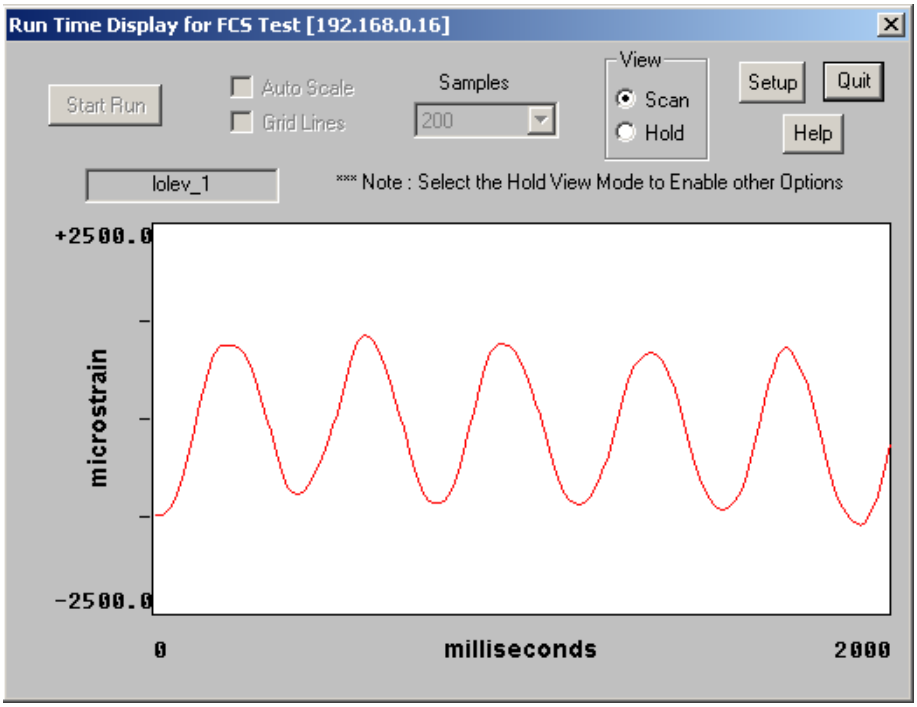


Figure 4-4: A TCE scope plot as a run-time display.

Samples
Select the desired number of samples to display on each scope scan.

Auto Scale
Select the auto scale option to switch to automatic y-axis scaling mode which sets the y-axis limits to the maximum and minimum values in the data set for each scope scan.

Grid Lines
Select the grid lines option to add grid lines to the scope display. The grid lines divide each axis into ten equal parts. If using the auto scale option, TCE only displays the x-axis grid lines.

4.5.5 Spectrum Plot

The spectrum plot display shows the frequency content of the signal. TCE scales the x-axis from 0 Hz to the Nyquist frequency (i.e., half the sample rate) and the log y-axis to cover up to six decades. The data points are the approximate sine amplitude of the signal components at each frequency. The data point at 0 Hz in the DC level of the signal. The spectrum plot is available for a single channel at pre-initialization, as a prerun option and as a run-time display. For more information on spectrum plot display preferences, see “Scope and Spectrum Display” on page 58.

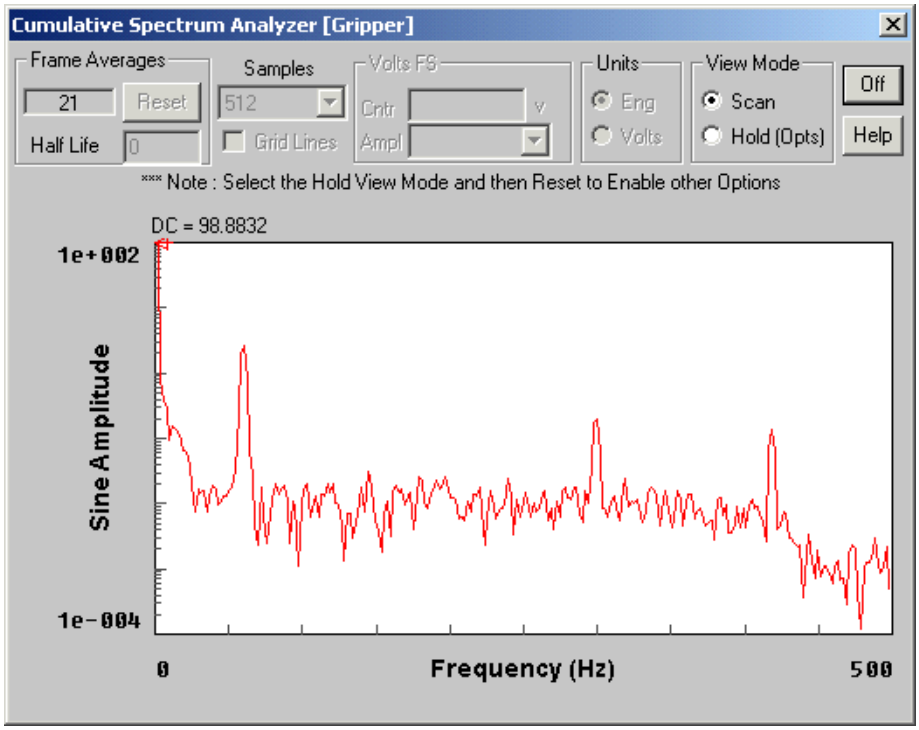


Figure 4-5: A TCE spectrum plot as a prerun option display.

Samples
Select the desired number of samples used in the FFT algorithm to generate the frequency spectrum.

Grid Lines
Select the grid lines option to add grid lines to the spectrum display. The grid lines divide the x-axis into 10 equal parts and the y-axis on a log scale in decades.

Half Life
Select the desired half life value. The spectrum half life specifies the amount of old data to combine with the newly acquired data. For example, if the half life is one, the contribution of the old spectrum data is half of the contribution from the new data. If the half life is ten, it takes ten new frames of data before the old data is at half its influence. The default value is zero which results in no data accumulation. For situations with stable signal content, a larger half life produces a display with fewer fluctuations and a better representation of signal content.

4.5.6 Digital Readout

The digital readout display continuously shows two sets of minimum and maximum readings in a digital format for up to 16 channels. The last reading min and max columns display the minimum and maximum values from the latest reading. The since reset min and max columns show the overall minimum and maximum values since the start of the display or the last reset. The digital readout is available as a run-time display only.

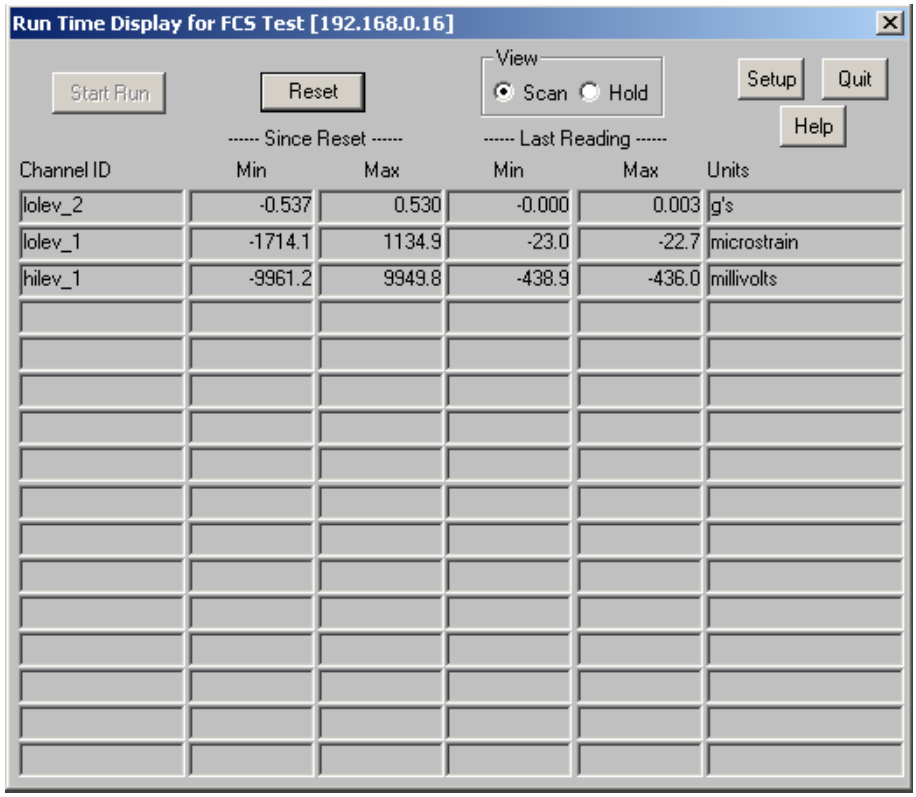


Figure 4-6: A TCE digital readout run-time display.

Reset

Click the Reset button or use the ALT+R keyboard shortcut to reset the tracking and display of the overall minimum and maximum values.

4.5.7 Bar Chart

The bar chart display uses solid horizontal bars to continuously show the most recent minimum and maximum data values for up to 16 channels. TCE uses an arrow head to point to the bar when the bar is very thin. The chart also uses cross-hatched horizontal bars to show the overall minimum and maximum values since the start of the display or the last reset. The FS min and max columns display the full-scale values defined for the channel. The bar chart is available as a run-time display only. For more information on bar chart display preferences, see “Run-Time Display” on page 59.

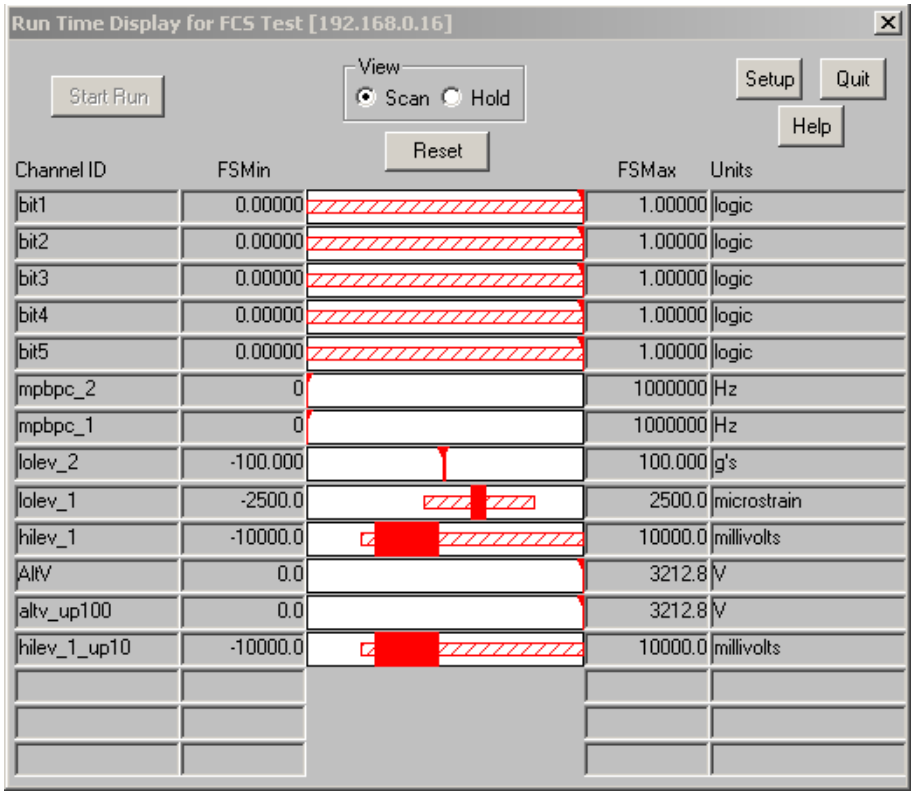


Figure 4-7: A TCE bar chart run-time display.

Reset

Click the Reset button or use the ALT+R keyboard shortcut to reset the tracking and display of the overall minimum and maximum values.

4.5.8 Strip Chart

The strip chart display shows the minimum and maximum readings for up to four channels as a sequence of solid vertical bars along the x-axis. The chart displays up to 400 most recent min-max readings. The strip chart is available as a run-time display only. For more information on strip chart display preferences, see “Run-Time Display” on page 59.

NOTE

The x-axis of the strip chart is not a linear time base. The display update period is determined by the processing time required plus a built-in delay. Actions such as changing the plot mode or placing the display on hold significantly affects the update period. In steady-state operation, the x-axis is usually a good approximation of a linear time base.

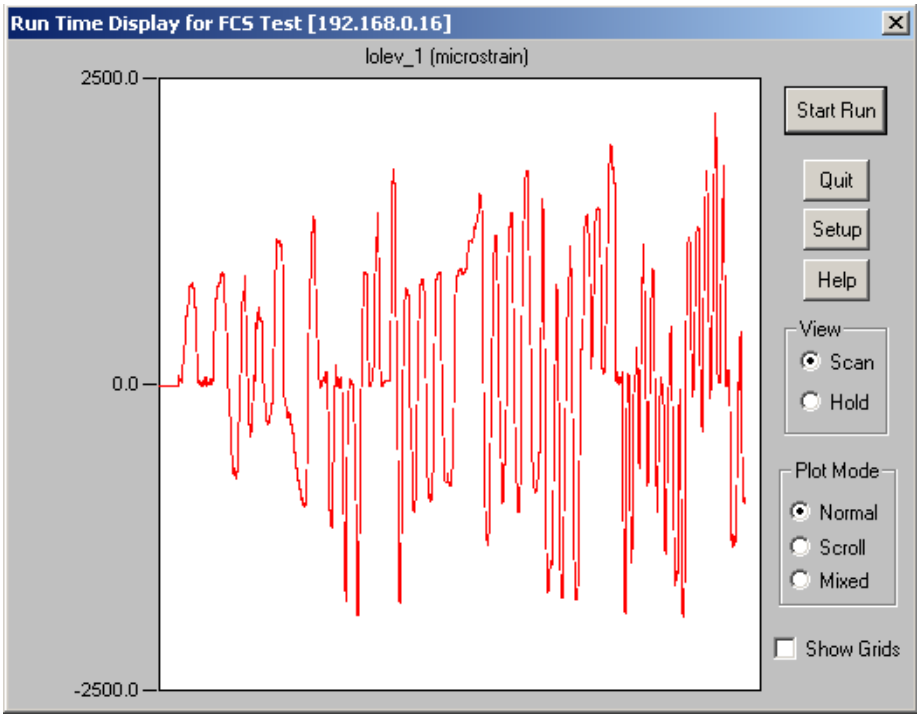


Figure 4-8: A TCE strip chart run-time display.

Plot Mode

Select one of three strip chart plotting modes.

Plot Mode	Description
Normal	When the plot reaches the end of the x-axis, TCE erases the display and draws the next vertical bar at the beginning of the x-axis.
Scroll	The vertical bars continuously scroll from left to right after the plot reaches the end of the x-axis for the first time. The latest min and max values are always at the end of the x-axis.
Mixed	When the plot reaches the end of the x-axis, TCE moves the last half of the display to the first half and resumes plotting from the middle of the display.

Show Grids

Select the show grids option to show the grid lines on the display.

4.6 Uploading Test Data

Uploading test data transfers all or selected test runs resident in the data file stored in the eDAQ to a user-specified PC disk file. Upload complete SIE or SIF files after stopping a test run. When using SIE data, partial files are available for upload during a test run.

After transferring the file to the support PC, use InField or other data analysis software to view and analyze the test data.

4.6.1 Uploading SIE Data Files

From the eDAQ
To upload SIE data from the RAM disk or PC Card storage in the eDAQ, select Upload Test Data from the Test Control menu or toolbar. Upload SIE test data at any time, including during a test run when partial test data is available. Use some caution when uploading during a test run as the upload task consumes some processing time and can result in a DeviceOverFlow error reset if the eDAQ cannot keep up with the processing requirements.

From a PC Card
If transferring data from a PC Card inserted in the support PC, simply copy the SIE file from the PC Card to a PC directory.

4.6.2 Uploading SIF Data Files

From the eDAQ
To upload SIF data from the RAM disk or PC Card storage in the eDAQ, select Upload Test Data from the Test Control menu or toolbar. If using RAM disk storage, TCE uploads the SIF file directly to the PC file. If the PC Card data storage option is in use, the eDAQ first consolidates the SIF data file from the RAM disk resident component file and the set of PC Card resident component files. A test run cannot be in progress to upload a SIF data file.
Upload SIF data after a test run or after ending a test. The upload option becomes unavailable as soon as a new test is initialized, since the eDAQ deletes the RAM disk SIF component file upon initialization.

NOTE
If there is a communications failure between the PC and the eDAQ during an upload of the files on the PC Card, TCE enters a loop of making repeated attempts to re-establish communications so that the upload process can recover and continue. This recovery scheme handles most types of communication failures such as power lost to the eDAQ temporarily or Ethernet connections broken temporarily. If necessary, abort the communications loop using the Abort option in the upload progress window.

NOTE
To increase data analysis performance, chain frame demultiplexing to the upload process using TCE General Preferences.

From a PC Card
If transferring SIF component files from a PC Card inserted in the support PC, first copy the SIC files from the PC Card to a PC directory. Then select Consolidate SIC Files from the File menu. The consolidate SIC files option generates a complete SIF file from the component files. TCE performs a number of validity checks on the SIC file set during the SIF file generation process.

NOTE
To increase data analysis performance, chain frame demultiplexing to the consolidate process using TCE General Preferences.

4.6.3 Extracting Data from SIE or SIF Files

SIE an SIF files contain more information than what is available when viewing uploaded data. To access this information, select Open SIE or SIF File from the File menu.

NOTE
When opening a SIF file, TCE checks the file for any frame multiplexed data records. If they are present, TCE presents the option to demultiplex all frame multiplexed data records. Analysis routines that run on a channel by channel basis typically execute significantly faster using fully demultiplexed data records.

Select one of the following options to access additional test and eDAQ information.

Keyword Extraction Options
The keyword extraction options provide the opportunity to extract some of the global keyword data sets that are embedded in the SIE or SIF data file. To access an available option, select the corresponding radio button and click OK.

Keyword Data Set	Description
TCE Setup File	Extract the TCE setup file to a PC file.
FCS Log File	Extract the eDAQ log file to a PC file.
Test Run Descriptions	Extract the TCE test run descriptions to a PC file.
State Mapper File	Extract the specified (by index) State Mapper ASCII definition file to a PC file. The file index starts from 1. TCE appends the original source ASCII file name to the extracted file. Delete this file name from the extracted file to reuse the ASCII file in a State Mapper computed channel (see “State Mapper” on page 144).

Keyword Data Set	Description
Reference Shunt Check Info	Extract the TCE reference shunt check information and display it in the same reference shunt checks TCE dialog window used during active test control. For more information, see "Reference Shunt Checks" on page 75.
Run Rezero File	Extract the run number indexed TCE transducer rezero ASCII file to a PC file. The run number index starts from 1. The first line of the file specifies the run number. The following lines contain the transducer channel ID and the zero offset value in engineering units. There is one line for every transducer channel that can be rezeroed. The offset value is the amount the transducer has been rezero offset since the test was first initialized. For more information, see "Rezero Display" on page 75.
Power Micro Run Status	Extract all of the power micro parameters to a PC file. The eDAQ stores the power micro parameters just before each test run starts and includes information such as battery change level and battery temperature. TCE also records the date and time of the start of each test run.

Message Channel Extraction Options

The message channel extraction options provide the opportunity to extract message channel data sets that are resident in the SIE or SIF file to a text file on the support PC. TCE presents a list box containing all of the message channels in the data file. Select one or more of the message channels and then save the message channel data sets to a PC file.

Example PC Message Channel Files

- ASCII Message Channel:

```
# msg_ascii@simmsg_asc.RN_1 (Sim Msg simmsg_asc)

RX 10.0000000: 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57
58 59 5A 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 (and so on...)

RX 20.0000000: 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57
58 59 5A 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 (and so on...)
```

- Binary Message Channel:

```
# msg_bin@simmsg_bin.RN_1 (Sim Msg simmsg_bin)

RX 4.0000000: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16
17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B (and so on …)

RX 8.0000000: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16
17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B (and so on …)
```

Generate Quickview Log File (SIF only)
The generate quickview log file option parses the SIF file channel list and generates an ASCII log file that summarizes the channel list with presentation of some of the channel header information combined with a small amount of the actual data for each channel. This option is provided primarily for troubleshooting corrupt SIF data files.

4.7 Using Remote Control Operation

Start and stop test runs remotely using the remote control operational mode. The remote control mode uses digital I/O lines for control inputs and status outputs. The eDAQ uses the ECPU layer digital lines. Use one digital input line to control test run starts and stops and up to four digital output lines for status indications. Configure the digital input and output line assignments in the TCE Remote Control Preferences dialog.
The remote control mode is enabled at test initialization and remains in effect until the test ends, unless manually suspended. When the remote control mode is active, many of the test control tasks are disabled.
The Remote Control Setup preferences configure the eDAQ for remote control of test runs using digital input and output lines. For more information or remote control preferences, see “Remote Test Run Control” on page 56.

4.8 Networking eDAQ Systems

Networking allows multiple eDAQ systems to acquire data synchronously using a single master sample rate (MSR) clock source. TCE supports defining the test setup configurations for networked systems in a single test setup file and coordinates most test control tasks for the network. For information on setting up the networked systems, see “Networking eDAQ Systems” on page 40.

NOTE
When an eDAQ is configured as either a master or a slave and a power failure or an error reset occurs, the eDAQ does not attempt to start a new test run.

The first step is to define the set of eDAQ systems used in the test in the network setup window. The networked nodes can consist of any combination of eDAQ and eDAQ-lite systems. Configure one node as the master or the GPS master and the rest of the nodes as slaves. The choice of which system is the master is largely arbitrary.

NOTE
All nodes in a network configuration must have the same master sample rate value.

Proceed to define the transducer channels, computed channels, and DataModes for the test in the same manner as for a single eDAQ. Multiple channel interactive setup tasks such as the group DVM display and parallel transducer calibrations require that the channel set reside on a individual network node. However, most non-interactive features (e.g., group edits and group deletions) are supported across network nodes.

With the test setup definition completed and all transducer channels calibrated, initialize and run the test in the same manner as for a single eDAQ test. TCE coordinates all interaction between network nodes during initializations and test runs.

NOTE
Run-time displays can only display channels from one eDAQ at a time.

While largely transparent, the details of starting or previewing and stopping test runs are discussed briefly below. TCE first prepares each slave eDAQ for a test run start or preview in a serial manner. The slave then waits for the master to assert the MSR clock source for the test run to actually begin on the slave. During this waiting period, the green and yellow LEDs on the slave blink in unison at a fairly slow rate. At the start of the test run or preview, the master asserts the MSR clock source which starts all test runs or previews synchronously. To stop a test run or preview, TCE stops the test run or preview on the master eDAQ, which results in the de-assertion of the MSR clock source. When this occurs, each slave detects the loss of the MSR clock source and stops the test run or preview synchronously.
TCE gets SIF file data from the eDAQ nodes in a serial manner. TCE appends a qualifier string to the default PC file name to distinguish the SIF files. For example, if the test setup file name is MyTest.tce and there are three networked nodes, the default SIF data file names are MyTest (1 of 3).sif, MyTest (2 of 3).sif and MyTest (3 of 3).sif. TCE applies the same default naming convention when transferring files from a PC Card.

4.8.1 Using Remote Control with a Network

For remote control with an eDAQ network, use the remote control hardware (i.e., the ECPU interface hardware) only on the master node. This applies to both the test run control input and the optional test monitoring output digital lines.

NOTE
The preview run option is not supported in remote control mode.

The slave eDAQ systems automatically start a new test run immediately after test initialization and after each test run stops, as long as the remote control is not suspended. Because of this, be careful to not start the master until the slaves are all running and waiting for the master to assert the MSR clock source. The green and yellow front panel LEDs blink in unison when the slave is in this ready state. Failure to do this prevents synchronization of the slave and master data.
The automatic test runs prevent normal actions such as removing the PC Card or ending the test after a test run stops. To perform these actions, first suspend the remote control and then stop the test. This should be done with the run control switch

on the master set in the off position so each slave increments the test run number and creates a new set of DataMode channels in the SIF file. Suspend and resume the remote control mode using the same TCE interface as a stand alone eDAQ.

NOTE
When the master eDAQ reboots after a power failure or an error reset, the system suspends the remote control mode to prevent starting a new test run on the master. In this scenario, stop all slave eDAQ systems with test runs still in progress and resume remote control on the master so that all nodes start the next test run in sync.

It is advised to experiment with using remote control for an eDAQ network and become thoroughly familiar with the details involved prior to using it in the field.

5 eDAQ Hardware

The following chapter provides details on the input and output channels and configuration options available on each eDAQ layer and module. Access the configuration options through the TCE hardware setup window by double clicking a hardware entry or highlighting an entry and selecting Config.

NOTE
For information on data synchronization across channels and hardware, see “Data Synchronization” on page 227.

5.1 ECPU (Base Processor)

The ECPU is the foundation of the eDAQ system. For more information on eDAQ capabilities contained in the ECPU such as battery power, Ethernet communications and on-board memory, see “Using the eDAQ” on page 25.

5.1.1 Available Inputs and Outputs

The ECPU is a multifunctional layer that supports two digital input modes, a digital output mode and serial bus data. Both of the digital input modes as well as the output mode can be used concurrently in a test run. An optional integral ECOM layer can be installed allowing for three dedicated CAN network interfaces, one vehicle bus module interface and a GPS communications port. For more information on the ECOM layer, see “ECOM (Vehicle Network Communications Layer)” on page 95.

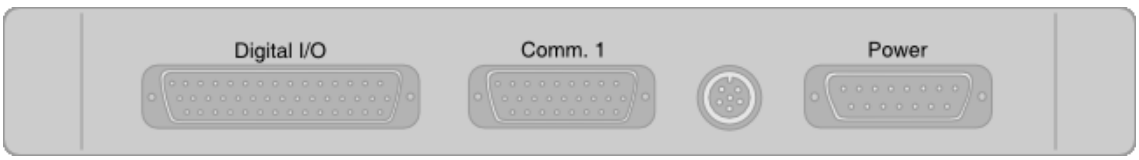


Figure 5-1: Diagram of the connectors on the back panel of an ECPU layer including the 44-pin D-Sub Digital I/O connector and the 9-pin D-Sub Comm port used for serial bus inputs.

Digital Input/Output

There are ten digital input/output lines available on the ECPU. Use TCE to configure any line as either an input or output. The input lines can be sampled individually to generate logical (i.e., Boolean) data streams for triggering or other logical operations. The output lines are updated at a low rate based on the user-defined pipe frame size and are designed to drive LED indicators, remote switches, etc. The eDAQ uses standard TTL switching logic to determine the Boolean state of the channels. Connect digital input and output channels to the eDAQ using the Digital I/O connector on the rear panel of the ECPU layer.

For more information on setting up digital inputs and outputs, see “Digital Input” on page 114 and “Digital Output” on page 177. For more information on wiring digital inputs and outputs on the ECPU layer, see “ECPU (Base Processor)” on page 215.

Pulse Counter
There are eight digital pulse counter channels available that can measure pulse width, count pulses or used in pairs to compute the duty cycle. The eDAQ uses standard TTL switching logic to determine the Boolean state of the channels. Connect pulse counter channels to the eDAQ using the digital I/O connector on the rear panel of the ECPU layer.
For more information on setting up pulse counter inputs, see “Pulse Counter” on page 115.

Serial Bus
The RS232 serial port can be configured as a data input port to acquire serial data streams from various sources. Specialized code must be written to deal with the specifics of the particular serial data streams. Therefore, serial data sources are supported on a custom basis for such things as serial GPS or customer specific vehicle buses. Refer to the installation instructions in the firmware installation directory for more information on installing custom modules. Connect serial data source to the eDAQ using the Comm connector on the rear panel of the ECPU layer.

5.1.2 Configuration Options

The ECPU offers several configuration options through the hardware setup window. The serial bus port appears as a separate entry in the hardware setup window and has its own configuration options which are identical to the vehicle bus configuration options. For more information on these options, see “Configuration Options” on page 101.

Pipe Frame Rate
Select the eDAQ test engine pipe frame rate. As data samples are collected from the transducer channels, the eDAQ places them in blocks of data (i.e., data frames) and routes (i.e., pipes) them into computed channels and DataModes. In the flow of data from the transducer inputs through the DataModes, the data frames are referred to as pipe frames.
The lowest pipe frame rate is considerably more efficient from a processing point of view when there are a large number of channels defined at lower sample rates ($\leq$ 500 Hz). Using the lowest pipe frame rate also modestly improves throughput performance for most tests with sample rates below 10000 Hz. At sample rates above 10000 Hz, a higher pipe frame rate generally results in the best throughput performance. Because TCE run-time displays run at the pipe frame rate, higher pipe frame rates may be desired.

NOTE
Select the default preference for the pipe frame rate using the FCS Specific preferences in TCE.

Enable Analog Output Inverting
Select the analog output inverting option to automatically invert the polarity of analog outputs from EHLS, EBRG and ELLB layers with the optional analog out function. Use this option in situations where the analog output polarity is opposite of the engineering units scaling polarity which is common of many transducers.

NOTE
The analog output settings are stored in nonvolatile memory and cannot be modified after test initialization.

Input/Output Configuration
Use the input/output configuration section to view or modify the current settings for each digital line. Configure a line as an input by checking the corresponding box or as an output by deselecting the corresponding box.

NOTE
The input/output settings are stored in nonvolatile memory and cannot be modified after test initialization.

PC Card Options
The PC Card options section contains four button controls for performing various tasks for the selected PC Card media.

PC Card Option	Description
Status	Display a short message detailing the eDAQ SIF component file directory status of the installed PC Card.
Purge	Purge the installed PC Card of all files. Note that purged files cannot be recovered.
Test	This function is no longer supported on the eDAQ.
Format	Open the eDAQ web interface to format the installed PC Card.

5.2 ECOM (Vehicle Network Communications Layer)

The ECOM is a multifunctional layer that supports three dedicated CAN vehicle bus sources, one generic vehicle bus module interface and a GPS communications port. The ECOM layer supports up to 254 vehicle bus channels per input. The layer comes with many predefined databases such as J1939 and OBDII. The GPS communications port is designed to work with SoMat GPS devices.

Figure 5-2: Diagram of the M8 connectors for CAN, VBM and GPS connections on an ECOM layer.

5.2.1 Available Inputs

Each vehicle bus and GPS port appears as separate hardware in the TCE hardware setup window. For more information on vehicle bus inputs and configuration options, see "Vehicle Bus Module" on page 101. For more information on the GPS module, see "EGPS-5HZ (SoMat GPS Receiver)" on page 99.

5.2.2 Configuration Options

Vehicle Bus Module Usage

The vehicle bus module usage parameter displays what type of vehicle bus module, if any, is defined in the current hardware setup.

GPS Clock Interface

Select the GPS clock interface option to open another dialog window with the enable GPS clock generation option. Select the GPS clock generation option to enable GPS-based master sample rate clock generation. Only one GPS-based clock generation source can be defined in a test setup. Define the network mode in the network setup window to either GPS master or GPS stand alone.

5.3 EDIO (Digital Input/Output Layer)

The EDIO is an extremely versatile layer that supports digital inputs and outputs, pulse counters, two vehicle bus module interfaces and optional GPS receiver.

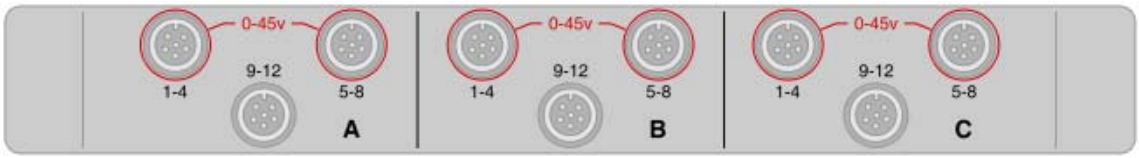


Figure 5-3: Diagram of the M8 connectors on an EDIO layer.

5.3.1 Available Inputs and Outputs

The digital I/O channels are grouped into three functionally identical banks (A, B and C). Each bank contains three connectors of four digital I/O channels (i.e., bits). The eight channels on connectors |1-4| and |4-8| are individually configurable to be either inputs or outputs. The four channels on connector |9-12| are dedicated wide-range input channels. Each connector also provides two pulse counter channels for a total of six pulse counter channels per bank.

One layer also supports up to two independent vehicle bus module interfaces and an optional GPS receiver, which appear as separate entries in the TCE hardware setup window. For more information on the GPS module, see "EGPS-5HZ (SoMat GPS Receiver)" on page 99. For more information on setting up vehicle bus modules, see "Vehicle Bus Module" on page 101.

Digital Input/Output

There are 12 digital input/output lines available for each bank on the EDIO. Use TCE to configure the lines on the |1-4| and |5-8| connectors as either inputs or outputs. The input lines can be sampled individually to generate logical (i.e., Boolean) data streams for triggering or other logical operations.

Use the EDIO bank configuration options to program the input threshold mode and limits for determining the Boolean state of the input channels. Connect channels to the EDIO using the numbered M8 connectors on the front panel of the layer.

The output lines are updated at a low rate based on the user-defined pipe frame size and are designed to drive LED indicators, remote switches, etc. Use the EDIO configuration options to set the power output at either nominal five volts or nominal 12 volts for each bank.

For more information on setting up digital inputs and outputs, see “Digital Input” on page 114 and “Digital Output” on page 177. For more information on wiring digital inputs and outputs on the EDIO layer, see “EDIO (Digital I/O Layer)” on page 216.

Pulse Counter

The pulse counter channels share the same input lines as the digital input/output channels. Two pulse counter channels are provided on each connector (|1-4|, |5-8| and |9-12|). Pulse counter channels can measure pulse width, count pulses or used in pairs as quadrature encoder inputs typically used to track angular or linear position. Connect pulse counter channels to the EDIO using the numbered M8 connectors on the front panel.

For more information on setting up pulse counter inputs, see “Pulse Counter” on page 115.

NOTE

Input bits (i.e., channels) used for pulse counters can simultaneously be used for digital input channels.

Limits on EDIO Input Voltages

The four channels on connector |9-12| on each bank of the EDIO are wide range inputs that can accept steady state voltages in the range of ±45 volts. These channels can also tolerate short duration spikes up to +100 volts (as can be encountered using inductive pickup devices).

The eight channels on connectors |1-4| and |5-8| on each bank of the EDIO are configurable as either inputs or outputs and can accept steady state voltages in the range of -0.2 to +45 volts. These channels can also tolerate short duration spikes up to +100 volts. In general, it is advised that these channels be used only with positive voltage input sources.

Exceeding the input ranges described above can result in component damage, requiring factory repair. Layer damage caused by exceeding input voltage limits is not covered by HBM warranty.

5.3.2 Configuration Options

Each bank on the EDIO layer is independently configurable. Click on the desired bank button in the configuration dialog for the specific parameters (indicated with “bank” in parentheses) available for each bank. The EDIO layer also has several configuration options for the Megadac® interface (indicated with “Megadac®” in parentheses).

Vehicle Module Usage (bank)
The vehicle bus module usage parameter displays what type of vehicle bus module, if any, is defined in the current hardware setup.

Input/Output Configuration (bank)
Configure the eight channels on connectors |1-4| and |5-8| as either inputs or outputs. Configure a line as an input by checking the corresponding box or as an output by deselecting the corresponding box. The channels on connector |9-12| are input only.

Input Threshold Mode (bank)
Select the desired mode for defining the input threshold limits. Selecting either the TTL or zero crossing options results TCE assigning specific upper and lower limits. Selecting the user defined option allows for a user-configurable upper limit.

Input Threshold Limits (bank)
When using the user-defined threshold mode, specify the upper input threshold limit to determine when an input channel switches from a logical value of TRUE to a logical value of FALSE and vice-versa. The difference between the upper and lower limits is fixed at nominal one volt. The maximum upper limit is 4.8 volts and the minimum upper limit is one millivolt.
The input threshold value assigned for any given bank applies to all input bits for that bank. Individual input bits in the same bank cannot have different input threshold values.

NOTE
If a vehicle bus module is connected, the eDAQ configures bank A with a 2500-millivolt upper input threshold.

Power Voltage (bank)
Select either the nominal 5-volt or nominal 12-volt option as the power output for digital outputs. Either voltage option can source up to one amp.

NOTE
If a vehicle bus module is connected, the eDAQ configures bank A with the 12-volt output power option.

NOTE
The 12-volt option operates correctly only if the input power to the eDAQ is about 14-15 volts. Otherwise, the output is less than 12 volts.

GPS Clock Interface
Select the GPS clock interface option to open another dialog window with the enable GPS clock generation option. Select the GPS clock generation option to enable GPS-based master sample rate clock generation. Only one GPS-based clock generation source can be defined in a test setup. Define the network mode in the network setup window to either GPS master or GPS stand alone. For more information on using GPS clock generation for wireless networking, see “Wireless Network” on page 40.

Enable Clock Generation (Megadac®)
Select the Megadac® clock generation option to enable Megadac® clock generation. Only one Megadac® clock generation source can be defined in the test setup.

Sync Delay Counts (Megadac®)
The sync delay counts parameter controls the time period that the clock generation is delayed relative to the time that the eDAQ turns on the source clock that drives data collection on both the eDAQ and the Megadac®.
For a MSR of 100 kHz, the eDAQ data collection start 1.00 seconds after the MSR clock is turned back on to start a synchronized test run. This 100 kHz clock is down sampled by ten to generate a 10000 Hz clock source for the Megadac® interface board. Therefore, if the Megadac® starts recording on the first clock pulse issued after switching to record mode, the sync delay counts should be set at the default value of 10000.
For a MSR of 98.304 kHz, the eDAQ data collection starts 1.25 seconds after the MSR clock is turned back on to start a synchronized test run. This 98.304 kHz clock is down sampled by 12 to generate a 8192 Hz clock source for the Megadac® interface board. Therefore, if the Megadac® starts recording on the first clock pulse issued after switching to record mode, the sync delay counts should be set at the default value of 8192.

NOTE
In general, the Megadac does not appear to start data collection on the first clock pulse. For accurate synchronization of eDAQ and Megadac® data, it is advised to experimentally determine the desired sync delay counts for the particular test configuration of interest.

Down Sample Factor (Megadac®)
Specify the factor by which the eDAQ down samples the MSR source clock to generate the desired Megadac® sample rate. The down sample factor can be any value in the range of 2 to 65535.

5.4 EGPS-5HZ (SoMat GPS Receiver)

The EGPS-5HZ is a commercial WAAS-enabled GPS receiver with a fixed 5 Hz navigational update rate. The receiver continuously tracks and uses up to 12 satellites to compute and update position. The receiver has a serial interface connection routed to the ECOM or EDIO rear panel.

Another feature available with the GPS receiver is GPS-based master sample rate clock generation. Use the configuration options of the parent layer (EDIO or ECOM) to enable GPS clock generation.

Notes on the Old GPS Module

The old GPS module has an antenna connection routed to the EDIO rear panel. This GPS module is a low-power consumption 12-channel GPS receiver that is WAAS-enabled. Navigational updates are fixed at a rate of 1 Hz.
At highway driving speeds, this older GPS module does not always maintain sufficient communications lock on the GPS satellites to consistently acquire GPS updates at a reasonable rate. This results in the GPS data going stale with invalid data fills brought into play. This appears to happen more frequently at highway speeds, but has been observed in other test scenarios. Furthermore, it can sometimes take a very long time for the GPS module to re-acquire satellite communications lock (several minutes in some cases).

5.4.1 Available Inputs

GPS

Available GPS channels include latitude, longitude, altitude, speed (m/s, mph or knots), heading, year, month, day, hour, minute, second, nanosecond and number of satellites. For more information on setting up GPS inputs, see “Bus-Oriented Input Channels” on page 129.

NOTE

Position accuracy varies with several factors including, but not limited to, GPS receiver configuration, location (geographic latitude, as it influences HDOP, and surrounding objects possibly blocking reception or causing multi-path reception), satellite constellation status and ionosphere conditions.

NOTE

There is an anomaly in the acquisition or processing of the GPS time that results in some small discontinuities in the absolute GPS time data. This occurs when the “nsec” channel rolls over and persists for about 20% of the time until the “nsec” channel rolls over again (which takes about 4 hours). As such, there is at least one second of uncertainty in the GPS time data stored in the data file whether or not the “nsec” channel is stored.

5.4.2 Configuration Options

Hardware Interface

Select the desired GPS hardware interface.

Databases

Select one or more database files from the presented list. The selected databases determine the channel types available when adding a GPS channel to the test setup.

5.5 Vehicle Bus Module

The ECOM and EDIO layers support vehicle bus modules (VBM). For the EDIO, only connectors |1-4| and |5-8| on bank A support a VBM. Use a SAC-EXT-VB Extension Cable (1-SAC-EXT-VB-2) to connect the VBM and eDAQ-. If using an additional extension cable, make sure the cable connected directly to the eDAQ is the SAC-EXT-VB cable. Keep cabling less than 30 meters in length to avoid transmission failures.

Plug in the VBM with the eDAQ power off. When power is supplied, the eDAQ recognizes the VBM during boot up. Each VBM supports one type of vehicle bus hardware interface. The available VBMs are:

- CAN
- J1850 VPW
- J1708
- ISO9141/KWP2000

NOTE

To use a VBM on the eDAQ EDIO layer, first install a special version of the layer firmware. Refer to the firmware installation instructions in the installation directory for specific details. When the VBM firmware is loaded, pulse counter channels on bank A are not available.

5.5.1 Available Inputs

Vehicle Bus

Each vehicle bus module supports up to 254 channels. The available channels depend on the vehicle bus type and the selected databases. When the eDAQ receives vehicle bus message packets, they are time stamped, processed into individual data streams and re-sampled as necessary to the user-selected output rate. For more information on setting up vehicle bus inputs, see “Bus-Oriented Input Channels” on page 129.

Vehicle Bus Message

A vehicle bus message channel acquires raw vehicle bus packets. Every packet is time stamped upon receipt and can subsequently be stored in the specialized Message Logger DataMode. For more information on setting up vehicle bus message inputs, see “Vehicle Bus Message Channel” on page 131.

5.5.2 Configuration Options

NOTE

These configuration options also apply to the serial bus port, the dedicated CAN interface on the ECOM layer and the EHLS vehicle bus sub-layer.

Hardware Interface

Select the desired vehicle bus hardware interface.

Databases
Select one or more database files from the presented list. The selected databases determine the channel types available when adding a vehicle bus channel to the test setup.

Hardware Specifics
Configure parameters that are applicable to specific vehicle bus hardware interfaces.

Option	VB Interface(s)	Description
Baud Rate	CAN, PWM, ISO9141/KW2000	Specify the desired baud rate.
Transducer Power	ECOM dedicated CAN ports only	Specify the desired transducer power in the range of 3 to 24 volts (±10%)
Internal Termination	CAN	Select to provide internal vehicle bus termination.

Disable Active Querying
Select the disable active querying option to disable active querying for all vehicle bus input channels.

Max Rate
If the disable active querying option is not selected, specify the maximum active query rate which overrides any higher query rates defined in the individual vehicle bus input channel setups.

Override Database Definitions
Select the override database definitions option to modify the default source address (i.e., vehicle bus node address).

Source Address
If the override option is selected, specify the desired source address byte in hexidecimal format.

5.6 EBRG (Bridge Layer)

The EBRG offers 16 simultaneously sampled, low-level, differential analog inputs through independent connectors. The EBRG layer works with both amplified and unamplified transducers including strain gauges, accelerometers, pressure transducers, load cells and other general analog signals. Connect transducers to the EBRG individually using the M8 connectors located on the front panel.

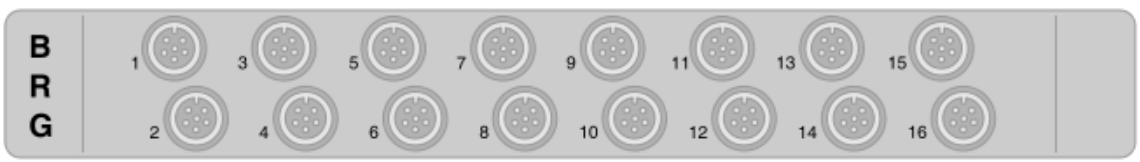


Figure 5-4: Diagram of the M8 connectors on an EBRG layer.

Each independent channel contains programmable excitation, an eight-pole Butterworth analog guard filter, a 16-bit A/D converter, software selectable digital filtering and output sample rate options of up to 100 kHz.

The EBRG layer supports full- and half-bridge types with a resistance from 100 to 10000 ohms and quarter-bridges with a resistance of either 120 or 350 ohms. All bridge configurations are accomplished using programmable switches (i.e., there are no jumpers), however, the quarter-bridge choice of 120- or 350-ohm completion resistor is a factory installed option. A set of internal shunt resistors with selectable shunt direction is available for calibration purposes.
For more information on setting up EBRG input channels, see “Bridge” on page 117.
For information on wiring EBRG inputs, see “EBRG (Bridge Layer)” on page 220.

MSBRG.01 Limitations on the Use of Full Bridges

The MSBRG.01 version of the EBRG layer cannot provide sufficient current to drive 16 full 120-ohm bridges with the eDAQ power source below 15 volts or to drive 16 full 350-ohm bridges with the eDAQ power source below 11 volts. A terse summary of currently known limitations based on limited testing is below.

- 16 full 120-ohm bridges OK at 15.0-volt eDAQ power
- 15 full 120-ohm bridges OK at 13.5-volt eDAQ power
- 13 full 120-ohm bridges OK at 10.0-volt eDAQ power
- 15 full 350-ohm bridges OK at 10.0-volt eDAQ power
- 16 full 350-ohm bridges OK at 11.0-volt eDAQ power

Analog Output

The EBRG is available with an optional analog output function to provide high level analog output signal for each channel. Outputs are filtered analog output signals that can be used in the creation of time-domain lab durability tests. Each output channel is associated with the corresponding (like-numbered) input channel on the EBRG board. Connect the analog outputs to the EBRG through the Analog Output connector on the back panel shown in the diagram below.

Figure 5-5: Diagram showing the analog out connector on the back panel of an EBRG layer.

The outputs are generated from a D/A converter implemented as a unity gain follower to the A/D converter. The eDAQ uses the non-inverting unity gain follower by default. Select the analog output inverting option in the ECPU hardware configuration to use the inverting unity gain follower.

NOTE

The EBRG uses a nominal ±2-volt A/D converter. However, do not assume that the user-defined full-scale values are even approximately equivalent to ±2 volts for any particular channel. This is primarily because TCE automatically provides a minimum overrange protection of 1% and the eDAQ can set gains only at certain discrete values resulting in actual overrange protection that is sometimes significantly larger than 1%.

TCE provides the option to generate an AOM calibration file which is an ASCII file containing all of the information required to scale the analog output signal voltages to equivalent engineering values. The file also includes SIE or SIF file analog output scale and offset keywords for each channel stored in a Time History DataMode. Select Save AOM File from the Test Control menu to generate the file. For more information on the AOM file, see “AOM Calibration File” on page 72.

5.7 EHLS (High Level Analog Layer)

The EHLS offers 16 simultaneously sampled, high-level, differential analog inputs through independent connectors. The EHLS layer supports a wide variety of inputs including thermocouples, strain gages, accelerometers, microphones and amplified and unamplified transducers. Single channel IEPE (Integral Electronics Piezoelectric) adapters and a variety of SMART modules are also available. Connect transducers to the EHLS individually using the M8 connectors located on the front panel.

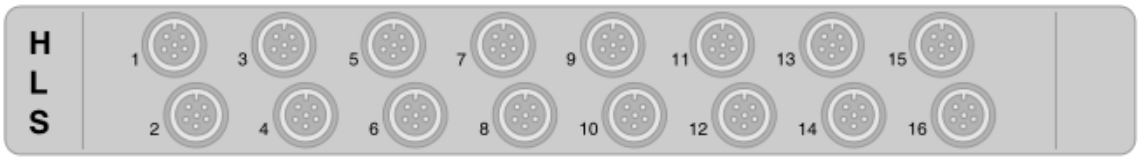


Figure 5-6: Diagram of the M8 connectors on an EHLS layer.

Each independent channel contains programmable transducer power, an eight-pole Butterworth analog guard filter, a 16-bit A/D converter, software selectable digital filtering and output sample rate options of up to 100 kHz. The EHLS also provides 400 milliwatts of transducer power supply with an adjustable supply voltage of 3-28 volts for every channel. Use the transducer power supplies in parallel for larger loads. For more information on setting up EHLS input channels, see “Simultaneous High Level” on page 120. For information on wiring EHLS inputs, see “EHLS (High Level Analog Layer)” on page 218.

NOTE

The analog guard filters on the EHLS channels result in some gain amplification for high frequency inputs. For more information, refer to the EHLS data sheet.

Analog Output

The EHLS is available with an optional analog output function to provide high level analog output signal for each channel. Outputs are filtered analog output signals that can be used in the creation of time-domain lab durability tests. Each output channel is associated with the corresponding (like-numbered) input channel on the EHLS board. Connect the analog outputs to the EHLS through the Analog Output connector on the back panel shown in the diagram below.

Figure 5-7: Diagram showing the analog out connector on the back panel of an EHLS layer.

The outputs are generated from a D/A converter implemented as a unity gain follower to the A/D converter. The eDAQ uses the non-inverting unity gain follower by default. Select the analog output inverting option in the ECPU hardware configuration to use the inverting unity gain follower.

NOTE
The EHLS uses a nominal ±2-volt A/D converter. However, do not assume that the user-defined full-scale values are even approximately equivalent to ±2 volts for any particular channel. This is primarily because TCE automatically provides a minimum overrange protection of 1% and the eDAQ can set gains only at certain discrete values resulting in actual overrange protection that is sometimes significantly larger than 1%.

TCE provides the option to generate an AOM calibration file which is an ASCII file containing all of the information required to scale the analog output signal voltages to equivalent engineering values. The file also includes SIE or SIF file analog output scale and offset keywords for each channel stored in a Time History DataMode. Select Save AOM File from the Test Control menu to generate the file. For more information on the AOM file, see “AOM Calibration File” on page 72.

5.8 SMART Modules

SMART module adapters act as an interface between a transducer and an EHLS input channel which powers the module. Each SMART module provides specialized signal conditioning as a front end to the EHLS signal conditioning and includes independent self-identification capabilities and self-calibration parameters. The following table lists the available SMART modules.

SMART Module	Order Number	Description
SMSTRB4 Strain SMART Module	1-SMSTRB4-120-2 or 1-SMSTRB4-350-2	The SMSTRB4 supports full-, half- and quarter- bridge transducers and includes 5- and 10-volt excitation options and internal shunt calibration using either 50- or 100-kilohm shunt resistors with both upscale and downscale shunting options.
SMITC Thermocouple SMART Module	1-SMITC-2	The SMITC supports fully-isolated thermocouples of type J, K, T or E over the full temperature range of the thermocouple.

For more information on setting up SMART module input channels, see “SMART Module Input Channels” on page 125. For information on wiring SMSTRB4 inputs, see “SMSTRB4 (Strain SMART Module)” on page 218.

Installation

The eDAQ does not sense when a SMART module is installed or removed. After connecting a module, either cycle the eDAQ power or perform a hardware query to detect the installed SMART module. In both of these cases, the eDAQ applies power and sends a query to all EHLS channels that support SMART modules. Note that the SMART modules remain in a default configuration until an action such as starting a

DVM display, performing a calibration or initializing a test. This also means that a configured SMART Module that is removed and reinstalled reverts to an unconfigured state until one of these same actions.

Flash Memory
All SMART modules have three logical segments of flash memory. Two are reserved for factory use; one to store the microprocessor execution code and the other to store serial number and factory calibration parameters. The third area is the user data segment broken into two logical partitions.

1. The first partition holds TCE parameters that can completely configure the TCE transducer channel setup when the SMART module is installed. If no information exists in this partition, TCE sets up the transducer channel in a default mode when the module is added.
2. The second partition is designed for pass-through information not used by TCE. Add any desired information such as physical locations of transducers or associated vehicle or system indentifications. All pass-through keywords must start with the prefix “UI_” (“UI” followed by the underscore character).

5.9 ENTB (Non-Isolated Thermocouple Layer)

The ENTB provides non-isolated thermocouple inputs in two banks (A and B) of 16 channels. The ENTB supports the four most common thermocouple types: J, K, T and E. The user-specified thermocouple type for each channel is independent of the other channels. The 16 channels of each bank share a common cold junction resulting in high channel-to-channel accuracy, which is particularly valuable when measuring thermal gradients.

Figure 5-8: Diagram of the 37-pin D-Sub connectors on an ENTB layer.

Each channel uses a notched filter processor that generates about seven samples per second. Since these channels are not isolated from each other, they can only be used in applications where the individual thermocouples are electrically isolated from each other. A cold junction box is required for each bank and is connected to the eDAQ with the cables provided using the connectors labeled “A01-A16” or “B01-B16” located on the front panel. Each thermocouple is connected to the miniature barrier strip type paired inputs in the junction box.

NOTE
Thermocouple leads should not exceed 30 meters in length from connector to tip.

The eDAQ uses the industry standard software compensation algorithm to generate the temperature data samples. The eDAQ first measures the cold-junction compensation (CJC) temperature and converts it to the equivalent microvolt value using a high-resolution lookup table. The eDAQ then subtracts the CJC equivalent

microvolt value from the thermocouple's output microvolt value. The temperature is found using another high-resolution lookup table. The lookups are based on the ITS-90 Thermocouple Direct and Inverse Polynomials.
For more information on setting up ENTB input channels, see "Thermocouple" on page 128.

Application Note on Measuring Differential Temperatures

To measure differential temperatures using the ENTB layer, select two or more adjacent channels on the same bank. Use matched thermocouples for optimum differential accuracy.
Due to instrumentation noise, it is recommended that the maximum sample rate (e.g., 5 Hz for the 100 KHz MSR option) and a Smoothing Filter computed channel be used for each input channel. Using a five- or seven-tap Smoothing Filter typically reduces the instrumentation noise to below 0.2° C peak to peak (for all thermocouple types). Using more taps can further reduce the noise.
To generate the differential temperature, use a simple Desk Calculator computed channel. Use a Down Sampler computed channel to achieve the desired data storage rate.

5.10 EITB (Isolated Thermocouple Layer)

The EITB provides eight channels of isolated thermocouple signal conditioning. The EITB is factory-configured for J, T, E or K type thermocouples and is operational over the full range of the thermocouple. Each channel has individual cold junction compensation and a notched filter processor that generates about seven samples per second. Each channel is also isolated from the other channels to 500 volts, which allows the thermocouples to be attached to structures that have large differences in ground potential. The thermocouples are connected to the eDAQ using the standard Omega miniature thermocouple connectors located on the front panel.

NOTE
Thermocouple leads should not exceed 30 meters in length from connector to tip.

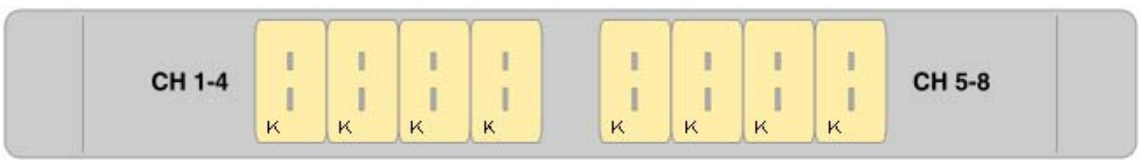


Figure 5-9: Diagram of the thermocouple connectors on an EITB layer configured for K-type thermocouples.

The eDAQ uses the industry standard software compensation algorithm to generate the temperature data samples. The eDAQ first measures the cold-junction compensation (CJC) temperature and converts it to the equivalent microvolt value using a high-resolution lookup table. The eDAQ then subtracts the CJC equivalent microvolt value from the thermocouple's output microvolt value. The temperature is found using another high-resolution lookup table. The lookups are based on the ITS-90 Thermocouple Direct and Inverse Polynomials.

For more information on setting up EITB input channels, see “Isolated Thermocouple” on page 128.

5.11 EHLB (High Level Layer)

NOTE
The EHLB is no longer in production.

The EHLB provides 16 single-ended analog channels for high level transducer inputs with full-scale input ranges independently set to either ±10 or ±20 volts. The 16 channels are multiplexed into a 16-bit A/D converter with a channel to channel skew of approximately 25 microseconds. Connect transducers to the eDAQ using the connector labeled “HiLev (1-16)/Veh. Bus” located on the front panel.
The EHLS layer also supports an optional vehicle bus sub-layer. For more information on vehicle bus configuration options, see “Configuration Options” on page 101.
For more information on setting up EHLB input channels, see “High Level” on page 122. For information on wiring EHLB inputs, see “EHLB (High Level Layer)” on page 221.

5.12 ELLB (Low Level Layer)

NOTE
The ELLB is no longer in production.

The ELLB provides eight analog channels of low level signal conditioning and supports a differential amplifier mode as well as full, half, and quarter bridge modes (selectable on a channel by channel basis). Connect transducers to the eDAQ using the connectors labeled “LoLev (1-4)” and “LoLev (5-8)” located on the front panel. A four-channel ICP accelerometer adapter module is also available for use with a single bank of low level channels. A maximum of 2 modules can be used with each ELLB.
The ELLB layer conditions each of the eight input signals by means of programmable excitation circuitry, a five-pole Butterworth analog guard filter, programmable amplifier gain and offset, 16-bit A/D converter sampling at 10000 Hz (or 8192 Hz) with simultaneous sampling for all eight channels, programmable digital filters and the output sample rate achieved by means of multiple stages of combined down sampling and digital filtering.
The ELLB layer supports full and half bridge types with a resistance from 100 to 10000 Ω and quarter bridges with a resistance of either 120, 350, or 1000 Ω. All bridge configurations are accomplished using programmable switches (i.e., there are no jumpers), however, the quarter bridge choice of 120-, 350-, or 1000-Ω completion resistor is a factory installed option. A set of internal shunt resistors with selectable shunt direction is available for calibration purposes.

For more information on setting up ELLB input channels, see “Low Level” on page 122. For information on wiring ELLB inputs, see “ELLB (Low Level Layer)” on page 222.

NOTE
The input impedance of the low level input channels is dependent on the excitation voltage. Signals with voltages greater than the excitation amplitude can be dragged down due to very low input impedance (on the order of 100 Ω). For example, if the excitation is set to the 10-volt range option (i.e., bipolar ±5 volt excitation), then any signal voltages beyond approximately ±6.0 volts are dragged down significantly. Since the excitation is set to 0 range on power up (or reset), then any signal voltages beyond approximately ±1.0 volts are dragged down significantly until the user-specified excitation is applied.

Analog Output
The ELLB is available with an optional analog output function to provide high level analog output signal for each channel. Outputs are filtered analog output signals that can be used in the creation of time-domain lab durability tests. Each output channel is associated with the corresponding (like-numbered) input channel on the ELLB board. The outputs are generated from a D/A converter implemented as a unity gain follower just before the A/D converter. The eDAQ uses the non-inverting unity gain follower by default. Select the analog output inverting option in the ECPU hardware configuration to use the inverting unity gain follower.

NOTE
The ELLB uses a nominal ±10-volt A/D converter. However, do not assume that the user-defined full-scale values are even approximately equivalent to ±10 volts for any particular channel. This is primarily because TCE automatically provides a minimum overrange protection of 1% and the eDAQ can set gains only at certain discrete values resulting in actual overrange protection that is sometimes significantly larger than 1%.

TCE provides the option to generate an AOM calibration file which is an ASCII file containing all of the information required to scale the analog output signal voltages to equivalent engineering values. The file also includes SIE or SIF file analog output scale and offset keywords for each channel stored in a Time History DataMode. Select Save AOM File from the Test Control menu to generate the file. For more information on the AOM file, see “AOM Calibration File” on page 72.

6 Input Channels

This chapter details all of the available input channels and their parameters. To acquire data during a test, define input channels for each input signal in the transducer setup window. Input channels can be transducer channels, message channels or data channels derived from various message-oriented data sources. Each channel definition contains some common information such as the ID tag, the hardware connector ID, output data type, desired full-scale range and output sample rate. In addition, each channel type has specific parameters that must be defined.

6.1 Common Input Channel Parameters

6.1.1 Desired Measurement

ID
Specify a unique identifier for the channel. The name must conform to ID naming conventions. Valid ID names:

- are case sensitive
- are limited to a maximum of 12 characters
- contain only valid characters (i.e., letters (a-z, A-Z), digits (0-9), and the underscore (_) character)
- start with a letter
- are not duplicates of system reserved names (sin, cos, log, etc.)

Connector
Hardware connector IDs identify connector assignments for transducers. The default ID consists of the eDAQ IP address or host name, layer identifier and the physical/logical channel as specified in the hardware setup. The following examples illustrate the eDAQ conventions.

- ECPU: Connector IDs MPB.c01 through MPB.c08 denote the eight pulse counter transducer channels and MPB.bwi denotes the set of digital inputs.
- EBRG: For an EBRG layer with an ID of Brg_1, connector IDs Brg_1.c01 through Brg_1.c16 denote the set of 16 bridge transducer connections.
- EDIO: For an EDIO layer with an ID of DIO_1, connector IDs DIO_1.apc1 through DIO_1.apc6 denote the set of 6 pulse counter connections on Bank A and DIO_1.bpc1 through DIO_1.bpc6 denote the set of 6 pulse counter connections on Bank B.

Description
Use up to 63 characters to more fully identify the transducer.

Type
Specify the type of measurement, such as strain, load or acceleration, associated with the transducer or computed channel. Select a type from the list or directly enter a user-defined type. Since TCE uses the value of the type field throughout the test setup process, always complete this field.

Units
Specify the measurement units for the transducer. Since TCE uses the value of the units field throughout the test setup process, always complete this field.

6.1.2 Output Sample Rate

Output Sample Rate
Select the sample rate for the input channel. The sample rate options are factors of the defined master sample rate (100 kHz or 98.04 kHz). The sample rate should be at least two times the maximum frequency content of the input signal to ensure that the bandwidth of the signal is completely characterized. When available, using a digital filter can limit the frequency content of the input signal.

6.1.3 Full-Scale Values

Full-Scale Min and Max
Specify the expected extreme values for the transducer. When storing a 32-bit float in a DataMode that uses an integer data type, the eDAQ uses the full-scale limits when converting from the floating point format to the integer format. The eDAQ also uses the full-scale estimates to set the default bin boundaries for histogram DataModes and to set the scales for run-time displays.
Input channels on layers that have programmable gain and offset capabilities use the full-scale values in conjunction with the calibration parameters to determine the gain and offset values. The eDAQ provides some over range protection of 1% on EHLS and EBRG channels and 5% on ELLB channels. For example, specifying full-scale values of ±2000 microstrain on an EHLS channel causes the eDAQ to set up the gain and offset circuitry as close as possible to ±2020 microstrain without going under.

6.1.4 Output Data Type

Output Data Type
Depending on the channel type, the eDAQ provides several data type options. When choosing the data type, consider factors such as data resolution, mass storage consumption and what computed channels or DataModes use the channel as an input. For a summary of the compatible data types for all computed channels and DataModes, see “Data Types” on page 195.

NOTE
The Engineering Scaler computed channel generates a 32-bit floating point output data stream from an integer type input channel. This permits storing data in an integer format to minimize data storage consumption while still using the data in a computed channel which requires a 32-bit floating point input data type. For more information on the Engineering Scaler computed channel, see “Engineering Scaler” on page 139.

6.1.5 Calibration Table

The calibration area of parameters includes the fields necessary to set up a calibration for an input transducer. Some transducer types have extra options not covered in this section. For more information on calibrating transducers, see “Calibrating Input Channels” on page 67.

Mode
Select the desired calibration mode.

Engineering Value
Specify the calibration value in engineering units.

Input Signal Value
Specify the corresponding signal value for the defined value and defined span calibration modes.

Calibrate
Select calibrate to begin calibration for the selected channel. If the transducer is already calibrated, TCE presents more calibration options.

NOTE
Calibration is only available for defined channels on a connected eDAQ.

Calibration Date
TCE automatically enters the calibration date upon transducer calibration.

6.1.6 Prerun Rezero

Mode
Select the prerun rezero mode for the transducer. Interactive rezeroing is available for all modes except “Not applicable.” Prerun rezeroing does not affect the fundamental transducer calibration definition. Prerun zero offsets are effective for the duration of the test only.

NOTE
The eDAQ never performs rezeroing on test runs started after a reset caused by an exception error (e.g., Timeout, Calibration or DeviceOverFlow).

Mode	Description
Not applicable	No rezeroing required.
Interactive only	Rezero interactively only (no automatic rezeroing).
First run only	Automatically rezero immediately prior to the start of the first test run only.
All runs (except power fails)	Automatically rezero immediately prior to the start of every test run except test runs initiated by eDAQ power fail resets.
All runs	Automatically rezero prior to the start of every test run. This option is not advised for low level inputs.

Value
Specify the engineering value associated with the transducer when rezeroed.

NOTE
There is a limitation on rezeroing low level signal conditioners when using high level input levels. If the rezero results in the situation where the full-scale values exceed the voltage limits of the signal conditioner, a calibration error occurs before the test run starts. For example, suppose the full-scale values are ±10.0 volts for a signal conditioner with a range of ±10.2 volts. If the rezero offset is 0.5 volts, the eDAQ attempts to set limits of -9.5 and +10.5 volts causing a calibration error to occur because the +10.5 volt limit cannot be achieved.

NOTE
For quadrature decoder channels, the eDAQ resets the internal counter value to zero before rezeroing.

6.1.7 Display Control

Scope
Select the Scope button to open a scope plot display for the input channel. Note that the Scope Plot is similar to an analog oscilloscope except that the display is not updated until the eDAQ acquires all of the data samples and transferred them to the host computer, which creates a delay in the data presentation. For more information on the scope plot, see “Scope Plot” on page 81.

DVM
Select the DVM button to open a DVM display of the input channel. In this display mode, the transducer signals are repetitively sampled and displayed in a digital format. For more information on the DVM display, see “DVM” on page 80.

6.2 Digital Input Channels

6.2.1 Digital Input
Add a digital input channel to any bit on an EDIO or ECPU layer. The eDAQ uses standard switching logic to determine the boolean state of the channels. For more information on EDIO digital inputs, see “Digital Input/Output” on page 97. For more information on ECPU digital inputs, see “Available Inputs and Outputs” on page 93.

NOTE
The last four bits (9-12) on each EDIO bank are dedicated to wide range input channels.

Output Data Type
The output data type for digital inputs is always 8-bit unsigned (logical).

6.2.2 Pulse Counter

For the ECPU, add a pulse counter channel to any input bit. Note that the duty cycle mode requires two adjacent input bits (i.e., 1-2, 3-4, 5-6 or 7-8) for each duty cycle pulse counter. The input signal must be physically connected to the odd numbered input connector pin only (i.e., 1, 3, 5 or 7).

For the EDIO, the eDAQ allows two pulse counter channels on each of the three connectors (i.e., bits |1-4|, |5-8| and |9-12|) on each EDIO bank (i.e., A, B and C). Note that the quadrature decoder mode requires two adjacent input bits (i.e., 1-2 or 3-4 for the first connector) and the odd numbered input connector pin is typically designated encoder output A, while the even numbered input connector pin is typically designated encoder output B.

For EDIO pulse counters, the connector selection is different from other input channels. For each pulse counter, select the EDIO layer from the board drop down list, bank and connector using the corresponding radio button and input bit from the provided drop down list.

For more information on ELDIO pulse counters, see “Pulse Counter” on page 97. For more information on ECPU pulse counters, see “Available Inputs and Outputs” on page 93.

NOTE

Because the duty cycle (ECPU) and quadrature decoder (EDIO) modes require two input bits, it is recommended to define these pulse counter first before other types of pulse counter channels.

Output Data Type

Select an output data type of 32-bit float, 32-bit unsigned or 32-bit integer. The 32-bit float data type allows any of the operational modes. The 32-bit unsigned type limits the available operational modes to time period, on time and pulse rate while the 32-bit integer type is available only with the quadrature decoder mode. The 32-bit unsigned and integer data types are considerably more efficient from a processing point of view.

NOTE

If the quadrature decoder input channel is expected to exceed about 16000000 counts then using the 32-bit integer data type is required since the 32-bit float data type starts to lose resolution around this count. To put this in some perspective, a 2048 counts per revolution quadrature encoder on a shaft rotating at 3000 RPM accumulates 16000000 counts in about 2.5 hours; however, it takes about 350 hours to accumulate 2147483647 counts, the maximum value of the 32-bit integer data type.

Mode

There are several operational modes available for the pulse counter channel.

Mode	Description
Pulse Time Period	Output the pulse period in microseconds. The unsigned 32-bit counter can measure pulse widths from 200 nanoseconds to approximately 850 seconds. Because this mode is the most efficient from a processing point of view, consider using it for measuring the same types of parameters as the frequency mode when the eDAQ is near its performance limit or when post test processing can perform the calculations.
Pulse Frequency	Output the instantaneous frequency of the input signal computed as the reciprocal of the period between the last two falling edges of the signal. Use this mode for applications including measuring vehicle speed and engine RPM. The output data type must be 32-bit float. For important application information, see "Pulse Frequency Mode Notes" on page 116.
Pulse Rate	Output the number of pulse counts in one sample period in units of pulses per second (Hz). Use this mode in conjunction with the Integrator computed channel to measure accumulated pulse counts or other parameters that are directly proportional to accumulated pulse counts (such as distance traveled, revolutions, etc.). The eDAQ can accumulate over 4 billion counts in each sample period; however, the maximum pulse rate is limited to approximately 1.0 MHz.
Duty Cycle (ECPU only)	Output the duty cycle as a dimensionless ratio. Use this mode for specialized transducers that generate output pulse trains where the duty cycle of the pulses is directly proportional to the desired measurement. The effective working range for this mode is nominally 0.5 Hz to 50 kHz. However, since there are two inputs with accuracy limitations, use this mode only for pulse trains running at 20 kHz or less for the best results.
Pulse On Time Period (EDIO only)	Output the time period in microseconds that the pulse is at logic 1. The unsigned 32-bit counter can measure pulse on time widths from 200 nanoseconds to approximately 850 seconds. Use a Desk Calculator computed channel (see "Desk Calculator" on page 136) to compute duty cycle as the pulse on time period divided by the pulse time period.
Quadrature Decoder (EDIO only)	Output the encoder position in terms of the accumulated encoder counts. The signed 32 bit counter can accumulate over 2 billion counts in either direction before the counter rolls over.

Pulse Frequency Mode Notes

Consider the following when using a pulse counter in frequency mode.

- The effective working range for the ECPU in this mode is nominally 0.5 Hz to 50 kHz. Because the EDIO uses a 32-bit counter instead of a 24-bit counter used by the ECPU, it has an effective working range in this mode of less than 0.002 Hz.
- The accuracy of the frequency measurement is inversely proportional to the measured frequency. For example, at a frequency of 50 kHz, 100 counts are accumulated in the counter resulting in a 1.0% measurement accuracy; at a frequency of 5 kHz, 1000 counts are accumulated in the counter resulting in a 0.1% measurement accuracy.
- When the input signal pulse frequency is greater than the sample rate, the eDAQ latches the first pulse frequency measured until it reads the value effectively ignoring subsequent pulses that occur in the sample period after the latched pulse. When the input signal pulse frequency is less than the sample rate, the eDAQ uses the stored pulse frequency for the previous output sample.

- When the input signal pulse train stops for an extended period of time, the following occurs. For the ECPU counters, the 24-bit register saturates in about 3.3 seconds. When this occurs, the saturation frequency of about 0.3 Hz is latched and output until the pulse train starts again. The EDIO counters use 32-bit registers, which saturate in about 850 seconds and keep track of the last output pulse period value and the time elapsed since the last pulse was detected. If sufficient time passes with no new pulse detected, the output is adjusted downward to account for the fact the pulse period is greater than what was previously latched. This results in the output pulse frequency value continuously decaying until a new pulse is detected.

High Frequency Inputs in the Pulse Rate Mode

Use the pulse rate mode to cover the high frequency input range that cannot be accurately covered using the frequency or time modes (i.e., 50 kHz to 1 MHz). The resolution of the average input frequency is equal to the input sample rate. For example, for an input with a 100 Hz sample rate and 6543 pulses in one sample period, the average input frequency over the sample period is 654300 Hz (i.e., the resolution is 100 Hz). To make use of the pulse rate mode, the channel must have a large number of pulses in each sample period.

To cover both low and high frequency inputs, route the input signal into two pulse counter channels—one configured in frequency mode and the other in rate mode—and use the following expression in a Desk Calculator computed channel (see “Desk Calculator” on page 136).

(X_r > R_max) * X_r + (X_r <= R_max) * X_f

where, X_r is the rate mode, X_f is the frequency mode and R_max is the crossover point where X_r is used instead of X_f. Set R_max to minimize accuracy loss. For example, if the sample rates are both 100 Hz, then set R_max to 25000 Hz, where the accuracy of X_f is 0.5% and the accuracy of X_r is 0.4%.

6.3 Analog Input Channels

6.3.1 Bridge

Add a bridge channel to any EBRG connector. For more information on the EBRG layer, see “EBRG (Bridge Layer)” on page 102.

NOTE

Each channel on the EBRG layer can have an independent sample rate and digital filter selection.

Output Data Type

Select an output data type of 16-bit signed, 32-bit float or 8-bit signed. The fundamental data type for bridge channels is 16-bit signed, which consumes the least amount of data storage while maintaining full 16-bit data resolution. The 32-bit float data type adds a great deal of computational overhead and is not recommended for high rate data collection. Use the 32-bit floating point option only if the input channel is to be used in subsequent computed channels or DataModes that require the input channels to be 32-bit floating point. The 8-bit signed data type adds some computational overhead, but may be useful when only a rough picture of the transducer data is required and/or data storage limitations are a major concern.

Digital Filter Type
Select the desired type of digital filtering for the channel. Digital filters ensure that aliasing of the input signal does not occur. Always use a digital filter unless absolutely certain of the frequency content of the input signal. The filter options are an eight-pole Butterworth filter or a linear phase filter. For more information on digital filtering, see “Digital Filtering” on page 233.

Break Frequency
Specify the break frequency in hertz for the selected digital filter. For a Butterworth filter, this is the approximate frequency at which the signal attenuation is 3 dB or 70.7% of the unfiltered signal voltage at that frequency. For a linear phase filter, the field is named the roll off start frequency and is the approximate frequency at which the signal starts to attenuate.
The eDAQ automatically selects a default break frequency value to ensure that no aliasing occurs. The selection is based on the A/D converter rate and the choice of digital filter type.

NOTE
The check box field labeled “data is protected from aliasing” indicates whether the current digital filter selection ensures no aliasing. TCE automatically updates the field when the digital filter configuration changes. For example, the 100-kHz sample rate option precludes aliasing because it is well over the Nyquist frequency of two times the 25 kHz analog guard filter. However, the 50-kHz sample rate option does not fully preclude against aliasing because the guard filter only attenuates about 30% of the 25-kHz input signal content.

Excitation Range
The excitation range setting determines the magnitude of the bipolar voltage applied to the red +EXC and black -EXC wires of the transducer cables. Note that a range of *X* volts DC results in +*X*/2 to -*X*/2 pin out voltages. Select one of the following discrete ranges: 10, 5, or 0 volts DC. The maximum current which can be supplied is 51 milliamps at either 5 or 10 volts DC.
If signal excitation is required for the transducer, which is always the case when using an actual bridge, consult the transducer manufacturer's specifications and/or suggestions for excitation settings. If signal excitation is not required for a particular transducer, leave the excitation in the default initial state and set the excitation proportional parameter to no.

NOTE
For the BRG.01 models, all channels must have the same excitation voltage for any given bridge layer. For the BRG.02 models and later, all channels in any given bank of four channels (1-4, 5-8, 9-12 and 13-16) must have the same excitation voltage.

Bridge Type
Select the bridge type to match the transducer or select the differential amplifier option if the transducer does not use a bridge. The available types are full bridge, half bridge, quarter bridge and differential amplifier.

Output Proportional to Excitation
Select the proportional excitation option if the output signal is linearly proportional to the applied excitation signal as it is for bridge type transducers. When using this option, the eDAQ makes a minor correction for the fact that the set excitation voltage cannot be exact.

Bridge Resistance
For quarter bridge configurations, the value defaults to the provided completion resistor. If necessary, modify the value if the actual strain gage has a slightly different resistance. For either full or half bridge configurations, select any resistance in the range of 100 to 10000 ohms.

Gage Factor
Define the gage factor for the specific strain gages used. TCE uses this value only in the shunt tool calibration option that defines an equivalent strain based on the gage factor and bridge factor values.

Bridge Factor
Define the bridge factor for the specific configuration of strain gages used. TCE uses this value only in the shunt tool calibration option that defines an equivalent strain based on the gage factor and bridge factor values. The bridge factor is defined here as the arithmetic sum of the active bridge legs for any bridge configuration. For quarter-bridge applications, the bridge factor is normally one; for half-bridge applications where both active gages are additive, it is normally two; and for full-bridge applications where all active gages are additive, it is normally four. Because there are special applications where the bridge factor can be a fraction and/or a negative value TCE considers any nonzero value valid.

Leadwire Resistance Correction
Select the leadwire resistance correction option to compensate for leadwire resistance effects when using the defined span or external span calibration modes.

NOTE
The eDAQ always performs leadwire resistance correction for shunt calibrations.

Leadwire Resistance
Specify the value of the leadwire resistance when using the leadwire resistance correction option. The resistance input is the resistance of one lead, ideally measured from the EBRG layer connector pin to the connection at the active bridge leg. It is presumed that all lead wires are approximately the same length. Quarter-bridge applications require the use of all three wires.

To accurately measure the leadwire resistance, use the four-wire resistance measurement method. Nominal resistance values for transducer cable wires can help to estimate the leadwire resistance (see “Cable Resistances” on page 245). However, since contact resistances at mechanical connections are difficult to estimate, measure the leadwire resistance for optimum accuracy.

Resistor to Shunt Across
Select either the upscale (-Sig to -Ex) shunt option or the downscale (-Sig to +Ex) shunt option. Note that the downscale shunt option results in a negative span signal value.

6.3.2 Simultaneous High Level

Add a simultaneous high level input to any EHLS connector. For more information on the EHLS layer, see “EHLS (High Level Analog Layer)” on page 104.

NOTE
Each channel on the EHLS layer can have an independent sample rate and digital filter selection.

Output Data Type
The fundamental data type for EHLS channels is 16-bit signed, which consumes the least amount of data storage while maintaining full 16-bit data resolution. The 32-bit float data type adds a great deal of computational overhead and is not recommended for high rate data collection. Use the 32-bit floating point option only if the input channel is to be used in subsequent computed channels or DataModes that require the input channels to be 32-bit floating point. The 8-bit signed data type adds some computational overhead, but may be useful when only a rough picture of the transducer data is required and/or data storage limitations are a major concern.

Digital Filter Type
Select the desired type of digital filtering for the channel. Digital filters ensure that aliasing of the input signal does not occur. Always use a digital filter unless absolutely certain of the frequency content of the input signal. The filter options are an eight-pole Butterworth filter or a linear phase filter. For more information on digital filtering, see “Digital Filtering” on page 233.

Break Frequency
Specify the break frequency in hertz for the selected digital filter. For a Butterworth filter, this is the approximate frequency at which the signal attenuation is 3 dB or 70.7% of the unfiltered signal voltage at that frequency. For a linear phase filter, the field is named the roll off start frequency and is the approximate frequency at which the signal starts to attenuate.

The eDAQ automatically selects a default break frequency value to ensure that no aliasing occurs. The selection is based on the A/D converter rate and the choice of digital filter type.

NOTE
The check box field labeled “data is protected from aliasing” indicates whether the current digital filter selection ensures no aliasing. TCE automatically updates the field when the digital filter configuration changes. For example, the 100-kHz sample rate option precludes aliasing because it is well over the Nyquist frequency of two times the 25-kHz analog guard filter. However, the 50-kHz sample rate option does not fully preclude against aliasing because the guard filter only attenuates about 30% of the 25-kHz input signal content.

SMART Module
Use the SMART module section of the setup to configure a connected SMART module. For more information on setting up a SMART module channel, see “SMART Module Input Channels” on page 125.

Voltage Divider Option
Use the voltage divider option to increase the full-scale input range from ±10.0 volts to ±74.9 volts. This option uses a resistive voltage divider circuit with an input impedance of only 100 kilohms compared to 10 megohms without the divider circuit. Ensure that the transducer output is not dragged down by this relatively low input impedance when using this option.

Transducer Power
Set the power supply voltage from 3 to 28 volts in integral steps of one volt. The power is limited to approximately 400 milliwatts for each channel. If the transducer does not require power, set the power to 0.

NOTE
For certain types of SMART modules, the transducer power is restricted to the following: 15 volts for the Strain SMART Module with ten-volt excitation, eight volts for the Strain SMART Module with five-volt excitation and eight volts for the SMITC.

NOTE
To supply power greater than 400 milliwatts to a single transducer, define multiple channels and tie their power sources together. All the channels used for a single transducer must have the same voltage settings.

6.3.3 High Level

NOTE
The same sample rate must be specified for all high level transducers for all high level layers in any eDAQ stack.

Output Data Type
The fundamental data type for high level channels is 16-bit signed, which consumes the least amount of data storage while maintaining full 16-bit data resolution. The 32-bit float data type adds a great deal of computational overhead and is not recommended for high rate data collection. Use the 32-bit floating point option only if the input channel is to be used in subsequent computed channels or DataModes that require the input channels to be 32-bit floating point. The 8-bit signed data type adds some computational overhead, but may be useful when only a rough picture of the transducer data is required and/or data storage limitations are a major concern.

Voltage Divider Option
Use the voltage divider option to increase the full-scale input range from ±10.0 volts to ±20.0 volts. This option uses a resistive voltage divider circuit with an input impedance of only 100 kilohms. Ensure that the transducer output is not dragged down by this relatively low input impedance when using this option.

6.3.4 Low Level

NOTE
The same sample rate and digital filter must be specified for all low level transducers for any given low level layer.

Output Data Type
The fundamental data type for low level channels is 16-bit signed, which consumes the least amount of data storage while maintaining full 16-bit data resolution. The 32-bit float data type adds a great deal of computational overhead and is not recommended for high rate data collection. Use the 32-bit floating point option only if the input channel is to be used in subsequent computed channels or DataModes that require the input channels to be 32-bit floating point. The 8-bit signed data type adds some computational overhead, but may be useful when only a rough picture of the transducer data is required and/or data storage limitations are a major concern.

Digital Filter Type
Select the desired type of digital filtering for the channel. Digital filters ensure that aliasing of the input signal does not occur. Always use a digital filter unless absolutely certain of the frequency content of the input signal. The filter options are an eight-pole Butterworth filter or a linear phase filter. For more information on digital filtering, see the “Digital Filtering” on page 233.

Break Frequency
Specify the break frequency in hertz for the selected digital filter. For a Butterworth filter, this is the approximate frequency at which the signal attenuation is 3 dB or 70.7% of the unfiltered signal voltage at that frequency. For a linear phase filter, the field is named the roll off start frequency and is the approximate frequency at which the signal starts to attenuate.
The eDAQ automatically selects a default break frequency value to ensure that no aliasing occurs. The selection is based on the A/D converter rate and the choice of digital filter type.

NOTE
The check box field labeled “data is protected from aliasing” indicates whether the current digital filter selection ensures no aliasing. TCE automatically updates the field when the digital filter configuration changes.

Excitation Range
The excitation range setting determines the magnitude of the bipolar voltage applied to the red +EXC and black -EXC wires of the transducer cables. Note that a range of *X* volts DC results in +*X*/2 to -*X*/2 pin out voltages. Select one of the following discrete ranges: nominal 22, 20, 10 or 5 volts DC. The maximum current which can be supplied is 42 milliamps at 5 volts, 29 milliamps at 10 volts or 21 milliamps at 20 volts. The nominal 22-volt range is an unregulated voltage and, therefore, cannot be used for bridge transducers or any other type of transducer that has an output proportional to the excitation voltage.

NOTE
TCE does not allow usage of the provided 0-volt excitation option.

If signal excitation is required for the transducer, which is always the case when using an actual bridge, consult the transducer manufacturer's specifications and/or suggestions for excitation settings. If signal excitation is not required for a particular transducer, leave the excitation in the default initial state and set the excitation proportional parameter to no.

NOTE
All channels for any given low level layer must have the same excitation voltage.

Bridge Type
Select the bridge type to match the transducer or select the differential amplifier option if the transducer does not use a bridge. The available types are full bridge, half bridge, quarter bridge, and differential amplifier.

Output Proportional to Excitation
Select the proportional excitation option if the output signal is linearly proportional to the applied excitation signal as it is for bridge type transducers. When using this option, the eDAQ makes a minor correction for the fact that the set excitation voltage cannot be exact.

Bridge Resistance
For quarter bridge configurations, TCE defaults this value to exactly match the completion resistor provided but allows modification in case the actual strain gage has a slightly different resistance. For either full or half bridge configurations, select any resistance in the range of 100 to 10000 ohms.

Leadwire Resistance Correction
Select the leadwire resistance correction option to compensate for leadwire resistance effects when using the defined span or external span calibration modes.

NOTE
TCE always performs leadwire resistance correction for shunt calibrations that do not use the six-wire shunt option.

NOTE
For bridge transducers configured for the six-wire shunt mode and also have significant leadwire resistance, TCE reports that the deviation from the ideal shunt behavior is off by a significant amount when calibrating the transducer channel. As an example, for a leadwire resistance of 5 ohms in each leg of a 350-ohm bridge, TCE reports a deviation of about 2.8%.

Leadwire Resistance
Specify the value of the leadwire resistance when using the leadwire resistance correction option. The resistance input is the resistance of one lead ideally measured from the ELLB connector pin to the connection at the active bridge leg. It is presumed that all lead wires are approximately the same length. Quarter bridge applications require the use of all three wires.
To accurately measure the leadwire resistance, use the 4-wire resistance measurement method. Nominal resistance values for transducer cable wires can help to estimate the leadwire resistance (see “Cable Resistances” on page 245). However, since contact resistances at mechanical connections are difficult to estimate, measure the leadwire resistance for optimum accuracy.
The nominal leadwire resistance value for a 2-meter SAC-EXDUC ELLB Transducer Cable (1-SAC-EXDUC-2) measured at the pigtails is 0.165 ohms for the 24 AWG cable and 0.445 ohms for the 28 AWG cable. The nominal leadwire resistance value measured at the solder pins of the D-Sub cable connector that mates to the eDAQ front panel D-Sub is 0.025 ohms.

Resistor to Shunt Across
Select either the upscale (-Sig to -Ex) shunt option or the downscale (-Sig to +Ex) shunt option. Note that the downscale shunt option results in a negative span signal value.

Six-Wire Shunt
Select the six-wire shunt option to use the six-wire shunt calibration mode for shunt calibrations. When using this option with the required six-wire SAC-EXDUC-6-V ELLB Transducer Cable (1-SAC-EXDUC-6-V-2), leadwire resistance corrections are not permitted, even when using very long lead wires.

6.4 SMART Module Input Channels

Add a SMART module channel to any EHLS connector with an installed SMART module. Complete the parameters for the EHLS parent channel as well as the SMART module specific parameters. Configure the SMART module parameters by selecting the configure option in the SMART module section of the EHLS channel setup window (on page two). For more information on SMART modules, see "SMART Modules" on page 105.

Using SMART Utilities

Access the SMART utilities in the TCE transducer setup window. Highlight a SMART channel or a set of SMART channels and select SMART Utils. TCE offers the following three options.

- *Program*—Serially program all selected SMART modules with the transducer channel definition that currently exists and with any added pass through keyword value entries.
- *Blank*—Erase the selected SMART modules, restoring the user-data areas to their original blanked states.
- *LED Locate*—Repetitively toggle the LEDs of the selected SMART modules indicating the physical location of the selected SMART modules. This function must be manually aborted.

6.4.1 SMSTRB4 (Strain SMART Module)

NOTE
The parameters for the SMSTRB4 are integral to the channel calibration. To edit any of these parameters, first delete the existing calibration.

Excitation Range
The excitation range setting determines the monopolar excitation voltage applied across the bridge. Select either 5- or 10-volt excitation for nominal bridge resistances of 350 ohms and greater. For smaller bridge resistances, only the 5-volt excitation range is available.
The signal input levels for SMSTRB4 transducers are limited by the excitation range selection and the nominal gain which is determined by the calibration curve and not directly configurable. For a 5-volt excitation range, the inputs are limited to ±180

millivolts for the nominal gain of 10 or ±18 millivolts for the nominal gain of 100. For a 10-volt excitation range, the inputs are limited to ±360 millivolts for the nominal gain of 10 or ±36 millivolts for the nominal gain of 100.

NOTE
The output voltage is always proportional to the excitation voltage. The eDAQ makes minor corrections required to deal with slight differences in the calibrated excitation voltage and the nominal excitation of 5 or 10 volts.

Bridge Type
Select the bridge type to match the transducer. The available types are full bridge, half bridge and quarter bridge.

NOTE
For older SMART bridge modules, the bridge type is fixed at production.

Bridge Resistance
For quarter-bridge configurations, the value defaults to the provided completion resistor. If necessary, modify the value if the actual strain gage has a slightly different resistance. For either full- or half-bridge configurations, select any resistance in the range of 100 to 10000 ohms.

Gage Factor
Define the gage factor for the specific strain gages used. TCE uses this value only in the shunt tool calibration option that defines an equivalent strain based on the gage factor and bridge factor values.

Bridge Factor
Define the bridge factor for the specific configuration of strain gages used. TCE uses this value only in the shunt tool calibration option that defines an equivalent strain based on the gage factor and bridge factor values. The bridge factor is defined here as the arithmetic sum of the active bridge legs for any bridge configuration. For quarter-bridge applications, the bridge factor is normally one; for half-bridge applications where both active gages are additive, it is normally two; and for full-bridge applications where all active gages are additive, it is normally four. Because there are special applications where the bridge factor can be a fraction and/or a negative value TCE considers any nonzero value valid.

Leadwire Resistance Correction
Select the leadwire resistance correction option to compensate for leadwire resistance effects when using the defined span or external span calibration modes.

NOTE
The eDAQ always performs leadwire resistance correction for shunt calibrations and transducers calibrated using the defined span or external span calibration modes.

Leadwire Resistance
Specify the value of the leadwire resistance when using the leadwire resistance correction option. The resistance input is the resistance of one lead, ideally measured from the SMART module connector pin to the connection at the active bridge leg. It is presumed that all lead wires are approximately the same length. Quarter-bridge applications require the use of all three wires.
To accurately measure the leadwire resistance, use the four-wire resistance measurement method. Nominal resistance values for transducer cable wires can help to estimate the leadwire resistance (see “Cable Resistances” on page 245). However, since contact resistances at mechanical connections are difficult to estimate, measure the leadwire resistance for optimum accuracy.

Resistor to Shunt Across
Select either the upscale (-Sig to -Ex) shunt option or the downscale (-Sig to +Ex) shunt option. Note that the downscale shunt option results in a negative span signal value.

NOTE
For older SMART bridge modules, the resistor to shunt across is fixed at production.

Hardware Configuration
Click the hardware button to view the SMART module user data parameters as they are defined in the hardware setup configuration. Note that TCE does not update reprogrammed SMART modules until a hardware query is performed.

6.4.2 SMITC (Thermocouple SMART Module)

NOTE
The eDAQ uses the full-scale min and max values defined in the EHLS parent channel to configure the converter that outputs analog voltage as a function of computed thermocouple temperature. To optimize the temperature measurement accuracy, set the full-scale values as close as possible to the temperature extremes expected in the test.

Thermocouple Type
Select the type of thermocouple as T, J, K or E. If the channel is calibrated, delete the calibration before selecting a different thermocouple type.

Hardware Configuration
Click the hardware button to view the SMART module user data parameters as they are defined in the hardware setup configuration. Note that TCE does not update reprogrammed SMART modules until a hardware query is performed.

6.5 Temperature Input Channels

6.5.1 Thermocouple

Add a thermocouple input channel to any ENTB connector. For more information on the ENTB layer, see “ENTB (Non-Isolated Thermocouple Layer)” on page 106.

Output Data Type
The output data type is always 32-bit float.

Thermocouple Type
Select the type of thermocouple as T, J, K, E, or thermocouple undefined.

Replace Lost Data Samples
Set this field to yes to fill the data samples with a fixed value of +1.0e+06 when the input voltage to an input channel is out of the thermocouple’s operating range. The most common cause for this is a broken thermocouple or not having a thermocouple plugged into the front panel input connector.

NOTE
Both lost data samples and out of range data samples are flagged as invalid in the test run pipe frames (i.e., the frames of data that are passed to the computed channel and DataMode modules). This allows the Valid Data Gate computed channel to keep track of all invalid data samples. For more information on the Valid Data Gate computed channel, see “Valid Data Gate” on page 163.

6.5.2 Isolated Thermocouple

Output Data Type
The output data type is always 32-bit float.

Replace Lost Data Samples
Set this field to yes to fill the data samples with a fixed value of +1.0e+06 when the input voltage to an input channel is out of the thermocouple's operating range. The most common cause for this is a broken thermocouple or not having a thermocouple plugged into the front panel input connector.

NOTE
Both lost data samples and out of range data samples are flagged as invalid in the test run pipe frames (i.e., the frames of data that are passed to the computed channel and DataMode modules). This allows the Valid Data Gate computed channel to keep track of all invalid data samples. For more information on the Valid Data Gate computed channel, see "Valid Data Gate" on page 163.

6.6 Bus-Oriented Input Channels

Each bus interface supports channels created from channel databases. Each channel in the database has pre-defined parameter values which are automatically transferred to the created channel. The bus-oriented input channels are:

- Serial bus - Add up to 128 serial bus channels to the serial bus connection on the base processor layer. For more information on the serial bus input, see "Serial Bus" on page 94.
- GPS - Add up to 128 GPS channels to an ECOM or EDIO GPS receiver. For more information on the GPS receiver, see "EGPS-5HZ (SoMat GPS Receiver)" on page 99.
- Vehicle bus - Add up to 254 vehicle bus channels to either a vehicle bus module (VBM) compatible with an ECOM or EDIO layer or an EHLB with vehicle bus capability. For more information on VBMs, see "Vehicle Bus Module" on page 101.

6.6.1 Common Bus Channel Parameters

NOTE
All bus-oriented input channels for any given connector must have the same sample rate.

NOTE
The connector parameter has no physical significance, but is a required parameter.

Enable Active Querying (serial and vehicle bus only)
Specify whether or not to use active querying.

Desired Rate (serial and vehicle bus only)
Set the query rate if active querying is in use. The limit on the query rate is a function of multiple parameters including the type of bus and the amount of broadcast data making it necessary to investigate this limit on a case-by-case basis.
Most active query requests are for packets that contain more that one bus channel. If the active query rate is equal for a set of channels with the same request value, the eDAQ ensures that the request is generated at the specified rate. If different query rates are specified for the channels in the set, the eDAQ sets the actual query rate as the maximum of the specified query rates.

NOTE
Use the active querying master control setting in the hardware configuration dialog to disable or limit active querying.

NOTE
There is a limit to the amount of active querying which is a function of multiple parameters including the type of bus and the amount of data broadcast on the bus. It is recommended to investigate this limit on a case-by-case basis.

Stale Data Expiration
Set the data expiration time period in seconds. If the specified time elapses before the receipt of a data update on the input channel, the eDAQ flags the data as invalid.

NOTE
If the expiration time period is less than the sample rate period, the eDAQ overrides the value and sets it such that the data will not expire in one sample period or less.

Invalid Data Output Value
Set the value to substitute for any data flagged as invalid. If the data type is 32-bit float, the substitution value can be any floating point value; otherwise, the substitution value must be in the range of the full range min and max values specified for the channel in the database definitions.
Bus channel inputs can be invalid for a number of reasons. The data may be marked as invalid when the eDAQ interface receives the data (e.g., the data may not be available at the source, the data may be marked as out of range at the source, etc.).

NOTE
The invalid value is defined in terms of the raw signal units as specified in the database definition. Subsequently scaling the output (e.g., by using calibration definitions that convert units) also scales the invalid value accordingly.

Raw Data Type
The raw data type is typically the data type defined in the database (i.e., 8-bit unsigned, 16-bit unsigned or 32-bit unsigned). However, for database bit sizes other than 8, 16 or 32, the eDAQ promotes the raw data type to one of these three bit lengths. For example, a 1-bit unsigned is promoted to 8-bit unsigned and a 24-bit unsigned is promoted to 32-bit unsigned.

Convert Raw Data to 32-Bit Float
Select the convert option to set the output data type to 32-bit float. The conversion adds some computational overhead, but this is relatively insignificant to overall eDAQ performance at the low sample rates typically used for bus inputs.

6.6.2 Vehicle Bus Message Channel

Use vehicle bus message channels to acquire raw vehicle bus packets. After selecting the desired channel type, complete the ID, connector and description fields. For more information on vehicle bus message channels, see “Vehicle Bus Message” on page 101.

6.7 Simulation Input Channels

Use a simulation transducer to simulate transducer input into the eDAQ. This type of transducer is independent of the signal conditioning hardware on the eDAQ. Simulation transducers are used extensively in the product development cycle at HBM, primarily to test computed channel and DataMode functionality. There are two types of simulation transducers available.

NOTE
The full-scale min and max values are required only if the simulation transducer data is stored in an integer format DataMode (i.e., 16-bit or 8-bit storage modes).

6.7.1 Simulation File

The file-based simulation transducer provides the capability to simulate input based on an ASCII file definition of the data stream allowing completely arbitrary input data streams. Because TCE reads the ASCII file using a C `fscanf()` function in float format, the data entries must be separated by white space only. There is no limit on the number of points, however be aware that the data points are stored in the eDAQ RAM disk consuming data storage memory.

Example Simulation Files
The following examples define the same data stream but use white space differently.

Example 1:

```
-100.0   500.0   -700.0   300.0
```

Example 2:

```
-100.0
500.0
-700.0
300.0
```

Output Data Type
The output data type is always 32-bit float.

File Name
Specify the full path name of the desired ASCII input file. Use the Browse button to select the desired file. Use the Check File option to parse the ASCII file and verify that the format is valid.

NOTE
Because TCE parses the ASCII file at test initialization, any changes to the file prior to initialization are effective for subsequent test runs.

Cycles
Set the value used to define the number of continuous cycles (i.e., passes through the file) to output. After the outputting the specified number of cycles, the eDAQ repeatedly outputs the last data value in the file.

Scale
Set the value used to scale the data values as defined in the file on a point-by-point basis.

Offset
Set the value used to offset the data values as defined in the file on a point-by-point basis.

Decay
Set the value used to adjust the scale value on a pass by pass basis. The scale factor is multiplied by the decay factor on each successive pass, which results in an exponential decay of the signal if the decay factor is a positive fraction. Note that the default value of one results in a consistent signal from pass to pass with no decay.

Drift
Set the value used to adjust the offset value on a pass by pass basis. The drift factor is added to the offset value on each successive pass. Note that the default value of zero results in a consistent signal from pass to pass with no drift.

6.7.2 Simulation Function Generator

The function generator (FG) based simulation transducer provides capabilities similar to a conventional analog function generator, i.e., a choice of various waveforms with frequency, range and mean level control, plus some extended capabilities.

Output Data Type
The output data type is always 32-bit float.

Function
Use the pick list to select the basic waveform shape of either sine, triangle or square. Note that the triangle and square waveforms start at the minimum signal level (assuming the signal is not inverted) and the sine waveform starts at the mean signal level. For all waveforms, the peak to peak limits are ±1.0 prior to the application of the user defined scale and offset values.

Period
Set the waveform period in terms of the number of samples. The waveform frequency (in Hz) is defined as the sample rate divided by the period. For example, a period of 100 samples at a sample rate of 1000 results in a 10 Hz signal.

Duty Cycle
Set duty cycle in percent for triangle and square waveforms modes only. The default value of 50% produces symmetric waveform shapes. Assuming the signal has not been inverted, the duty cycle represents the percentage of time that the square waveform is in the low state or the percentage of time that the triangle waveform is in the ramp up state.

Cycles
Set the value used to define the number of continuous cycles (i.e., passes through the file) to output. After the outputting the specified number of cycles, the eDAQ repeatedly outputs the last data value in the file.

Scale
Set the value used to scale the data values as defined in the file on a point-by-point basis.

Offset
Set the value used to offset the data values as defined in the file on a point-by-point basis.

Decay
Set the value used to adjust the scale value on a pass by pass basis. The scale factor is multiplied by the decay factor on each successive pass, which results in an exponential decay of the signal if the decay factor is a positive fraction. Note that the default value of one results in a consistent signal from pass to pass with no decay.

Drift
Set the value used to adjust the offset value on a pass by pass basis. The drift factor is added to the offset value on each successive pass. Note that the default value of zero results in a consistent signal from pass to pass with no drift.

6.7.3 Simulation Message

Output Data Type
The output data type is always 8-bit unsigned message.

Format
Select either an ASCII or binary message format. The ASCII format pouts a repeating pattern of the 26 letters from A to Z. The binary format outputs a repeating pattern of byte values from 0 to 255.

Message Size
Specify the message size in bytes.

Message Interval
Specify the period in seconds for repetitive generation of the simulated message.

7 Computed Channels

This chapter details the available computed channels and their associated parameters. A computed channel is a data channel derived from one or more transducer channels or from previously defined computed channels. For example, a computed channel can generate a channel having a higher or lower sample rate (using Up Sampler or Down Sampler), be constructed from data using a mathematical formula or expression (using the Desk Calculator) or integrate data samples (using the Integrator). Define computed channels in the computed channel setup window.

NOTE
Defining computed channels in a test setup is optional

7.1 Common Computed Channel Parameters

The following parameters are common to all computed channels.

Network Node
This field displays the IP address or host name of the eDAQ for which the channel has been defined.

ID
Enter a unique identifier for the channel. The name must conform to ID naming conventions. Valid ID names:

- are case sensitive
- are limited to a maximum of 12 characters
- contain only valid characters (i.e., letters (a-z, A-Z), digits (0-9), and the underscore (_) character)
- start with a letter
- are not duplicates of system reserved names (sin, cos, log, etc.)

Description
Enter a more detailed description of the computed channel. TCE sets the description field to match the input channel description, but modifications are permitted.

Type
Define the type of measurement associated with the transducer or computed channel. Typical types include strain, load and acceleration. Select a type from the list or directly key in a user-defined type. Since TCE uses the type definition in subsequent sections of the test setup process, completing the field is recommended.

Units
Define the units of measurement for the computed channel. Since TCE uses the units definition in subsequent sections of the test setup process, completing the field is recommended.

Input Channel
Select the desired input channel(s) to the computation. The number of input channels permitted depends on the computed channel type.

Output Data Type
Depending on the channel type, the eDAQ provides several data type options. When choosing the data type, consider factors such as data resolution, mass storage consumption and what computed channels or DataModes use the channel as an input. For a summary of the compatible data types for all computed channels and DataModes, see "Data Types" on page 195.

Full-Scale Min and Max
The min and max full-scale fields define the expected extreme values of the computed channel expression. When storing a 32-bit float in a DataMode that uses an integer data type, the eDAQ uses the full-scale limits when converting from the floating point format to the integer format. The eDAQ also uses the full-scale estimates to set the default values for any histograms specified in the test setup DataModes.

7.2 Arithmetic Computed Channels

7.2.1 Desk Calculator

Desk Calculator computed channels generate data streams of either arithmetic (floating point) or logical (Boolean) results.

Input Channel
All input channels to a single Desk Calculator channel must have the same sample rate, which also determines the computed channel sample rate. The required input data types for the Desk Calculator operator set are listed in table below.

NOTE
The time functions (e.g., _utc_day()) require an input from a Time Channel computed channel with a 32-bit float data type (see "Time Channel" on page 156).

Operator	Input Type	Output Type
sin, cos, tan, asin, acos, atan, log, log10, abs, exp, sgn, round, floor, ceil, +,-,*,/,%,^	32-bit float	32-bit float
float	8-bit unsigned	32-bit float
>,>=,<,<=,==,!=	32-bit float	8-bit unsigned
!,&&,||	8-bit unsigned	8-bit unsigned
time functions	32-bit float Time Channel	32-bit float

Output Data Type
The output data types for the Desk Calculator operator set are listed in the table above.

Desk Calculator Expression

Build the Desk Calculator expression using keyboard entry or by double clicking an input channel or operation to add it to the expression. Syntax for the Desk Calculator expression is modeled after the standard C programming language and follows the same operator precedence rules. All operators and referenced input channels are case sensitive. Operand data type consistency is strictly enforced in the parsing of the Desk Calculator expression operators. TCE warns of any syntax errors it detects after clicking OK.

Floating point exceptions can occur with the misuse of certain Desk Calculator operators such as taking the square root or logarithm of a negative number. When detecting these exceptions, the eDAQ sets the MathException status flag. The results of such operations are usually some form of IEEE NAN (not a number).

Category	Operator	Syntax	Return
Arithmetic	abs	abs(*a*)	The absolute value of *a*.
	sqrt	sqrt(*a*)	The square root of *a*.
	log	log(*a*)	The natural logarithm of *a*.
	log10	log10(*a*)	The base-10 logarithm of *a*.
	exp	exp(*a*)	The exponential function of *a*.
	sgn	sgn(*a*)	-1 for *a* < 0, 1 for *a* > 0 and 0 for a = 0.
	float	float(*a*)	*a* in floating point data type.
	round	round(*a*)	The nearest integer to *a*.
	floor	floor(*a*)	The largest integer less than *a*.
	ceil	ceil(*a*)	The smallest integer greater than *a*.
	^	*a*^*b*	*a* raised to the power of *b*.
	*	*a***b*	The product of *a* and *b*.
	/	*a*/*b*	The quotient of *a* and *b*.
	%	*a*%*b*	The modulus of *a* and *b*.
	+	*a*+*b*	The sum of *a* and *b*.
	-	*a*-*b*	The difference of *a* and *b*.
Trigonometric (all angles in radians)	sin	sin(*a*)	The sine of *a*.
	cos	cos(*a*)	The cosine of *a*.
	tan	tan(*a*)	The tangent of *a*.
	asin	asin(*a*)	The arcsine of *a* in the range [-PI/2, PI/2].
	acos	acos(*a*)	The arccosine of *a* in the range [0, PI].
	atan	atan(*a*)	The arctangent of *a* in the range [-PI/2, PI/2].

Category	Operator	Syntax	Return
Logical	>	*a*>*b*	TRUE if *a* is greater than *b*; else FALSE.
	>=	*a*>=*b*	TRUE if *a* is greater than or equal to *b*; else FALSE.
	<	*a*<*b*	TRUE if *a* is less than *b*; else FALSE.
	<=	*a*<=*b*	TRUE if *a* is less than or equal to *b*; else FALSE.
	==	*a*==*b*	TRUE if *a* is equal to *b*; else FALSE.
	!=	*a*!=*b*	TRUE if *a* is not equal to *b*; else FALSE.
	!	!*a*	TRUE if *a* is FALSE; else FALSE.
	&&	*a*&&*b*	TRUE if *a* and *b* are TRUE; else FALSE.
	||	*a*||*b*	TRUE if either *a* or *b* are TRUE; else FALSE.
Time (input must be a Time Channel)	_utc_subsecond	_utc_subsecond(*a*)	The subsecond (0-1) in UTC.
	_utc_second	_utc_second(*a*)	The second (0-60) in UTC.
	_utc_minute	_utc_minute(*a*)	The minute (0-59) in UTC.
	_utc_hour	_utc_hour(*a*)	The hour (0-23) in UTC.
	_utc_day	_utc_day(*a*)	The day (1-31) in UTC.
	_utc_month	_utc_month(*a*)	The month (1-12) in UTC.
	_utc_year	_utc_year(*a*)	The year in UTC.
	_utc_day_week	_utc_day_week(*a*)	The day of the week (1-7) in UTC.
	_utc_day_year	_utc_day_year(*a*)	The day of the year (1-366) in UTC.
	_local_subsecond	_local_subsecond(*a*)	The subsecond (0-1) in local time.
	_local_second	_local_second(*a*)	The second (0-60) in local time.
	_local_minute	_local_minute(*a*)	The minute (0-59) in local time.
	_local_hour	_local_hour(*a*)	The hour (0-23) in local time.
	_local_day	_local_day(*a*)	The day (1-31) in local time.
	_local_month	_local_month(*a*)	The month (1-12) in local time.
	_local_year	_local_year(*a*)	The year in local time.
	_local_day_week	_local_day_week(*a*)	The day of the week (1-7) in local time.
	_local_day_year	_local_day_year(*a*)	The day of the year (1-366) in local time.

NOTE
The second time functions can return a value of 60 which indicates the rare case of a leap second. The resulting time sequence in this case is `23:59:59, 23:59:60, 00:00:00`.

NOTE
The subsecond time functions return the fractional part of a second at a resolution dependent on the sample rate of the Time Channel input. For example, a sample rate of 100 Hz results in a resolution of 0.01 seconds and a sample rate of 1000 Hz results in a resolution of 0.001 seconds.

Application Note: Piecewise Linear Relationships
In the following example, the desired output of the Desk Calculator channel (*y*) is defined as follows, based on the value of the input channel (*x*).

$$y = \begin{cases} 2.1x + 100, & x > 100 \\ 2.2x + 90, & 50 < x \leq 100 \\ 2.3x + 80, & 0 < x \leq 50 \\ 2.4x + 70, & x \leq 0 \end{cases}$$

The first step is to define the required set of logical Desk Calculator channels (s1, s2, s3, s4) as follows :

```
s1: x>10e0
s2: x>50 && x<=100
s3: x>0 && x<=50
s4: x<=0
```

The second step is to define the required set of arithmetic Desk Calculator channels (y1, y2, y3, y4) as follows :

```
y1: 2.1*x+100
y2: 2.2*x+90
y3: 2.3*x+80
y4: 2.4*x+70
```

The third step is to define the final Desk Calculator channel (y) as follows :

```
y: y1*float(s1)+ y2*float(s2)+ y3*float(s3)+ y4*float(s4)
```

Note that it is not necessary to define the intermediate variables and, in fact, it is less efficient from a processing point of view to use intermediate variables when they are not used more than once in the set of computed channels. However, they have been used above to clarify the general approach.

7.2.2 Engineering Scaler

The Engineering Scaler channel generates a 32-bit float output channel scaled to engineering units from an integer data type input channel.

Input Channel
The input channel data type must be 8-bit integer, 8-bit unsigned, 16-bit integer, 16-bit unsigned, 32-bit integer, or 32-bit unsigned.

Output Data Type
The output channel data type is 32-bit float.

7.2.3 Integer Scaler

The Integer Scaler channel generates an integer data type output channel from any 32-bit float input channel.

Input Channel
The input channel data type must be 32-bit float.

Output Data Type
The output data type must be 8-bit integer, 8-bit unsigned, 16-bit integer, 16-bit unsigned, 32-bit integer, or 32-bit unsigned.

7.2.4 Integrator

The Integrator channel generates an output channel that is the integral of the input channel. As long as the integrator is not reset or suppressed, each output channel sample is the cumulative sum of the current and all previous input channel samples multiplied by a user-defined scale factor and added to a user-defined initial value. A logical channel set as a trigger can reset the integrator or suppress integration. The integrator can also reset when exceeding a user-defined summation value.

Input Channel
The input channel data type must be 32-bit float, 32-bit integer or 32-bit unsigned.

Output Data Type
The output data type is the same as the input channel data type.

Integrate Only When TRUE
Select the integrate only when TRUE option to suppress integration when the trigger channel is FALSE.

Enable Triggered Reset
Select the enable triggered reset option to reset the integrator to the initial value when the trigger channel satisfies the defined condition.

Trigger Channel
Specify the input channel used for the reset enable or sum on trigger options.

Reset Mode
Select how to use the specified trigger channel for the reset enable option. The available trigger condition options are below.

Reset Mode	Description
When TRUE	Reset when the trigger channel is TRUE.
On FALSE-TRUE edge	Reset when the trigger transitions from FALSE to TRUE.
On TRUE-FALSE edge	Reset on the sample after the trigger channel transitions from TRUE to FALSE. If the sum on trigger option is not selected, then the output sample after the TRUE to FALSE edge is the sum of the initial value and the scaled input sample.

NOTE
When using the sum on trigger option, the trigger condition is limited to on a TRUE to FALSE edge.

Reset on Sum Exceed
Select the reset on sum exceed option to reset the integrator to the initial value when the absolute value of the integrator sum exceeds the value specified in the sum exceed value field.

NOTE
If using the reset on sum exceed option, the eDAQ does not allow any other trigger or reset options.

Initial Value
Specify the value for the integration sum at the start of each run and on a reset if using the reset enable option.

NOTE
For an input data type of 32-bit unsigned or 32-bit signed, the initial value is fixed at zero.

Scale Factor
Specify the value to scale each input sample before adding it to the previous integration sum. Setting the scale factor to the sample period results in the time integral of the input channel.

NOTE
For an input data type of 32-bit unsigned or 32-bit signed, the scale factor is fixed at one.

Use 64-bit Float for Sum
Select the 64-bit float for sum option to ensure that the integration is not subject to the inherent limitations of using a 32-bit float to accumulate the integration sum. This is particularly critical for long term or high sample rate testing where relatively small values are added to an ever increasing sum. It is strongly recommended to use the 64-bit float for sum option whenever possible.

Using the Integrator to Measure Accumulated Pulse Counts

The use of the Integrator computed channel to yield accumulated counts varies based on the selected output data type.

- 32-Bit Unsigned: The most efficient way to use the Integrator computed channel is with this data type; the integrator can then accumulate up to 4294967295 counts. This is the suggested approach for simply counting pulses or events. The scaling to hertz is performed by an associated scale factor used only when needed, such as for DataMode storage. Therefore, the output data stream is the stream of unsigned integer counts.

- 32-Bit Float: If the this output mode is used, then the scale factor field in the Integrator should be set to the reciprocal of the pulse counter sample period to yield counts; additional scaling can be incorporated into the scale factor field for conversion to distance, revolutions, etc. It should also be kept in mind that a 32-bit float can only accumulate about 16.7 million counts before it saturates as an integral counter. The scaling to hertz is performed on a sample-by-sample basis as the data is acquired.

For more information on pulse counter inputs, see “Pulse Counter” on page 115.

7.2.5 Pulse Counter

The Pulse Counter computed channel is used to measure pulse frequencies primarily in conjunction with digital inputs. Each FALSE to TRUE transition signifies the end of a pulse period and initiates an update of the current pulse frequency, which is output at a user-defined rate. The pulse counter frequency also updates if the time period since the last transition exceeds the current pulse counter frequency output, resulting in improved response as the pulse train slows or stops.

NOTE
The current pulse frequency initializes to 0 Hz and remains at this initial value until two FALSE to TRUE transitions occur.

The accuracy of the pulse frequency measurements is dependent on the sample rate of the digital input channel only (i.e., it is not dependent on the output sample rate which is set indirectly by the factor parameter). For example, using an input channel sampled at 2000 Hz provides 1% accuracy of a 20 Hz pulse signal or 0.1% accuracy of a 2 Hz pulse signal. As a rule of thumb, the input sample rate should be 100 times the maximum expected pulse frequency to provide 1% or better accuracy over the entire range of pulse frequency content.

Input Channel
The input channel data type must be 8-bit unsigned (logical).

Output Data Type
The output channel data type is 32-bit float.

Output Rate Factor
Specify the desired down sample factor which sets the output sample rate based on the sample rate of the input channel. For example, if the input channel sample rate is 2000 Hz, a factor of 100 results in an output sample rate of 20 Hz.

Cal Scale Factor
Specify the desired scale factor for converting measured pulse frequency in Hz to the desired engineering units.

Minimum Frequency Limit
Specify the desired minimum frequency limit for the Pulse Counter. If there is no new pulse within the period ($1/f_{min}$), the channel outputs this frequency value.

NOTE
The minimum frequency limit parameter provides a solution when a pulse train stops. For example, if a 50 Hz pulse train stops, the Pulse Counter output remains at 50 Hz until there is a new pulse frequency.

7.2.6 Directional Velocity

The Directional Velocity channel generates a signed velocity output from two input channels. One input channel is the unsigned velocity; the second input channel is a position channel and sets the sign of the output channel.
The sign of the output channel is determined from the position channel as follows. If the position on the current data sample is greater than the position on the previous data sample, the sign is positive. If the position on the current data sample is less than the position on the previous data sample, the sign is negative. If the position on the current data sample is equal to the position on the previous data sample, the sign retains its current value.

Input Channel
The velocity input channel data type must be 32-bit float. The direction input channel data type must be either 32-bit float or 32-bit integer.

Output Data Type
The output channel data type is 32-bit float.

NOTE
It is strongly recommended that the direction input channel have a data type of 32-bit integer, which is the raw data type of the quadrature decoder Pulse Counter channel. Using a 32-bit float works only if the quadrature decoder output stays in the approximate range of +/- 16000000 counts. The 32-bit integer data type allows use of the full range of the quadrature decoder pulse channel of +2147483647 to -2147483648 counts.

Check for Int32 Rollover
If the direction input channel is a 32-bit integer channel, use the int32 rollover check to detect rollover of the signed 32-bit counter. If the counter jumps by more than 24000000 counts from one sample to the next, the eDAQ assumes that the counter has rolled over. For example, if the counter jumps from +2100000000 to -2140000000, the eDAQ detects a rollover and sets the sign to positive.

NOTE
Use the rollover check option on an as-needed basis as it does add some processing overhead to the channel.

Pulse Counter Application Note: Quadrature Encoder

This Directional Velocity channel was developed primarily to provide a signed RPM output channel using a quadrature encoder connected to a EDIO layer. Configure one of the two pulse trains from the quadrature encoder as a pulse frequency transducer channel to yield the unsigned velocity input channel. Define a normal quadrature decoder Pulse Counter channel using both pulse trains to yield the position input channel. For more information on quadrature encoder inputs, see "Pulse Counter" on page 115.

7.2.7 State Mapper

The State Mapper channel maps the input channel into a discrete state output channel based on a set mapping conditions defined in an ASCII file. Define each mapping condition in terms of a minimum input value, a maximum output value, and the associated output state value. The number of mapping conditions must be 32 or less. The ASCII file should be a line-based file with the three ordered entries per line separated by spaces or tabs.

NOTE

The State Mapper channel can consume significant eDAQ computational resources depending on the sample rate and the number of mapping conditions defined.

State Mapper Example: Angular Position

Consider mapping an input channel that generates angular position in the range of 0 to 360 degrees into an output channel that specifies which 60 degree sector the input channel is in. Use the following mapping conditions where x is the input and y is the output.

$$y = \begin{cases} 1, & 0 \le x < 60 \\ 2, & 60 \le x < 120 \\ 3, & 120 \le x < 180 \\ 4, & 180 \le x < 240 \\ 5, & 240 \le x < 300 \\ 6, & 300 \le x < 360 \end{cases}$$

One way to write the ASCII file for this example is as follows.

```
0    60 1
60  120 2
120 180 3
180 240 4
240 300 5
300 360 6
```

Input Channel

The input channel data type must be 32-bit float.

Output Data Type

The output channel data type is 32-bit float.

ASCII File
Specify the full path name of the ASCII file that defines the mapping conditions. Use the Browse button to select the desired file. Use the Check File option to parse the ASCII file and verify that the format is valid.

NOTE
Because TCE parses the ASCII file at test initialization, any changes to the file prior to initialization are effective for subsequent test runs.

Use Default Output
Select the default output option to output a default value when the input channel does not meet any of the mapping conditions. If not selected, the output remains in its existing state.

Default Out
Specify the default value for the output. The channel outputs the value if the first input sample does not meet any mapping conditions. Also, when using default out, the channel outputs the default value throughout the test run when the input does not meet any mapping conditions.

Latch Period
Specify the time in seconds that the input channel must consistently map to the same output state before the output state switches. The latch period is similar to a duty cycle on the output state preventing the output state from switching for at least this period of time. This feature can eliminate state switching transients in the output channel data stream. If the latch period is 0.0, then the output state switches on each sample.

7.2.8 Statistical Analysis

The Statistical Analysis channel generates statistical output data from source transducer or computed channel input data.

Input Channel
The input channel data type must be 32-bit float.

Output Data Type
The output data type is 32-bit float.

Statistic
Select one of six available statistical modes. The following table defines the algorithms used to compute the statistical values where N is the number of data samples in the analysis window and X_{mean} is the mean of the data in the analysis window.

Statistic	Algorithm
Mean	$\frac{1}{N}\sum_{i=1}^{N} X_i$
Standard deviation	$\sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(X_i - X_{mean})^2}$
RMS	$\sqrt{\frac{1}{N}\sum_{i=1}^{N} X_i^2}$
Kurtosis	$K = N\sum_{i=1}^{N}(x_i - x_{mean})^4 / \{\sum_{i=1}^{N}(x_i - x_{mean})^2\}^2$
Skewness	$\sum_{i=1}^{N}(X_i - X_{mean})^3 / \sqrt{\frac{1}{N}\{\sum_{i=1}^{N}(X_i - X_{mean})^2\}^3}$
Xth-percentile	TCE sorts the data samples in the analysis window in ascending order and interpolates as required between the array element data values that border the exact Xth-percentile array element. For more information on processing limitations when using the Xth-percentile mode, see "Xth-Percentile Benchmark Tests" on page 241.

Percentile
Specify the *X* value for the Xth-percentile mode. The value can be an integer between 0 and 100.

NOTE
Setting the Xth-percentile parameter to zero returns the minimum value in the analysis window. Setting the Xth-percentile parameter to 100 returns the maximum value in the analysis window.

Window Samples
Specify the number of input samples used to generate one output sample. This sets the analysis window size and associated output sample rate. Specify any positive integer value greater than one.

7.2.9 Damage Equivalent Load

The Damage Equivalent Load channel generates an accumulated equivalent load range value as a function of the user-defined damage slope parameter and the associated accumulated rainflow cycle count for the selected input channel.

NOTE
The Damage Equivalent Load channel has two outputs, load and cycle, each of which has its own name, description, type, units, full-scale min and max, and data type fields.

The eDAQ processes the input channel through a rainflow cycle counter using the user-defined hysteresis value for peak picking. For each closed cycle, the eDAQ computes a load damage parameter as (closed cycle range ^ damage slope) and adds it to the running sum that accumulates load damage on a cycle-by-cycle basis. For each output sample, the eDAQ processes the residual peak-valley sequence through the rainflow cycle counter to account for the additional accumulated load damage and accumulated closed cycle counts. The Damage Equivalent Load output value (S_{eq}) is computed using the following equation:

$$S_{eq} = \left(\frac{1}{N}\sum_{i=1}^{N} x_i\right)^{1/m}$$

where, x_i is the load damage for each closed cycle, N is the number of closed cycles and m is the damage slope.
For more information on the data processing algorithms used, see “Data Processing Algorithms” on page 243.

Input Channel
The input channel data type must be 32-bit float.

Output Data Type
Both output channel data types are 32-bit float.

Hysteresis
Set the desired hysteresis level for the peak valley processing algorithm.

Damage Slope
Set the damage slope used in the processing algorithm as described above. This can be any value from 1.0 to 20.0.

Window Samples
Specify the number of input samples used to generate one output sample. This sets the analysis window size and associated output sample rate. Specify any positive integer value greater than one.

NOTE
There can be fairly significant computational overhead in generating each output sample, particularly when the residual peak-valley sequence is relatively long (i.e., 100 residual peak-valleys or more). Consider the computational overhead when specifying the window samples.

Application Note: Load-Life Fatigue Damage

If the input channel is a linear function of load, the outputs of this channel can translate to a simple load-life fatigue damage assessment for the test run. For example, assuming that a load-life relationship is given by

$$S = S_o N_f^{-1/m}$$

where, N_f is the constant load range cycles to failure, S_o is the load range when N_f equals 1 and m is the damage slope. Assuming that S equals the product of some coefficient k and the input channel, it follows that the fractional fatigue damage per block (i.e., per test run), $1/B_f$ is given by

$$\frac{1}{B_f} = N(k\frac{S_{eq}}{S_o})^m$$

Note that load-life relationships are most typically defined in terms of load amplitude versus cycles to failure, instead of in terms of load range versus cycles to failure as in the above example.

7.2.10 Fatigue Damage

The Fatigue Damage channel generates an output stream of fatigue damage for the selected input channel. The fatigue damage computations are based on the selected fatigue damage model, material parameters and on optional input and output scaling parameters.

Scaling the input channel can be useful, for example, in converting transducer data in microstrain units to dimensionless strain units required for the fatigue processing models. TCE processes the optionally scaled input channel on a point-by-point basis through a rainflow cycle counter using the user-defined hysteresis value for peak picking. For each closed cycle, the computed fatigue damage is added to the running sum of cumulative fatigue damage based on the user-selected fatigue damage model. For each output sample, the residual peak-valley sequence is processed through the rainflow cycle counter to account for the additional accumulated fatigue damage. The output values are effectively scaled based on the user-selected damage units option.

NOTE

The use of the scaling options does not result in any processing overhead because of the way that these parameters are integrated into the fatigue damage solvers.

For more information on the data processing algorithms used, see “Data Processing Algorithms” on page 243.

Input Channel

The input channel data type must be 32-bit float.

Output Data Type

The output channel data type is 32-bit float.

Scale Factor

Specify the desired scaling factor typically used to convert the input channel data into the proper units based on the damage model. For example, the scale factor converts input channel data in microstrain units to dimensionless strain units when using the strain-life damage model.

Sum Damage Only When TRUE
Select the sum damage only when TRUE option to filter out input data samples that are not to be used in the fatigue damage accumulation processing.

Trigger Channel
Specify the trigger channel used in the sum on trigger feature. The trigger channel can be any logical channel that has the same sample rate as the input channel.

Accumulate Across Test Runs
The accumulate across test runs option is not currently supported.

Damage Model
Select one of three available damage models. The following table defines each model in terms of a $\log_{10}$-$\log_{10}$ linear relationship.

Model	Description
Load-Life	The load-life relationship is defined by $$P = P_o N_f^b$$ where N_f is cycles to failure, P is the applied load range and P_o and b are, respectively, the user-defined intercept and slope of the $\log_{10}$-$\log_{10}$ function. For each rainflow cycle, the damage, $1/N_f$, computed from the load range, P, is added to the cumulative damage sum.
Stress-Life	The stress-life relationship is defined by $$S = S_o N_f^b$$ where N_f is cycles to failure, S is the applied stress range and S_o and b are, respectively, the user-defined intercept and slope of the $\log_{10}$-$\log_{10}$ function. For each rainflow cycle, the damage, $1/N_f$, computed from the stress range, S, is added to the cumulative damage sum.
Strain-Life	The strain-life relationship is defined by $$e_l = (S_{f'}/E)(2N_f)^b$$ where $2N_f$ is reversals to failure, e_l is elastic strain amplitude and S_f'/E and b are, respectively, the user-defined intercept and slope of the $\log_{10}$-$\log_{10}$ function; $$e_p = e_{f'}(2N_f)^c$$ where e_p is plastic strain amplitude and e_f' and c are, respectively, the user-defined intercept and slope of the $\log_{10}$-$\log_{10}$ function; and $$e = e_l + e_p$$ where e is the total strain amplitude. For each rainflow cycle, the damage per cycle, $2/2N_f$, computed from the stress range, $2e$, is added to the cumulative damage sum.

NOTE
These basic damage models do not provide any corrections for the mean values of the load ranges affecting the cumulative damage.

NOTE
Existing material databases may be defined in terms of either reversals to failure ($2N_f$), load amplitude ($P/2$) or stress amplitude ($S/2$). Convert to the required parameters as necessary.

Edit Model Parameters
Depending on the model selected, several parameters used in the computation are available for modification by clicking the Edit Model Parameters button. The following table lists the available model parameters and their corresponding variables in each damage model.

Parameter	Load-Life	Stress-Life	Strain-Life
Elastic modulus	-	-	E
Fatigue strength coefficient	P_o	S_o	S_f'
Fatigue strength exponent	b	b	b
Fatigue ductility coefficient	-	-	e_f'
Fatigue ductility exponent	-	-	c
Fatigue limit	load limit	stress limit	-

NOTE
TCE accumulates no damage if the applied load or stress range is less than the fatigue limit parameter.

Hysteresis
Specify the desired hysteresis level for the peak valley processing algorithm.

Damage Units
Select the desired output channel damage units. The available units are damage, percent life or microdamage. Note that the output channel full-scale estimates are automatically assigned based on this selection.

Window Samples
Specify the number of input samples used to generate one output sample. This sets the analysis window size and associated output sample rate. Specify any positive integer value greater than one.

NOTE
There can be some fairly significant computational overhead in generating each output sample, particularly when the residual peak-valley sequence is relatively long (i.e., 100 residual peak-valleys or more). Consider this fact when setting the window samples parameter.

7.3 Triggering Computed Channels

Trigger computed channels generate a logical channel data stream useful for triggering DataModes or other computed channels.

7.3.1 Interactive Trigger

The Interactive Trigger channel provides a means to trigger DataModes and computed channels directly from TCE. Up to eight Interactive Triggers are supported. For more information on interactive triggering, see “Using Interactive Triggers” on page 76.

Input Channel
The input channel sets the sample rate of the channel. All data types are supported.

Output Data Type
The output channel data type is 8-bit unsigned (logical).

Trigger Index
Set the trigger index from 1 to 8.

Invert Trigger
Select the invert trigger option to reverse the logic of the trigger.

7.3.2 Trigger Generator

The Trigger Generator channel generates a trigger channel that consists of an optional initial delay period followed by a repetitive cycle of on (TRUE) periods and off (FALSE) periods. The eDAQ ensures that there is at least one output sample for both the on period and the off period.
Use a Trigger Generator channel to create an elapsed time trigger for DataModes or other computed channels that support triggering. For example, the eDAQ can use a generated trigger channel to store 10 minutes of data every hour. The Trigger Generator channel is ideally suited for long-term acquisitions such as temperature measurements of civil structures.

NOTE
The upper limit for all periods in seconds is 4.25E+09 divided by the sample rate.

Input Channel
The input channel sets the sample rate of the channel. All data types are supported.

Output Data Type
The output channel data type is 8-bit unsigned (logical).

Initial Delay Period
Specify the initial delay period in seconds. After the delay period, the output switches to the on state. If set to zero, the output starts in the on state.

On Period
Specify the on period in seconds. The output switches to the off state after this period.

Off Period
Specify the off period in seconds. The output switches back to the on state after this period.

7.3.3 Timed Trigger

The Timed Trigger computed channel generates a logical output based on a logical input and user-defined timing parameters.

Input Channel
The input channel data type must be 8-bit unsigned (logical).

Output Data Type
The output channel data type is 8-bit unsigned (logical).

Trigger Start Mode
Select the start mode of the trigger from three available trigger start modes.

Trigger Start Mode	Description
When TRUE	Start when the input channel is TRUE.
On FALSE-TRUE edge	Start when the input channel transitions from FALSE to TRUE.
On TRUE-FALSE edge	Start on the sample after the input channel transitions from TRUE to FALSE.

Enable Delay
Select the enable delay option to enable the delay mode.

Delay Period
When using the delay option, specify the delay period in seconds after the input channel triggers to set the channel output. The maximum value for the delay period is 4294967295 times the sample period.

Delay Conditional Mode
Select one of three available delay modes to conditionally set the output channel state based on the behavior of the input channel during the delay period.

Delay Mode	Description
Unconditional	Set the output to TRUE regardless of the input channel behavior during the delay period.
If TRUE at end	Set the output to TRUE if the input channel is TRUE on the last sample of the delay period. Otherwise, the search for a new trigger start condition begins.
If TRUE continuously	Set the output to TRUE if the input channel is continuously TRUE on all samples of the delay period. If the input channel is FALSE at any point during the delay period, the search for a new trigger start condition begins.

Enable Sustain
Select the enable sustain option to enable the sustain mode. If not enabled, the channel outputs TRUE for one sample before reverting to FALSE.

Sustain Period
When using the sustain option, specify the desired sustain period in seconds. The maximum value for the sustain period is 4294967295 times the sample period.

Sustain Conditional Mode
Select one of two available sustain modes to conditionally set the output channel state based on the behavior of the input channel during the sustain period.

Sustain Mode	Description
Unconditional	Set the output to TRUE for the duration of the sustain period regardless of the input channel behavior during the sustain period.
While true	Set the output channel to TRUE only while the input channel is TRUE during the sustain period. Note that if the input channel is FALSE when the sustain period begins, the output value will not be set to TRUE effectively canceling the trigger. At the end of the sustain period, the output value is set to FALSE and the search for the next trigger start condition begins.

7.3.4 Triggered Zero Suppression

The Triggered Zero Suppression channel generates output channels that zero suppress the input channel when a trigger condition is satisfied.

NOTE
The Triggered Zero Suppression computed channel is designed primarily to provide a reset for quadrature decoder channel outputs when a triggering event occurs. For more information on quadrature encoder inputs, see “Pulse Counter” on page 115.

Input Channel
The input channel data type must be 32-bit float, 32-bit integer or 32-bit unsigned.

Output Data Type
The output data type is the same as the input data type.

Trigger Channel
Select the input channel used to determine when to zero suppress the input channel based on the trigger condition.

Trigger Mode
Select from three available trigger modes to specified the trigger channel behavior. The available trigger mode options are below.

Trigger Mode	Description
When TRUE	Suppress when the trigger channel is TRUE.
On FALSE-TRUE edge	Suppress when the trigger transitions from FALSE to TRUE.
On TRUE-FALSE edge	Suppress on the sample after the trigger channel transitions from TRUE to FALSE.

Suppression Value
Define the desired suppression value. The default suppression value is zero. Keep in mind that if the input channel is a 32-bit float, the suppression value is in engineering units, but if the input channel is either a 32-bit integer or a 32-bit unsigned, the suppression value is in integer counts. For clarification, suppose a quadrature decoder

channel uses the 32-bit integer data output option, the calibration slope is defined such that 2048 counts equals 360 degrees, and the calibration intercept is zero. To set the desired suppression in engineering units to zero degrees, set the suppression value to zero integer counts. However, there is no way to set the desired suppression in engineering units to exactly 7 degrees, since 7 degrees is equivalent to 39.822 counts which is not an integer value. To avoid this problem, set the calibration intercept to 7.0 degrees and then use a suppression value of zero.

7.3.5 Bitmap Trigger

The Bitmap Trigger computed channel produces a logical output based on the match of the input bitmap channel and the user-specified bitmap mask. Use with an Anomaly Detect computed channel to generated a trigger when the eDAQ detects a defined anomaly. For more information on the Anomaly Detect computed channel, see “Anomaly Detect” on page 162.

Input Channel

The input channel data type must be the output of an Anomaly Detect computed channel, which is the only eDAQ channel with an output data type of 8-bit unsigned (bitmap).

Output Data Type

The output channel data type is 8-bit unsigned (logical).

Bitmap Check Mode

Select the desired bitmap check mode from the two available options.

Bitmap Check Mode	Description
Any bit in mask set	If any bit in the specified bit mask is set, the output value is TRUE; otherwise it is FALSE.
All bits in mask set	If all of the bits in the specified bit mask are set, the output value is TRUE; otherwise it is FALSE.

Bit Mask

Specify the desired bit mask in hexadecimal format ranging from 0x1 to 0xFF.

Invert Output Logic

Select the invert output logic option to invert the output logic defined in the bitmap check mode. Note that using inversion can identify anomaly-marked data segments and output a trigger stream to gate out these data segments in any desired computed channels or DataModes.

7.3.6 Test Run Stopper

The Test Run Stopper channel stops a test run when the input channel becomes TRUE.

NOTE

To automatically start a test run after the Test Run Stopper stops a run, use the remote control option with the run control switch always in the run position. For more information on remote control, see “Using Remote Control Operation” on page 90.

NOTE
The test run does not stop immediately when the input channel becomes TRUE. Because the input channel is processed in frames that can be buffered, the test run typically stops in a fraction of a second after the input channel becomes TRUE. In the worst case, assume that several seconds could elapse before the test run actually stops.

Input Channel
The input channel data type must be 8-bit unsigned (logical).

Output Data Type
The output channel data type is 8-bit unsigned (logical).

Application Note: Stopping a Test After a Defined Time Period
To stop a test run after a certain amount of run time, do the following: Define a Time Channel computed channel (see "Time Channel" on page 156) and select the 32-bit float data type option. Then define a Desk Calculator computed channel (see "Desk Calculator" on page 136) with an expression such as `ElapsedTime >= 600`, where `ElapsedTime` is the ID of the Time Channel, and 600 seconds is the desired test run duration.
To limit the data stored in any DataMode to the exact test run duration specified, use the gate triggering options, using the Desk Calculator computed channel defined above as the trigger channel.

7.4 Time, Sample Rate and Filter Computed Channels

7.4.1 Time Channel

The Time Channel provides a time base channel for use with other computed channels or for storage in the Time History (see "Time History" on page 167) and Peak/Valley Slice (see "Peak Valley Slice" on page 172) DataModes. For each data sample in the selected input channel, the channel outputs the corresponding elapsed time in seconds since the start of the test run. The first sample is at time equal to zero seconds.

Input Channel
The input channel can be any data type.

Output Data Type
Select an output data type of 32-bit float or 32-bit unsigned.

NOTE
Time channels are unique in that the selected data type determines the data type used in the DataModes.

Use 64-bit Float for Sum
Select the 64-bit float for sum option to minimize the limited precision error that results from using the 32-bit float data type. This error becomes more significant for tests of long duration.

7.4.2 Time Base Shifter

The Time Base Shifter channel generates an output channel that either leads or lags the selected input channel by a user defined number of samples.
Note that the channel fills the first n+1 output samples with the initial value of the input channel.

Input Channel
The input channel can be any data type.

Output Data Type
The output data type is the same as the input data type.

Shift Direction
Select the output channel shift direction to either lag or lead the input channel by the specified shift count.

Shift Count
Specify the number of samples between 1 and 1000 for the output channel to lead or lag the input channel.

7.4.3 Down Sampler

The Down Sampler channel reduces the number of samples taken from the input channel by a user-defined factor, simulating a lower sample rate and decreasing the amount of memory needed data storage. For example, a factor of three causes the channel to output one out of three input samples as illustrated below.

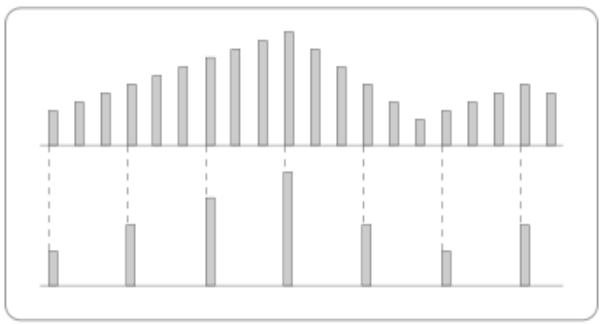


Figure 7-1: An illustration of the Down Sampler computed channel.

NOTE
Use the Down Sampler only when data values in the input channel change slowly and the possibility of losing significant data is minimal.

Input Channel
The input channel can be any data type.

Output Data Type
The output data type is the same as the input data type.

Factor
Specify the desired down sample factor.

7.4.4 Up Sampler

The Up Sampler channel increases the number of samples taken from the input channel by a user-defined factor, enabling correlation of input data with that of a channel with a higher sample rate on a point-for-point basis. Each input channel sample repeats a number of times during the interval between the first sample and the next one based on a conversion factor value. For example, a factor of three causes the channel to repeat the sample twice after the original, giving three samples per original sample as shown in the graphic below.

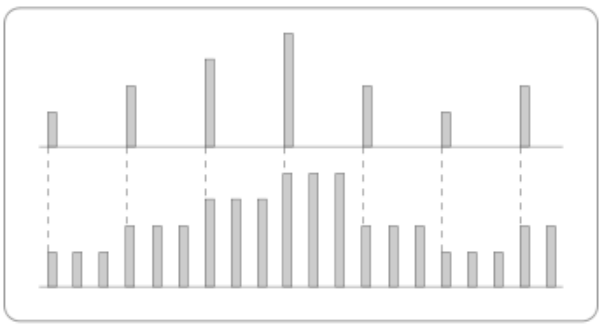


Figure 7-2: An illustration of the Up Sampler computed channel.

NOTE
Storing the output in memory increases the memory required for test data proportional to the up factor. Using the output only for intermediate calculations does not affect data storage memory.

Input Channel
The input channel can be any data type.

Output Data Type
The output data type is the same as the input data type.

Factor
Specify the desired up sample factor.

7.4.5 Smoothing Filter

The Smoothing Filter channel generates an output channel that is a smoothed representation of the input channel without generating any phase lead or lag. The filter is a simple boxcar filter where each output sample is the linear average of a user-specified number of input samples. For example, for a tap count of five, the filter averages the current sample, the two samples before and the two samples after. Note

that the channel backfills the initial output samples with the first fully filtered output value. For example, if the tap count is nine, the first four output samples are assigned the same value as the fifth output sample value.

NOTE
The Smoothing Filter can result in loss of data significance if not used properly. In general, it should not be necessary for analog input channels that use digital anti-aliasing filters. It is provided primarily for digital pulse counter inputs.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer.

Output Data Type
The output data type is the same as the input data type.

Filter Length
Specify the desired length of the boxcar filter. The number must be an odd number between 3 and 201.

7.4.6 Digital Filter

The Digital Filter computed channel generates an FIR digitally filtered output channel based on an ASCII file. The file format conforms to the conventions used by MATLAB® to generate ASCII filter files including the following:

- All fields are floating point values, using only whitespace delimiters (e.g., spaces, tabs, newlines etc.).
- The first field is the number of tap coefficients. There must be at least two taps.
- The second field is the filter delay which synchronizes the filtered output data with the input data. The value can range from zero to the number of taps minus one.
- The third field is the filter gain. This field is optional in the sense that TCE does not use it directly. However, it does provide a check. If the gain value is not 0.0, then TCE checks the gain value against the sum of the tap coefficients and reports any significant conflict.
- The remaining fields are the ordered array of tap coefficients.

Numerous examples are available in the TCE installation kit. See the files in the hsfilter and sfilter subdirectories under the main TCE install directory.

Digital Filter Processing Notes

- In the steady-state, the taps coefficients are multiplied by the input data sample values and these products are summed to form a single filtered data output value. This process is obviously computationally intensive if there are a large number of taps.
- If the filter delay is greater than zero (which is typically the case), the first output samples cannot be fully filtered. The eDAQ backfills these first output samples using the first fully filtered data value. For example, if the delay is nine, the first nine output samples are assigned the same value as the tenth output sample value.

Input Channel
The input channel data type must be 32-bit float.

Output Data Type
The output channel data type is 32-bit float.

File
Specify the full path name of the ASCII file that defines the filter. Use the browse button to select the desired file. Use the check file option to parse the ASCII file and verify that the format is valid.

NOTE
Because TCE parses the ASCII file at test initialization, any changes to the file prior to initialization are effective for subsequent test runs.

Normalize
Select the normalize tap coefficients option to normalize all tap coefficients for a unity gain.

7.5 Tracking Computed Channels

7.5.1 Max Track

The Max Track channel generates an output channel that tracks the maximum value of the input channel. A logical channel specified as a trigger can reset the output channel tracking.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer.

Output Data Type
The output data type is the same as the input data type.

Enable Triggered Reset
Select the triggered reset option to enable triggered resets of the tracker.

NOTE
Resetting the tracker sets the maximum value to the current sample value.

Trigger Channel
If using the reset enable feature, specify the desired trigger channel.

Trigger Mode
If using the reset enable feature, specify one of three available trigger reset modes.

Trigger Mode	Description
When TRUE	Reset when the trigger channel is TRUE.
On FALSE-TRUE edge	Reset when the trigger transitions from FALSE to TRUE.
On TRUE-FALSE edge	Reset on the sample after the trigger channel transitions from TRUE to FALSE.

7.5.2 Min Track

The Min Track channel generates an output channel that tracks the minimum value of the input channel. A logical channel specified as a trigger can reset the output channel tracking.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer.

Output Data Type
The output data type is the same as the input data type.

Enable Triggered Reset
Select the triggered reset option to enable triggered resets of the tracker.

NOTE
Resetting the tracker sets the minimum value to the current sample value.

Trigger Channel
If using the reset enable feature, specify the desired trigger channel.

Trigger Mode
If using the reset enable feature, specify one of three available trigger reset modes.

Trigger Mode	Description
When TRUE	Reset when the trigger channel is TRUE.
On FALSE-TRUE edge	Reset when the trigger transitions from FALSE to TRUE.
On TRUE-FALSE edge	Reset on the sample after the trigger channel transitions from TRUE to FALSE.

7.5.3 Range Track

The Range Track channel generates an output channel that tracks the range of the input channel. A logical channel specified as a trigger can reset the output channel tracking.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer.

Output Data Type
The output data type is 32-bit float if the input channel data type is 32-bit float and 16-bit unsigned if the input channel data type is 16-bit integer.

Enable Triggered Reset
Select the triggered reset option to enable triggered resets of the tracker.

NOTE
Resetting the tracker sets the range value to zero.

Trigger Channel
If using the reset enable feature, specify the desired trigger channel.

Trigger Mode
If using the reset enable feature, specify one of three available trigger reset modes.

Trigger Mode	Description
When TRUE	Reset when the trigger channel is TRUE.
On FALSE-TRUE edge	Reset when the trigger transitions from FALSE to TRUE.
On TRUE-FALSE edge	Reset on the sample after the trigger channel transitions from TRUE to FALSE.

7.5.4 Anomaly Detect

The Anomaly Detect channel generates an output marking possible anomalies in transducer or computed channel data flow. The eDAQ continuously tracks the selected parameters in the analysis window of a user-defined size and outputs a status byte for each window. Each bit in the status byte corresponds to a particular anomaly detection routine. Use with a Bitmap Trigger computed channel to generate triggers based on the anomaly detection. For more information on the Bitmap Trigger computed channel, see “Bitmap Trigger” on page 155.

Bit	Routine	Description
Bit 1	Flat line	Determine if the data is nearly constant over a user-defined time period.
Bit 2	Drift	Determine if the data mean drifts from the start of the test run.
Bit 3	Limit	Determine if the data exceeds user-defined maximum or minimum limits.
Bit 4	Kurtosis	Detection determine if the data exceeds the user-defined kurtosis coefficient limit.
Bits 5 through 8 are reserved for future expansion.		

The units parameter is always logic and the full-scale min is fixed at zero. The full-scale max is the integer value of the largest possible output byte. For example, if using the kurtosis and drift detection routines, the highest active bitmap is binary 00001010, which equals ten.

Input Channel
The input channel data type must be 32-bit float.

Output Data Type
The output channel data type is 8-bit unsigned (bitmap). The only computed channel or DataMode that accepts a bitmap input is the Bitmap Trigger computed channel.

Window Samples
Specify the number of input samples to to generate one output sample. This sets the analysis window size and associated output sample rate. The factor can be any positive integer greater than one.

Flat Line Detect
Select the flat line detect routine to enable flat line detection. If the difference between the maximum and minimum data samples in the analysis window is less than the specified range gate, bit 1 of the output byte is set to 1.

Drift Detect
Select the drift detect routine to enable drift detection. TCE sets the reference mean as the mean value of the first window for each test run. If the difference between the current window mean and the reference mean exceeds the specified mean gate, bit 2 of the output byte is set to 1.

Limit Detect
Select the limit detect routine to enable limit detection. If any data sample in the analysis window is greater than the specified maximum limit or less than the specified minimum limit, bit 3 of the output byte is set to 1.

Kurtosis Detect
Select the kurtosis detect routine to enable kurtosis detection. If the kurtosis coefficient for the data in the analysis window is greater than the specified maximum limit, then bit 4 of the output byte is set to 1. The eDAQ uses the following equation to calculate the kurtosis coefficient:

$$K = N\sum_{i=1}^{N}(x_i - x_{mean})^4 / \{\sum_{i=1}^{N}(x_i - x_{mean})^2\}^2$$

where, *N* is the number of data samples in the analysis window and x_{mean} is the mean of the data samples in the analysis window.

7.5.5 Valid Data Gate

The Valid Data Gate channel generates a logical channel data stream on a sample by sample basis marking samples containing invalid data. The output sample is TRUE if and only if the data samples for all input channels are valid; otherwise, the output sample is FALSE. Use the Valid Data Gate channel by itself or in conjunction with other logical channels as a gate trigger for DataModes to eliminate any invalid data samples.

Input Channel
The only channels that currently use invalid flags are vehicle bus, serial bus, GPS and temperature channels. All data types are supported.

Output Data Type
The output channel data type is 8-bit unsigned (logical).

8 DataModes™

This chapter details the available DataModes and their associated parameters and discusses data storage and memory considerations. DataModes determine how the eDAQ stores and displays test data. A DataMode definition consists of a list of input channels, a data storage/processing rate, triggering conditions and other parameters specific to the DataMode.

8.1 DataMode™ Memory Consumption

The defined DataModes determine the rate at which the eDAQ consumes memory. There is some overhead for storing the test setup file and other eDAQ files, but typically these files require much less that 1 MB for most large channel count test setups and proportionately less for tests with fewer channels.

For SIE data files, there is additional overhead for the data file internal linkage and consistency check parameters. The overhead is usually insignificant, consuming only a few percent of the data file.

For SIF data files, there is additional overhead for the data file header information and internal pointers. This overhead is usually fairly insignificant, consuming only a few percent of the data file. However, there are some situations where this overhead can become very significant. In particular, the overhead in storing burst data records in the Burst History DataMode (see “Burst History” on page 168) can be very significant when a small number of burst points (less than 100) is specified. Also, a large number of short test runs can significantly add to the overhead required.

Different DataModes and data type compression modes require different amounts of memory. The eDAQ consumes raw data storage memory, excluding overhead, as detailed in the following table.

DataMode	Data Type	Memory Consumption
Sequential	32-bit float	4 bytes per data point per channel
	16-bit integer	2 bytes per data point per channel
	8-bit integer	1 byte per data point per channel
Histogram	32-bit unsigned	4 bytes per bin per channel

NOTE

The Rainflow DataMode (see “Rainflow” on page 175) adds 4096 bytes of 32-bit float data per channel for the rainflow stack size.

8.2 Common DataMode™ Parameters

ID

Unique identifier for the channel. This must conform to ID naming conventions. Valid ID names:

- are case sensitive
- are limited to a maximum of 12 characters

- contain only valid characters (i.e., letters (a-z, A-Z), digits (0-9), and the underscore (_) character)
- start with a letter
- are not duplicates of system reserved names (sin, cos, log, etc.)

Input Channel
Select the input channel or channels to the DataMode. The total number of input channels for any DataMode is limited to 256. Use multiple DataModes for more than 256 input channels. All input channels to a single DataMode must have the same sample rate and be defined for the same network node. For a summary of the data types compatible with each DataMode, see “Data Types” on page 195.

Network Node
This field displays the defined network node for the DataMode.

Triggering Option
Select one of four available triggering options. Triggering provides a mechanism for eliminating undesired segments of the input data stream before it is processed by any particular DataMode algorithm.

Triggering Option	Description
Always On	Do not use triggering. Data sampling is always on from the start of the test.
Trigger	Data sampling starts when the trigger channel becomes TRUE. Once the trigger channel is TRUE, data sampling runs continuously, irrespective of any future changes in the trigger channel.
Gate	Data sampling occurs if and only if the trigger channel is TRUE. Data sampling stops when the trigger channel is FALSE.
One Shot	Take a single data sample when the trigger channel transitions from FALSE to TRUE or if the trigger channel is TRUE on the first sample of any run.

Trigger Channel
Specify the trigger input when using a trigger option other than always on.

NOTE
The optional trigger channel must have the same sample rate as the set of input channels to the DataMode.

Data Storage
Select whether to store test data on the RAM disk or on the PC Card media (external PC Card, DRAM or internal Flash) as selected in the web interface. For more information on data storage options, see "Data Storage Options" on page 36.

NOTE
The eDAQ does not support storing SIE data on the RAM Disk. Regardless of the data storage setting, the eDAQ saves SIE data to the storage device selected in the web interface. If the PC Card storage device is selected and there is no PC Card in the eDAQ, the TCE cannot initialize the test.

Data Storage Option	Description
PC Card	The eDAQ stores all data in a file on the PC Card file system media. For SIF data collection, other file components, such as the header file and keywords, are stored on the RAM disk. For histogram DataModes, the eDAQ maintains the histogram data in DRAM memory while the test is running and then copies the data to a file on the PC Card after test completion.
RAM disk (SIF only)	The eDAQ builds the SIF data file in RAM disk memory.

For more information on data storage options, see Data Storage.

8.3 Sequential DataModes™

8.3.1 Time History

The Time History DataMode stores multiple channels of triggered or un-triggered time history data streams in the output data file.

NOTE
If using the trigger, gate or one shot trigger conditions, the *x*-axis label in InField is collection time to distinguish from the time from the start of the test run. If using the always on trigger condition, the label is simply time.

CAUTION
If the setup file has a Time History DataMode that uses any trigger channel and if an eDAQ error reset occurs while a test run is in progress, some of the acquired Time History data will be lost. The maximum amount of data that can be lost is the data frame size for the Time History input channels. For example, if the sample rate is 100 Hz and the pipe frame size is 2.5 Hz, then the frame size is 40 data samples. While this is not a big number, it can represent significant data losses if using the one shot trigger mode to capture rare events.

Input Channel
The input channels can be any data type.

Data Type
For 32-bit float input channels, select one of three available formats for data storage and conversion.

Data Type	Description
32-bit float	No conversion is necessary. Use the 32-bit float mode for computed channels where full-scale estimates are uncertain or unknown.
16-bit integer	Maintain the resolution of both the 12-bit and 16-bit A/D converters.
8-bit integer	Lose significant resolution in both the 12-bit and 16-bit A/D converters. Use the 8-bit integer mode only for a rough picture of channel behavior.

NOTE
Using the integer data types requires that valid full-scale minimum and maximum values are defined for each input channel selected for the DataMode.

8.3.2 Burst History

The Burst History DataMode stores one or more bursts of data when a user-defined triggering event occurs. The term burst refers to a set of contiguous data samples. The Burst History DataMode is particularly useful for characterizing rare events at high data sampling rates. The eDAQ uses a circular buffer to allow storage of data both before and after the specified trigger.

NOTE
The total number of points stored is the sum of the post-trigger and pre-trigger time periods multiplied by the selected data sampling rate plus one since the trigger sample is always stored.

Input Channel
The input channels can be any data type.

Data Type
For 32-bit float input channels, select one of three available formats for data storage and conversion.

Data Type	Description
32-bit float	No conversion is necessary. Use the 32-bit float mode for computed channels where full-scale estimates are uncertain or unknown.
16-bit integer	Maintain the resolution of both the 12-bit and 16-bit A/D converters.
8-bit integer	Lose significant resolution in both the 12-bit and 16-bit A/D converters. Use the 8-bit integer mode only for a rough picture of channel behavior.

NOTE
Using the integer data types requires that valid full-scale minimum and maximum values are defined for each input channel selected for the DataMode.

Post-Trigger Time
Specify the desired period of time in seconds for data sampling after the trigger.

Pre-Trigger Time
Specify the desired period of time in seconds for data sampling before the trigger.

Number of Bursts
Specify an upper limit on the number of bursts the eDAQ can store. The DataMode effectively turns off after storing this number of bursts.

NOTE
Using the max bursts mode option limits the number of bursts to 250.

Max Bursts Mode
Select enable max bursts mode to store the most significant burst records according to the following criteria. After storing the user-defined maximum number of burst records, the eDAQ compares each new burst record to the least significant burst already stored. If the new burst is more significant, the eDAQ overwrites the least significant burst record with the new burst record, retaining the most significant burst records. The max bursts mode adds significant processing overhead.

NOTE
The max bursts mode option is not available if using the PC Card data storage mode.

Max Bursts Reference Value
Specify the reference value used in determining burst significance for the max bursts mode.

DRAM Buffering
Selecting the DRAM buffering mode allocates the circular buffer used for burst data capture in DRAM memory. Otherwise, the eDAQ allocates the circular buffer directly on the Linux file system media. DRAM buffering is only available when using the external PC Card or internal CompactFlash memory for data storage.

NOTE
SIE file data always uses the DRAM buffering option.

CAUTION
All test data in DRAM memory is lost if the eDAQ powers down or resets for any reason.

Selecting the DRAM buffering option is advised as long as the DRAM allocations required are not too large. Updating the circular buffer allocated in DRAM is very efficient as is copying the circular buffer filled with a burst record to the PC Card memory in a linear manner.
Allocating, the circular buffer directly in the PC Card file system memory is somewhat less efficient in general because of the overhead in constantly writing to the PC Card memory. Furthermore, for rotating disks, the seeks required when the circular buffer wraps around will adds a periodic burden to performance efficiency. Also note that repetitively overwriting the same flash memory area produces wear and reduces the life of the flash memory.

NOTE
When considering DRAM buffering, note that the eDAQ can only copy full burst records for DRAM to PC Card memory. Not using the DRAM buffering mode allows the eDAQ to store partial burst records if, for example, the test run stops before the burst is full.

Application Note: Guidelines for Setting the DRAM Buffering Option
If the total DRAM allocation for all Burst History channels for a single burst record is 500 kB or less, selecting the DRAM option is advised for maximum throughput efficiency. If the total DRAM allocation is 4 MB or more, then selecting the DRAM option is not advised and can cause a DeviceOverFlow error when the eDAQ attempts to copy the DRAM buffers to the PC Card memory. For the gray area in the 500 kB to 4 MB range, first try not using the DRAM buffers.
Examples:

- Do not use DRAM buffering: One Burst History DataMode defined with 16 channels of 16-bit integer data sampled at 1000 Hz for 600 seconds requires 9200000 bytes (16*2*1000*600) per burst record.

- Use DRAM buffering: One Burst History DataMode defined with 16 channels of 16-bit integer data sampled at 500 Hz for 20 seconds requires 320000 bytes (16*2*500*20) per burst record.
- Try not using DRAM buffering: One Burst History DataMode defined with 16 channels of 16-bit integer data sampled at 500 Hz for 10 seconds requires 320000 bytes (16*2*500*20) per burst record and a second burst DataMode defined with 8 channels of 32-bit float data sampled at 2000 Hz for 10 seconds requires 640000 bytes (8*4*2000*10) per burst record for a total of 960000 bytes.

8.3.3 Event Slice

The Event Slice DataMode stores a set of master channels and a set of slave channels in the output data file. The set of master channels provides a sequence of events, which are defined as changes in the state of any master input channel. For each event, the eDAQ stores data samples for all channels (masters and slaves) in the output data file.

Master Input Channels

Select the desired set of master input channels using CTRL to select more than one channel. The master input channels can be any data type.

Slave Input Channels

Select the desired set of slave input channels using CTRL to select more than one channel. The slave input channels can be any data type.

Data Type

For 32-bit float input channels, select one of three available formats for data storage and conversion.

Data Type	Description
32-bit float	No conversion is necessary. Use the 32-bit float mode for computed channels where full-scale estimates are uncertain or unknown.
16-bit integer	Maintain the resolution of both the 12-bit and 16-bit A/D converters.
8-bit integer	Lose significant resolution in both the 12-bit and 16-bit A/D converters. Use the 8-bit integer mode only for a rough picture of channel behavior.

NOTE

Using the integer data types requires that valid full-scale minimum and maximum values are defined for each input channel selected for the DataMode.

Time Input Channel

Optionally, select a Time Channel computed channel from the provided list. For more information on the Time Channel computed channel, see “Time Channel” on page 156).

Store Initial State

Set the store initial state parameter to yes to always store the initial state at the start of each test run.

8.3.4 Message Logger

Use the Message Logger DataMode to store input message channels in the data file.

NOTE

The Message Logger supports the PC Card data storage option only.

Input Channel

The input channel is limited to message channel sources, which are all 8-bit unsigned.

8.3.5 Peak Valley

The Peak Valley DataMode stores multiple channels of peak and valley sequences in the output data file. The eDAQ acquires peaks and valleys from triggered or un-triggered time history data streams using the user-specified hysteresis value and the peak valley processing algorithm. For more information on the peak valley processing algorithm, see “Peak Valley Processing Algorithm” on page 243.

Input Channel

The input channel data type must be 8-bit integer, 16-bit integer or 32-bit float.

Data Type

For 32-bit float input channels, select one of three available formats for data storage and conversion.

Data Type	Description
32-bit float	No conversion is necessary. Use the 32-bit float mode for computed channels where full-scale estimates are uncertain or unknown.
16-bit integer	Maintain the resolution of both the 12-bit and 16-bit A/D converters.
8-bit integer	Lose significant resolution in both the 12-bit and 16-bit A/D converters. Use the 8-bit integer mode only for a rough picture of channel behavior.

NOTE

Using the integer data types requires that valid full-scale minimum and maximum values are defined for each input channel selected for the DataMode.

Hysteresis

Specify the desired hysteresis level for the peak valley processing algorithm.

8.3.6 Peak Valley Slice

The Peak Valley Slice DataMode stores a set of master channels and a set of slave channels in the output data file. The set of master channels provides a peak/valley sequence acquired using the user-specified hysteresis value and the peak valley processing algorithm. For each peak or valley on any master channel, the eDAQ

stores data samples for all channels (master and slaves) in the output data file. For more information on the peak valley processing algorithm, see “Peak Valley Processing Algorithm” on page 243.

NOTE
If no slave channels are required, it is more efficient to use the Peak Valley DataMode (see “Peak Valley” on page 172).

Master Input Channel
Select the desired set of master input channels using CTRL to select more than one channel. The master input channel data type must be 8-bit integer, 16-bit integer or 32-bit float.

Slave Input Channel
Select the desired set of slave input channels using CTRL to select more than one channel. The slave input channels can be any data type.

Data Type
For 32-bit float input channels, select one of three available formats for data storage and conversion.

Data Type	Description
32-bit float	No conversion is necessary. Use the 32-bit float mode for computed channels where full-scale estimates are uncertain or unknown.
16-bit integer	Maintain the resolution of both the 12-bit and 16-bit A/D converters.
8-bit integer	Lose significant resolution in both the 12-bit and 16-bit A/D converters. Use the 8-bit integer mode only for a rough picture of channel behavior.

NOTE
Using the integer data types requires that valid full-scale minimum and maximum values are defined for each input channel selected for the DataMode.

Time Input Channel
Optionally, select a Time Channel computed channel from the provided list. For more information on the Time Channel computed channel, see “Time Channel” on page 156.

Plateau Size
Specify the criterion for storing a peak or valley candidate slice as a plateau event. The size refers to the minimum number of peak and valley slices in the holding queue that must exist before the eDAQ stores the blocking peak or valley candidate slice as a plateau event. For example, if the plateau size is 50, then at least 50 peak and valley slices must exist in the holding queue before treating the blocking peak or valley

candidate slice as a plateau. Note that for most typical usages of the Peak/Valley Slice DataMode using multiple master channels, there will be very few (if any) slices stored on this plateau criterion.

Hysteresis
Specify the desired hysteresis level for the peak valley processing algorithm.

8.4 Histogram DataModes™

8.4.1 Common Histogram Parameters

Accumulate Runs Across All Tests
Selecting the accumulate runs across all tests option generates one histogram for all test runs. Otherwise, the eDAQ generates a unique histogram for each run.

NOTE
The option to accumulate across all test runs is available only when using the eDAQ RAM storage option with the SIF data format.

Histogram Bin Type
Select evenly-divided or user-defined bin types. Each histogram bin can accumulate counts up to 4294967295.

Bin Type	Description
Evenly Divided	The width of each bin is equal. The default histogram limits for each input channel are based on the defined full-scale values for the input channel. The bin size is simply the difference between the histogram limits divided by the number of bins. Use the slider in the histogram bin editor to select the number of bins.
User Defined	The width of each bin is defined independently. Use the buttons in the histogram bin editor to add or delete bins. Define the bin boundaries for each dimension of the histogram in the histogram window.

NOTE
For either of the bin types, the eDAQ uses underflow and overflow bins to count the occurrences that fall outside of the defined histogram limits.

Number of Bins
Select the desired number of bins for each histogram. See the entry for each DataMode for specific information on the number of bins for each DataMode.

8.4.2 Peak Valley Matrix

The Peak Valley Matrix DataMode stores multiple channels of peak valley reversal histograms in the output data file. The eDAQ acquires peaks and valleys from triggered or un-triggered time history data streams using the user-specified hysteresis value and the peak valley processing algorithm. The resulting peak valley stream

defines the set of peak valley reversals which are histogrammed using the user-defined options for the type and size of histogram. For more information on the peak valley processing algorithm, see “Peak Valley Processing Algorithm” on page 243.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer. If using the user-defined bins option, the input channel data type must be 32-bit float.

Histogram Mode
Select one of three available histogramming modes.

Mode	Description
Range-Mean	Accumulate reversal counts in bins with both a reversal range dimension and a cycle mean value dimension.
Range Only	Accumulate reversal counts in bins with only a reversal range dimension.
To-From	Accumulate reversal counts in bins with both a to dimension and a from dimension. The eDAQ assigns to and from designations to each reversal.

Hysteresis
Specify the desired hysteresis level for the peak valley processing algorithm.

Number of Bins
Specify the desired number of bins up to 500 for the histogram. For the range-mean and the to-from histogram modes, the value is for both histogram dimensions. The total number of bins per dimension is the user-specified number of bins plus two for underflow and overflow bins. For the range-mean and to-from histogram modes which have two dimensions, the total number of bins for the DataMode is the product of the total number of bins for each dimension.

8.4.3 Rainflow

The Rainflow DataMode stores multiple channels of rainflow cycle histograms in the output data file. The eDAQ acquires peaks and valleys from triggered or un-triggered time history data streams using the user-specified hysteresis value and the peak valley processing algorithm. The resulting peak valley stream runs through the rainflow cycle counting algorithm to yield the set of closed cycles. The closed cycles are histogrammed using the user-defined options for the type and size of histogram. For more information on the data processing algorithms used, see “Data Processing Algorithms” on page 243.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer. If using the user-defined bins option, the input channel data type must be 32-bit float.

Histogram Mode
Select one of three available histogramming modes.

Mode	Description
Range-Mean	Accumulate cycle counts in bins with both a cycle range dimension and a cycle mean value dimension.
Range Only	Accumulate cycle counts in bins with only a cycle range dimension.
To-From	Accumulate cycle counts in bins with both a to dimension and a from dimension. The eDAQ assigns to and from designations to the first reversal instead of the second on which the cycle actually closes.

Hysteresis
Enter the desired hysteresis level for the peak valley processing algorithm.

Number of Bins
Specify the desired number of bins up to 500 for the histogram. For the range-mean and the to-from histogram modes, the value is for both histogram dimensions. The total number of bins per dimension is the user-specified number of bins plus two for underflow and overflow bins. For the range-mean and to-from histogram modes which have two dimensions, the total number of bins for the DataMode is the product of the total number of bins for each dimension.

8.4.4 Time at Level (One Dimensional)

The Time at Level (1D) DataMode stores one-dimension Time at Level histograms in the output data file. Specify multiple input channels to generate multiple one-dimensional Time at Level data channels.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer. If using the user-defined bins option, the input channel data type must be 32-bit float.

Number of Bins
Specify the desired number of bins. The total number of bins is the user-specified number of bins plus two for underflow and overflow bins.

8.4.5 Time at Level (Multidimensional)

The Time at Level (mD) DataMode stores a multiple-dimension Time at Level histogram in the output data file.

Input Channel
The input channel data type must be 32-bit float or 16-bit integer. If using the user-defined bins option, the input channel data type must be 32-bit float.

Number of Bins
Select the desired number of bins for each dimension. Separate the individual bin count specifications by spaces or commas. The total number of bins for each dimension is the user-specified number of bins plus two for underflow and overflow bins. The total number of bins for the DataMode is the product of the total number of bins for each dimension. For example, defining the number of bins for four input channels as 10, 20, 5 and 15 results in 31416 (i.e. 12*22*7*17) total number of bins.

8.5 Digital Output

A Digital Output is a pseudo-DataMode. Digital outputs are compatible with the first eight bits on each EDIO bank and any digital bit on the ECPU. For more information on EDIO digital outputs, see “Digital Input/Output” on page 97.
Use the Digital Output definition window for each layer to define all desired digital outputs for that layer. For each desired output target bit, specify the associated logical control channel, output mode, initial state and stop run action. Use the control channel select area of the window or type the desired values directly into the digital output list.

NOTE
When using the control channel select area, double click the desired logical channel to complete each digital output definition.

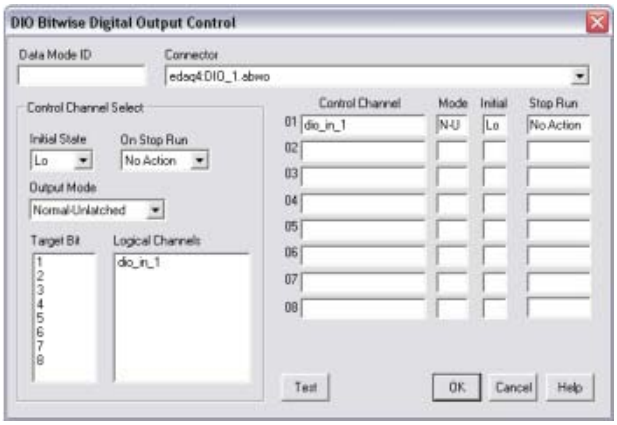


Figure 8-1: TCE Digital Output DataMode definition window.

Use the Test button to open a window for testing the digital output bits and the devices tied to the output lines. The test window contains a set of check boxes corresponding to the set of available digital output lines. Check or uncheck the desired bits and select Set Bits to set the digital output lines based on the bit selections. A checked box sets the output to high (TRUE) and an unchecked box sets the output to low (FALSE).

Target Bit

Select the desired digital output bit on the selected connector. A bit must be configured as an output using the ECPU or EDIO configuration options. If a selected bit is configured as an input, TCE issues a warning. For more information on configuring digital bits as outputs on the EDIO layer, see “Configuration Options” on page 97.

Control Channel

The control channel specifies the logical input channel to drive the digital output. Use the presented list to select any defined logical channel with a data type of 8-bit unsigned (logical).

Initial State

For each digital output, select the initial state as either high (TRUE) or low (FALSE). The eDAQ imposes the initial state at the start of the test run.

Stop Run Action
For each digital output, select the desired action when the test run stops.

Stop Run Action	Description
No Action	Do not change the output line when the test run stops.
Set Hi	Set the output line to high (TRUE) when the test run stops.
Set Lo	Set the output line to low (FALSE) when the test run stops.

Output Mode
Each digital output has five available output modes. The sample interval is the time period associated with the sample rate of the input channels. Since the input channels defined in the data mode can have different sample rates, the sample interval can vary from channel to channel. The abbreviation used in the channel definition is in parentheses.

Output Mode	Description
Normal-Unlatched (N-U)	Output TRUE if the sample interval contains a TRUE value; otherwise, output FALSE.
Invert-Unlatched (I-U)	Output FALSE if the sample interval contains a TRUE value; otherwise, output TRUE.
Normal-Latched (N-L)	Output TRUE and hold through the end of the test if the sample interval contains a TRUE value.
Invert-Latched (I-L)	Output FALSE and hold through the end of the test if the sample interval contains a TRUE value.
Toggle-Latched (T-L)	Toggle output between TRUE and FALSE for every sample interval containing a TRUE value. The toggle rate is nominally one second.

9 eDAQ Web Interface

The eDAQ web interface provides controls to activate saved test initializations, start and stop test runs, monitor test status, and end initialized tests. The web interface can also perform a number of system configuration and other utility operations, including formatting PC Cards, modifying ethernet and serial communication settings, and upgrading eDAQ firmware with new version releases.

9.1 Main Page

With a TCP/IP connection between the support computer and eDAQ, enter the eDAQ's IP address into any web browser to access the main page of the eDAQ web interface.

Figure 9-1: Main page of the eDAQ web interface.

The information bar across the top of the page displays the eDAQ's IP address, the date and time that the page was loaded and a battery status indicator. When a test is initialized, the information bar also indicates the name of the test setup, the run number and either a go control when the test is stopped or a stop control when a test is running. Refresh the page to update the displayed information as the interface does not automatically refresh.

The tab menu just below the information bar provides access to categories of available operations. Open the page for each category by clicking on the appropriate tab. The subsequent sections of this chapter describe the available operations.

9.2 System Tab

The System tab provides several tools for setting up, maintaining and monitoring the eDAQ.

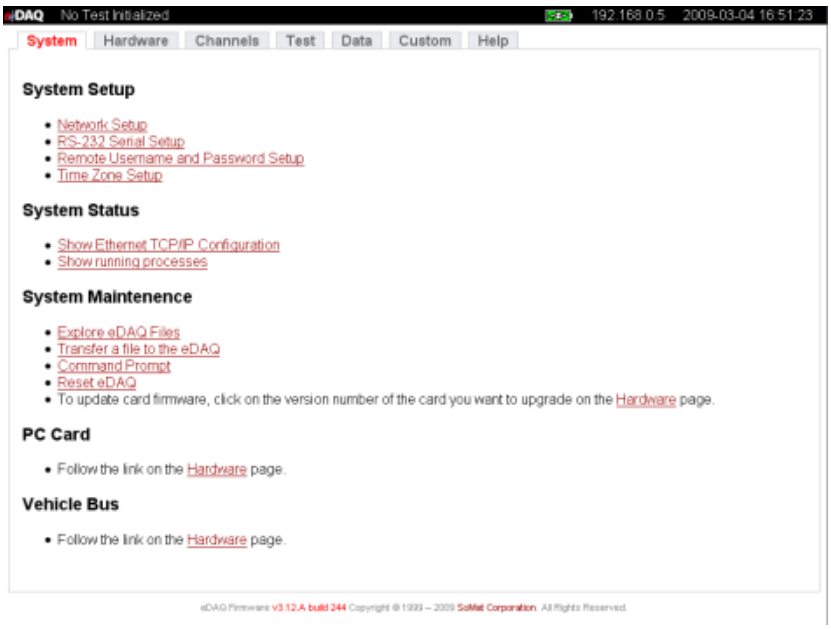


Figure 9-2: System tab of the eDAQ web interface.

9.2.1 System Setup

The system setup group of pages provide methods to modify the network configuration parameters, RS-232 communication parameters, remote user name and password and the time zone in which the eDAQ resides.

Network Setup

Use network setup parameters to modify the host name, IP number, netmask and gateway as required.

RS-232 Setup

Set the serial communication parameters within the eDAQ by modifying file pgetty.conf, the file containing all configuration information for serial communication.

CAUTION

Errors within pgetty.conf can cause all serial communication to cease to function. Use extreme caution when modifying this file.

Remote Username and Password Setup

Set the usernames and passwords that are allowed remote access to the eDAQ through a dial-up connection. To make changes to this setup, modify the file as needed. In the default configuration shown below, “ppp” is the remote username and “123” is the password for that user.

Time Zone Setup

Set the current time zone in which the eDAQ resides. The current time zone, local time and universal time (UTC) are provided.

9.2.2 System Status

The system status group of operations provides access to information about the current state of the eDAQ system.

Show Ethernet TCP/IP Configuration
Display information about the current configuration of the ethernet TCP/IP communication system setup.

Show Running Processes
Display a list of the currently running processes on the eDAQ.

9.2.3 System Maintenance

Explore eDAQ Files
Open the eDAQ file system to browse its contents. The copy file option opens the interface for transferring a file from the PC to the eDAQ. The current location within the file system is the default destination path in the copy interface.

Transfer a File to the eDAQ
Open the interface to copy a file from the PC to the eDAQ. Enter the path and file name of the file to copy and the destination path within the eDAQ file system. Click Copy to eDAQ to copy the file.

Command Prompt
Open the command prompt interface that allows direct entry of Linux shell commands to the eDAQ operating system. This operation is for expert use only.

CAUTION
Serious damage to the system can occur through the use of system commands. Therefore, use extreme caution should when entering shell commands.

Reset eDAQ
Perform a programmed reset of the eDAQ unit. Use this option only if necessary, such as when the system is not responding.

9.3 Hardware Tab

The Hardware tab contains information about the hardware contained in the eDAQ stack including the network node associated with the hardware, the type of layer and its serial number, the version number of the code contained in the flash memory and information about the PC Card (if installed).

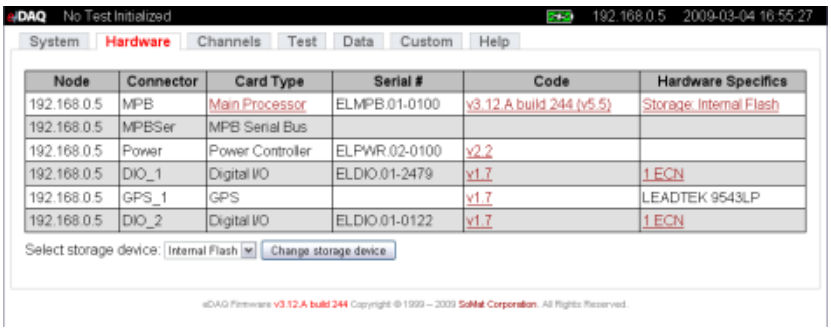


Figure 9-3: Hardware tab of the eDAQ web interface.

9.3.1 Hardware Table

Node
The node column indicates the associated network node by its IP address.

Connector
The connector column indicates the layer identifier prefix used in hardware connector IDs.

Card Type
The card type column shows each layer type. Certain eDAQ layers allow for additional configuration such as enabling message logging and editing of parameter databases. When this additional configuration is available, the card type listed is enabled as a hyperlink and, when selected, opens additional pages for configuration options. The additional configuration available for the vehicle bus layer includes editing parameter databases, importing a vector CANdb database, logging messages, viewing status and resetting the vehicle bus hardware. Navigate to the Help tab for more detailed information on vehicle bus options.

Serial Number
The serial number column indicates the unique serial number of the layer in the stack.

Code
The code column displays the version of the code (i.e., firmware) that controls the layer. To update the code from the web interface, click the hyperlink. For layers that place more than one entry in the hardware list, only one of the entries allows an update to the firmware. For more information on updating firmware, see “Updating Firmware” on page 28.

CAUTION
Failures during a critical point in any upgrade/reflash can cause the hardware to malfunction, requiring its return to HBM for repair by a qualified HBM technician.

Hardware Specifics
The hardware specifics column includes other pertinent details about the layer such as applicable ECNs, the selected storage media or GPS model.
An ECN is an engineering change notice signifying a physical modification made to the hardware of a layer to correct or improve its performance. These changes are recorded in non-volatile memory within the layer. Click the link to view the ECN number and the date of the change.
Use the storage link in the MPB row to view details or reformat the PC Card media.

9.3.2 Select Storage Device

Use the pick list to select PC Card (if installed), internal Flash or DRAM and click Change Storage Device to change the storage media used for test data storage. For more information on eDAQ data storage, see “Data Storage Options” on page 36.

9.4 Channels Tab

The Channels tab provides information about the defined transducer, message and computed channels in the most recently initialized test. The information displayed for the transducer and message channels includes the unique ID, the connector, the transducer type, the sample rate, the calibration date and other information pertinent to the channel. The information displayed for computed channels includes the network node associated with the channel, the unique ID, the prefix, a description and other information pertinent to the channel.

9.5 Test Tab

The test tab provides information about the current test including the name of the setup file, the current or next run number and the elapsed run time. Refresh the page to update the test information.

Test Status
View a summary of test and eDAQ information including test run status, RAM disk files, RAM disk memory and PC Card memory.

View eDAQ Logbook
View the log file maintained on the eDAQ unit. This file contains information on significant eDAQ events (e.g., resets, test initializations, etc.) and the values of pertinent eDAQ state variables. It is available primarily for HBM internal development and field service troubleshooting.

Get TCE Setup File
Transfer the test setup file stored in the eDAQ to a user-specified PC disk file.

USB Display Setup
Set up the values to display on the optional USB LCD display.

Minimal Control Panel
Open a test control panel with the ability to start and stop test runs and upload SIF data. The panel also includes indicators for run number, run time and PC Card memory.

9.6 Data Tab

The Data tab provides access to view and save test data.

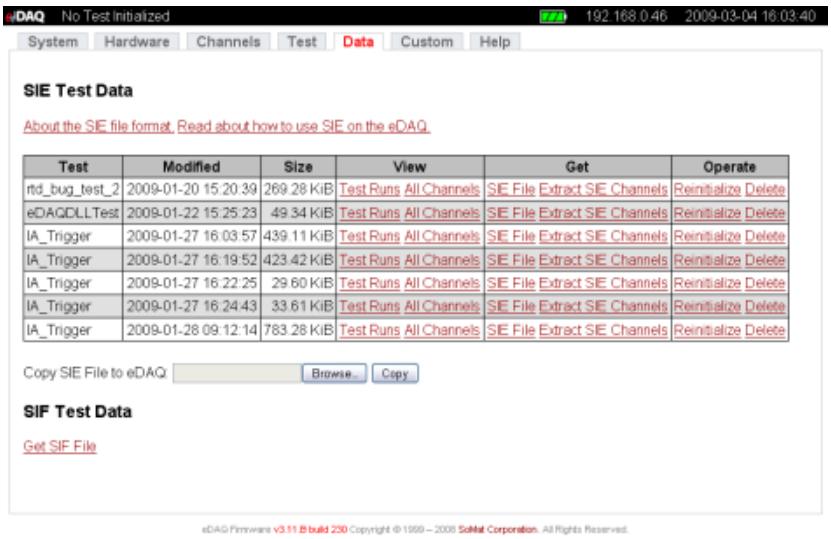


Figure 9-4: Data tab of the eDAQ web interface.

9.6.1 SIE Test Data

The SIE test data table shows all the SIE data files present on the eDAQ. The table shows the name of each file, the date it was modified and options to view, transfer, initialize and delete the file.

In the get column, click SIE File to upload the complete SIE file or Extract SIE Channels to upload only select channel data. In the operate column, select Reinitialize to initialize the eDAQ with the TCE setup file contained in the SIE file or Delete to remove the SIE file from the eDAQ.

Click on Test Runs in the view column to view the test data as a set of test runs with their start and stop times, elapsed time and test description. Click an individual test run to open a table of the channels in the test run. Click All Channels in the view column to display all of the channels in the data file with their descriptions, DatMode types, sample rates and output samples.

When viewing a table of channels, click on Plot in the plot column to view a simple plot of the channel data as a function of time. Click the name of the channel in the name column to view basic channel information and the actual data collected during the test run.

9.6.2 SIF Test Data

Use the get SIF file option to transfer the SIF data file from the eDAQ to the PC. The table lists the completed test runs with the date and time of the run. Clicking on the test run opens a table of channels that displays the run number, channel number, DataMode type, sample rate and number of data points. Click on the channel name to view basic channel information and the actual data collected during the test run. Currently Time History and message channels are the only data types viewable via the web interface.

9.7 Custom Tab

Use the Custom tab to install custom modules, such as a serial bus module, in the eDAQ system. See the installation instructions provided with the firmware installation for information on specific modules.

When custom modules are installed in the eDAQ, the page displays a table with the name and installation path of the module, the current status (enable or disabled) and a list of operations available for the module (enable/disable and remove).
To discuss a custom module created specifically for your company's needs, contact your HBM sales representative.

9.8 Help Tab

The help tab contains links to help topics on using SIE data and vehicle buses.

10 Troubleshooting

10.1 Troubleshooting Procedure

When experiencing unusual problems with the eDAQ, contact HBM customer service for assistance in resolving the situation. Expedite this process by being aware of the tools and indicators available for tracking down problems and performing some actions prior to calling HBM customer service. The following actions are recommended.

Document the problem

If possible, make a detailed note of the conditions under which the problem occurs. It is particularly helpful to know if the problem is repeatable, happens occasionally or happened only once and cannot now be repeated. Providing a test setup file can also expedite the troubleshooting.

Check known problems

Check for the symptom in Known Problems and perform the recommended action. If the problem is not solved, note the results for communication with HBM customer service.

Use the eDAQ error reporting tools

The eDAQ has a significant amount of built in checks to flag error conditions and provide information back to the user or HBM customer service.
Use the following eDAQ reporting tools:

1. Take note of the eDAQ front panel LEDs. When the eDAQ detects an abnormal situation, it responds by turning the red LED on. For more information on the status LEDs, see “Status LEDs” on page 25.
2. With the eDAQ connected to the PC, get the test status using TCE or the web interface. Note any error or status flags and check the eDAQ Flags section for their meaning. In a few cases, the flags may provide sufficient information to understand the problem. For more information on getting the test status, see “Monitoring Test Status” on page 77.
3. View the eDAQ log using TCE or the web interface. The log usually provides more detailed information about the error or status flags and can be useful to HBM customer service. In TCE, the eDAQ log is available from the FCS Setup menu.

Perform diagnostic test

If the eDAQ cannot repeatedly run the FTP diagnostic test without generating any errors, there is most likely a problem with the ECPU, the communication cables or the PC hardware or system configuration. If the errors occur at the same spot each time, the RAM disk memory is the most likely problem. Run an FTP diagnostic test from the Diagnostic submenu in the FCS Setup menu.

Format RAM disk

This is a way of resetting the RAM Disk allocations to a known state. Formatting destroys all files in the RAM Disk memory, including any SIF data file components, so use it with caution. If eDAQ to PC communications can be established, format the RAM disk. The Format RAM Disk option is available from the FCS Setup menu.

10.2 Known Problems

Test data lost or corrupted after power cycling
If the eDAQ data file is lost or corrupted after a power cycle, the main backup battery is most likely not properly charged. Test for a proper charge by turning on the eDAQ and disconnecting the power source. The eDAQ should stay powered from the backup battery for about 45 seconds.

PC Card file system is corrupt
If the PC Card is removed or if the eDAQ loses power during a test run with the PC Card data storage option in use, then the PC Card file system can become corrupted. If this occurs or is suspected, immediately attempt to transfer the test data to the PC using the tools in TCE. If TCE reports corruption or any other anomalies, contact HBM customer service. For more details, see Corrupt SIF File Data Recovery.

10.3 eDAQ Flags

10.3.1 Status Flags

The eDAQ status flags are set only when the eDAQ encounters an abnormal operating condition. These flags do not result in a reboot of the eDAQ.

BadNVRAM
The BadNVRAM flag indicates that the NVRAM flash memory contains invalid data. The NVRAM memory area holds a number of eDAQ configuration parameters, including the default ECPU digital I/O configurations, the master sample rate preference and the eDAQ reset options. When this occurs, the eDAQ resets the NVRAM parameters to their default values.

BootError
The BootError flag indicates that the eDAQ did not complete the boot process. The eDAQ writes additional information to the log file when this occurs. Please report this error to HBM customer service.

CharChecksum
This CharChecksum flag indicates that the checksum stored with eDAQ layer characterization data does not match the checksum computed for the characterization data structure. Data acquired using an invalid characterization data structure is not valid data.

Calibration
The Calibration flag indicates that a transducer calibration or rezero was not completed in the expected manner. The two main reasons for this status flag are faulty hardware and unexpected signal values, such as the voltage exceeding the defined safe limits after rezeroing. The eDAQ generates Calibration errors only on the channels that have programmable gain and offset capabilities (e.g., ELLB, EHLS and EBRG channels).

eDAQReset
The eDAQReset flag indicates any eDAQ reboot. As such, it is simply an informative message only.

MathException
The MathException flag indicates a floating point math exception such as taking the square root of a negative number in a Desk Calculator computed channel. While not a fatal error in itself, it does indicate a situation that is most likely undesirable.

ParityStatus
The ParityStatus flag indicates that there is a recoverable inconsistency in a RAM Disk pointer structure. The RAM Disk pointers are stored in triple redundant fields. If only one of the three pointers is inconsistent, the eDAQ changes it to match the other two and sets this flag. If none of the three pointers are consistent, the eDAQ sets the ParityError flag and resets itself.

PCMAccessError
The PCMAccessError flag indicates that the eDAQ cannot access the PC Card during the start of test initialization, the start of a test run or the restart of a test run after a power failure or an error reset. It is likely that the PC Card has been removed. If this is the case, re-insert the PC Card and initialize or start the test.

PCMDataLosses
The PCMDataLosses flag indicates that a test did not complete the power failure exit procedure or an error reset exit procedure. The flag can only occur if the test is running with the PC Card data storage option. The typical scenario is a power failure with a dead or disconnected backup battery. In almost all cases, this flag indicates loss of some of the test data from the previous run.

PCMDiskError
The PCMDiskError flag indicates that there was a PC Card I/O error while running a test or attempting to transfer data from the eDAQ. It is likely that the PC Card has been removed, been damaged in some way or has had some intermittent problem. Data integrity is suspect.

PCMDiskFull
The PCMDiskFull flag indicates that there is no more PC Card storage space available for test data. DataModes that require additional memory (for example, Time History, Peak/Valley, etc.) are suspended, but histogram DataModes keep running normally. Let the test run continue or stop the test as desired. Note that attempting to start a new test run without sufficient PC Card space to start causes the eDAQ to reboot itself.

PCMSIFCorrupt
The PCMSIFCorrupt flag indicates that the eDAQ has found corruption in the SIF data file component on the RAM Disk. This flag stops the test run and ends the test. Transfer the test data to the PC and reformat the RAM Disk. There can be major losses of test data.

RainFlow
The Rainflow flag indicates a rainflow stack overflow in a Rainflow DataMode channel. The eDAQ shuts down the channel on which the overflow occurred and proceeds in an otherwise normal manner.

RAMDiskFull
The RAMDiskFull flag indicates that there is no more RAM Disk memory available for storing test data. DataModes that require additional memory (e.g., Time History or Peak/Valley) are suspended, but histogram DataModes keep running normally. Let the test run continue or stop the test as desired. Note that attempting to start a new test run without sufficient RAM Disk memory to start causes the eDAQ to reboot itself.

SmartModuleError
The SmartModuleError flag indicates that there is an error in eDAQ communications to a SMART module or there is an error in the SMART module factory or user data parameters. The eDAQ also sets this flag when detecting an unknown type of SMART module based on the serial number.

10.3.2 Error Flags

The eDAQ error flags are set only when the eDAQ detects a serious error. When such an error occurs the eDAQ automatically resets. If a test run is in progress, a new test run may start based on the user-specified FCS Reset Options.

BadRequest
The BadRequest error flag indicates that a serious error condition exits on the eDAQ unit most likely resulting from a hardware failure or a software deficiency. It is unlikely that this error can result from an operator mistake.

CardException
The CardException flag indicates that a type II layer has reported an error status to the eDAQ main processor. As such, it can have several meanings. The eDAQ writes additional information to the log file when this occurs.

DeviceOverFlow
The DeviceOverFlow flag indicates that the defined test exceeds the eDAQ unit's processing capabilities. This may occur when many channels are taking data at very high sample rates or large numbers of computed channels are defined. For a thorough discussion of this problem, see Tips on Eliminating eDAQ OverFlow Errors.

Internal
The Internal error flag indicates that a serious error condition exits on the eDAQ unit most likely resulting from a hardware failure or a software deficiency. It is unlikely that this error can result from an operator mistake.

InvalidConnector
The InvalidConnector error flag indicates that a serious error condition exits on the eDAQ unit most likely resulting from a hardware failure or a software deficiency. It is unlikely that this error can result from an operator mistake.

Memory
The Memory flag indicates that the eDAQ has run out of the memory reserved for eDAQ buffering and other processing tasks. This may occur when many channels are taking data at very high sample rates or large numbers of computed channels are defined. For a discussion on how to attempt to alleviate the problem, see Tips on Eliminating eDAQ OverFlow Errors.

MissedInterrupt
The MissedInterrupt flag indicates that the eDAQ unit is interrupt bound (i.e., it cannot service data acquisition interrupts fast enough). The only recourse is to reduce the sample rate for the transducers that generated the missed interrupt.

ParityError
The ParityError flag indicates that there is a unrecoverable inconsistency in a RAM Disk pointer structure. The RAM Disk pointers are stored in triple redundant fields. If none of the three pointers are consistent, the eDAQ sets the error flag and resets itself. It is unlikely that this error can result from an operator mistake.

QueueOverFlow
The QueueOverFlow flag indicates that the defined test exceeds the eDAQ unit's processing capabilities. This may occur when many channels are taking data at very high sample rates or large numbers of computed channels are defined. For a thorough discussion of this problem, see Tips on Eliminating eDAQ OverFlow Errors.

RAMDiskCorrupt
The RAMDiskCorrupt flag indicates a corruption of the RAM Disk memory. Transfer any existing test data files to the PC and reformat the RAM Disk. Consider the test data file suspect.

RingBufInterface
The RingBufInterface error flag indicates that a serious error condition exits on the eDAQ unit most likely resulting from a hardware failure or a software deficiency. It is unlikely that this error can result from an operator mistake.

RingBufInvalid
The RingBufInvalid flag indicates that there is an interruption in the incoming data stream that would result in a missed data sample and the option for an error reset on this event is enabled. The eDAQ uses this flag only for input data processed using the ring buffer interface scheme (e.g., vehicle bus data).

TimeOut
The TimeOut error flag indicates that a serious error condition exits on the eDAQ unit most likely resulting from a hardware failure or a software deficiency. It is unlikely that this error can result from an operator mistake.

10.4 Corrupt SIF File Data Recovery

NOTE
This topic is applicable to the SIF data format only.

Data stored in the SIF format can be corrupted in the unlikely event of one or more power failures during a test run when there is insufficient charge in the backup battery. Corruption can also occur if the PC Card is removed from the eDAQ with the eDAQ powered even if a test run is not in progress.

Understanding that these corruptions do happen, HBM does attempt to evaluate and, if possible, recover SIF data file contents. This is handled on a case-by-case basis and is subject to a service charge. The SIF component file set (i.e., all of the SIF#####.SIC files) must be sent intact. There is very limited hope of recovering data from a consolidated corrupt SIF file alone.
If TCE reports that any test runs have ended abnormally or there is any other reason to believe that the SIF data file is corrupt (after using the TCE SIC consolidate task), proceed as follows.
For internal Flash memory or an external PC Card formatted with Linux, the only way to copy the eDAQ resident SIC files is to use the eDAQ web browser. Select the Explore eDAQ Files option in the system tab and copy the SIC files under the /hd/eDAQ folder to the PC. Note that this can be very time consuming if there are a large number of SIC files.
For a PC Card formatted with MSDOS, remove the PC Card with power turned off and send the card to HBM customer service. Alternatively, copy the PC Card component file set to a PC directory and send this to HBM or place it on the HBM FTP site per arrangement with customer service.

10.5 Tips on Eliminating eDAQ OverFlow Errors

The eDAQ generates a DeviceOverFlow or QueueOverFlow error when the defined test exceeds the eDAQ unit's processing capabilities. Following are some suggestions for test setup changes to avoid a DeviceOverFlow or QueueOverFlow error.

Use integer data types for transducers

Significant improvement in processing throughput can be achieved by using integer output data types instead of the floating point data type in the transducer channel definitions. 16-bit integer data requires only half the storage space as 32-bit floating point data. The main drawback with integer data types is that they are not supported by all computed channels and DataModes. There is no loss of accuracy when using the 16-bit integer data type for any of the data sources that originate from eDAQ A/D converters since these are all 16-bit A/D converters.

Use Engineering Scaler computed channels

If transducer channels that originate as 16-bit integer data types (e.g., ELLB, EHLB, EHLS and EBRG channels) are used in a Desk Calculator computed channel, it is usually more efficient to use the 16-bit integer data type in the transducer channel definition and create an Engineering Scaler computed channel to generate the floating point data needed for most calculator expressions. The main advantage of this is that the eDAQ can store the original transducer channel as a 16-bit integer instead of as a 32-bit float. For more information on the Engineering Scaler computed channel, see "Engineering Scaler" on page 139.

Use the large pipe frame size option

Using the larger pipe frames significantly improves throughput performance particularly when there are a large number of transducer and/or computed channels running at slower sample rates (i.e., 500 Hz or slower). Using the larger pipe frames modestly improves throughput performance for most tests with sample rates below or around 10000 Hz. At sample rates above 10000 Hz, the small pipe frame size option

generally results in the best throughput performance. This option is selectable on a per test setup basis using the ECPU configuration options (see “Pipe Frame Rate” on page 94).

Use the Linux PC Card format option
Using the Linux format significantly improves throughput performance compared to using the less efficient DOS format. Of course, this is not an option if the PC Card is to be removed and later consolidated on a Windows-based PC.

Avoid redundant calculations in calculator computed channels
This is illustrated by the following example of an inefficient usage of eDAQ Desk Calculator computational resources.

```
Comp_1 = (In_1 + In_2) / sqrt(In_1^2 + In_2^2)
Comp_2 = (In_1 - In_2) / sqrt(In_1^2 + In_2^2)
```

Here is a much more efficient usage.

```
Temp_1 = sqrt(In_1^2 + In_2^2)
Comp_1 = (In_1 + In_2) / Temp_1
Comp_2 = (In_1 - In_2) / Temp_1
```

Also, although probably much less obvious, the `Temp_1` expression is more efficient when written as follows.

```
Temp_1 = sqrt(In_1 * In_1 + In_2 * In_2)
```

For more information on the Desk Calculator computed channel, see “Desk Calculator” on page 136.

Minimize the number of defined DataModes
For a test with 20 transducer channels defined at the same sample rate, it is much more efficient to store all 20 channels in a single Time History DataMode, rather than storing each channel in a separate DataMode. The reason for this is that there is only one PC Card file opened and manipulated for each Time History DataMode and having just one file to manipulate is much more efficient than having to manipulate 20 PC Card files at the same time.

Up sample digital input channels used for triggers
Often, a digital input channel is used to manually trigger DataMode storage. If the input channels are defined for a 2500 Hz sample rate and storage rate, it is more efficient to define the digital input channel at 100 Hz and then up sample by a factor of 25 to get to the 2500 Hz sample rate required for the DataMode trigger. For more information on the Up Sampler computed channel, see “Up Sampler” on page 158.

Do not use min-max tracking
The enable min-max tracking preference for Time History DataModes is in the TCE Preferences menu. Min-max tracking can consume significant CPU cycles with a lot of Time History DataMode storage.

Use a second eDAQ or eDAQ-lite in networked mode

If another eDAQ or eDAQ-lite is available, use it in networked mode with the first eDAQ and split the processing load as evenly as possible between the two eDAQ systems. For more information on networking, see “Networking eDAQ Systems” on page 40 and “Networking eDAQ Systems” on page 90.

Reduce the scope of the test

As a last resort, reduce the scope of the test by reducing sample rates, reducing channel counts or eliminating computed channels and DataModes.

11 Data Types

The eDAQ supports the following data types:

- 32-bit float
- 32-bit integer
- 32-bit unsigned
- 16-bit integer
- 16-bit signed
- 16-bit unsigned
- 8-bit integer
- 8-bit signed
- 8-bit unsigned (logic, bitmap, message)

The following table summarizes the data types supported by each input channel, computed channel and DataMode.

Category	Channel Type	Input Data Type	Output Data Type
Input Channel	Bridge	--	16-bit signed 32-bit float 8-bit signed
	Bus-Oriented Vehicle Bus GPS Serial Bus	--	8-bit unsigned 16-bit unsigned 32-bit unsigned 32-bit float (using conversion)
	Digital Input	--	8-bit unsigned (logic)
	High Level	--	16-bit signed 32-bit float 8-bit signed
	Simultaneous High Level	--	16-bit signed 32-bit float 8-bit signed
	Isolated Thermocouple	--	32-bit float
	Low Level	--	16-bit signed 32-bit float 8-bit signed
	Pulse Counter	--	32-bit float 32-bit unsigned* 32-bit integer* **limited by selected mode*
	Simulation File	--	32-bit float
	Simulation Function Generator	--	32-bit float
	Simulation Message	--	8-bit unsigned (msg)
	Thermocouple	--	32-bit float

Category	Channel Type	Input Data Type	Output Data Type
Computed Channel	Anomaly Detect	32-bit float	8-bit unsigned (bmp)
	Bitmap Trigger	8-bit unsigned (bmp)	8-bit unsigned (logic)
	Damage Equivalent Load	32-bit float	32-bit float
	Desk Calculator	Based on specific operators (below)	
	sin, cos, tan, asin, acos, atan, log, log10, abs, exp, sgn, round, floor, ceil, +,-,*,/,%,^	32-bit float	32-bit float
	float	8-bit unsigned (logic)	32-bit float
	>,>=,<,<=,==,!=	32-bit float	8-bit unsigned (logic)
	!,&&,||	8-bit unsigned (logic)	8-bit unsigned (logic)
	Directional Velocity	velocity: 32-bit float direction: 32-bit float 32-bit integer	32-bit float
	Down Sampler	all	same is input
	Engineering Scaler	8-bit integer 8-bit unsigned 16-bit integer 16-bit unsigned 32-bit integer 32-bit unsigned	32-bit float
	Fatigue Damage	32-bit float	32-bit float
	Integer Scaler	32-bit float	8-bit integer 8-bit unsigned 16-bit integer 16-bit unsigned 32-bit integer 32-bit unsigned
	Integrator	32-bit float 32-bit integer 32-bit unsigned	same as input
	Interactive Trigger	all	8-bit unsigned (logic)
	Max Track	32-bit float 16-bit integer	same as input
	Min Track	32-bit float 16-bit integer	same as input
	Pulse Counter	8-bit unsigned (logic)	32-bit float
	Range Track	32-bit float 16-bit integer	32-bit float for 32-bit float input, 16-bit unsigned for 16-bit integer input

Category	Channel Type	Input Data Type	Output Data Type
Computed Channel (continued)	Smoothing Filter	32-bit float 16-bit integer	same as input
	State Mapper	32-bit float	32-bit float
	Statistical Analysis	32-bit float	32-bit float
	Test Run Stopper	8-bit unsigned (logic)	8-bit unsigned (logic)
	Time Base Shifter	all	same as input
	Time Channel	all	32-bit float 32-bit unsigned
	Timed Trigger	8-bit unsigned (logic)	8-bit unsigned (logic)
	Trigger Generator	all	8-bit unsigned (logic)
	Triggered Zero Suppression	32-bit float 32-bit integer 32-bit unsigned	same as input
	Up Sampler	all	same is input
	Valid Data Gate	all	8-bit unsigned (logic)
DataMode	Burst History	all	--
	Digital Output	8-bit unsigned (logic)	--
	Event Slice	all	--
	Message Logger	8-bit unsigned (msg)	--
	Peak/Valley	8-bit integer 16-bit integer 32-bit float	--
	Peak/Valley Matrix	32-bit float 16-bit integer* **evenly divided bins only*	--
	Peak/Valley Slice	master: 8-bit integer 16-bit integer 32-bit float slave: all	--
	Rainflow	32-bit float 16-bit integer* **evenly divided bins only*	--
	Time at Level (1D)	32-bit float 16-bit integer* **evenly divided bins only*	--
	Time at Level (mD)	32-bit float 16-bit integer* **evenly divided bins only*	--
	Time History	all	--

12 Cable Pinouts

12.1 ECPU (Main Processor)

12.1.1 Communications Cable

The eDAQ is compatible with several different communications cables each of which provide a 26-pin D-Sub connector for connection to the eDAQ Comm port. The following table lists the communications cables and their connectors.

Communications Cable	Ethernet (X/O)	Ethernet (HUB)	Serial	Sync
1-E-ETHERNET X/O-2	X			
1-E-ETHERNET HUB-2		X		
1-SAC-ESR9/XO-2	X		X	
1-SAC-ESR9/HUB-2		X	X	
1-SAC-ESYNCADAPT-2		X		X
1-SAC-ESYNCADAPT-SC-2		X	X	X

The 26-pin D-Sub connector has dedicated pins for each type of available connector. As shown in the diagram below, pins 1-4 are for Ethernet communication, pins 5-9 are for the networking sync connectors and pins 10-18 correspond to the serial 9-pin connector.

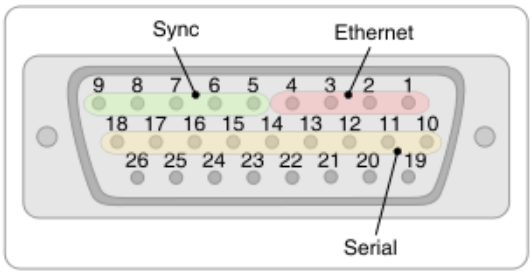
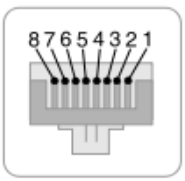


Figure 12-1: Diagram of the 26-pin D-Sub connector on the communications cables for connection to the eDAQ.

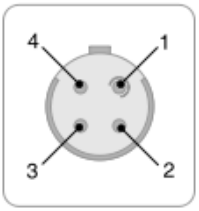
The following tables list the pinouts for each type of available connector and the corresponding pin on the 26-pin D-Sub Comm connector.

RJ-45 Ethernet Connector



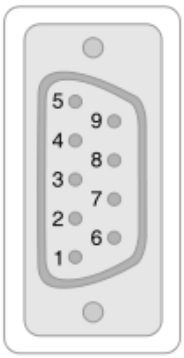
Function	26-Pin D-Sub	RJ-45 Pin	Wire Color (X/O)	Wire Color (HUB)
10/100 BASE-T Receive +	3	3	Orange/White	Green/White
10/100 BASE-T Receive -	4	6	Orange	Green
10/100 BASE-T Transmit +	2	1	Green/White	Orange/White
10/100 BASE-T Transmit -	1	2	Green	Orange

LEMO Networking Connector



Connector	Function	26-Pin D-Sub	LEMO Pin	Wire Color
Sync 1	Clock +	5	1	Red
	Clock -	8	2	Black
	Shield	7	3	bare wire
Sync 2	Clock +	6	1	Red
	Clock -	9	2	Black
	Shield	7	3	bare wire

9-Pin D-Sub Serial Connector

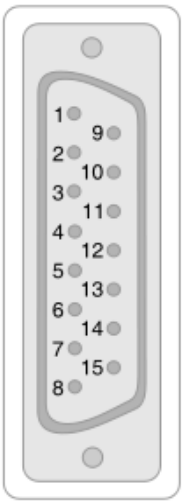


Function	26-Pin D-Sub	Serial Pin	Wire Color
CTS (clear to send)	17	7	Yellow
DCD (data carrier detect)	10	4	Red
DSR (data set ready)	15	1	Violet
DTR (data terminal ready)	13	6	Orange
Rx (received)	11	3	Brown
RI (ring indicator)	18	9	Blue
RTS (request to send)	16	8	Green
Tx (transmitted)	12	2	Black
Ground	14	5	Gray

NOTE
This information is for the current communications cable, which is a fully molded connector/cable assembly. The original communications cable is not a molded assembly and differs as follows from the current cable: ground on the serial connector is white instead of gray and the HUB 10/100BASE-T Receive+ and Transmit+ colors are white/orange and white/green, respectively.

12.1.2 Power Cable

The SoMat EPWR15 Power Cable (1-EPWR15-2) has a 15-pin D-Sub connector for connection to the Power port on the eDAQ and two sets of pigtail wires: one for main power and one for remote power. The following table lists the pinouts for the EPWR15 cable.



Cable	Function	Pin	Wire Color
Main Power Cable (gray)	+ Main Power	1	Red
	- Main Power	8	Black
Remote Power Control Cable (black)	+ Remote Power	6	Red
	- Remote Power	14	Black

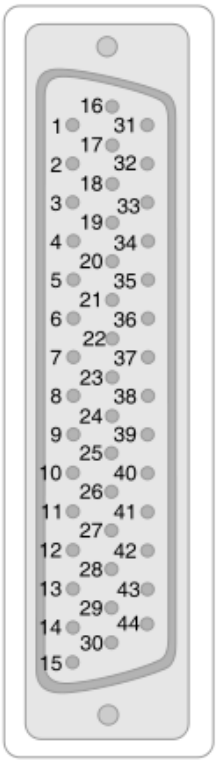
Pin 3 is jumpered to pin 4.

NOTE
Though the current EPWR15 cables use only one pin each for power and ground, the Power connector on the eDAQ can receive + Main Power on pins 1, 2 and 9 and - Main Power on pins 7, 8 and 15.

12.1.3 Digital I/O and Pulse Counter Cable

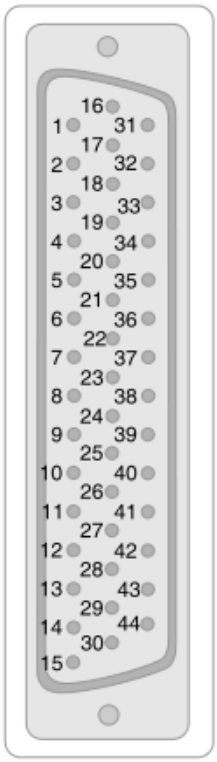
The SoMat SAC-EDIO Digital I/O Transducer Cable (1-SAC-EDIO-2) for ECPU digital inputs/outputs and pulse counters has a 44-pin D-Sub connector for connection to the Digital I/O port on the ECPU and a set of color-coded pigtail wires.

NOTE
There are two versions of this cable that have the same part number, but have different color coded wires. The newer assembly is a split cable labeled “SAC-EDIGIO.” The cable pin outs for the newer cable are in the first table and the cable pin outs for the older cable are in the second table.



SAC-EDIO Cable (newer, labeled “SAC-EDIGIO”)

Function	Pin	Wire Color	Function	Pin	Wire Color
PC Signal 1	2	Green	PC Return 1	1	Black
PC Signal 2	4	Red	PC Return 2	3	Gray
PC Signal 3	6	Blue/White	PC Return 3	5	Red/White
PC Signal 4	8	Orange	PC Return 4	7	Brown
PC Signal 5	10	Pink	PC Return 5	9	Orange/White
PC Signal 6	12	White	PC Return 6	11	Purple
PC Signal 7	14	Red/Black	PC Return 7	13	Green/White
PC Signal 8	16	Purple/White	PC Return 8	17	Light Green
I/O Signal 1	24	Green	I/O Return 1	23	Black
I/O Signal 2	26	Red	I/O Return 2	25	Gray
I/O Signal 3	28	Blue/White	I/O Return 3	27	Red/White
I/O Signal 4	30	Orange	I/O Return 4	29	Brown
I/O Signal 5	32	Pink	I/O Return 5	31	Orange/White
I/O Signal 6	34	White	I/O Return 6	33	Purple
I/O Signal 7	36	Red/Black	I/O Return 7	35	Green/White
I/O Signal 8	38	Light Green	I/O Return 8	37	Purple/White
I/O Signal 9	40	Yellow	I/O Return 9	39	Brown/White
I/O Signal 10	42	Black/White	I/O Return 10	41	Blue



SAC-EDIO Cable (older)

Function	Pin	Wire Color	Function	Pin	Wire Color
PC Signal 1	2	White	PC Return 1	1	Black
PC Signal 2	4	Red	PC Return 2	3	Green
PC Signal 3	6	Orange	PC Return 3	5	Blue
PC Signal 4	8	White/Black	PC Return 4	7	Red/Black
PC Signal 5	10	Orange/Black	PC Return 5	9	Green/Black
PC Signal 6	12	Blue/Black	PC Return 6	11	Black/White
PC Signal 7	14	Red/White	PC Return 7	13	Green/White
PC Signal 8	16	Orange/Red	PC Return 8	17	Blue/White
I/O Signal 1	24	White	I/O Return 1	23	Black
I/O Signal 2	26	Red	I/O Return 2	25	Green
I/O Signal 3	28	Orange	I/O Return 3	27	Blue
I/O Signal 4	30	White/Black	I/O Return 4	29	Red/Black
I/O Signal 5	32	Orange/Black	I/O Return 5	31	Green/Black
I/O Signal 6	34	Blue/Black	I/O Return 6	33	Black/White
I/O Signal 7	36	Red/White	I/O Return 7	35	Green/White
I/O Signal 8	38	Blue/White	I/O Return 8	37	Orange/Red
I/O Signal 9	40	Black/Red	I/O Return 9	39	White/Red
I/O Signal 10	42	Blue/Red	I/O Return 10	41	Red/Green

12.2 ECOM (Vehicle Communications Layer)

Transducer Cable for Dedicated CAN Interface

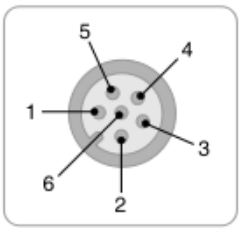
The dedicated CAN interface on the ECOM layer uses a SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) with an M8 connector and a set of color-coded pigtail wires. The following table lists the pinouts for the SAC-TRAN-MP cable when used with a dedicated CAN interface on the ECOM layer.

NOTE

Connection to both the SWC pin and the CAN pins is allowed, but only one source can be used at any given time.

NOTE

Always provide the +12 volt REF voltage for the SWC interface. For other CAN interfaces, the red power wire can be used to power transducers with a user-configurable range of 3 to 24 volts.

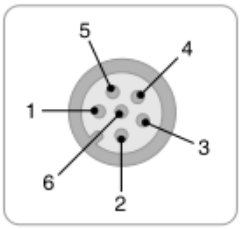


Function	Pin	Wire Color
SWC	1	Brown
CANH	2	White
AGnd	3	bare wire
Power	5	Red
+12 V REF	5	Red (SWC)
CANL	6	Green

12.3 EHLS (High Level Analog Layer)

12.3.1 Transducer Cable

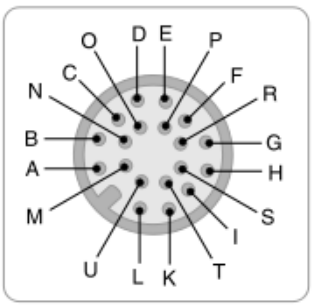
The EHLS layer uses a SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) with an M8 connector and a set of color-coded pigtail wires. The following table lists the pinouts for the SAC-TRAN-MP cable when used for an EHLS input.



Function	Pin	Wire Color
reserved	1	Brown
+ Signal Input	2	White
Shield	3	bare wire
Ground	4	Black
Power	5	Red
- Signal Input	6	Green

12.3.2 Analog Output Cable

The following table lists the pinouts for the SoMat SAC-TRAN-AO Analog Output Cable (1-SAC-TRAN-AO-2-2) when used with EHLS analog outputs.



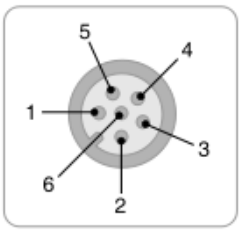
Function	Pin	Wire Color
1 Out	B	White/Green
2 Out	M	Brown
3 Out	A	Red/Blue
4 Out	E	Green
5 Out	N	Pink
6 Out	C	Gray
7 Out	O	Yellow
8 Out	D	Brown/Green
9 Out	K	Gray/Brown
10 Out	U	Blue

Function	Pin	Wire Color
11 Out	L	Gray/Pink
12 Out	G	Black
13 Out	T	Yellow/Brown
14 Out	I	White/Gray
15 Out	S	Purple
16 Out	H	White/Yellow
Ground	P	White
Ground	R	Red
Shield	F	bare wire

12.4 EBRG (Bridge Layer)

12.4.1 Transducer Cable

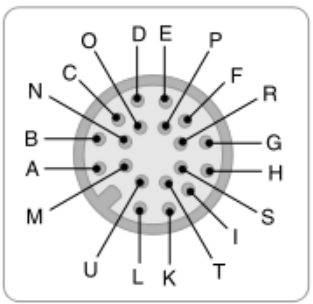
The EBRG layer uses a SoMat SAC-TRAN-MP Transducer Cable (SAC-TRAN-MP) with an M8 connector and a set of color-coded pigtail wires. The following table lists the pinouts for the SAC-TRAN-MP cable when used for an EBRG input.



Function	Pin	Wire Color
reserved	1	Brown
+ Signal Input	2	White
Shield/Ground	3	bare wire
- Excitation	4	Black
+ Excitation	5	Red
- Signal Input	6	Green

12.4.2 Analog Output Cable

The following table lists the pinouts for the SoMat SAC-TRAN-AO Analog Output Cable (SAC-TRAN-AO-2-2) when used with EBRG analog outputs.



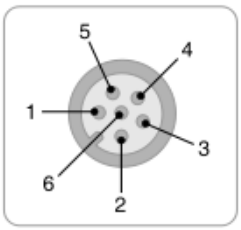
Function	Pin	Wire Color
1 Out	B	White/Green
2 Out	M	Brown
3 Out	A	Red/Blue
4 Out	E	Green
5 Out	N	Pink
6 Out	C	Gray
7 Out	O	Yellow
8 Out	D	Brown/Green

Function	Pin	Wire Color
9 Out	K	Gray/Brown
10 Out	U	Blue
11 Out	L	Gray/Pink
12 Out	G	Black
13 Out	T	Yellow/Brown
14 Out	I	White/Gray
15 Out	S	Purple
16 Out	H	White/Yellow
Ground	P	White
Ground	R	Red
Shield	F	bare wire

12.5 EDIO (Digital I/O Layer)

Transducer Cable for Digital I/O and Pulse Counter

The EDIO layer uses the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) with an M8 connector and a set of color-coded pigtail wires. The following table lists the pinouts for the SAC-TRAN-MP cable when used for EDIO inputs. The I/O pin depends on the bank connector (i.e., |1-4|, |5-8| or |9-12|).



Function	Pin	Wire Color	Quad Encoder Usage
I/O 4, 8 or 12	1	Brown	Encoder 2, output B
I/O 3, 7 or 11	2	White	Encoder 2, output A
GND/Shield	3	bare wire	Return
I/O 1, 5 or 9	4	Black	Encoder 1, output A
Power	5	Red	Power
I/O 2, 6 or 10	6	Green	Encoder 1, output B

NOTE

The quadrature encoder outputs as specified are for default signal polarity which assigns the positive direction to clockwise rotation. To reverse polarity, interchange encoder outputs A and B.

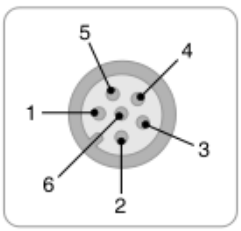
12.6 Vehicle Bus Modules (VBM)

The vehicle bus modules use the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) with an M8 connector and a set of color-coded pigtail wires. The following sections list the pinouts for the SAC-TRAN-MP cable when used with each available VBM interface.

12.6.1 Transducer Cable for VPW Interface

The following table lists the pinouts for the SAC-TRAN-MP cable when used with the VPW interface.

NOTE
Always provide the +12 volt REF voltage for the VPW module to function.

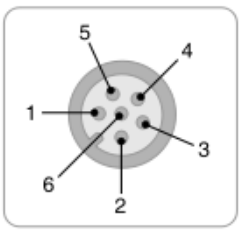


Function	Pin	Wire Color
VPW_bus	2	White
AGnd	3	bare wire
+12 V REF	5	Red

12.6.2 Transducer Cable for J1708/LIN BUS Interface

The following table lists the pinouts for the SAC-TRAN-MP when used with the J1708/LIN interface. Connect to either the LIN_BUS pin or the J1708 pins but not both.

NOTE
Always provide the +12 volt REF voltage for the J1708/LIN module to function.



Function	Pin	Wire Color
LIN_BUS	1	Brown
J1708_A	2	White
AGnd	3	bare wire
+12 V REF	5	Red
J1708_B	6	Green

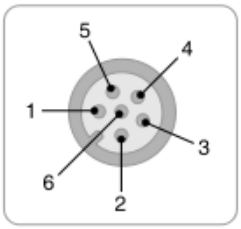
12.6.3 Transducer Cable for CAN/SWC Interface

The following table lists the pinouts for the SAC-TRAN-MP cable when used with the CAN/SWC interface

NOTE
Connection to both the SWC pin and the CAN pins is allowed, but only one source can be used at any given time.

NOTE
SWC operation is restricted to the EMCAN.04 version of the CAN VBM.

NOTE
Always provide the +12 volt REF voltage for the SWC interface.

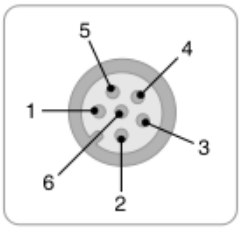


Function	Pin	Wire Color
SWC	1	Brown
CANH	2	White
AGnd	3	bare wire
Power	5	Red
+12 V REF	5	Red (SWC)
CANL	6	Green

12.6.4 Transducer Cable for ISO9141/KW2000 Interface

The following table lists the pinouts for the SAC-TRAN-MP cable when used with the ISO9141/KW2000 interface.

NOTE
Always provide the VBAT+ voltage for the ISO9141/KW2000 module to function.



Function	Pin	Wire Color
ISO9141 K-Line	2	White
AGnd	3	bare wire
VBAT+	5	Red
ISO9141 L-Line	6	Green

12.7 EHLB (High Level Layer)

12.7.1 EHLB Transducer Cable

The SoMat SAC-EHLB1 EHLB Transducer Cable (1-SAC-EHLB1-2) has a 62-pin D-Sub connector for connection to the EHLB and a set of color-coded pigtail wires.

NOTE

There are two versions of this cable that have the same part number, but have different color coded wires. The newer assembly is labeled “SE74020-C” on the outer PVC shield. The cable pin outs for the newer cable are in the first table and the cable pin outs for the older cable are in the second table.

SAC-EHLB1 Cable (newer, labeled “E74020-C”)

Function	Pin	Wire Color	Function	Pin	Wire Color
+ Excitation	61	Gray/Red	- Excitation	59	Light Blue/Black
1 In	29	Black	1 Ground	49	Brown
2 In	8	Red	2 Ground	7	Orange
3 In	31	Yellow	3 Ground	51	Green
4 In	10	Blue	4 Ground	9	Purple
5 In	33	Gray	5 Ground	53	White
6 In	12	Pink	6 Ground	11	Light Green
7 In	55	Black/White	7 Ground	34	Brown/White
8 In	35	Red/White	8 Ground	56	Orange/White
9 In	14	Green/White	9 Ground	13	Blue/White
10 In	57	Purple/White	10 Ground	36	Red/Black
11 In	37	Orange/Black	11 Ground	58	Yellow/Black
12 In	16	Green/Black	12 Ground	15	Gray/Black
13 In	39	Pink/Black	13 Ground	60	Pink/Green
14 In	18	Pink/Red	14 Ground	17	Pink/Purple
15 In	41	Light Blue	15 Ground	62	Light Blue/Brown
16 In	20	Light Blue/Red	16 Ground	19	Light Blue/Purple

SAC-EHLB1 Cable (older)

Function	Pin	Wire Color	Function	Pin	Wire Color
+ Excitation	61	Red	- Excitation	59	Black
1 In	29	White	1 Ground	49	Green
2 In	8	Orange	2 Ground	7	Blue
3 In	31	Brown	3 Ground	51	Yellow

Function	Pin	Wire Color	Function	Pin	Wire Color
4 In	10	Purple	4 Ground	9	Gray
5 In	33	Pink	5 Ground	53	Tan
6 In	12	Red/Green	6 Ground	11	Red/Yellow
7 In	55	Red/Black	7 Ground	34	White/Black
8 In	35	White/Red	8 Ground	56	White/Green
9 In	14	White/Yellow	9 Ground	13	White/Blue
10 In	57	White/Brown	10 Ground	36	White/Orange
11 In	37	White/Gray	11 Ground	58	White/Purple
12 In	16	White/Red/Blue	12 Ground	15	White/Black/Green
13 In	39	White/Black/Yellow	13 Ground	60	White/Black/Blue
14 In	18	White/Black/Brown	14 Ground	17	White/Black/Orange
15 In	41	White/Black/Gray	15 Ground	62	White/Black/Purple
16 In	20	White/Black/Black	16 Ground	19	White/Red/Green

12.7.2 EHLB Transducer Cable with Vehicle Bus

The SoMat SAC-EHLB1-VB EHLB Transducer Cable with Vehicle Bus (1-SAC-EHLB1-VB-2) has a 62-pin D-Sub connector for connection to the EHLB and a set of color-coded pigtail wires.

NOTE

There are two versions of this cable that have the same part number, but have different color coded wires. The newer assembly is labeled “SE74020-C” on the outer PVC shield. The cable pin outs for the newer cable are in the first table and the cable pin outs for the older cable are in the second table.

SAC-EHLB1-VB Cable (newer, labeled “E74020-C”)

Function	Pin	Wire Color	Function	Pin	Wire Color
CANL	1	Black	K-Line	4	Red
CANH	23	Brown	L-Line	44	Light Green
AGnd	26	Pink	AGnd	48	Black/White
SWC_bus	24	Orange	+12 V	45	Brown/White
AGnd	46	Yellow	CCD+	5	Red/White
VPW_bus	2	Green	CCD-	25	Orange/White
AGnd	47	Blue	AGnd	30	Green/White

Function	Pin	Wire Color	Function	Pin	Wire Color
AGnd	27	Purple	PWM_bus+	22	Blue/White
ALDL_bus	3	Gray	PWM_bus-	43	Purple/White
AGnd	28	White	AGnd	32	Red/Black

SAC-EHLB1-VB Cable (older)

Function	Pin	Wire Color	Function	Pin	Wire Color
CANL	1	Black	K-Line	4	Black/White
CANH	23	White	L-Line	44	Blue/Black
AGnd	26	Green	AGnd	48	Green/White
SWC_bus	24	Red	+12 V	45	Red/White
AGnd	46	Blue	CCD+	5	Orange/Red
VPW_bus	2	Orange	CCD-	25	Blue/White
AGnd	47	Red/Black	AGnd	30	White/Red
AGnd	27	White/Black	PWM_bus+	22	Black/Red
ALDL_bus	3	Green/Black	PWM_bus-	43	Red/Green
AGnd	28	Orange/Black	AGnd	32	Blue/Red

12.8 ELLB (Low Level Layer)

12.8.1 ELLB Transducer Cable

The following table lists the pinouts for the SoMat 4-wire SAC-EXDUC ELLB Transducer Cable and the SoMat 6-wire SAC-EXDUC-6-V ELLB Transducer Cable.

Input Cable

The calibration inputs apply only to the 6-wire SAC-EXDUC-6-V cable.

NOTE

For a quarter bridge configuration only, wire colors for + Excitation and - Signal are reversed.

Function	1/5 Pin	2/6 Pin	3/7 Pin	4/8 Pin	Wire Color
+ Excitation	35	13	28	6	Red
+ Signal	16	31	9	24	White
+ Calibration	34	12	27	5	Blue
Ground	17	32	10	25	shield

Function	1/5 Pin	2/6 Pin	3/7 Pin	4/8 Pin	Wire Color
- Excitation	15	30	8	23	Black
- Signal	33	11	26	4	Green
- Calibration	14	29	7	22	Brown

Analog Out Cable

Analog out is provided with the SAC-EXDUC-6-V cable only.

Function	Pin	Wire Color	Function	Pin	Wire Color
Volt Out 1/5	19	Brown	Ground 1/5	18	Black
Volt Out 2/6	37	Red	Ground 2/6	36	Green
Volt Out 3/7	2	Orange	Ground 3/7	3	White
Volt Out 4/8	20	Yellow	Ground 4/8	21	Blue
Ground	1	shield			

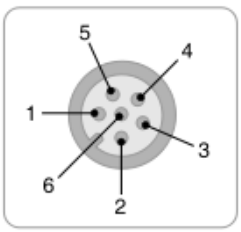
12.8.2 ELLB M8 Connector Option

The following table lists the pinouts for the ELLB M8 input connectors option .

Transducer Cable

NOTE

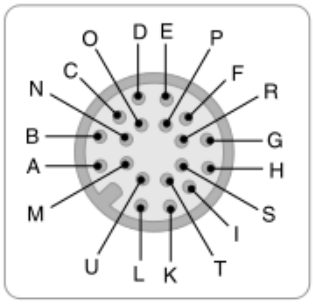
For a quarter bridge configuration only, wire colors for + Excitation and -Signal are reversed.



Function	Pin	Wire Color
reserved	1	Brown
+ Signal Input	2	White
Shield	3	bare wire
- Excitation	4	Black
+ Excitation	5	Red
- Signal Input	6	Green

Analog Out Cable

The analog output cable is optional.



Function	Pin	Wire Color
Ground	P	White
Analog 1 Out	B	White/Green
Analog 2 Out	M	Brown
Analog 3 Out	A	Red/Blue
Analog 4 Out	E	Green
Analog 5 Out	N	Pink
Analog 6 Out	C	Gray
Analog 7 Out	O	Yellow
Analog 8 Out	D	Brown/Green
Shield	F	bare wire

13 Device Wiring

The following sections provide device wiring diagrams for all applicable layer types. For more information on using each transducer, see “eDAQ Hardware” on page 93 and “Input Channels” on page 111. For complete pinouts for the cables used in the following sections, see “Cable Pinouts” on page 199.

13.1 ECPU (Base Processor)

13.1.1 Digital Input

Use the SoMat SAC-EDIO Digital I/O Transducer Cable (1-SAC-EDIO-2) to wire ECPU digital inputs.

Preferred Switch

Whenever possible, a single-pole, double-throw switch, wired as shown below, should be used for switched inputs. This circuit solidly switches the input line to either ground or +5 volts and prevents coupling of the input line to other digital input lines. Moving the switch to the ground side is identified as FALSE

Figure 13-1: Wiring diagram for the preferred SPDT switch configuration.

Alternate Switch

The following diagram shows the circuit wiring for an alternate digital input involving a switch closure function. An open switch as shown is TRUE; a closed switch is FALSE. This circuit is adequate for most applications.

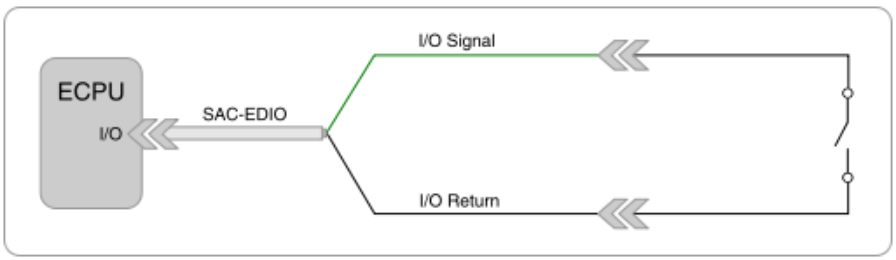


Figure 13-2: Wiring diagram for the alternate SPST switch configuration.

13.1.2 Digital Output

Use the SoMat SAC-EDIO Digital I/O Transducer Cable (1-SAC-EDIO-2) to wire ECPU digital outputs.

Operating a Light Emitting Diode (LED)

The following diagram shows the use of an LED as an indicator in the digital output circuit. A logical FALSE causes the diode to light. The total of all diode currents must be less than 250 mA for the ECPU. The resistor R limits the current through the diode when the LED is on. For more information on output current limitations, refer to the ECPU-PLUS data sheet.

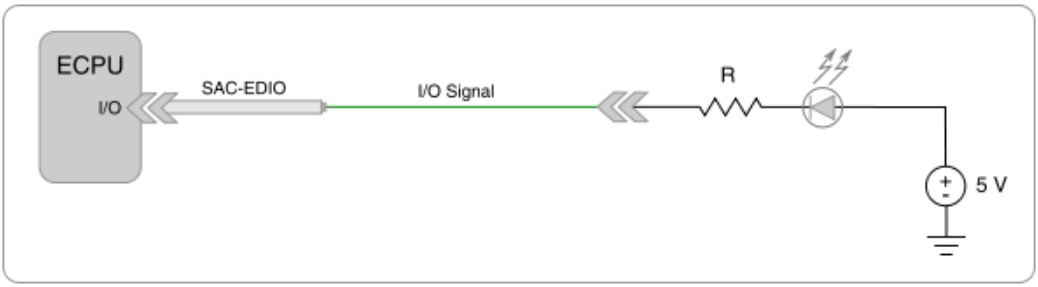


Figure 13-3: Wiring diagram for using an LED as a digital output.

13.2 EDIO (Digital I/O Layer)

13.2.1 Digital Input

Use the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) to wire EDIO digital inputs.

Preferred Switch

Whenever possible, a single-pole, double-throw switch, wired as shown below, should be used for switched inputs. This circuit solidly switches the input line to either ground or +5 volts and prevents coupling of the input line to other digital input lines. Moving the switch to the ground side is identified as FALSE.

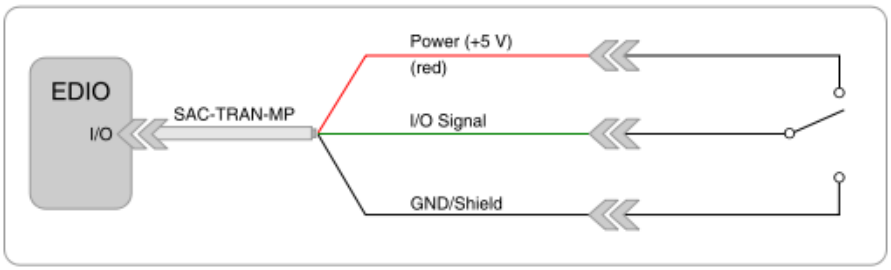


Figure 13-4: Wiring diagram for the preferred switch configuration on an EDIO input.

Alternate Switch

The following diagram shows the circuit wiring for an alternate digital input involving a switch closure function. An open switch as shown is TRUE; a closed switch is FALSE. This circuit is adequate for most applications.

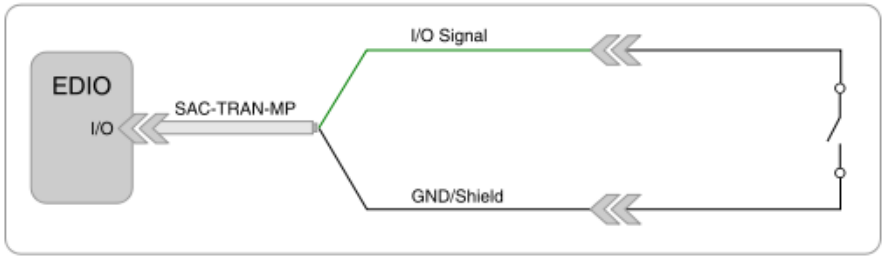


Figure 13-5: Wiring diagram for the alternate switch configuration on an EDIO input.

13.2.2 Digital Output

Use the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) to wire EDIO digital outputs.

Operating a 12-volt Incandescent Bulb

The following diagram shows an incandescent bulb (3 watts maximum) used as an indicator in the digital output circuit. An external 12-volt DC power supply provides power for the bulb. A three-watt bulb uses the current capacity of all lines in an EDIO bank. The light turns on when the output is set to FALSE.

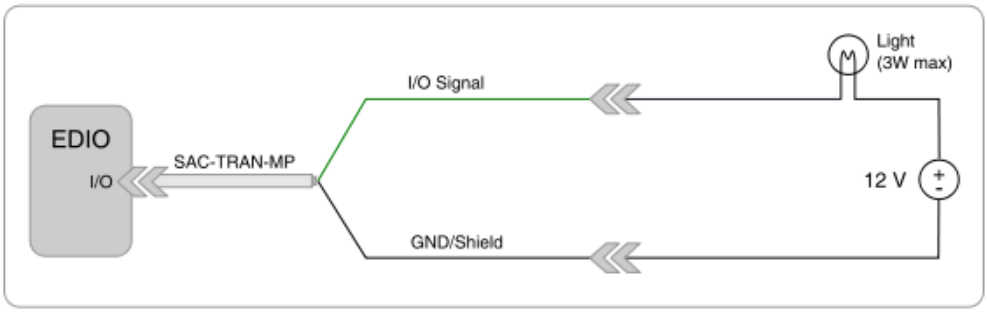


Figure 13-6: Wiring diagram for using an incandescent bulb on an EDIO output.

Operating a Light Emitting Diode (LED)

The following diagram shows the use of an LED as an indicator in the digital output circuit. A FALSE output causes the diode to light. The total of all diode currents must be less than 250 mA for the an EDIO bank. The resistor R limits the current through the diode when the LED is on. For more information on output current limitations, refer to the EDIO data sheet.

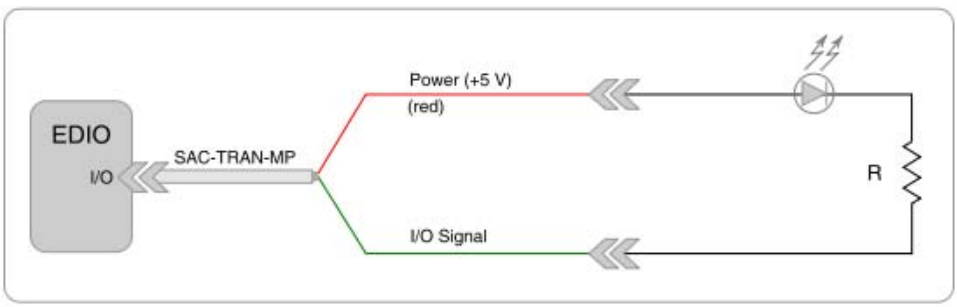


Figure 13-7: Wiring diagram for using an LED on an EDIO output.

13.3 EHLS (High Level Analog Layer)

13.3.1 Analog Input

Use the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) to wire EHLS analog inputs.

NOTE

Do not use this wiring diagram for EBRG, ELLB or EHLB channels.

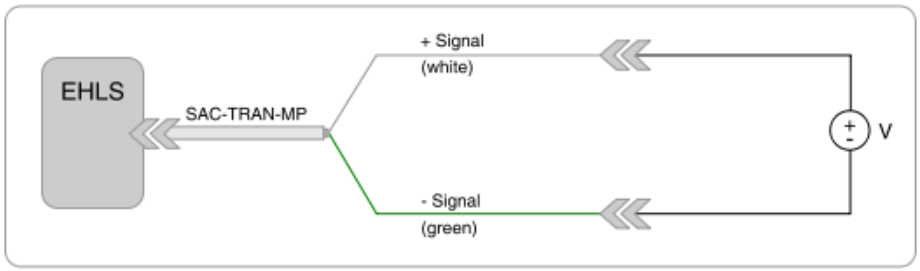


Figure 13-8: Wiring diagram for a standard analog input on an EHLS layer.

CAUTION

If the eDAQ chassis is not grounded sufficiently, connect the black Ground wire to the green -Signal wire at the negative terminal of the voltage source. Leave the bare shield wire unconnected and assure it does not contact any other surface by either protecting it or trimming it close to the wire insulation. When using non-HBM extending cables, attach the shield to the shield of the extending wire, but leave the shield extension unconnected. Failure to follow this procedure may result in damage to the EHLS during a high-voltage surge.

13.3.2 SMSTRB4 (Strain SMART Module)

Use the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) to wire SMSTRB4 inputs. The following diagrams are also applicable to older SMART bridge modules that support one fixed bridge type.

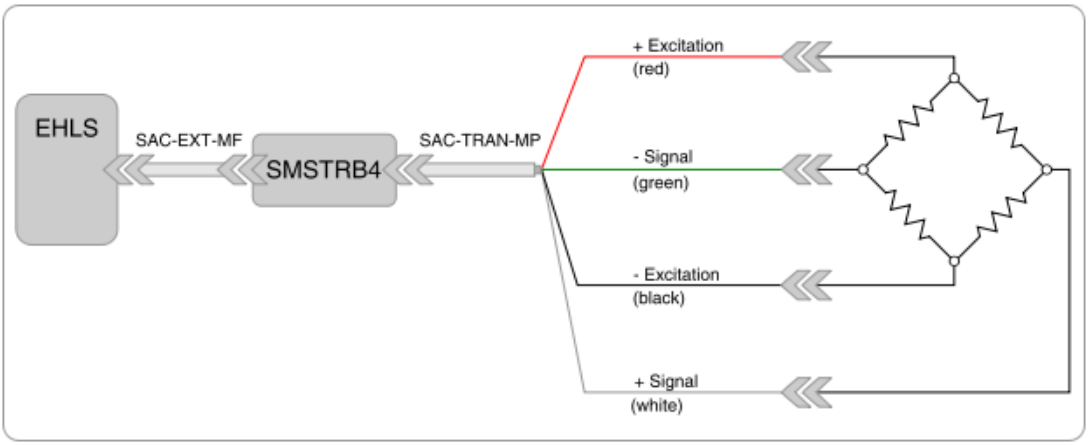


Figure 13-9: Wiring diagram for a full-bridge configuration using a Strain SMART Module.

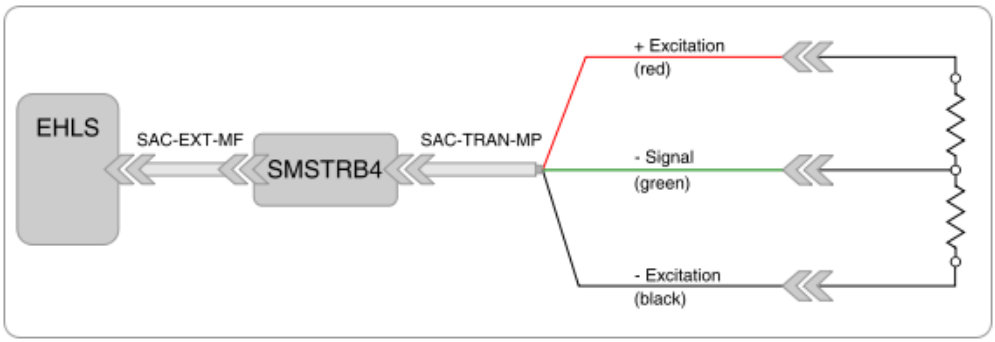


Figure 13-10: Wiring diagram for a half-bridge configuration using a Strain SMART Module.

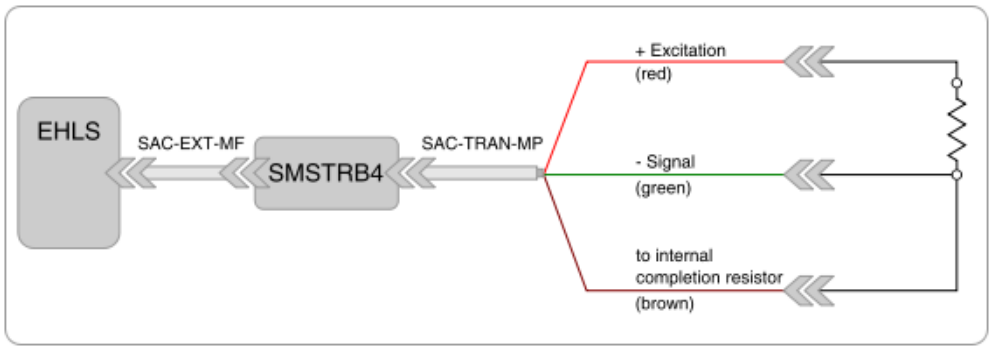


Figure 13-11: Wiring diagram for a quarter-bridge configuration using a Strain SMART Module.

NOTE

For the SMSTRB4, the brown lead wire is routed to the internal completion resistor. For the older fixed quarter-bridge SMART modules (i.e., modules with serial numbers starting with SMSTRQB), the white lead wire is routed to the internal completion resistor.

13.4 EBRG (Bridge Layer)

13.4.1 Bridge Transducers

Use the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) to wire EBRG bridge transducer inputs.

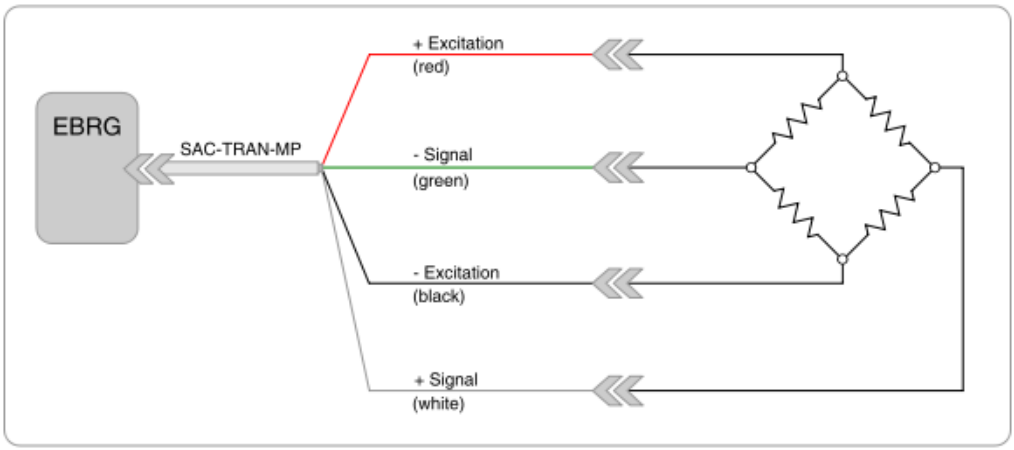


Figure 13-12: Wiring diagram for a full-bridge configuration on an EBRG layer.

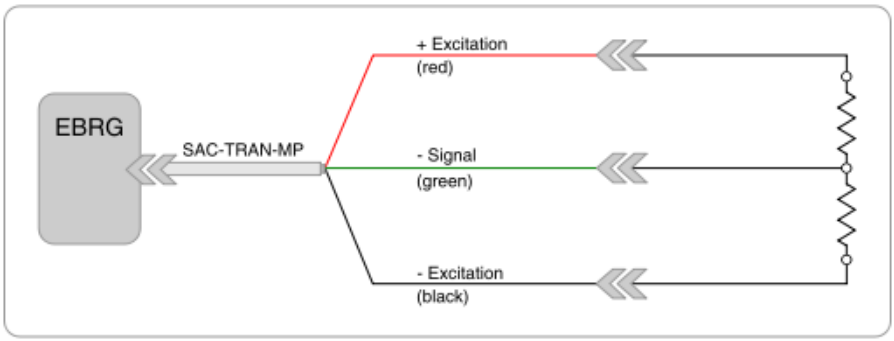


Figure 13-13: Wiring diagram for a half-bridge configuration on an EBRG layer.

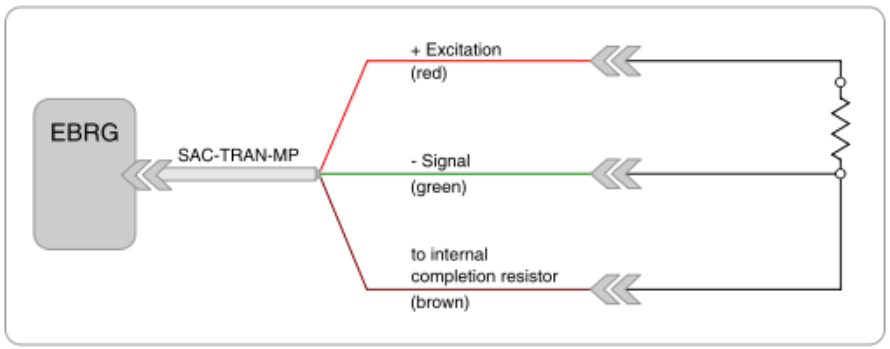


Figure 13-14: Wiring diagram for a quarter-bridge configuration on an EBRG layer.

13.4.2 Analog Input

Use the SoMat SAC-TRAN-MP Transducer Cable (1-SAC-TRAN-MP-2-2 or 1-SAC-TRAN-MP-10-2) to wire EBRG analog inputs.

NOTE
Do not use this wiring diagram for EHLS channels.

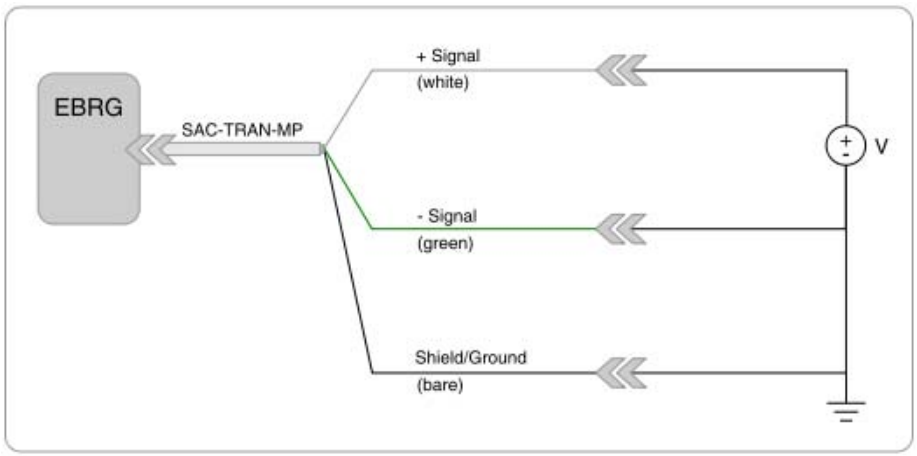


Figure 13-15: Wiring diagram for a standard analog input on an EBRG layer.

13.5 EHLB (High Level Layer)

Use the SoMat SAC-EHLB1 EHLB Transducer Cable (1-SAC-EHLB1-2) to wire EHLB inputs.

NOTE
Do not use this wiring diagram for the EHLS channels.

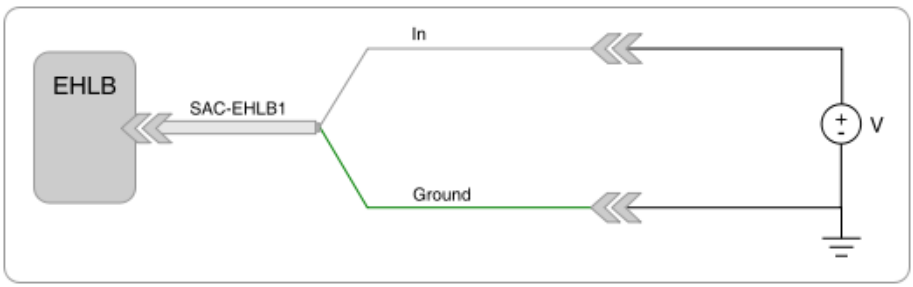


Figure 13-16: Wiring diagram for an EHLB input.

13.6 ELLB (Low Level Layer)

13.6.1 Bridge Four-Wire Option

Use the 4-wire SAC-EXDUC ELLB Transducer Cable (1-SAC-EXDUC-2) for shunt calibrations where the shunt resistors are installed directly across excitation and signal leads in the eDAQ unit. Corrections for leadwire resistance must be considered during shunt calibration.

NOTE

Connect the shield drain wire in transducer cables to circuit ground at the eDAQ end of the cables.

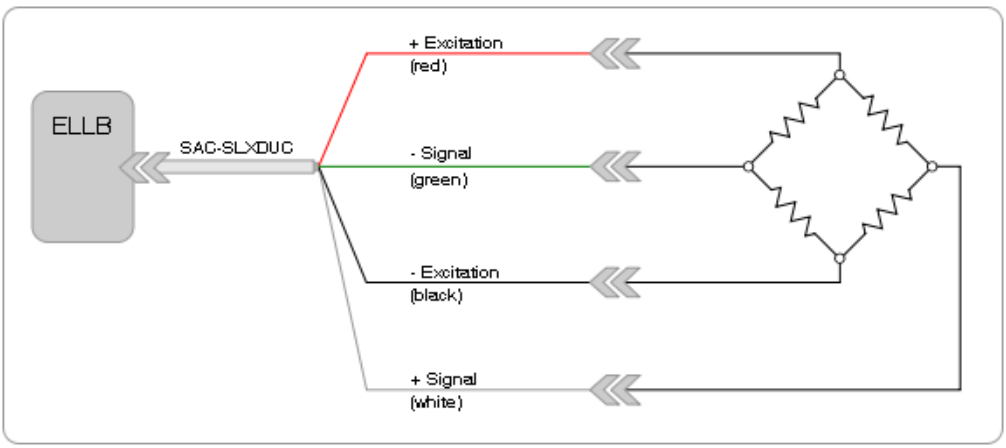


Figure 13-17: Wiring diagram for a full-bridge transducer on the ELLB layer using the four-wire cable.

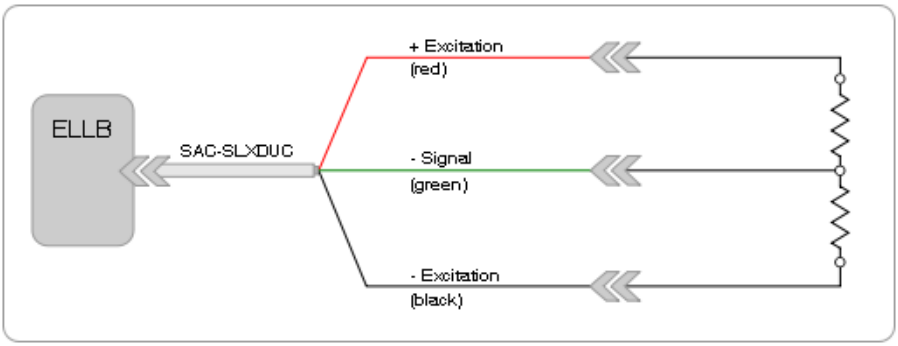


Figure 13-18: Wiring diagram for a half-bridge transducer on the ELLB layer using the four-wire cable.

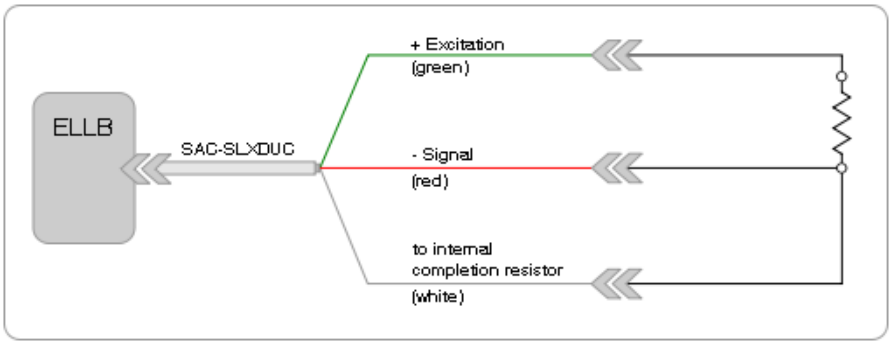


Figure 13-19: Wiring diagram for a quarter-bridge transducer on the ELLB layer using the four-wire cable.

13.6.2 Bridge Six-Wire Option

Use the 6-wire SAC-EXDUC-6-V ELLB Transducer Cable (1-SAC-EXDUC-6-V-2) for shunt calibrations where the shunt resistors are installed across the two extra wires provided; those wires are connected to one leg of the bridge. Leadwire resistance compensation is not an issue when the shunt calibration is done.

NOTE
Connect the shield drain wire in transducer cables to circuit ground at the eDAQ end of the cables.

Downscale Calibrations

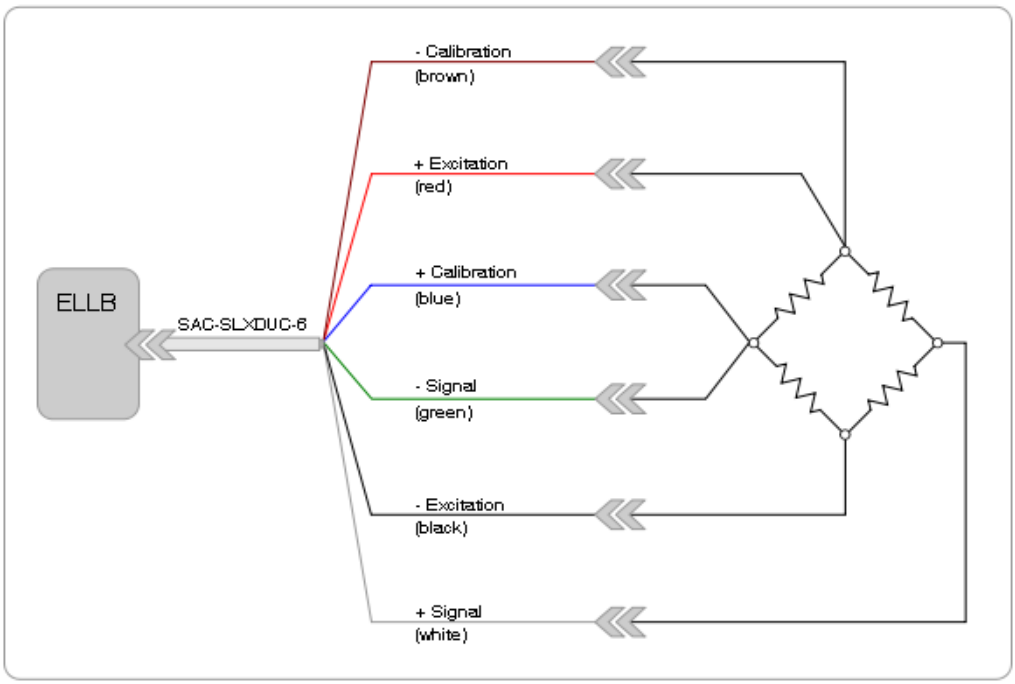


Figure 13-20: Wiring diagram for a full-bridge transducer on the ELLB layer using the six-wire cable and downscale calibration.

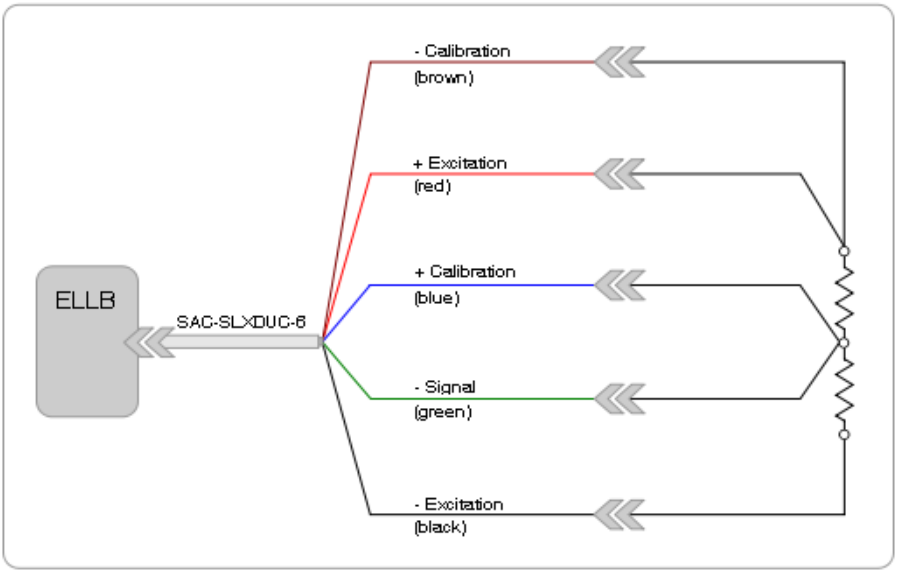


Figure 13-21: Wiring diagram for a half-bridge transducer on the ELLB layer using the six-wire cable and downscale calibration.

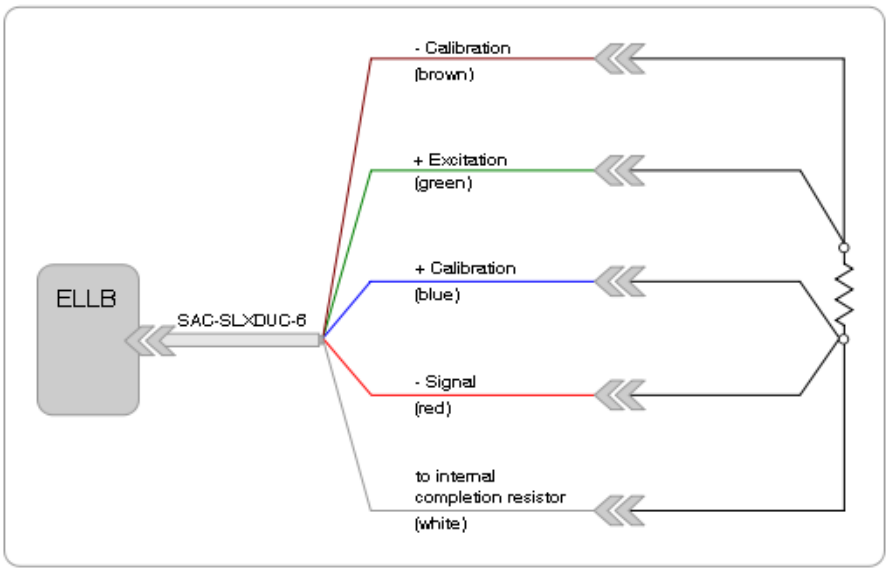


Figure 13-22: Wiring diagram for a quarter-bridge transducer on the ELLB layer using the six-wire cable and downscale calibration.

Upscale Calibrations

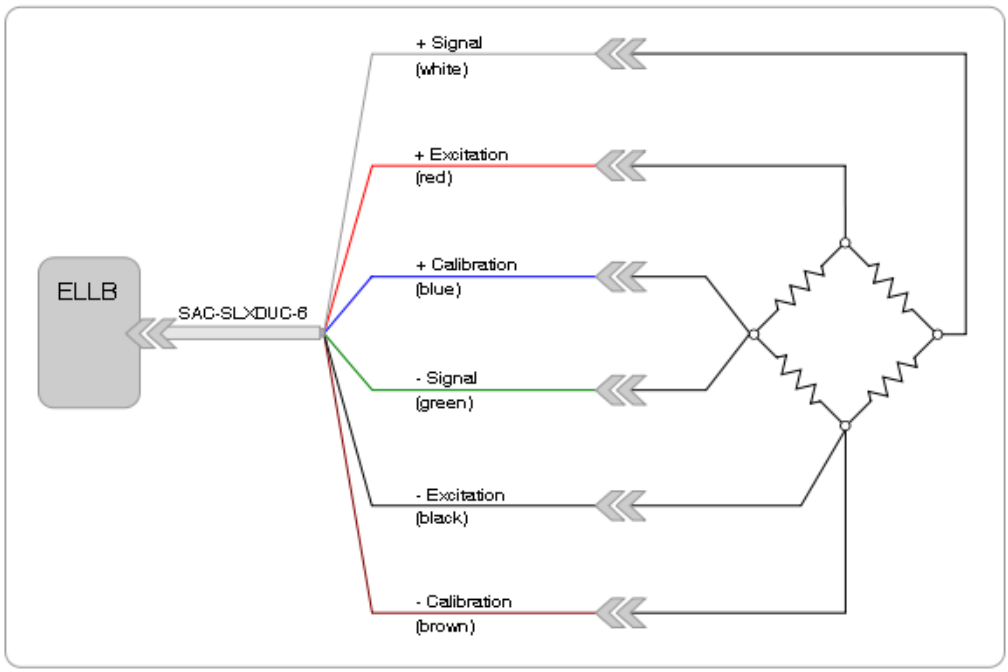


Figure 13-23: Wiring diagram for full-bridge transducer on the ELLB layer using the six-wire cable and upscale calibration.

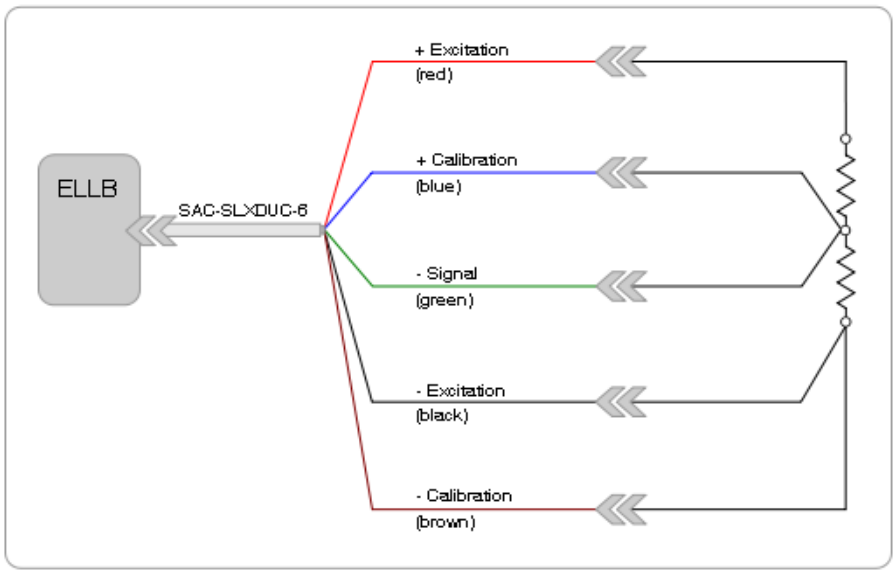


Figure 13-24: Wiring diagram for full-bridge transducer on the ELLB layer using the six-wire cable and upscale calibration.

13.6.3 Analog Input

The following wiring diagram is applicable for ELLB layer transducer channels.

NOTE

Do not use this wiring diagram for the EHLS transducer channels.

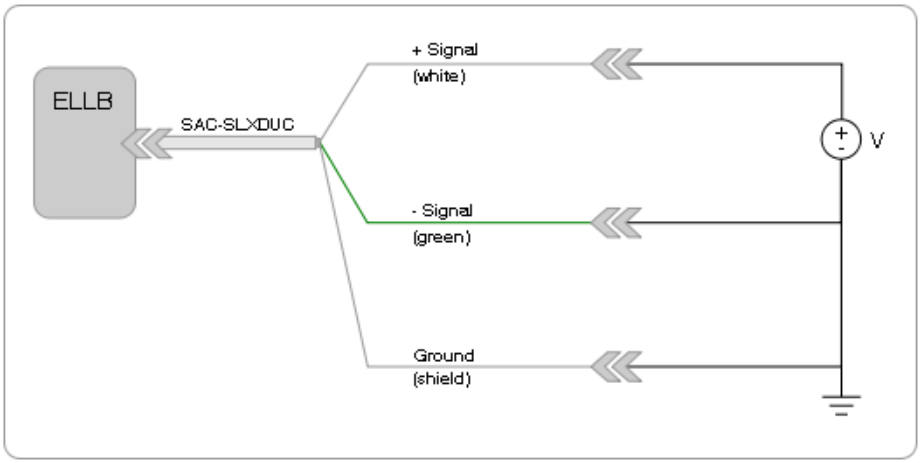


Figure 13-25: Wiring diagram for standard analog input on an ELLB layer.

14 Data Synchronization

This section describes the limitations on the synchronization of the data samples. eDAQ data acquisition synchronization across channels is accomplished by using a single master clock source that drives the data acquisition hardware. The term lag indicates that, in a Time History plot, the data appears later than it should while the term lead indicates that the data appears earlier than it should.

NOTE
Unless otherwise noted, the following discussion and numerical examples assume a 100000 Hz master clock rate.

14.1 Data Synchronization Characterization Method

To characterize eDAQ data synchronization, a ±5000-millivolt triangle function generator waveform is fed in parallel into all channels to be characterized. The frequency of the waveform is set at the sample rate divided by 1000 to yield 1000 sample points per cycle. For each reversal, all data samples that fall between ±2000 millivolts are least squares fit to provide a very accurate measurement of the zero crossing time. The differences in these zero crossing times from one channel to the next represent the data skew from one channel to the next. For each test run, the data skew on at least 200 consecutive reversals is measured and then averaged. At least 3 test runs are performed and the average data skew over the set of test runs is the characterized data skew value.

14.2 Analog Channel Synchronization

The ELLB, EHLS and EBRG channels all employ pre-start periods to compensate for their analog guard filters. In addition to the guard filter skew, there are some other secondary factors that influence data synchronization, such as A/D converter conversion time and transport delays through gain amplifiers.

NOTE
This discussion assumes no digital filtering. Ideally, linear phase digital filters do not result in phase shifts. For the EHLS and EBRG channels, however, the linear phase filters for sample rates at or below 10000 Hz result in a five microsecond lead data skew. The Butterworth digital filters are designed to match their analog equivalents and, therefore, these filters do generate significant phase shifts which, in turn, significantly affect synchronization with other transducer channels.

Following is a table that contains actual data skew characterization test results (in microseconds) for one eDAQ stack. The data in this table is consistent with the data skew times discussed in this section. The first channel on the first EHLS layer was arbitrarily used as the data sync time reference channel. The test covered the first four channels on two EHLS layers, the first four channels on one EBRG layer, the first four

channels on one ELLB layer and the first four channels on one EHLB layer. Where applicable, the data sync was characterized using three different sample rates for both the 100 kHz and the 98.304 kHz master sample rates.

	Sample Rate (Hz)					
Channel	**25000**	**10000**	**2500**	**32768**	**8192**	**2048**
HLSS_1.c01	0.00	0.00	0.00	0.00	0.00	0.00
HLSS_1.c02	0.37	0.37	0.37	0.37	0.40	0.38
HLSS_1.c03	-0.09	-0.10	-0.05	-0.09	-0.07	-0.06
HLSS_1.c04	-0.08	-0.09	-0.09	-0.09	-0.07	-0.05
HLSS_2.c01	0.11	0.14	0.21	0.10	0.15	0.05
HLSS_2.c02	0.16	0.17	0.19	0.15	0.23	0.16
HLSS_2.c03	0.12	0.14	0.17	0.11	0.16	0.11
HLSS_2.c04	0.31	0.32	0.37	0.30	0.33	0.30
Brg_1.c01	1.65	1.64	1.68	1.60	1.60	1.57
Brg_1.c02	1.55	1.54	1.59	1.50	1.49	1.46
Brg_1.c03	1.42	1.42	1.45	1.38	1.37	1.38
Brg_1.c04	1.57	1.57	1.63	1.52	1.49	1.55
LoLev_1.c01	--	11.50	11.57	--	-64.30	-64.47
LoLev_1.c02	--	10.69	10.75	--	-65.11	-65.24
LoLev_1.c03	--	11.72	11.81	--	-64.06	-64.22
LoLev_1.c04	--	13.15	13.22	--	-62.68	-62.77
HiLev_1.c01	--	--	-2.61	--	--	-12.42
HiLev_1.c02	--	--	-25.79	--	--	-35.54
HiLev_1.c03	--	--	-48.75	--	--	-58.52
HiLev_1.c04	--	--	-71.75	--	--	-81.52

14.2.1 EHLS and EBRG Channel Synchronization

For EHLS and EBRG channels, the relative data synchronization across all channels in any given eDAQ stack is typically within a few microseconds. All of these channels use the same type of Butterworth 8-pole analog guard filter, which produces a delay of around 42 microseconds (±2 microseconds). The eDAQ compensates for this delay by using a fixed value of 40 microseconds for the 100 kHz MSR to pre-start digital data sampling and align the digital data as close as possible to the actual sample rate clock. Following is a histogram showing a typical distribution of data skews in microseconds for all EHLS channels and a variety of sample rates. Note that the data skew for all channels at all sample rates is less than one microsecond, which is typical for both EHLS and EBRG layers in general.

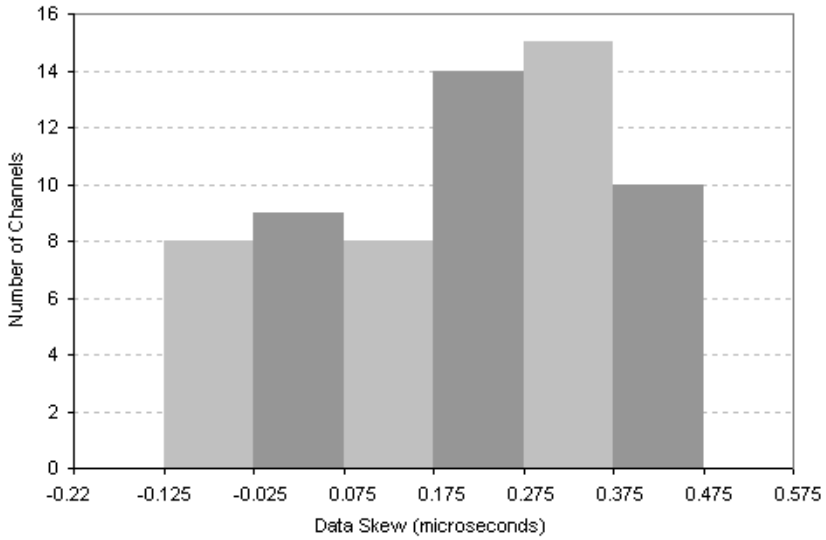


Figure 14-1: Typical data skew distribution of 64 EHLS channels for several sample rates.

14.2.2 ELLB Channel Synchronization

The ELLB channels have a 5-pole Butterworth guard filter, which creates a time lag of approximately 315 microseconds (±15 microseconds). The eDAQ compensates for this delay by using a fixed value of 300 microseconds for the 100 kHz MSR to pre-start data sampling and align the digital data as close as possible to the actual sample rate clock.

For a typical ELLB layer, the worst case channel-to-channel variation in data skew is less than five microseconds. This is significantly more than the channel-to-channel variations seen on EHLS and EBRG channels (which are typically less than one microsecond). The reason for this is that the ELLB analog guard filters have a much lower low-pass attenuation frequency (around 2.2 kHz compared to around 25.0 kHz) and, as a result, exhibit more phase shift variation on a channel-to-channel basis.

14.2.3 EHLB Channel Synchronization

The EHLB layer has only one A/D converter and no analog guard filter. The 16 input channels are run through a multiplexer ahead of the A/D converter resulting in only the first channel (c01) being in close data sync to the sample clock and the other analog channels. There is an approximate 23-microsecond delay from one EHLB channel to the next, which results in the last channel (c16) lagging the first channel (c01) by about 350 microseconds.

NOTE

The EHLB analog channels consistently lag all other channels by one sample period on about one out of every ten test runs. The channels are in sync for the other nine runs.

14.3 Digital Channel Synchronization

The ECPU and EDIO digital input channels are synchronized to the analog channels as closely as possible. The eDAQ reads the state of the digital input status register for each digital channel on each edge of the sample clock signal (i.e., when the analog channel A/D converters are read). However, because the digital status registers are updated when a digital input channel changes states, the precise time when a digital input channel changes state is, in general, somewhere in between sample clock edges and hence is not known exactly. Because of this, the digital input channels are expected to lag the analog channels by about half of the sample period on average.

NOTE

The ECPU digital input channels consistently lag all other channels by one sample period on about one out of every ten test runs. The channels are in sync for the other nine runs.

14.4 Resampled Channel Synchronization

Resampled channels include vehicle bus, serial bus, GPS and thermocouple channel inputs. The common aspect of all of these channels is that the data is not sourced from the MSR clock. As such, the data synchronization of these channels to the channels that are sourced from the eDAQ MSR is always somewhat less deterministic.
The major issue in dealing with these channels is referred to as resampling. In general, when the eDAQ reads and time stamps the data samples, the time stamps fall somewhere between eDAQ sample periods. For example, for a thermocouple channel output at 1.0 Hz, the input data samples almost always have fractional time stamps such as 1.345 seconds or 3.360 seconds. The eDAQ runs its resampling algorithm to generate data outputs (at one second intervals in this example).
While the specific details of the current resampling algorithm are beyond the scope of this document, the general characteristics are as follows. First, the resampling function is biased towards introducing a synchronization lead (i.e., the resampled time is always less than or equal to the time stamp time). In the example case, the data output associated with the 1.0 second time slot is set with the last data sample that has a time stamp of at least 1.0 seconds and less than 2.0 seconds. Because of this, the resampled channels can lead by up to one full sample period. If the data samples are sourced at a much higher rate than the resampled output rate (e.g., 50 Hz to 1 Hz), then the synchronization lead will be almost one full second consistently.

14.4.1 Bus-Oriented Channel Synchronization

The vehicle bus, serial bus, and GPS messages are time stamped as they are received by the eDAQ. The time stamps are synchronized to the same eDAQ MSR clock used for all other inputs. As such, the inherent skew (always a lag) for vehicle bus inputs is dependent on how much time elapses between the actual data sampling on the vehicle computer(s) and the time it takes for the vehicle bus message to be posted by the source processor and read and time stamped by the eDAQ.

14.4.2 Thermocouple Channel Synchronization

The ENTB and EITB channels source from a clock on these layers that is not synchronized to the eDAQ MSR clock. There is a latency of about 70 milliseconds between the actual time the data is sampled and the time the data is made available to the eDAQ (for reading and time stamping).

14.5 Analog Output Synchronization

Based on experimental testing, the data skew between ELLB and EHLS or EBRG analog outputs is very consistent at about 220 to 230 microseconds, with ELLB channels lagging the EHLS and EBRG channels. This is very close to what is ideally expected based on the following factors.

- The ELLB guard filter generates a time delay of about 300 to 350 microseconds.
- The EHLS or EBRG guard filter generates a time delay of about 40 microseconds. There is a 10-20 microsecond delay in loading the EHLS or EBRG A/D converter data into the analog output D/A converter and about another 40 microsecond transport delay in the D/A smoothing filter. The total delay is about 90 to 100 microseconds.

Following is typical test data acquired by inputting a 500 Hz sine wave into both EHLS and ELLB channels and then measuring the analog outputs using another eDAQ. The time axis (x-axis) is divided into 1000 microsecond spans. The EBRG measurements are identical to the EHLS results.

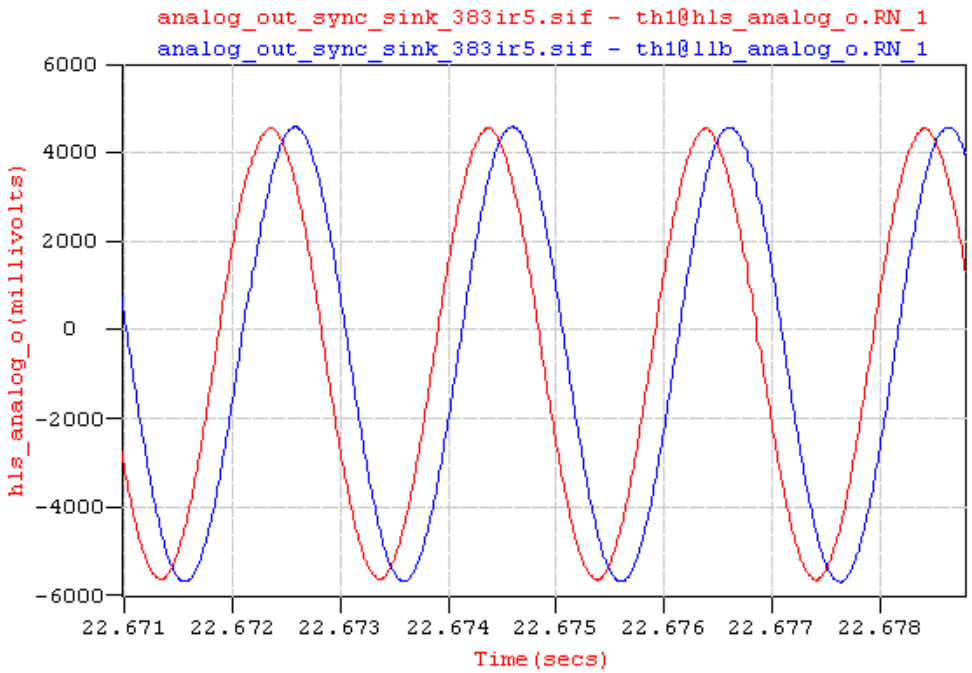


Figure 14-2: Measured data skew between ELLB and EHLS channels.

14.6 Networked eDAQ System Synchronization

14.6.1 Hardwired Network Synchronization

Master Mode

For a set of hardwired networked eDAQ systems, the data acquired on all of the slave nodes lead the data acquired on the master node by approximately one to two microseconds. The reason for this is that there is a one to two microsecond delay in the propagation of the sample clock signal from the master to the slaves.

GPS Master Mode

When using the GPS master network mode, the slave data channels lead the master by the following:

- EDIO GPS clock, 100-kHz MSR - 90-microsecond lead time
- EDIO GPS clock, 98.304-kHz MSR - 112-microsecond lead time
- ECOM GPS clock, 100 kHz-MSR - variable amount (not deterministic)
- ECOM GPS clock, 98.304-kHz MSR - variable amount (not deterministic)

Because of these limitations on GPS master data synchronization, it is recommended to use the GPS master mode with EDIO GPS clock generation only at low sample rates on the order of 100 Hz and to not use the GPS Master mode with ECOM GPS clock generation under any circumstances.

14.6.2 Wireless Network Synchronization

For wireless eDAQ networking using a GPS timing signal, test results for the accuracy of the synchronization show that data can be synchronized to 0.1 milliseconds or better assuming all systems maintain consistent GPS lock. If an eDAQ loses GPS lock for only a short period of time (i.e., 10 minutes or less), then the synchronization is still maintained to within 1.0 milliseconds or better as long as there are no sudden or significant temperature changes in the eDAQ GPS hardware.

15 Digital Filtering

The following sections provide information on the user-configurable digital filtering available for ELLB, EHLS and EBRG channels. For information on the analog filtering for each layer, refer to layer data sheet.

15.1 Signal Aliasing

In the process of converting analog input signals to digital data representations, signal aliasing can occur if the digital sample rate is too low compared to the frequency content of the analog signal. This is often referred to as under sampling the analog signal. This section discusses how the eDAQ handles aliasing.

The eDAQ has analog guard filters that work in combination with user selectable digital filters to provide low pass filters that limit the frequency content of the digitized signal. Furthermore, if an anti-aliasing filter is selected, this filtering guarantees that the digitized signal is not aliased by higher frequency content components of the analog signal. In other words, the digitized signal accurately represents all frequency content of the analog signal below the nominal low pass filter cut-off value). Note that the analog and digital filters do not have infinitely sharp low pass characteristics. The amount of filter attenuation as a function of frequency is highly dependent on the type(s) of digital filters used.

Use of these filters is most critical for low-level signal conditioning (e.g., for low level Strain SMART Module channels). Low-level signal conditioners are more susceptible to both eDAQ external and eDAQ internal electronic noise aliasing, since the strain signals are typically in the millivolt range. The signal conditioner gain amplifiers amplify the noise components as well as the actual strain signal components. In harsh electromagnetic interference (EMI) environments, the noise contributions can even be larger in magnitude than the actual strain signal contributions. Fortunately, these EMI contributions often have much higher frequency content than the actual strain contributions and can therefore be eliminated with the use of the appropriate analog and digital filters.

Note that there are situations where the EMI frequency content is in the same range as the actual signal frequency content. One classic example of this is 60 Hz AC power line noise induction. The analog and digital filters cannot eliminate this type of signal corruption, which is not aliasing in the strict definition. In this scenario, the 60 Hz noise must be eliminated before it enters the eDAQ signal conditioner.

All of the above discussion on the use of anti-aliasing filters to ensure that the digital data acquired accurately represents the input signal refers to accurately representing the frequency content of the input signal. It by no means ensures that the digital data will represent the input signal in terms of providing accurate peak-valley data that is critical to time domain analyses (such as fatigue analysis). In fact, to get peak-valley data that is guaranteed to provide 1% amplitude accuracy, the sample rate must be over 20 times the maximum frequency content of the input signal.

15.2 Digital Filter Characteristics

TCE provides two types of digital filters for analog input channels. One type emulates an eight-pole, analog Butterworth filter. The second type is an equiripple, linear-phase, finite impulse response (FIR) digital filter.

The linear-phase filter provides superior performance and is recommended over the Butterworth filter. Use the Butterworth filters when it is required to match results with other test systems.
The characteristics of these filters are shown in the following sections according to the input channel type.

15.2.1 EHLS and EBRG Digital Filters

Butterworth Eight-Pole Filter
The Butterworth digital filter closely matches the attenuation and step response characteristics of a conventional analog Butterworth filter. The magnitude, phase and step responses are shown below.

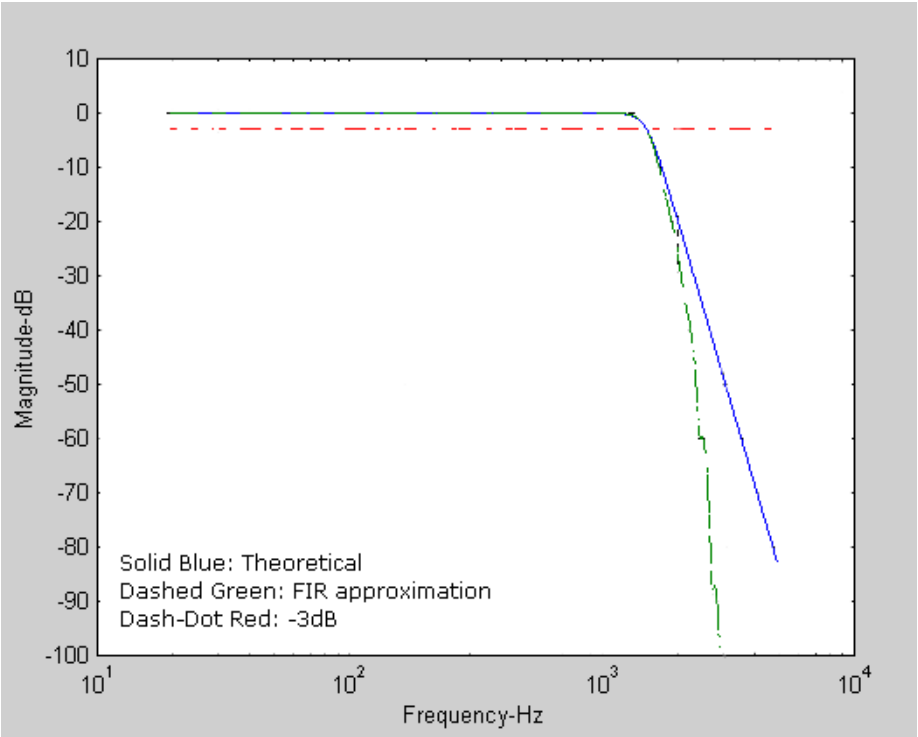


Figure 15-1: Magnitude response of an approximate eight-pole Butterworth filter.

The -3 dB frequency (break frequency) is 1500 Hz. The sharper than exact roll off in the transition band is achieved by filtering the data stream using linear phase filters before applying the approximate Butterworth filter.

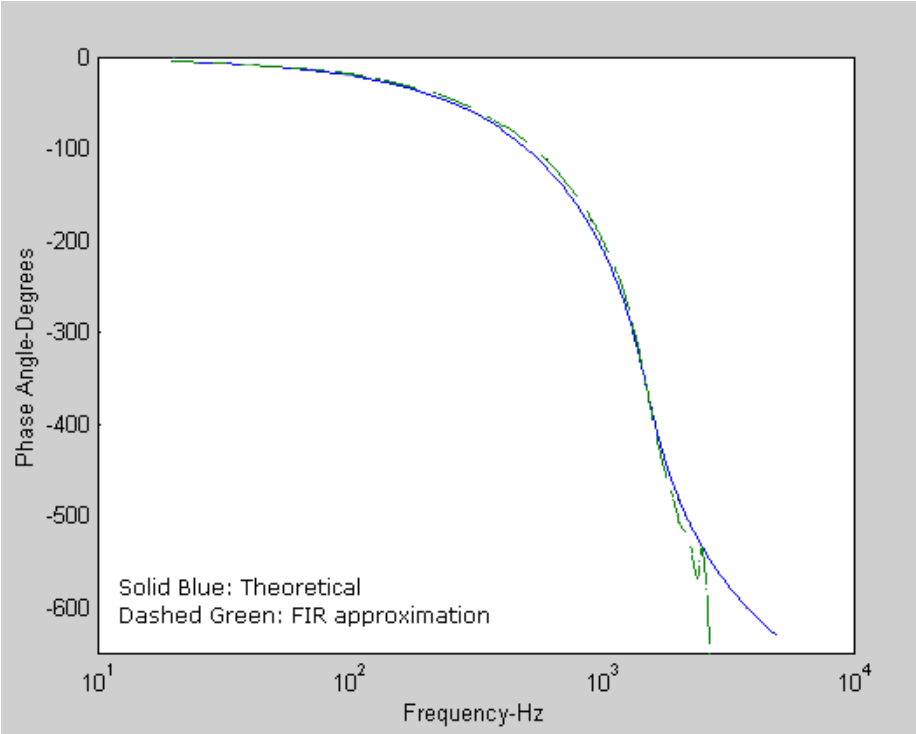


Figure 15-2: Phase response of an approximate eight-pole Butterworth filter

Note that the phase error is reasonably small up to the break frequency (1500 Hz). The phase match between any two EHLS channels using this filter is exact.

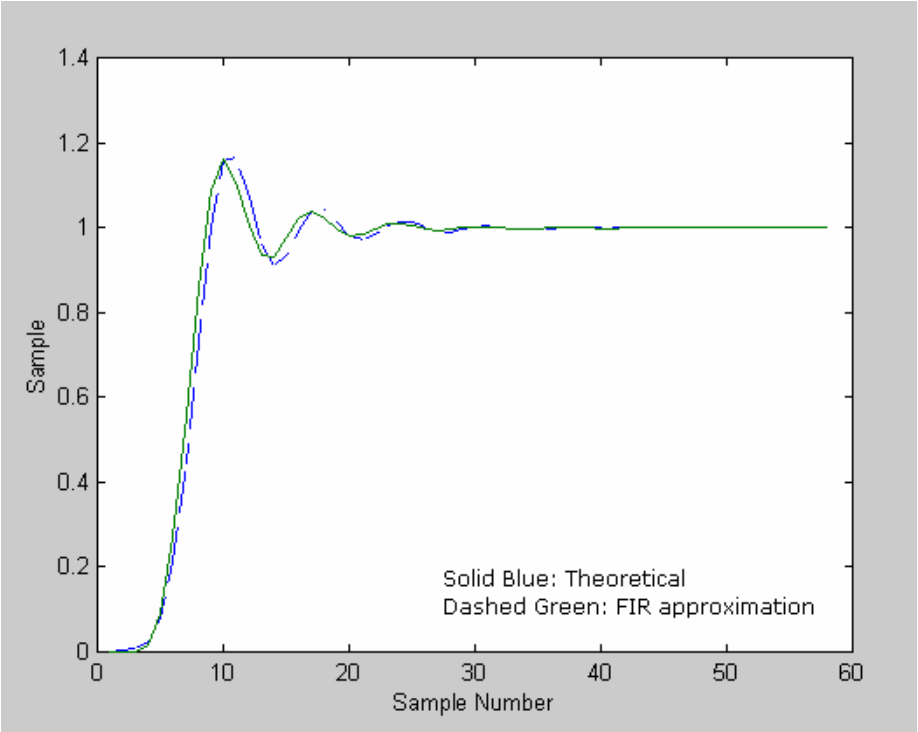


Figure 15-3: Unit step response of an eight-pole Butterworth filter approximated by a 35-coefficient FIR filter.

The unit step response closely resembles that of an analog Butterworth filter.

Linear-Phase Filter

The linear phase filter is designed using the well-known Remez algorithm. This filter provides a much sharper attenuation curve than the corresponding curve for the Butterworth filter. Notice that a linear phase filter with a roll-off start frequency of 1000 Hz at a 2500 samples per second sample rate is provided for compatibility with the similar low level layer sample rate and filter combination.

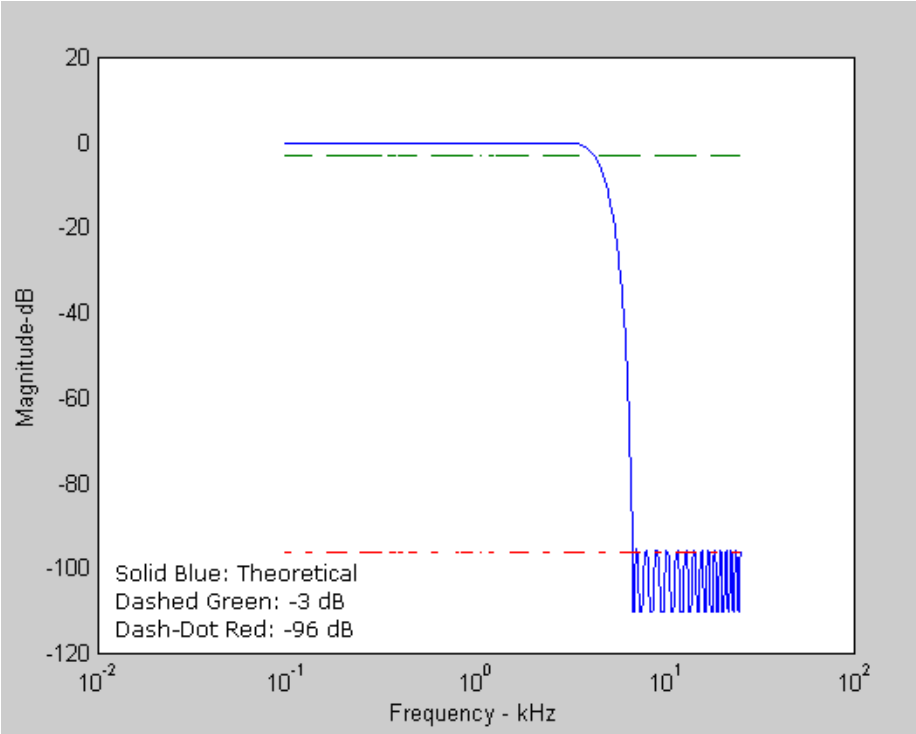


Figure 15-4: Frequency response of a typical equiripple, linear-phase FIR filter.

The filter used for the frequency response is a 37-tap filter used twice to achieve 96 dB attenuation in the stop bands. The response is calculated for a sample frequency of 10 Hz, the roll-off start frequency is 3.33 kHz, and the noise floor begins at 6.667 kHz.

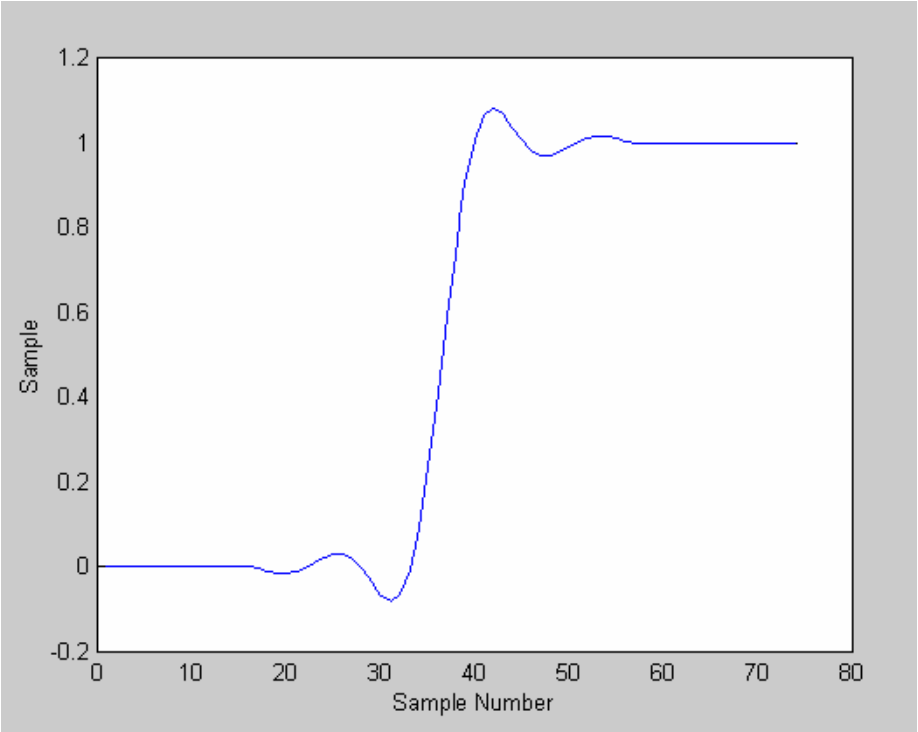


Figure 15-5: Unit step response of a typical linear-phase filter achieved by using a 37-tap equiripple FIR filter twice

Notice that the unit step response of the filter has less overshoot than that of the Butterworth filter. The response has a group delay of 37 samples, but the eDAQ compensates for the delay so that the filtered data displays no phase shift in the stored data set. Normally decimation occurs after filtering. In this case, every fifth sample is stored (decimation by five). The exact pattern of the stored data varies depending on where the decimation occurs relative to the input step edge.

15.2.2 ELLB Digital Filters

Butterworth Eight-Pole Filter

The Butterworth digital filter closely matches the attenuation and step response characteristics of a conventional analog Butterworth filter. The attenuation and the step response are shown below.

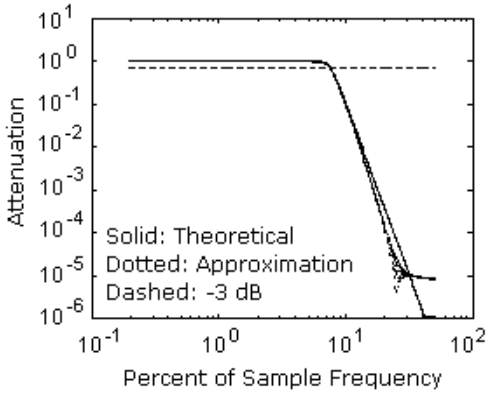


Figure 15-6: Attenuation of an eight-pole Butterworth filter.

The filter is approximated by a 111-tap FIR filter. The attenuation shows a -3 dB frequency (break frequency) of 7.5% of the sample frequency and a noise floor of about 25% of the sample frequency.

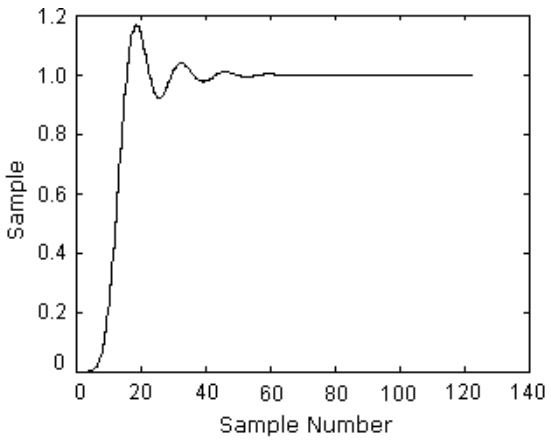


Figure 15-7: Unit step response of an eight-pole Butterworth filter.

The unit step response closely resembles that of an analog Butterworth filter.

Linear-Phase Filter

The linear phase filter is designed using the well known Remez algorithm. The ratio of stop band to pass band frequency is 1.5:1. This filter provides a much sharper attenuation curve than the corresponding curve for the Butterworth filter.

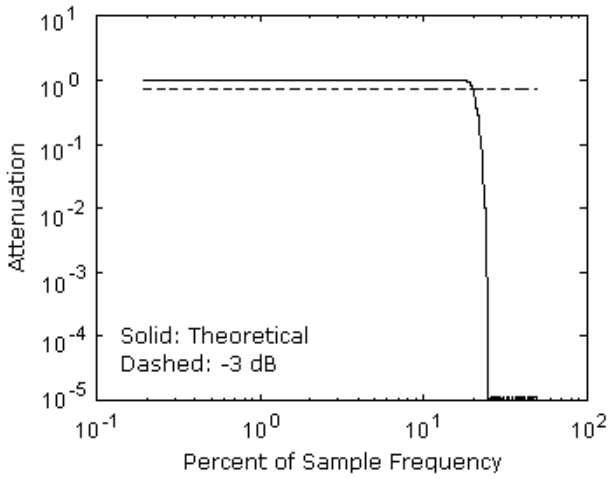


Figure 15-8: Attenuation of a 71-tap equiripple, linear-phase FIR filter.

From the attenuation curve, notice that the roll-off frequency is 16.88% of the sample frequency, the roll-off span is 8.325% of the sample frequency and the noise floor frequency is 25% of the sample frequency.

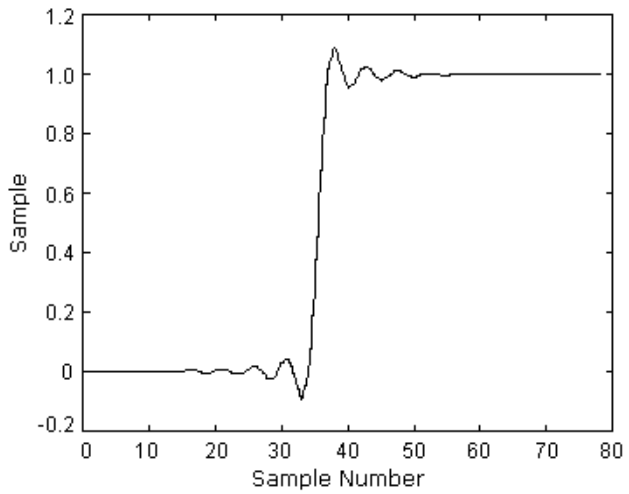


Figure 15-9: Unit step response of a 71-tap equiripple, linear-phase FIR filter.

Notice that the unit step response of the filter has less overshoot than that of the Butterworth filter. The response has a group delay of 35 samples, but the eDAQ compensates for the delay so that the filtered data displays no phase shift in the stored data set.

16 Xth-Percentile Benchmark Tests

The following benchmark tests give an indication of the eDAQ processing limitations for the special case of using the Xth-percentile mode of the Statistical Analysis computed channel. The primary reason for this benchmark testing is that sorting large arrays can become very time consuming as the size of the arrays increase.
All of the tests have the following configuration properties.

- An input data signal using a function generator to produce highly unordered data where nearly every data sample represents a reversal as shown in the plot below.

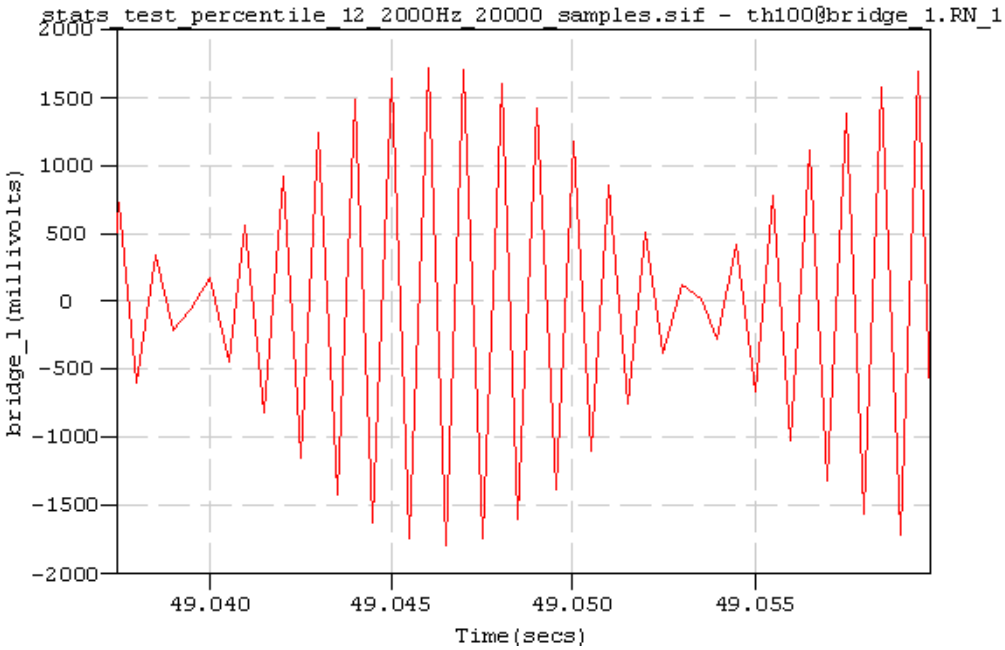


Figure 16-1: Plot of the input signal to the eDAQ- as sampled by a test bridge channel.

- Four bridge channels with 32-bit float output data types.
- Twelve Statistical Analysis computed channels using the Xth-percentile mode to compute the 10%, 50% and 90% percentile values for each of the four bridge channels.
- Two Time History DataModes: one to store the four bridge channels and the other to store the twelve Xth-percentile mode Statistical Analysis computed channels.
- All data storage in the eDAQ internal flash memory.

After some preliminary testing, the following four tests were performed for final benchmarking. The only varied parameters were the bridge channel sample rate and the size of the Statistical Analysis channel analysis window.

Test	Bridge Sample Rate	Analysis Window Size
Test 1	2000 Hz	20000 samples
Test 2	2000 Hz	50000 samples
Test 3	5000 Hz	20000 samples
Test 4	5000 Hz	50000 samples

All of the tests were run for several minutes to determine if the eDAQ can handle the processing load. The first three tests ran with no problems. However, Test 4 reset on a DeviceOverFlow error shortly after the start of the test run.

17 Data Processing Algorithms

17.1 Peak Valley Processing Algorithm

There are three states in the peak valley processing algorithm. The algorithm starts in the initialize state. Thereafter it toggles between the peak search and valley search states. These states are detailed as follows.

Initialize

The algorithm tracks the maximum and minimum input values until the difference between the maximum and minimum exceeds the specified hysteresis level. If the minimum value preceded the maximum value, then the minimum value is the first valley and the algorithm state switches to peak search. If the maximum value preceded the minimum value, then the maximum value is the first peak and the algorithm state switches to valley search.

Peak Search

The algorithm searches for a peak, tracking the maximum and minimum values since the last stored valley until their difference exceeds the hysteresis level. At this point, the maximum value is output as the next peak and the algorithm state switches to valley search.

Valley Search

The algorithm searches for a valley, tracking the maximum and minimum values since the last stored peak until their difference exceeds the hysteresis level. At this point, the minimum value is output as the next valley and the algorithm state switches to peak search.

17.2 Rainflow Cycle Counting Algorithm

Rainflow counted cycles are typically used in low cycle fatigue damage analyses. The rainflow counting algorithm is based on the “one-pass” algorithm described in the paper Simple Rainflow Counting Algorithms, International Journal of Fatigue, January 1982, by D. Socie and S. Downing. The algorithm described in this paper generates the set of closed cycles for the input peak valley sequence, assuming that the sequence repeats itself.
However, to support proper “rainflow histogram addition” (i.e., generating a composite rainflow histogram from multiple rainflow histograms defined in a specific sequence), the eDAQ stores both the sequence of unclosed reversals and the histogrammed set of closed cycles in the Rainflow DataMode.

NOTE

The algorithm requires an allocated memory stack to store the reversals that have not yet closed. The eDAQ uses a fixed stack size of 1024, which should suffice for the vast majority of applications. In the rare event that this allocation is insufficient, the eDAQ aborts the Rainflow DataMode processing and sets an error flag in the output data file.

18 Cable Resistances

The following table lists measured resistances for a selection of SoMat cables.

Cable	Length (m)	Order Number	Resistance (Ohms)
Transducer Cable	2	1-SAC-TRAN-MP-2-2	0.27
	10	1-SAC-TRAN-MP-10-2	1.25
Extension Cable	0.4	1-SAC-EXT-MF-0.4-2	0.06
	2	1-SAC-EXT-MF-2-2	0.23
	5	1-SAC-EXT-MF-5-2	0.61
	10	1-SAC-EXT-MF-10-2	1.20
	15	1-SAC-EXT-MF-15-2	1.84

19 CE Compliance

The following section provides important notes on the CE compliance of the eDAQ hardware and cables.

19.1 eDAQ Hardware

CAUTION
Do not remove any CE-labeled component or modify a CE-labeled component from its original condition. Do not disassemble individual layers. HBM cannot ensure the CE compliance of any hardaware that has been modified.

The only recent modification to the eDAQ for CE compliance is on the back panel of analog-out enabled EHLS and EBRG layers. The Analog Out connector cutout is left unpainted to ensure solid metal-to-metal contact between the internal and external connectors.

19.2 Cables

CAUTION
HBM cannot ensure the CE compliance of any cable that has been modified from its original condition.

The following cables have been recently modified to be CE compliant. All other cables are also CE compliant.

- SAC-EPWR15 Power Cable (1-SAC-EPWR15-2)
- SAC-EXT-VBM Vehicle Bus Module Extension Cable (1-SAC-EXT-VBM-2)
- SAC-TRAN-AO Analog Out Transducer Cable (1-SAC-TRAN-AO-2)

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