# *P801 – PC Debug Card*

# *User' s Manual*

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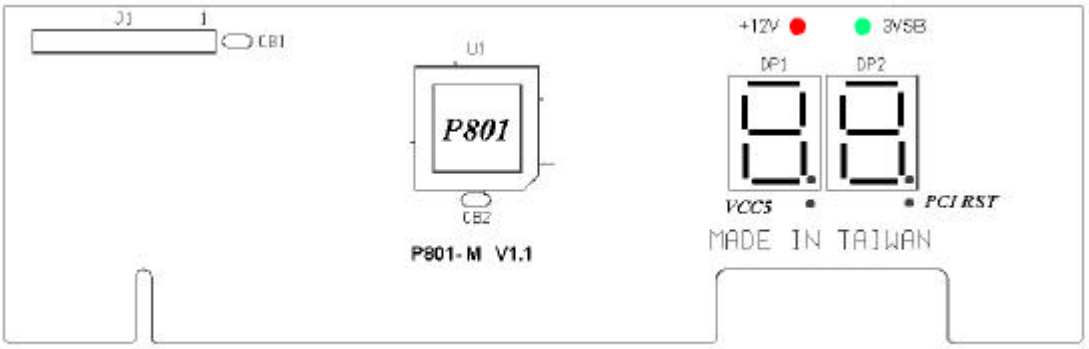
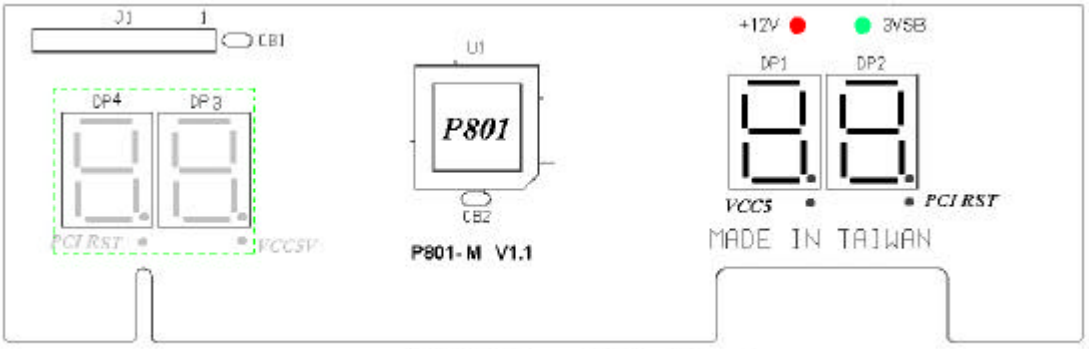
## *P801- 2 LED*



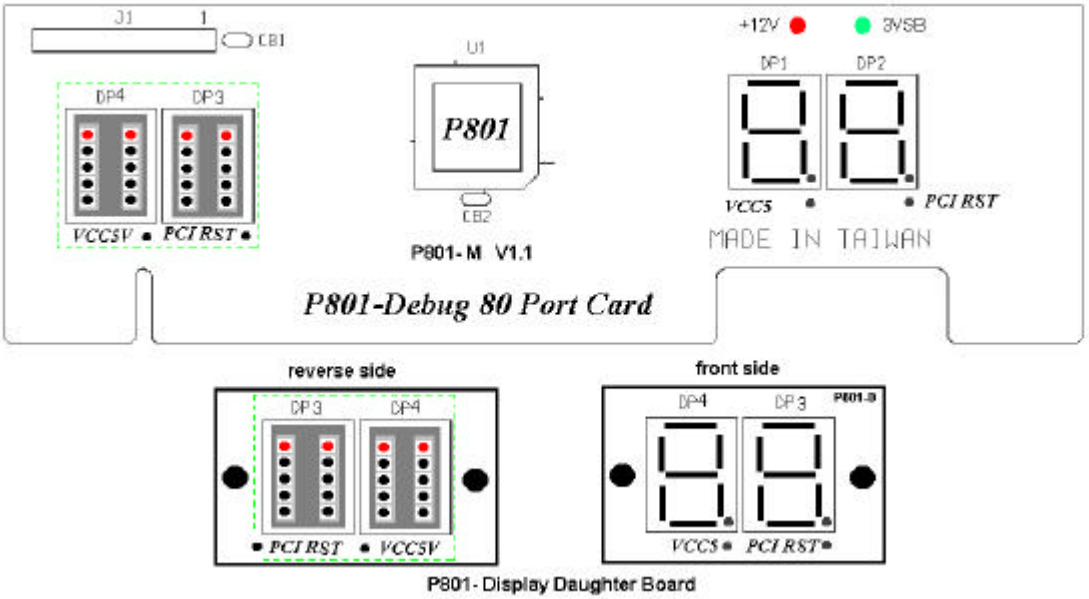

*P801-Debug 80 Port Card*

## *P801- 4 LED*

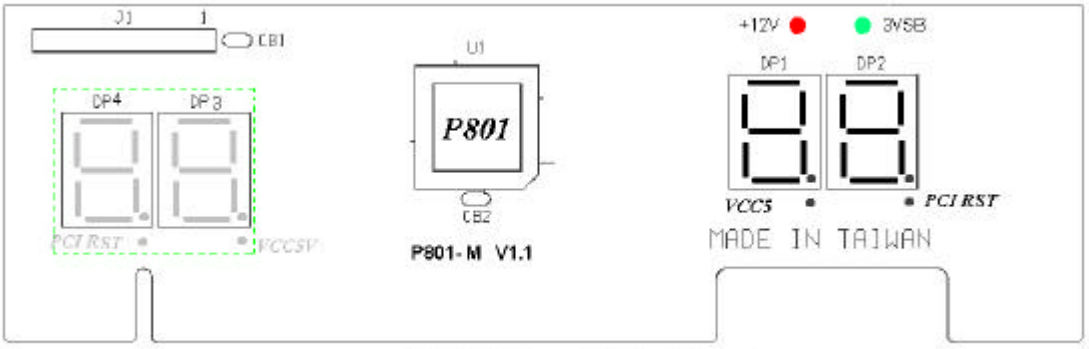



*P801-Debug 80 Port Card*

## *P801- M 4 LED*




P801- Display Daughter Board




*P801-Debug 80 Port Card*

1. **On board Display " DP1/DP2",**
2. **Optional "DP3/DP4" on the reverse side. or pin header on front side.**
3. **PCI RST, VCC +5V, VCC +12V, VCC 3VSB LED Display**
4. **P801 board will be to detect "PCICLK", some board (P4) have to disable BIOS manual item "Frequency/Voltage Control - Auto Detect PCI CLK"**

AWARD SOFTWARE™

# POST Error Code

## BIOS6.00 Revision 1.0

**NOTE:** **EISA POST** codes are typically output to port address 300h
**ISA POST** codes are output to port address 80h

| POST (hex) | Description |
|---|---|
| CFh | Test CMOS R/W functionality. |
| C0h | Early chipset initialization:<br>-Disable shadow RAM<br>-Disable L2 cache (socket 7 or below)<br>-Program basic chipset registers |
| C1h | Detect memory<br>-Auto-detection of DRAM size, type and ECC.<br>-Auto-detection of L2 cache (socket 7 or below) |
| C3h | Expand compressed BIOS code to DRAM |
| C5h | Call chipset hook to copy BIOS back to E000 & F000 shadow RAM. |
| 01h | Expand the Xgroup codes locating in physical address 1000:0 |
| 02h | Reserved |
| 03h | Initial Superio_Early_Init switch. |
| 04h | Reserved |
| 05h | 1. Blank out screen<br>2. Clear CMOS error flag |
| 06h | Reserved |
| 07h | 1. Clear 8042 interface<br>2. Initialize 8042 self-test |
| 08h | 1. Test special keyboard controller for Winbond 977 series Super I/O chips.<br>2. Enable keyboard interface. |
| 09h | Reserved |

| POST (hex) | Description |
|---|---|
| 0Ah | 1. Disable PS/2 mouse interface (optional).<br>2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional).<br>3. Reset keyboard for Winbond 977 series Super I/O chips. |
| 0Bh | Reserved |
| 0Ch | Reserved |
| 0Dh | Reserved |
| 0Eh | Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker. |
| 0Fh | Reserved |
| 10h | Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support. |
| 11h | Reserved |
| 12h | Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override. |
| 13h | Reserved |
| 14h | Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers. |
| 15h | Reserved |
| 16h | Initial onboard clock generator if Early_Init_Onboard_Generator is defined. See also POST 26h. |
| 17h | Reserved |
| 18h | Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686). |
| 19h | Reserved |
| 1Ah | Reserved |
| 1Bh | Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR. |
| 1Ch | Reserved |
| 1Dh | Initial EARLY_PM_INIT switch. |
| 1Eh | Reserved |
| 1Fh | Load keyboard matrix (notebook platform) |
| 20h | Reserved |
| 21h | HPM initialization (notebook platform) |
| 22h | Reserved |
| 23h | 1. Check validity of RTC value:<br>e.g. a value of 5Ah is an invalid value for RTC minute.<br>2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. |
| 24h | Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. |
| 25h | Early PCI Initialization:<br>-Enumerate PCI bus number.<br>-Assign memory & I/O resource<br>-Search for a valid VGA device & VGA BIOS, and put it into C000:0 |

| POST (hex) | Description |
|---|---|
| 26h | 1. If Early_Init_Onboard_Generator is not defined Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots.<br>2. Init onboard PWM<br>3. Init onboard H/W monitor devices |
| 27h | Initialize INT 09 buffer |
| 28h | Reserved |
| 29h | 1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address.<br>2. Initialize the APIC for Pentium class CPU.<br>3. Program early chipset according to CMOS setup. Example: onboard IDE controller.<br>4. Measure CPU speed. |
| 2Ah | Reserved |
| 2Bh | Invoke Video BIOS |
| 2Ch | Reserved |
| 2Dh | 1. Initialize double-byte language font (Optional)<br>2. Put information on screen display, including Award title, CPU type, CPU speed, full screen logo. |
| 2Eh | Reserved |
| 2Fh | Reserved |
| 30h | Reserved |
| 31h | Reserved |
| 32h | Reserved |
| 33h | Reset keyboard if Early_Reset_KB is defined e.g. Winbond 977 series Super I/O chips. See also POST 63h. |
| 34h | Reserved |
| 35h | Test DMA Channel 0 |
| 36h | Reserved |
| 37h | Test DMA Channel 1. |
| 38h | Reserved |
| 39h | Test DMA page registers. |
| 3Ah | Reserved |
| 3Bh | Reserved |
| 3Ch | Test 8254 |
| 3Dh | Reserved |
| 3Eh | Test 8259 interrupt mask bits for channel 1. |
| 3Fh | Reserved |
| 40h | Test 8259 interrupt mask bits for channel 2. |
| 41h | Reserved |
| 42h | Reserved |
| 43h | Test 8259 functionality. |
| 44h | Reserved |
| 45h | Reserved |
| 46h | Reserved |
| 47h | Initialize EISA slot |
| 48h | Reserved |

| POST (hex) | Description |
|---|---|
| 49h | 1. Calculate total memory by testing the last double word of each 64K page.<br>2. Program write allocation for AMD K5 CPU. |
| 4Ah | Reserved |
| 4Bh | Reserved |
| 4Ch | Reserved |
| 4Dh | Reserved |
| 4Eh | 1. Program MTRR of M1 CPU<br>2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range.<br>3. Initialize the APIC for P6 class CPU.<br>4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical. |
| 4Fh | Reserved |
| 50h | Initialize USB Keyboard & Mouse. |
| 51h | Reserved |
| 52h | Test all memory (clear all extended memory to 0) |
| 53h | Clear password according to H/W jumper (Optional) |
| 54h | Reserved |
| 55h | Display number of processors (multi-processor platform) |
| 56h | Reserved |
| 57h | 1. Display PnP logo<br>2. Early ISA PnP initialization<br>-Assign CSN to every ISA PnP device. |
| 58h | Reserved |
| 59h | Initialize the combined Trend Anti-Virus code. |
| 5Ah | Reserved |
| 5Bh | (Optional Feature)<br>Show message for entering AWDFLASH.EXE from FDD (optional) |
| 5Ch | Reserved |
| 5Dh | 1. Initialize Init_Onboard_Super_IO<br>2. Initialize Init_Onbaord_AUDIO. |
| 5Eh | Reserved |
| 5Fh | Reserved |
| 60h | Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility. |
| 61h | Reserved |
| 62h | Reserved |
| 63h | Reset keyboard if Early_Reset_KB is not defined. |
| 64h | Reserved |
| 65h | Initialize PS/2 Mouse |
| 66h | Reserved |
| 67h | Prepare memory size information for function call:<br>INT 15h ax=E820h |
| 68h | Reserved |
| 69h | Turn on L2 cache |
| 6Ah | Reserved |

| POST (hex) | Description |
|---|---|
| 6Bh | Program chipset registers according to items described in Setup & Auto-configuration table. |
| 6Ch | Reserved |
| 6Dh | 1. Assign resources to all ISA PnP devices.<br>2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO". |
| 6Eh | Reserved |
| 6Fh | 1. Initialize floppy controller<br>2. Set up floppy related fields in 40:hardware. |
| 70h | Reserved |
| 71h | Reserved |
| 72h | Reserved |
| 73h | (Reserved |
| 74h | Reserved |
| 75h | Detect & install all IDE devices: HDD, LS120, ZIP, CDROM... |
| 76h | (Optional Feature)<br>Enter AWDFLASH.EXE if:<br>-AWDFLASH.EXE is found in floppy drive.<br>-ALT+F2 is pressed. |
| 77h | Detect serial ports & parallel ports. |
| 78h | Reserved |
| 79h | Reserved |
| 7Ah | Detect & install co-processor |
| 7Bh | Reserved |
| 7Ch | Init HDD write protect. |
| 7Dh | Reserved |
| 7Eh | Reserved |
| 7Fh | Switch back to text mode if full screen logo is supported.<br>-If errors occur, report errors & wait for keys<br>-If no errors occur or F1 key is pressed to continue:<br>◆Clear EPA or customization logo. |
| 80h | Reserved |
| 81h | Reserved |
| **E8POST.ASM starts** | |
| 82h | 1. Call chipset power management hook.<br>2. Recover the text fond used by EPA logo (not for full screen logo)<br>3. If password is set, ask for password. |
| 83h | Save all data in stack back to CMOS |
| 84h | Initialize ISA PnP boot devices |
| 85h | 1. USB final Initialization<br>2. Switch screen back to text mode |
| 86h | Reserved |
| 87h | NET PC: Build SYSID Structure. |
| 88h | Reserved |
| 89h | 1. Assign IRQs to PCI devices<br>2. Set up ACPI table at top of the memory. |
| 8Ah | Reserved |

| POST (hex) | Description |
|---|---|
| 8Bh | 1. Invoke all ISA adapter ROMs<br>2. Invoke all PCI ROMs (except VGA) |
| 8Ch | Reserved |
| 8Dh | 1. Enable/Disable Parity Check according to CMOS setup<br>2. APM Initialization |
| 8Eh | Reserved |
| 8Fh | Clear noise of IRQs |
| 90h | Reserved |
| 91h | Reserved |
| 92h | Reserved |
| 93h | Read HDD boot sector information for Trend Anti-Virus code |
| 94h | 1. Enable L2 cache<br>2. Program Daylight Saving<br>3. Program boot up speed<br>4. Chipset final initialization.<br>5. Power management final initialization<br>6. Clear screen & display summary table<br>7. Program K6 write allocation<br>8. Program P6 class write combining |
| 95h | Update keyboard LED & typematic rate |
| 96h | 1. Build MP table<br>2. Build & update ESCD<br>3. Set CMOS century to 20h or 19h<br>4. Load CMOS time into DOS timer tick<br>5. Build MSIRQ routing table. |
| FFh | Boot attempt (INT 19h) |

# POST Error Code
## BIOS4.51G Revision 1.0

**NOTE:** **EISA POST** codes are typically output to port address 300h
**ISA POST** codes are output to port address 80h

| POST (hex) | | Description |
|---|---|---|
| C0 | Turn off chipset Cache | OEM specific-cache control |
| 1 | Processor Test1 | Processor status (1FLAGS) Verification.<br>Tests the following processor status fllages:<br>Carry, zero, sign, overflow, The BIOS sets each flag, verifies they are set, then turns each flag off and verifies it is off. |
| 2 | Processor Test2 | Read / Write / Verify all CPU registers, except ss , sp, andbp with date<br>pattern FF and 00 |

| POST (hex) | | Description |
|---|---|---|
| 3 | Initialize Chips | Disable NMI, PIE, AIE, UEI, SQWV<br>Disable Video, parity checking, DMA Reset mach coprocessor, Clear all page registers, CMOS shutdown byte Initialize timer 0, 1, and 2, including set EISA timer to a known state Initialize DMA controllers 0 and 1.Initialize interrupt controllers 0 and 1Initialize EISA extended registers. |
| 4 | Test Memory Refresh Toggle | RAM must be periodically refreshed to keep the memory from decaying. This function is working properly. |
| 5 | Blank video, Initialize keyboard | keyboard controller initialization. |
| 6 | Reserved | Reserved |
| 7 | Test CMOS Interface and Battery Status | Verifies CMOS is working correctly, detects bad battery. |
| BE | Chipset default Initialization | Programming chipset Register with power on BIOS defaults. |
| C1 | Memory presence Test | OEM specific – Test to size on-board memory. |
| C5 | Early shadow | OEM Specific – Early shadow enable for fast boot. |
| C6 | Cache presence | External cache size detection test . |
| 8 | Setup low memory | Early chip set initialization memory presence test OEM chip set routines, Clear low 64k of memory, Test first 64k memory. |
| 9 | Early Cache Initialization | Cyrix CPU initialization, Cache Initialization. |
| A | Setup Interrupt Vector Table | Initialize first 120 interrupt vectors with SPURIOUS – INT – H DLR<br>and initialize INT 00h-1Fh according to INT – TBL |
| B | Test CMOS RAM Checksum | Test CMOS RAM Chceksum, if bad, or insert key pressed, load defaults. |
| C | Initialize keyboard | Detect type of keyboard controller(optional) Set NUM – COCK status. |
| D | Initialize Video | Detect CPU clock, Read CMOS location 14h to find out, Type of video in use. Detect and Initialize Video Adapter. |
| E | Test Video Memory | Test video memory, write sign – on message to screen, Setup shadow RAM – Enable shadow According to Setup. |
| F | Test DMA Controller 0 | BIOS checksum test. keyboard detect and initialization. |
| 10 | Test DMA Controller 1 | BIOS checksum test. keyboard detect and initialization. |
| 11 | Test DMA page registers | Test DMA Page registers. |
| 12 | Reserved | Reserved |
| 13 | Reserved | Reserved |

| POST (hex) | | Description |
|---|---|---|
| 14 | Test Timer Counter 2 | Test 8254 Timer 0 Counter 2. |
| 15 | Test 8259-1 MASK Bits | Verify 8259 channel 1 masked interrupts by alternately turning off and on the interrupt lines. |
| 16 | Test 8259-2 MASK Bits | Verify 8259 channel 2 masked interrupts by alternately turning off and on the interrupt lines. |
| 17 | Test Stuck 8259 Interrupts | Turn off interrupt then verify no interrupt is on. |
| 18 | Test 8259 Interrupt Functionality | Force an interrupt and verify the Interrupt occurred. |
| 19 | Test Stuck NMI Bits(Parity / IO Check) | Verify NMI can be cleared. |
| 1A | Display CPU clock | Display CPU clock |
| 1B - 1E | Reserved | Reserved |
| 1F | Set EISA Mode | If EISA non – volatile memory checksum is good, execute EISA initialization, if not, execute ISA tests an clear EISA node flag. Test EISA Configuration Memory Integrity ( checksum a communication Interface ). |
| 20 | Enable Slot 0 | Initialize slot 0 ( system board ). |
| 21 – 2F | Enable Slots 1 – 15 | Initialize slots 1 through 15 |
| 30 | Size Base and Extended Memory | size base memory form 256k to 640k and extended memory above 1MB. |
| 31 | Test Base and Extended Memory | Test base memory from 256k to 640k and extended memory above 1MB Using various patterns. NOTE : This test is skipped in EISA mode and can be skipped with ESC key in ISA mode. |
| 32 | Test EISA | If EISA Mode flag is set then test EISA memory found is slots Initialization. NOTE : This test is skipped in ISA mode and can be skipped with ESC key in ISA mode. |
| 33 – 3B | Reserved | Reserved |
| 3C | Setup Enabled | Setup Enabled |
| 3D | Initialize & Install Mouse | Detect if mouse is present, initialize mouse, install interrupt vectors. |
| 3E | Setup Cache Controller | Initialize cache controller. |
| 3F | Reserved | Reserved |
| BF | Chipset Initialization | Program chipset registers with setup values |
| 40 | Display | Display virus protect disable or Enable |

| POST (hex) | | Description |
|---|---|---|
| 41 | Initialize Floppy Drive Controller | Initialize floppy disk controller and any drives. |
| 42 | Initialize Hard Drive & Controller | Initialize hard disk controller and drives. |
| 43 | Detect & Initialize Serial / Parallel Ports | Initialize any serial and parallel posts ( also game port ). |
| 44 | Reserved | Reserved |
| 45 | Detect & Initialize Math Coprocessor | Initialize math coprocessor |
| 46 – 4D | Reserved | Reserved |
| 4E | Manufacturing POST Loop or Display Messages | Reboot if Manufacturing POST Loop pin is set. Otherwise display any messages (I, e,. any non – fatal error that were detected during POST) and enter setup. |
| 4F | Security Check | Ask password security ( optional ) . |
| 50 | Write CMOS | Write all CMOS values back to RAM and clear screen. |
| 51 | Pre – boot Enable | Enable parity checker, Enable NMI, Enable cache before boot. |
| 52 | Initialize Option ROMs | Initialize any option ROMs present from C8000h to EFFFFh NOTE : When FSCAN option is Enabled, ROMs initialize form C8000h to E7FFFh. |
| 53 | Initialize Time value | Initialize time value in 40h : BIOS area. |
| 60 | Setup Virus Protect | Setup virus protect according to Setup. |
| 61 | Setup Boot Speed | Set system speed for boot |
| 62 | Setup Num Lock | Setup NumLock status according to setup. |
| 63 | Boot Attempt | Set low stack Boot via INT 19h |
| B0 | Spurious | If interrupt occurs in protected |
| B1 | Unclaimed NMI | If unmasked NMI occurs, display Press F1 to disable F1 NMI, F2 reboot. |
| E1 -EF | Setup Pages | E1 – Page 2, etc. |
| FF | Boot | Boot |

# POST Error Code
## BIOS4.00 Release 6.x.

| POST (hex) | | Description |
|---|---|---|
| Code | Beeps | |
| 02h | | Verify Real Mode |
| 03h | | Disable Non-Maskable Interrupt (NMI) |
| 04h | | Get CPU type |
| 06h | | Initialize system hardware |
| 07h | | Disable shadow and execute code from the ROM. |
| 08h | | Initialize chipset with initial POST values |
| 09h | | Set IN POST flag |
| 0Ah | | Initialize CPU registers |
| 0Bh | | Enable CPU cache |
| 0Ch | | Initialize caches to initial POST values |
| 0Eh | | Initialize I/O component |
| 0Fh | | Initialize the local bus IDE |
| 10h | | Initialize Power Management |
| 11h | | Load alternate registers with initial POST values |
| 12h | | Restore CPU control word during warm boot |
| 13h | | Initialize PCI Bus Mastering devices |
| 14h | | Initialize keyboard controller |
| 16h | 1-2-2-3 | BIOS ROM checksum |
| 17h | | Initialize cache before memory Auto size |
| 18h | | 8254 timer initialization |
| 1Ah | | 8237 DMA controller initialization |
| 1Ch | | Reset Programmable Interrupt Controller |
| 20h | 1-3-1-1 | Test DRAM refresh |
| 22h | 1-3-1-3 | Test 8742 Keyboard Controller |
| 24h | | Set ES segment register to 4 GB |
| 28h | | Auto size DRAM |
| 29h | | Initialize POST Memory Manager |
| 2Ah | | Clear 512 kB base RAM |
| 2Ch | 1-3-4-1 | RAM failure on address line ***xxx***x* |
| 2Eh | 1-3-4-3 | RAM failure on data bits ***xxx***x* of low byte of memory bus |
| 2Fh | | Enable cache before system BIOS shadow |
| 32h | | Test CPU bus-clock frequency |
| 33h | | Initialize Phoenix Dispatch Manager |
| 36h | | Warm start shut down |
| 38h | | Shadow system BIOS ROM |
| 3Ah | | Auto size cache |
| 3Ch | | Advanced configuration of chipset registers |
| 3Dh | | Load alternate registers with CMOS values |
| 41h | | Initialize extended memory for RomPilot |
| 42h | | Initialize interrupt vectors |
| 45h | | POST device initialization |

| POST (hex) | | Description |
|---|---|---|
| Code | Beeps | |
| 46h | 2-1-2-3 | Check ROM copyright notice |
| 47h | | Initialize I20 support |
| 48h | | Check video configuration against CMOS |
| 49h | | Initialize PCI bus and devices |
| 4Ah | | Initialize all video adapters in system |
| 4Bh | | QuietBoot start (optional) |
| 4Ch | | Shadow video BIOS ROM |
| 4Eh | | Display BIOS copyright notice |
| 4Fh | | Initialize MultiBoot |
| 50h | | Display CPU type and speed |
| 51h | | Initialize EISA board |
| 52h | | Test keyboard |
| 54h | | Set key click if enabled |
| 55h | | Enable USB devices |
| 58h | 2-2-3-1 | Test for unexpected interrupts |
| 59h | | Initialize POST display service |
| 5Ah | | Display prompt "Press F2 to enter SETUP" |
| 5Bh | | Disable CPU cache |
| 5Ch | | Test RAM between 512 and 640 kB |
| 60h | | Test extended memory |
| 62h | | Test extended memory address lines |
| 64h | | Jump to UserPatch1 |
| 66h | | Configure advanced cache registers |
| 67h | | Initialize Multi Processor APIC |
| 68h | | Enable external and CPU caches |
| 69h | | Setup System Management Mode (SMM) area |
| 6Ah | | Display external L2 cache size |
| 6Bh | | Load custom defaults (optional) |
| 6Ch | | Display shadow-area message |
| 6Eh | | Display possible high address for UMB recovery |
| 70h | | Display error messages |
| 72h | | Check for configuration errors |
| 76h | | Check for keyboard errors |
| 7Ch | | Set up hardware interrupt vectors |
| 7Dh | | Initialize Intelligent System Monitoring |
| 7Eh | | Initialize coprocessor if present |
| 80h | | Disable onboard Super I/O ports and IRQs |
| 81h | | Late POST device initialization |
| 81h | | Detect and install external RS232 ports |
| 83h | | Configure non-MCD IDE controllers |
| 84h | | Detect and install external parallel ports |
| 85h | | Initialize PC-compatible PnP ISA devices |
| 86h | | Re-initialize onboard I/O ports. |
| 87h | | Configure Motherboard Configurable Devices(optional) |
| 88h | | Initialize BIOS Data Area |
| 89h | | Enable Non-Maskable Interrupts (NMIs) |
| 8Ah | | Initialize Extended BIOS Data Area |

| POST (hex) | | Description |
|---|---|---|
| Code | Beeps | |
| 8Bh | | Test and initialize PS/2 mouse |
| 8Ch | | Initialize floppy controller |
| 8Fh | | Determine number of ATA drives (optional) |
| 90h | | Initialize hard-disk controllers |
| 91h | | Initialize local-bus hard-disk controllers |
| 92h | | Jump to UserPatch2 |
| 93h | | Build MPTABLE for multi-processor boards |
| 95h | | Install CD ROM for boot |
| 96h | | Clear huge ES segment register |
| 97h | | Fix up Multi Processor table |
| 98h | 1-2 | Search for option ROMs. One long, two short beeps on checksum failure |
| 99h | | Check for SMART Drive (optional) |
| 9Ah | | Shadow option ROMs |
| 9Ch | | Set up Power Management |
| 9Dh | | Initialize security engine (optional) |
| 9Eh | | Enable hardware interrupts |
| 9Fh | | Determine number of ATA and SCSI drives |
| A0h | | Set time of day |
| A2h | | Check key lock |
| A4h | | Initialize typematic rate |
| A8h | | Erase F2 prompt |
| AAh | | Scan for F2 key stroke |
| ACh | | Enter SETUP |
| AEh | | Clear Boot flag |
| B0h | | Check for errors |
| B1h | | Inform RomPilot about the end of POST. |
| B2h | | POST done - prepare to boot operating system |
| B4h | 1 | One short beep before boot |
| B5h | | Terminate QuietBoot (optional) |
| B6h | | Check password (optional) |
| B7h | | Initialize ACPI BIOS |
| B9h | | Prepare Boot |
| BAh | | Initialize SMBIOS |
| BBh | | Initialize PnP Option ROMs |
| BCh | | Clear parity checkers |
| BDh | | Display MultiBoot menu |
| BEh | | Clear screen (optional) |
| BFh | | Check virus and backup reminders |
| C0h | | Try to boot with INT 19 |
| C1h | | Initialize POST Error Manager (PEM) |
| C2h | | Initialize error logging |
| C3h | | Initialize error display function |
| C4h | | Initialize system error handler |
| C5h | | PnPnd dual CMOS (optional) |
| C6h | | Initialize note dock (optional) |
| C7h | | Initialize note dock late |

| POST (hex) | | Description |
|---|---|---|
| Code | Beeps | |
| C8h | | Force check (optional) |
| C9h | | Extended checksum (optional) |
| CAh | | Redirect Int 15h to enable remote keyboard |
| CBh | | Redirect Int 13h to Memory Technologies Devices such as ROM, RAM, PCMCIA, and serial disk |
| CCh | | Redirect Int 10h to enable remote serial video |
| CDh | | Re-map I/O and memory for PCMCIA |
| CEh | | Initialize digitizer and display message |
| D2h | | Unknown interrupt |
| **The following are for boot block in Flash ROM** | | |
| E0h | | Initialize the chipset |
| E1h | | Initialize the bridge |
| E2h | | Initialize the CPU |
| E3h | | Initialize system timer |
| E4h | | Initialize system I/O |
| E5h | | Check force recovery boot |
| E6h | | Checksum BIOS ROM |
| E7h | | Go to BIOS |
| E8h | | Set Huge Segment |
| E9h | | Initialize Multi Processor |
| EAh | | Initialize OEM special code |
| EBh | | Initialize PIC and DMA |
| ECh | | Initialize Memory type |
| EDh | | Initialize Memory size |
| EEh | | Shadow Boot Block |
| EFh | | System memory test |
| F0h | | Initialize interrupt vectors |
| F1h | | Initialize Run Time Clock |
| F2h | | Initialize video |
| F3h | | Initialize System Management Manager |
| F4h | | Output one beep |
| F5h | | Clear Huge Segment |
| F6h | | Boot to Mini DOS |
| F7h | | Boot to Full DOS |

★ If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays an additional word-bitmap (*xxxx*) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32-bit bus. The BIOS also sends the bitmap to the port-80 LED display. It first displays the checkpoint code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

# POST Error Code

## AMIBIOS 071596 VERSION 6.24 CHECK PONT LIST

Following is checkpoint list in AMIBIOS in order of execution

Check point Description

Uncompressed INIT code checkpoints

| POST (hex) | Description |
|---|---|
| D0 | NMI IS Disabled. CPU ID saved.<br>Init code Checksum verification starting. |
| D1 | To do DMA INIT, Keyboard controller BAT test, start memory refresh and going to 4GB flat mode. |
| D3 | To start Memory sizing. |
| D4 | To comeback to real mode. Execute OEM patch. Set stack. |
| D5 | E000 ROM enabled. Init code is copied to segment 0 and control to be transferred to segment 0. |
| D6 | Control is segment 0. To check <CTRL><HOME> key and verify main BIOS checksum.<br>If either <CTRL><HOME> is pressed or main BIOS checksum is bad, go to check point E0 else go to check point D7 |
| D7 | To pass control to Interface Module. |
| D8 | Main BIOS runtime code is to be decompressed. |
| D8 | Control to be passed to main BIOS in shadow RAM. |
| **Boot Block Recovery Code Check Points** | |
| E0 | On Board Floppy Controller ( if any ) is intialzed. |
| E1 | To star base 512K memory test. |
| E2 | To initialize interrupt vector table. |
| E6 | To enable floppy and timer IRQ, enable internal cache. |
| ED | Initialize floppy drive. |
| EE | Start looking for a diskette in drive A: and read 1st sector of the diskette. |
| EF | Floppy read error. |
| F0 | Start searching “ AMIBOOT.ROM ” file in root directory. |
| F1 | “ AMIBOOT.ROM “ file not present in root directory. |
| F2 | Start reading FAT table and analyze FAT to find the cluster occupied by “ AMIBOOT.ROM “ file. |
| F3 | Start reading “ AMIBOOT.ROOM” file cluster by cluster. |
| F4 | “ AMIBOOT.ROM “ file not of proper size. |
| F5 | Disable internal cache. |
| FB | Detect Flash type present. |
| FC | Erase Flash. |
| FD | Program Flash. |
| FF | Flash program successful. BIOS is restart. |
| **Runtime code is uncompressed in F000 shadow ram** | |
| 03 | MI is Disabled. To check soft reset / power – on |
| 05 | BIOS stack set. Going to disable Cache if any. |
| 06 | POST code to be uncompressed. |
| 07 | CPU init and CPU data area init to be done. |
| 08 | CMOS checksum calculation to be done next. |

| POST (hex) | Description |
|---|---|
| 0B | Any initialization before Keyboard BAT to be done next. |
| 0C | KB controller I / B free. To issue the BAT command to Keyboard controller. |
| 0E | Any initialization after KB controller BAT to be done next. |
| 0F | Keyboard command byte to be written. |
| 10 | Going to issue Pin – 23, 24 blocking / unblocking command. |
| 11 | Going to check pressing of < INS > < END > Key during power - on |
| 12 | To init CMOS if " Init CMOS is every boot " is set or < END > key is Pressed. Going to disable DMA and Interrupt controllers. |
| 13 | Video display is disable and port – B is initialized. Chipset init about to start. |
| 14 | 254 timer test about to start. |
| 19 | About to start memory refresh test. |
| 1A | Memory Refresh line is toggling. Going to check 15us ON / OFF time. |
| 23 | Read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable. |
| 24 | To do any setup before Int vector init. |
| 25 | Interrupt vector initialization about to being . To clear password if necessary. |
| 27 | Any initialization before setting video mode to be done. |
| 28 | Going for monochrome mode and color mode setting. |
| 2A | Different BUSes init ( system , static , output devices ) to start if present. |
| 2B | To give control for any setup required before optional video ROM check. |
| 2C | To look for optional video ROM and give control. |
| 2D | To give control to do any processing after video ROM returns control. |
| 2E | If EGA / VGA not found then do Display memory R/W test. |
| 2F | EGA / VGA not found. Display memory R/W test about to begin. |
| 30 | Display memory R/W test passed. About to look for the retrace checking. |
| 31 | Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test. |
| 32 | Alternate Display memory R/W test passed. To look for the alternate Display retrace checking. |
| 34 | Video display checking over. Display mode to be set next. |
| 37 | Display mode set. Going to display the power on message. |
| 38 | Different BUSes init ( input , IPL , general devices ) to start if present.( please see Appendix for details of different BUSes ) . |
| 39 | Display different BUSes initialization error messages. ( please see Appendix for details of different BUSes ) . |
| 3A | New cursor position read and saved. To display the Hit < DEL > message. |
| 40 | To prepare the descriptor tables. |
| 42 | To enter in virtual mode for memory test. |
| 43 | To enable interrupts for diagnostics mode. |

| POST (hex) | Description |
|---|---|
| 44 | To initialized data to check memory wrap around at 0:0 |
| 45 | Data initialized Going to check for memory wrap around at 0:0.<br>and finding the total system memory size. |
| 46 | Memory wrap around test done. Memory size calculation over.<br>About to go for writing patterns to test memory. |
| 47 | Patterns to be tested written in extended memory.<br>Going to write patterns in base 640K memory. |
| 48 | Patterns written in base memory.<br>Going to findout amount of memory below 1M memory. |
| 49 | Amount of memory below 1M found and verified.<br>Going to findout amount of memory above 1M memory. |
| 4B | Amount of memory above 1M found and verified.<br>Check for soft reset and going to clear memory below 1M for sort reset. ( If power on, go to check point # 4Eh ) |
| 4C | Memory below 1M cleared. ( SOFT RESET ) Going to clear memory above 1M. |
| 4D | Memory above 1M cleard. (SOFT RESET) Going to save the memory size. ( Go to check point #52h ). |
| 4E | Memory test started. ( NOT SOFT RESET ) about to display the first 64K memory size. |
| 4F | Memory size display started. This will be updated during memory test. Going for sequential and random memory test. |
| 50 | Memory testing / initialization below 1M complete.<br>Going to adjust displayed memory size for relocation / shadow. |
| 51 | Memory size display adjusted due to relocation / shadow.<br>Memory test above 1M to follow. |
| 52 | Memory testing / initialization above 1M complete.<br>Going to save memory size information. |
| 53 | Memory size information is saved. CPU registers are saved.<br>and disable parity / NMI |
| 54 | Shutdown successful, CPU in real mode. Going to disable gate A20 Line and disable parity/NMI. |
| 57 | A20 address line, parity / NMI disable successful.<br>Going to adjust memory size depending on relocation / shadow. |
| 58 | Memory size adjusted or relocation / shadow.<br>Going to clear Hit < DEL > message. |
| 59 | Hit < DEL > message cleared < WAIT > message displayed.<br>About to start DMA and interrupt controller test. |
| 60 | DMA page register test passed. To do DMA # 1 base register test. |
| 62 | DMA # 1 base register test passed. To do DMA # 2 base register test. |
| 65 | DMA # 2 base register test passed. To program DMA unit 1 and 2. |
| 66 | DMA unit 1 and 2 programming over.<br>To initialize 8259 interrupt controller. |
| 7F | Extended NMI sources enabling is Progress. |
| 80 | Keyboard test started. clearing output buffer, checking for stuck key , to issue keyboard reset command. |
| 81 | Keyboard reset error / stuck key found. To issue keyboard controller interface test command. |

| POST (hex) | Description |
|---|---|
| 82 | Keyboard controller interface test over. To write command byte and Init circular buffer. |
| 83 | Command byte written , Global data init done. To check for Lock - key |
| 84 | Lock – key checking over. To check for memory size mismatch with CMOS. |
| 85 | Memory size check done. To display soft error and Check for password or bypass setup. |
| 86 | Password checked. About to do programming before setup. |
| 87 | Programming before setup complete. To uncompress SETUP code and execute CMOS setup. |
| 88 | Returned form CMOS setup program and screen is cleared. About to do programming after setup. |
| 89 | Programming after setup complet. Going to display power on screen message. |
| 8B | First screen message displayed. < WAIT…> message displayed. |
| 8C | Setup options programming after CMOS setup about to start. |
| 8D | Going to hard disk controller reset. |
| 8F | Hard disk controller reset done. Floppy setup to be done next. |
| 91 | Floppy setup complet. Hard disk setup to be done next. |
| 95 | Init of different BUSes optional ROMs form C800 to start. |
| 96 | Going to do any init before C800 optional ROM control. |
| 97 | Any Init before C800 optional ROM control is over. Optional ROM check and control will be done next. |
| 98 | Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache. |
| 99 | Any initialization required after optional ROM test over. Going to setup timer data area and printer base address. |
| 9A | Return after setting timer data area and printer base address. Going to set the RS-232 base address. |
| 9B | Return after RS-232 base address. Going to do any initialization before Coprocessor is over. |
| 9C | Required initialize the Coprocessor next. |
| 9D | Coprocessor initialized. Going to do any initialization after Coprocessor test. |
| 9E | Initialization after Coprocessor test is complete. Going to check exit. Keyboard , keyboard ID and num – lock, Keyboard ID command to be. |
| A2 | Going to display complete. |
| A3 | Soft error display complete. Going to set keyboard typematic rate. |
| A4 | Keyboard typematic tate set. To program memory WAIT STATES. |
| A5 | Going to enable parity / NMI. |
| A7 | NMI and parity enable. Going to do any initalization Required before giving control to optional ROM at E000 |
| A8 | Initialization before E000 ROM control voer. |
| A9 | Returned form E000 ROM control . Going to do any initialization required after E000 optional ROM control is over. |

| POST (hex) | Description |
|---|---|
| AA | Initialization after E000 optional ROM control is over.<br>Going to display the system configuration. |
| AB | To build MP table if needed. |
| AC | To uncompress DMI data and execute DMI POST init. |
| B0 | System configuration is displayed. |
| B1 | Going to copy any code to specific area. |
| 00 | Copying of code to specific area done.<br>Going to give control to INT – 19 boot loader. |

# POST Error Code

## AMIBIOS 071596 VERSION 6.24 CHECK PONT LIST

**APPENDIX**

The system BIOS gives control to the different BUSes at checkpoints to do

Various tasks on the different BUSes

**CHECK – POINT DESCRIPTION OF CHECK – POINT**

| POST (hex) | Description |
|---|---|
| 2A | Different BUSes init ( system , start , output devices ) to<br>start if present. |
| 38 | Different BUSes init ( input , IPL , general devices ) to start if<br>present. |
| 39 | Display different BUSes initialization error messages. |
| 95 | Init of different BUSes optional ROMs from C800 to start. |

While control is inside the different BUS routines , checkpoints are output to post 80h as WORD to identify the routines under execution. These are WORD checkpoints , the LOW BYTE of checkpoint is the system BIOS checkpoint from where the control is passed to the different BUS routines and the HIGH BYTE of checkpoint is the indication of which routine is being executed in different BUSes. The details of HGH BYTE of these checkpoints are as follow :

**HIGH BYTE XY**

The upper nibble " x " indicates the function # is being executed. " x " can 0 to 7.

0 = fun # 0, disable all devices on the BUS concerned.
1 = fun # 1, static devices init on the BUS concerned.
2 = fun # 2, output device init on the BUS concerned.
3 = fun # 3, input device init on the BUS concerned.
4 = fun # 4, IPL device init on the BUS concerned.
5 = fun # 5, general device init on the BUS concerned.
6 = fun # 6, error reporting for the BUS concerned.
7 = fun # 7, add – on ROM init for all BUSes.

the lower nibble " Y " indicates the BUS on which the different routines are being executed. " Y " con be from 0 to 5.

0 = Generic DIM ( Device initialization Manager ).
1 = On – board system devices
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

## Notice:

Dear Customer,

Thank you for purchasing the *P801 PC Debug Card*. Please read user' s manual thoroughly before you install and use the debug card. The product that you have purchased comes with two-year warranty, but we will not be responsible for any misusing of the product. Therefore, we strongly urge you to read the manual first before using the product.

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