BCM Advanced Research

FM519

External Product Specification

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Revision History

Revision	Date	Description
X0.0	04/30/97	Preliminary release for internal review.
X0.1	05/12/97	Changes and additions
X0.2	05/19/97	Changes and additions

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Preface

This document specifies the architecture for a Cyrix™ Processor based MultiMedia motherboard; The “FM519” is a High-volume Integrated desktop motherboard incorporating advanced Graphics and a sound subsystem. The system incorporates the recommended functionality to support Windows ‘95.

Features

Processor/Cache	
Processor	Cyrix GX86 Single Chip Computer. 30/120, 33/133, 30/150 Operation
System Memory	
Memory Size	8 MB minimum to 128 MB maximum. With Single and Double sided SIMM’s. EDO DRAM
Memory Sites	4x72 pin SIMM Sockets
SIMM Type	4, 8, 16, 32, 64 with Parity and Non-parity (x32 or x36)
Access Time	60ns EDO or faster
Chipset	Cyrix 5510 PCI/ISA Chipset.
Integrated Graphics	
Graphics Controller	Integrated PCI Graphics & Video Accelerator.
Video Memory Organization	Shared Frame Buffer in Main Memory 1MB to 2MB
TV Output	TV Output using Chrontel CH7002
Integrated I/O	
I/O Controller	SMC FDC37C935 (Plug & Play Compliant)
Serial Ports	Two Asynch serial ports, two 9 Pin connectors using High Speed 16C550 compatible ports with 16-byte FIFOs
Infrared Interface	One 6 pin infrared port with IrDA and ASKIR
Parallel Port	One 25 pin supporting EPP, ECP and Centronics Interface
Hard Disk Controller	PCI Bus Mastering IDE. Native and Compatible Mode Support. IDE Transfer with Scatter Gather. Multiword DMA Transfers Mode 0,1,2. Enhanced IDE PIO Mode 3&4
Hard Disk Connector	2 PCI IDE Connectors for 4 Drives Support
Floppy Controller	1.2, 1.44 and 2.88 MB support
Keyboard Port	PS/2 (Integrated in the FDC37C935)
Mouse Port	PS/2 (Integrated in the FDC37C935)
Real Time Clock	Integrated in the FDC37C935 (DS1287 Compatible)
Integrated Sound	
Sound Chip	Sound Blaster compatible sound
CODEC	Analog Devices AD1874DAC, 16-bit Stereo

FM Synthesis	Built-in (OPL3 compatible)

System BIOS

BIOS Type	Phoenix Technologies (Phoenix BIOS ’95) 2MB Flash BIOS. Award BIOS also available
Hard Disk Driver	IDE, Auto-configuring
Plug&Play Support	Steerable DMA Channels and Interrupts. ISA Plug&Play
Special Features	**Windows 95 ready. Multi-Boot. PCI add-in card auto-configuration.**

Power Management

Green Features	APM1.2. Meets EPA Mod 2.0 (SMI, Stop Clock, HDD, and Monitor Shutdown)

Jumpers and Front Panel Connectors

Connectors	Reset Switch. Green (Suspend/Resume) Button, Green LED, PC Speaker. HD LED. IRDA. IR Remote.
Jumpers	Password/CMOS Clear. BIOS Recovery. NTSC/PAL TV Out selection

Headers and Rear Panel Connectors

Headers	Floppy. IDE 1&2. Serial 2 Port. Game Port. CD-IN. Modem In
Connectors	VGA Port. Serial 1. Keyboard & Mouse. Parallel Port. TV Out. Mic In. Line Out.

Mechanical

Board Style	LPX form factor
Board Size/Type	9.0” x 8.0”, four layer board

Expansion Slots

Description	One EISA riser slot for ISA and PCI buses

Document Structure and Outline

The information contained in this document is organized into 5 sections. Each section is of a modular format with non-numbered headings for each major topic and sub-topics. First level headings (16 point Times New Roman) always appear at the top of a new page and indicate the beginnings of a new major topic. Pages are numbered by chapter and page (e.g. 1-1). Figures and tables are numbered by chapter and sequence within the chapter.

The modular format allows for easy update of the documents as new information becomes available, or as specifications change. Some pages may contain more blank spaces than others; this is done to confine major topics to page boundaries.

References from one section to topics in another are by section title rather than number. This is done to maintain modularity. For example, a reference to a topic in Section 3 would be as follows: Refer to “Topic Heading” in the “Functional Architecture” section.

The content of each section is summarized below:

Section 1: Introduction
Provide an overview of the FM519 motherboard showing functional blocks.

Section 2: Functional Architecture
Describes the way each functional block of the FM519 motherboard works. Summarizes major bus interface signal pin names and their meaning. Their mnemonics appear throughout this document.

Section 3: Configuration
The FM519 configuration tables with considerations for all the different environments the hardware can be set to is given.

Section 4: Operating Environments
Describes the Software and Operating System environment. The current Performance benchmarks are listed.

Section 5: Electrical, Environmental and Mechanical Specifications
Specifies electrical and operational parameters, considerations and other hardware specifications.

References

The Following documents should be available for reference when using this document:

Order of Preference

In the event of conflict between the requirements set forth in this document and the documents herein, the requirements of this document shall prevail. The order of precedence shall be:

1) FM519 Specification (this document)
2) Referenced BCM internal documents
3) Referenced external documents

Referenced BCM Internal Documents

Several documents are required during the process of design, regulatory approvals, manufacturing and servicing the FM519 product family. The required documents are as follows:

- FM519 PWB Fabrication Drawing
- FM519 PWB Layout Artwork for each revision of PWB
- FM519 PWB Gerber Files
- FM519 Schematics for each revision of PWB & PWA
- FM519 Assembly Drawings and Process Instructions
- All production level ECOs
- Bill of Material (BOM) with Approved Vendor List (AVL)
- Configuration Jumper combinations

Referenced External Documents

- PCI System Design Guide. Revision 1.0
- IBM AT Technical Reference Manual
- Cyrix GX86 Processor User's Manual and Data Sheet
- Cyrix 5510 External Design Specification
- AD AD1874DAC Data Book
- SMC FDC37C935 Data Sheet

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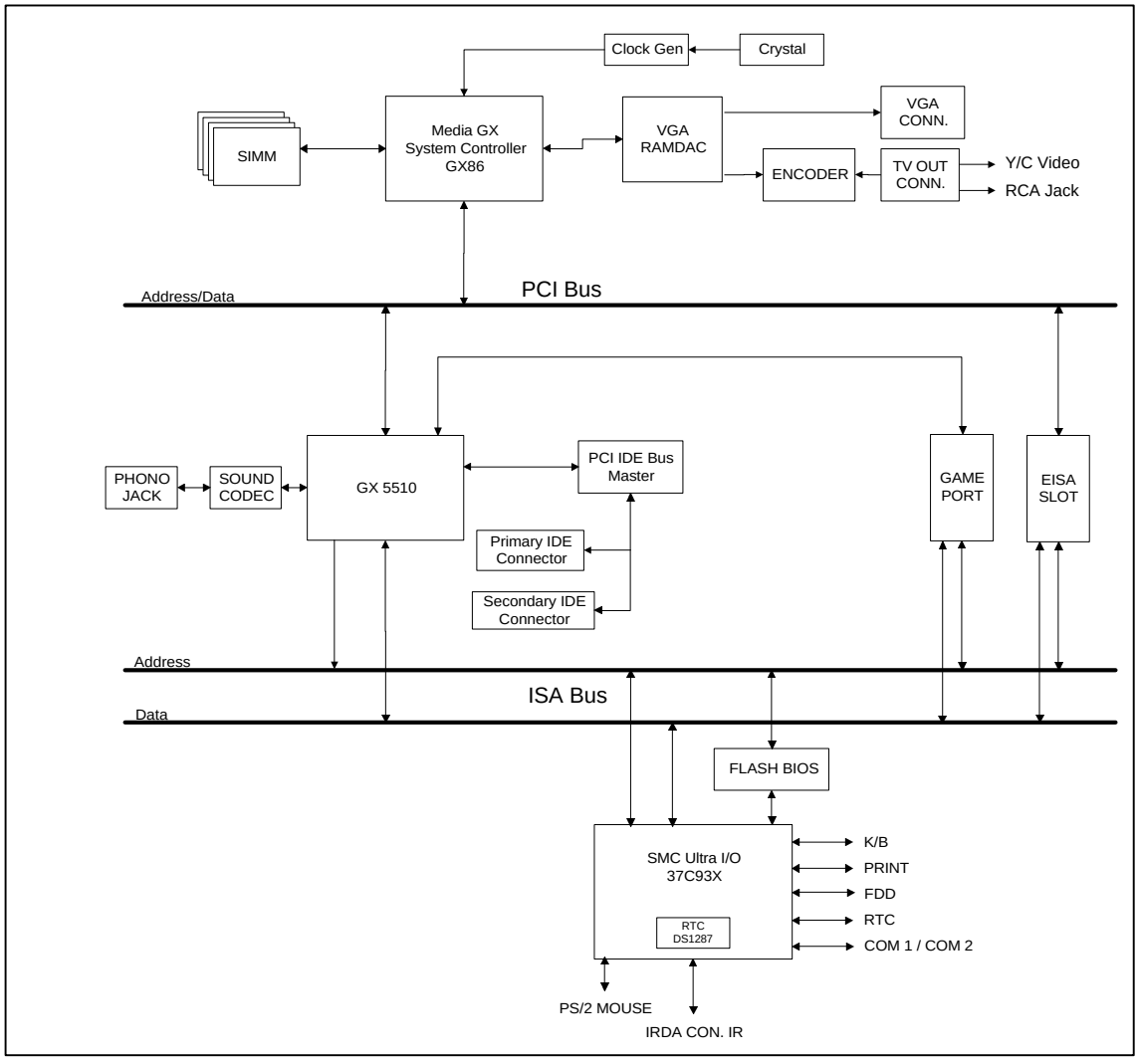
1

Introduction

This section provides an overview for a Cyrix 6x86 based PCI/ISA Printed Wiring Assembly (PWA), code named "FM519". It describes functional blocks and their relationship. The following diagram shows the functional blocks of the FM519.

Figure 1-1. FM519 Motherboard Block Diagram



Overview

The FM519 is an implementation of BCM Advanced Research for a High-Volume motherboard featuring these subsystems:

- Cyrix GX86 Single Chip Processor
- Cyrix 5510 Chipset
- One EISA Riser Card
- Sound Blaster Pro compatible sound
- Wavetable upgrade socket
- Integrated PCI Graphics/Video Accelerator
- PCI IDE Bus Master interface
- Embedded advanced I/O support
- LPX form-factor motherboard

The target Operating Systems for the FM519 are: DOS/Windows, Windows 95, Windows NT, OS/2 and UNIX.

Processor Subsystem

The FM519 has the Cyrix® Gx86 Processor soldered on the motherboard. The Cyrix® Gx86 Processor is an integrated 64-bit x86-compatible microprocessor. The integration includes a high-performance 2D graphics subsystem, an integrated PCI interface, and a unified memory subsystem. Enhancements to the SMM architecture enable Cyrix's Virtual System Architecture (VSA) for Virtual VGA and Virtual Audio. Cyrix's *Display Compression Technology* eliminates the performance degradation associated with traditional UMA system designs.

Cache and Memory Subsystem

The cache and main memory DRAM control functions are part of the Cyrix® Gx86 Processor. The 16-KByte internal write-back unified cache is a data/instruction cache and is configured as four-way set associative. The cache stores up to 16 KBytes of code and data in 1024 cache lines. The Gx86 provides the ability to allocate a portion of the L1 Cache as a scratchpad which is used to accelerate the Virtual Systems Architecture algorithms as well as for some graphics operations.

The FM519 provides no second level cache.

Main Memory is provided through four (4) 72-pin SIMM socket sites supporting either single or double-sided DRAM modules in a 64-bit wide two bank arrangement. The FM519 can support up to 128MB (2 Banks) of DRAM. Each bank can be single or double sided EDO (Extended Data Out) DRAM. The

installed DRAM type can be 4MB, 8MB, 16MB, 32MB or 64MB SIMMs, and both Symmetrical or Asymmetrical DRAM technology are supported. When only one bank of SIMMs is used it must be installed in Bank 0.

PCI I/O Bus

The primary I/O bus for the FM519 is PCI. It supports up to three masters on the PCI bus. The PCI bus operates at 33 MHz.

Embedded PCI Devices

The PCI bus contains 2 embedded PCI devices: PCI IDE interface and PCI Video/Graphics controller using the Gx86 processor's internal video interface. Arbitration for the PCI bus is performed by the Gx86 PCI GX Arbiter.

PCI Video/Graphics Controller

A high-performance graphics Accelerator is integrated into the Cyrix Gx86 Processor. Video memory is shared with system memory, however by using Cyrix's Display Compression Technology (DCT), the performance degradation inherent in traditional UMA systems is eliminated. An external video RAM-DAC provides the output for the monitor.

TV Output

A Chrontel CH7002 chip provides video output for a TV. Both RCA and a S-Video connectors are provided for this purpose.

PCI Bus Master IDE

The Cyrix Cx5510 chip provides two integrated IDE controllers with two high performance IDE interfaces for up to four devices, such as Hard Drives and CD-ROM.

PCI Add-in Cards

High Performance PCI I/O cards can be used in the FM519 through the expansion connectors in the riser card. The PCI bus is specified to support 10 loads. Each embedded controller or bridge (Video, PCI to ISA bridge) count as 1 load, each PCI expansion slot used in the riser card count as 1.5 loads (the connector to the riser card count as 1.5 loads).

Sound Subsystem

The Sound Section is intended to provide an integrated audio solution for business audio, education, entertainment sound, games and multimedia applications. Full compatibility with all of the De-facto standards is provided.

The FM519 incorporates all of the functions and interfaces for compatibility with the Sound Blaster card..

Embedded I/O Subsystem

The SMC (Standard Microsystems Corp.) Plug and Play Ultra I/O controller “FDC37C935” represents the newest technology in functionality and integration. While providing the standard PC I/O requirements the Ultra I/O complies with the ISA Plug-and-Play standard version 1.0a, and provides for the recommended functionality to support Windows ‘95. The Ultra I/O qualifies 16-bit address to allow relocation of 480 different addresses, with 13 IRQ options and 3 DMA channels available for each logical device.

Other features of the Ultra I/O are: 8042 keyboard controller. Real Time Clock. An Infrared interface for IrDA and ASKIR. Floppy interface. Two serial ports with 16-byte FIFOs. One EPP/ECP supported bi-directional parallel port.

2

Functional Architecture

Processor Subsystem

The Cyrix Gx86 processor that is used on the FM519 motherboard is soldered directly on the FM519 Motherboard and runs at either 30/120, 33/133 MHz or 30/150 MHz. A large heat sink is glued on the processor to eliminate the danger of over- heating.

Memory Subsystem

DRAM Subsystem

The FM519 supports four 36-bit (72-pin) SIMM sockets (SIMM1, SIMM2, SIMM3, SIMM4), allowing system memory from 8 MB to 128 MB of main DRAM. Population must be done in pairs of SIMMs of the same memory type. There are no jumpers settings required for the memory size or type, which is automatically detected by the system BIOS. The SIMM sockets have tin-lead contacts, rather than the more expensive gold contacts.

The SIMMs are rated at 60ns or better. Only EDO (Extended Data Out) SIMMs are supported. When only one bank is used the EDO SIMMs must be placed in bank 0 (SIMM1 and SIMM2). All the allowable memory size configurations are described on table 2.1 (Refer to Table 3.2 in the "Configuration" section for the different combinations and sizes of SIMMs).

Table 2.1. DRAM memory configurations in Megabytes.

8	**16**	**24**	**32**	**40**	**48**	**64**	**72**	**80**	**96**	**128**

DRAM (SIMM) Sockets

Connection to the main system DRAM is via four (4) connectors on the system PWA.

Reference:	SIMM1, SIMM2, SIMM3, SIMM4
Connector Type:	female, 72 pin SIMM, in-line connector
Connector Part Number:	AMP 822110-3 or equivalent

Table 2.2. DRAM SIMM Pinout Description

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SIGNAL-GROUND	37	PARITY DATA 1
2	DATA 0	38	PARITY DATA 3
3	DATA 16	39	SIGNAL-GROUND
4	DATA 1	40	CAS 0*
5	DATA 17	41	CAS 2*
6	DATA 2	42	CAS 3*
7	DATA 18	43	CAS 1*
8	DATA 3	44	RAS 0*
9	DATA 19	45	RAS 1*
10	VCC	46	N/C
11	N/C	47	WRITE-ENABLE*
12	ADDRESS 0	48	N/C
13	ADDRESS 1	49	DATA 8
14	ADDRESS 2	50	DATA 24
15	ADDRESS 3	51	DATA 9
16	ADDRESS 4	52	DATA 25
17	ADDRESS 5	53	DATA 10
18	ADDRESS 6	54	DATA 26
19	ADDRESS 10	55	DATA 11
20	DATA 4	56	DATA 27
21	DATA 20	57	DATA 12
22	DATA 5	58	DATA 28
23	DATA21	59	VCC
24	DATA 6	60	DATA 29
25	DATA 22	61	DATA 13
26	DATA 7	62	DATA 30
27	DATA 23	63	DATA 14
28	ADDRESS 7	64	DATA 31
29	N/C	65	DATA 15
30	VCC	66	N/C
31	ADDRESS 8	67	N/C
32	ADDRESS 9	68	N/C
33	RAS 3*	69	N/C
34	RAS 2*	70	N/C
35	PARITY DATA 2	71	N/C
36	PARITY DATA 0	72	LOGIC-GROUND

System BIOS

The system and video BIOS are stored in a 2MB (256KBx8) Flash Memory device (U4). The system BIOS is shadowed and cached.

Address Maps

Memory Map

The following table describes the breakdown of the FM519 memory areas and how they are assigned.

Table 2.3. Memory Map

LOCATION	SIZE	TO	DESCRIPTION
FFF80000-FFFFFFFF	128KB	4GB	BIOS ROM
00F00000-00FFFFFF	1MB	16MB	Optional memory space gap
000F0000-000FFFFF	64KB	1MB	System BIOS (Shadowed in DRAM)
000C8000-000EFFFF	160KB	960KB	Expansion region (Shadowed in DRAM)
000C0000-000C7FFF	32KB	800KB	Video BIOS (Shadowed in DRAM)
000A0000-000BFFFF	128KB	768KB	Video Buffer (SMM space Non-Cacheable)
00080000-0009FFFF	128KB	640KB	Optional memory space gap (DOS Apps)
00000000-0007FFFF	512KB	512KB	DOS applications (No read/write protect) (Always cacheable)

I/O Address Map

The following table represents the system I/O address map. I/O address range 000H to 0FFH are reserved for the system board I/O. Address range 100h to 3FFH are available to the I/O on-board resources.

Table 2.4. I/O Address Map

HEX-RANGE	SIZE	Plug&Play	USAGE
0060	1 byte	N/A	KEYBOARD CONTROLLER DATA BYTE
0064	1 byte	N/A	KEYBOARD CONT. CMD/STATUS BYTE
0070-007F	16 bytes	N/A	REAL-TIME CLOCK, NMI MASK
00E0-00EF	16 bytes	N/A	RESERVED
00F0	1 byte	N/A	CLEAR MATH COPROCESSOR ERROR
00F1	1 byte	N/A	RESET MATH COPROCESSOR
0F8-0FF	8 bytes	N/A	MATH COPROCESSOR

200,202,207	3 bytes	YES (Rev 1.1)	GAME I/O
220-22F	17 bytes	YES (Rev 1.1)	SOUND PORT
238-23F	8 bytes	YES	SERIAL PORT 4 (USED FOR REMAPPING)
278-27F	8 bytes	YES	PARALLEL PORT 2
2B0-2DF	48 bytes		ALTERNATE EGA ADAPTER
2F8-2FF	8 bytes	YES	SERIAL PORT 2
338-33F	8 bytes	YES	SERIAL PORT 3 (USED FOR REMAPPING)
370-375	6 bytes	YES	FLOPPY CONT. (SECONDARY ADDRESS)
376	1 byte	NO	SECONDARY IDE CHANNEL CMD PORT
377	1 byte	NO	SECONDARY IDE CHANNEL STAT PORT
378-37F	8 bytes	YES	PARALLEL PORT 1
3B0-3BF	16 bytes		MONO DISPLAY & PRINTER ADAPTER
3C0-3CF	16 bytes		EGA ADAPTER
3D0-3DF	16 bytes		CGA ADAPTER
3F0-3F5, 3F7	7 bytes	YES	FLOPPY CONTROLLER (PRIMARY)
3F8-3FF	8 bytes	YES	SERIAL PORT 1
CF8-CFF	8 bytes	N/A	PCI CONFIGURATION SPACE

Interrupt Allocation

Table 25. Interrupts Allocation

INTERRUPT	Plug&Play	DESCRIPTION
IRQ0	N/A	TIMER
IRQ1	YES	KEYBOARD CONTROLLER
IRQ2	N/A	IRQ FROM SECOND INTERRUPT CONTROLLER
IRQ3	YES	COM2 AND COM4
IRQ4	YES	COM1 AND COM3
IRQ5	YES	SOUND PORT
IRQ6	YES	FLOPPY DISK CONTROLLER
IRQ7	YES	PRIMARY LPT
IRQ8	N/A	REAL-TIME CLOCK
IRQ9	YES	AVAILABLE
IRQ10		AVAILABLE
IRQ11		AVAILABLE
IRQ12	YES	ON-BOARD PS/2 MOUSE
IRQ13	N/A	MATH COPROCESSOR
IRQ14	NO	PRIMARY IDE HARD DRIVE
IRQ15	NO	SECONDARY IDE HARD DRIVE IF PRESENT, ELSE USER AVAILABLE

DMA Channels

Table 2.6. DMA Channels Allocation

CHANNEL	Plug&Play	DESCRIPTION
DMA0	YES (Rev 1.1)	ON-BOARD AUDIO (default)
DMA1	YES (Rev 1.1)	ON-BOARD AUDIO (default)
DMA2	YES	FLOPPY DISK CONTROLLER
DMA3	YES	PARALLEL PORT IN ECP/EPP MODE
DMA4	N/A	16-BIT DRQ/DACK FROM SECOND DMA CONTROLLER
DMA5		AVAILABLE
DMA6		AVAILABLE
DMA7		AVAILABLE

Video Subsystem

Gx86 Integrated Functions

The Cyrix Gx86 Integrated Processor integrates the following functions typically implemented using external devices:

- High-performance graphics accelerator
- Display Controller for the CRT
- EDO memory controller
- PCI Bridge
- Power management

The processor has also been enhanced to support Cyrix's proprietary Virtual Systems Architecture implementation. The Gx86 Integrated Processor is the first processor to implement a Unified Memory Architecture. By using Cyrix's Display Compression Technology (DCT), the performance degradation inherent in traditional UMA systems is eliminated.

Graphics Accelerator

The graphics accelerator is a full-featured GUI accelerator. The graphics pipeline implements a bitBLT engine for frame buffer bitBLTs and rectangular fills. The bitBLT engine also assists the CPU in bitBLTs between system memory and the frame buffer by cooperating with new instructions in the integer core. This combination of hardware and software is used by the display driver to provide very fast transfers in both directions between system memory and the frame buffer. The bitBLT engine also draws randomly-oriented vectors, and scanlines for polygon fill. All of the pipeline operations described in the following list can be applied to any bitBLT operation.

• Pattern Memory. Render with 8x8 dither, 8x8 monochrome, or 8x1 color pattern.

• Color Expansion. Expand monochrome bitmaps to full-depth 8-bit or 16-bit colors.

• Transparency. Suppresses drawing of background pixels for transparent text.

• Raster Operations. Boolean operation combines source, destination, and pattern bitmaps.

Display Controller

The display port interfaces directly to a RAMDAC to drive a CRT display. The display controller retrieves image data from the frame buffer region of memory, performs a color-look-up if required, inserts the cursor overlay into the pixel stream, generates display timing, and formats the pixel data for output to a variety of display devices. The display controller contains Display Compression Technology that allows the Gx86 processor to refresh the display from a compressed copy of

the frame buffer. DCT typically decreases the screen-refresh bandwidth requirement by a factor of 15 to 20, further minimizing bandwidth contention.

Video DAC

The ICS5342 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit, and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contain 8 frequencies, all of which are programmable by the user. The memory clock has two programmable frequency locations.

The three 8-bit DACs on the ICSS342 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and VDD ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

Features

- Triple video DAC, dual clock generator, and 16 bit pixel port
- Dynamic mode switch allows switching color depth on a pixel by pixel basis
- 24 (packed and sparse), 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGAmodes
- High speed 256x6x3 color palette (135MHz) with bypass mode & 8-bit DACs
- Eight programmable video (pixel) clock frequencies (CLK0)
- DAC power down in blanking mode
- Anti-sparkle circuitry
- On-chip loop filters reduce external components
- Standard CPU interface
- Single external crystal (typically 14.318 MHz)
- Monitor sense
- Internal voltage reference
- Very low clock jitter

Video (Monitor) Connector

Connection to VGA monitor is via a connector on the rear panel on the system PWA.

Reference: P1 (VGA)
Connector Type: female, high density DB15S, 15-pin AT-compatible
Connector Part Number: 3M 927F55-01-15-10 or equivalent

Table 2.7. Video Monitor Connector Pinout

PIN	Description
1	RED
2	GREEN
3	BLUE
4	N/C
5	LOGIC-GROUND
6	RED GROUND RETURN
7	GREEN GROUND RETURN
8	BLUE GROUND RETURN
9	+5V PULL-UP
10	LOGIC GROUND
11	N/C
12	DDC DAT
13	HORIZONTAL-SYNC
14	VERTICAL-SYNC
15	DDC CLK
16	LOGIC-GROUND[1]
17	LOGIC-GROUND[1]

1: Pins 16 and 17 are connector mounting holes connected to logic ground.

TV Output

The TV output is generated by the CH7002 which is a fully integrated system solution for converting analog RGB and synchronization signals from a standard VGA source into high-quality NTSC or PAL video signals. This solution involves both hardware and software elements which work together to produce an optimum TV screen image based oh the original computer generated pixel data. All essential circuitry for this conversion are integrated on chip. On chip circuitry includes memory, memory control, scaling, PLL,ADC, DAC, filters, and NTSC/PAL encoder. All internal signal processing, including NTSC/PAL encoding, is performed using digital techniques to ensure that the high-quality video signals are not affected by drift issues associated with analog components.

The CH7002 is a complete TV output subsystem which uses both hardware and software element to produce an image on TV which is virtually identical to the image that would be displayed on a monitor. Simply creating a compatible TV output from a VGA input is a relatively straightforward process. This process includes a standard conversion from RGB to YUV color space, converting from a non-interlaced to an interlaced frame sequence, and encoding the pixel stream into NTSC or PAL compliant format. However, creating an optimum computer generated image on a TV screen involves a highly sophisticated process of scaling, deflickering, and filtering. This results in a compatible TV output that displays a sharp and stable image, of the right size with minimal artifacts from the conversion process.

As a key part of the overall system solution, the CH7002 software establishes the correct framework for the VGA input signal to enable this process. Once-the display is set to a supported resolution (either 640x480 or 800x600), the CH7002 software may be invoked to establish the appropriate TV output display. The software then programs the various timing parameters of the VGA controller to create an output signal that will be compatible with the chosen resolution, operating mode, and TV format. Adjustments performed in software include pixel clock rates, total pixels per line, and total lines per frame. By performing these adjustments in software, the CH7002 can render a superior TV image without the added cost of a full frame buffer memory normally used to implement features such as scaling and full synchronization. Without this added system software, TV output solutions can only guarantee compatible operation in VGA standard mode 12 (640x480x16 color, 60 Hz).

The CH7002 hardware accepts direct VGA output (analog RGB inputs), which is digitized on a pixel-by-pixel basis by three 8-bit video A/D converters. The digitized RGB inputs are then color space converted into YUV in 4-2-2 format (encoded into luminance (Y) and color-difference (U,V) signals and stored in a line buffer memory. The stored pixels are fed into a block where scan-rate conversion, underscan scaling and 3-line vertical flicker filtering are performed. The scan-rate converter transforms the VGA horizontal scan-rate to either NTSC or PAL scan-rates, the vertical flicker filter eliminates flicker at the output while the underscan scaling reduces the size of the displayed image to fit onto a TV screen. The resulting YW signals are filtered through digital filters to minimize aliasing problems. The digital encoder receives the filtered signals and transforms them to composite and S-video outputs, which are converted by the three 8-bit DACs into analog outputs.

TV Output Connectors

Two connectors are provided to connect a TV to the board.

Reference: (RCA JACK)
Connector Type: TBD
Connector Part Number: TBD

Table 2.8. RCA Jack Connector Pinout

PIN	SIGNAL
1	Composite Video
2	GROUND
3	GROUND
4	GROUND

Reference: J2 (Y/C Video)
Connector Type: TBD
Connector Part Number: TBD

Table 2.9. Y/C Video Connector Pinout

PIN	SIGNAL
1	GROUND
2	GROUND
3	LUMA
4	CHROMA
5	GROUND
6	GROUND
7	GROUND

Sound Subsystem

The Cx5510 System controller incorporates features of the Virtual System Architecture (VSA) for the generation and capture of audio using an external DAC or Codec. Virtual Audio is compatible with software written for the Sound Blaster II, Pro, and 16, and the Adlib audio cards. Virtual Audio also emulates an MPU-401 UART using a COM port for MIDI serial transmit and receive. The Cx5510 Virtual Audio hardware includes two 128-byte audio FIFOs to hold 32 audio samples (two channels at 16 bits per channel) for buffering digitized audio input and output from/to the external DAC or Codec. The audio FIFOs provide communication between the internal parallel bus and an external serial DAC or Codec. The Cx5510 also contains a full set of configuration audio registers and hardware comparators for trapping and signalling I/O accesses to the audio address range. Cyrix Virtual Audio software emulates audio functions that are trapped by the Cx5510. This software is available to OEMs for incorporation into the system BIOS ROM. The Cx5510 interfaces to the Analog Devices AD1847 Codec for audio playback and record.

The VSA Virtual Audio hardware resources in the Cx5510 perform the following functions:

- Buffers the input and output with two 128-byte FIFOs, each holding 32 32-bit samples (the 32-bit sample is 16 bits per stereo channel). One FIFO is for audio input and one FIFO is for audio output.
- For audio input/output, it interfaces with AD1847 Serial Port Codec.
- Generates an SMI to alert software of required data update. SMI is generated when either FIFO drops below separately programmable thresholds, or when output FIFO is empty or input FIFO is full. Also generates an SMI on I/O traps.
- Traps I/O accesses for Sound Blaster compatibility at either 220h-22Fh, 240h-24Fh, 260h-26Fh, or 280h-28Fh.
- Traps I/O accesses for ADLIB compatibility at 388h-38Bh.
- Traps I/O accesses for Roland MPU 401UART interface at 300h-301h or 330h-331h.
- Traps I/O accesses for MIDI serial input and output at COM2 (2F8h-2FFh) or COM4 (2E8h-2EFh).
- Supports I/O trapping for low (00h-0Fh) and/or high (C0h-DFh) DMA accesses.
- Supports hardware status register reads in Cx5510, minimizing SMI overhead.
- Generates IRQs for SB DSP chip compatibility: support for software-generated IRQs on IRQ 2, 3, 5, 7, 10, 11, 12, 13,14, and 15.

GAME Port Header

The FM519 provides access to the Joystick game compatible interface through a header in the system PWA.

Reference:	HDR1 (GAME)
Connector Type:	male, 2 x 8, 0.100" centerline, straight

Connector Part Number: AMP 103322-8 or equivalent

Table 2.10. MIDI/Game port Connector Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION
1		9	
2		10	
3		11	
4		12	
5		13	
6		14	
7		15	
8		16	

Line Out Connector

The audio subsystem provides external sound through a user accessible stereo jack connector (J16) soldered to the PWA. This jack will allow the connection of self-amplified speakers.

Reference: J14 (LINE OUT)
Connector Type: 1/8 in. Banana Jack Connector
Connector Part Number: Vendor 10XXXX-2

Line Out Header

The audio subsystem also provides external sound through a header (J15) soldered to the PWA. This header will allow a jack on the front panel of the enclosure to be connected via a cable.

Reference: J15
Connector Type: 1X3 male straight, .100 centers
Connector Part Number: AMP 103321-3 or equivalent

Microphone In Connector

An external accessible jack connector (J14) is soldered to the PWA to allow the connection of a microphone for voice input.

Reference: J12 (MIC IN)
Connector Type: 1/8 in. Banana Jack Connector
Connector Part Number: Vendor 10XXXX-2

Microphone In Header

The audio subsystem also provides a microphone input through a header (J13) soldered to the PWA. This header will allow a jack on the front panel of the enclosure to be connected via a cable.

Reference:	J13
Connector Type:	1X3 male straight, .100 centers
Connector Part Number:	AMP 103321-3 or equivalent

ISA/PCI I/O Riser Card

The FM519 system will support an ISA only, PCI only or shared ISA-PCI slots riser card. The ISA/PCI I/O riser card contains decoupling capacitors between the voltage planes and ground to assist in both EMI and general voltage plane noise reduction. The ISA/PCI I/O riser will be inserted into the system PWA during the system assembly process. The riser connects to the system PWA through the J10 connector.

ISA Interface

The FM519 incorporates a fully ISA bus compatible master and slave interface. It is capable of driving five (5) ISA Slots without external data buffers. This drive capability is required to ensure signal integrity for the ISA bus under loading conditions with the ISA/PCI I/O riser and expansion cards installed. The ISA interface also provides byte swap logic and I/O recovery support.

AT Bus Refresh

The Cx5510 supports the standard ISA refresh function. ISA refreshes are enabled by setting bit 6 in the ISA Configuration Register. When enabled, *Timer 1* in the programmable interval timer is used to generate an internal refresh request signal. When the ISA bus is not in use by the ISA bus controller, the DMA controller, or an ISA bus master, the refresh control logic generates the ISA refresh cycle. No DMA or PCI-to-ISA cycles occur until after the completion of this refresh cycle. If the ISA bus is in use when the refresh request occurs, the refresh controller waits until the bus is free and then generate a refresh cycle.

The Cx5510 also supports refresh requests initiated by ISA masters.

PCI Interface

The Gx86 CPU includes an integrated PCI controller with the following features.

X-bus PCI Slave
- 16-byte PCI write buffer
- 16-byte PCI read buffer from X-bus
- Synchronization of 1x, 2x, 3x, 4x, 5x PCI to X-bus
- Supports cache line bursting
- Write/Inv line support
- Pacing of data for read or write operations with X-bus
- No active byte enable transfers supported

X-bus PCI Master
- 16 byte X-bus to PCI write buffer
- Synchronization of 1x, 2x, 3x, 4x, 5x X-bus to PCI
- Configuration read/write Support
- Int Acknowledge support
- Lock conversion
- Support fast back-to-back cycles as slave

PCI Arbiter
- Fixed, rotating, hybrid, or ping-pong arbitration (programmable)
- Support four masters, three on PCI
- Internal REQ for CPU
- Master retry mask counter
- Master dead timer.
- Resource or total system lock support

ISA/PCI I/O Riser Connector

Connection to the PCI/ISA riser is via a connector on the system PWA.

Reference:	J10
Connector Type:	female, 198 pin edge connector
Connector Part Number:	AMP 646039-1 or equivalent

Table 2.11. PCI/ISA Riser Connector

PIN	SIGNAL NAME	PIN	SIGNAL NAME
B1	GND	A1	IOCHK*
B2	RSTDRV	A2	SD7
B3	VCC	A3	SD6
B4	IRQ9	A4	SD5
B5	-5VDC	A5	SD4
B6	DRQ2	A6	SD3
B7	-12VDC	A7	SD2
B8	OWS*	A8	SD1
B9	+12VDC	A9	SD0

B10	GND	A10	CHRDY
B11	SMEMW -	A11	AENn
B12	SMEMR -	A12	SA19
B13	IOW -	A13	SA18
B14	IOR -	A14	SA17
B15	DACK3 -	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1 -	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH -	A19	SA12
B20	SYSCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2 -	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	VCC	A29	SA2
B30	OSC	A30	SA1
B31	GND	A31	SA0
D1	MEMCS16 -	C1	SBHE
D2	IQCS16 -	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ13	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0-	C8	LA17
D9	DRQ0	C9	MRDC*
D10	DACK5 -	C10	MWTC*
D11	DRQ5	C11	SD8
D12	DACK6 -	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7 -	C14	SD11
D15	DRQ7	C15	SD12
D16	+VCC	C16	SD13
D17	MASTER -	C17	SD14
D18	GND	C18	SD15
F1	GND	E1	GND
F2	GND	E2	GND
F3	PCI INT3 -	E3	PCI INT1-
F4	PCI INT4 -	E4	PCI INT2-

F5	VCC	E5	VCC
F6	KEY	E6	KEY
F7	VCC	E7	VCC
F8	PCLKF	E8	PCIRST-
F9	GND	E9	GNTO -
F10	GNT1 -	E10	REQ0 -
F11	GND	E11	GND
F12	REQ1 -	E12	PCIKE
F13	AD31	E13	GND
F14	AD30	E14	AD30
F15	N/C	E15	N/C
F16	KEY	E16	KEY
F17	N/C	E17	N/C
F18	AD27	E18	AD28
F19	AD26	E19	AD28
F20	CBE3 -	E20	AD24
F21	AD23	E21	AD22
F22	AD21	E22	AD20
F23	AD10	E23	AD18
F24	N/C	E24	N/C
F25	KEY	E25	KEY
F26	N/C	E26	N/C
F27	AD17	E27	AD16
F28	IRDY -	E28	FRAME -
F29	DEVSEL -	E29	CBE2 -
F30	PLOCK -	E30	TRDY -
F31	PERR -	E31	STOP -
H1	SERR -	G1	SDONE
H2	AD15	G2	SBO -
H3	AD14	G3	CBE1 -
H4	AD12	G4	PAR
H5	GND	G5	GND
H6	KEY	G6	KEY
H7	GND	G7	GND
H8	AD10	G8	AD13
H9	AD8	G9	AD11
H10	AD7	G10	AD9
H11	AD5	G11	CBE0 -
H12	AD3	G12	AD6
H13	AD1	G13	AD4
H14	AD0	G14	AD2
H15	KEY	G15	KEY
H16	VCC	G16	VCC
H17	VCC	G17	VCC

H18	GND	G18	GND
H19	GND	G19	GND

Storage Subsystem

IDE Hard Disk Drive Interface

The FM519 provides two (2) independent high performance PCI IDE interfaces capable of supporting PIO Mode 3 and Mode 4 devices. The integrated IDE interface can control up to four IDE devices allowing for both CD-ROM and Hard Disk drives. IDE PRI & IDE SEC are the primary and secondary IDE connectors. Both IDE controllers can be disabled through BIOS to allow for external disk drive controllers. Connection to the IDE hard disks is via headers on the system PWA.

Reference: J6, J4 (PRIMARY, SECONDARY)
Connector Type: male, 2 x 20, 0.100" centerline, straight
Connector Part Number: AMP 2-103322-0

Table 2.12. IDE Connector Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RESET*	2	LOGIC-GROUND
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	LOGIC-GROUND	20	N/C[1]
21	N/C	22	LOGIC-GROUND
23	I/O-WRITE	24	LOGIC-GROUND
25	I/O-READ	26	LOGIC-GROUND
27	HDCHRDY	28	LOGIC-GROUND
29	N/C	30	LOGIC-GROUND
31	IRQ	32	N/C
33	ADDRESS1	34	N/C
35	ADDRESS0	36	ADDRESS2
37	CHIP-SELECT0*	38	CHIP-SELECT1*
39	DISK-ACTIVE	40	LOGIC-GROUND

[1]: Pin 20 is *removed* as a key pin.

Floppy Disk Drive Interface

The FM519 has an integrated 765B compatible floppy disk controller using the SMC "FDC37C935" component. The FDC sub-section can control two (1.2, 1.44 and 2.88MB) floppy disks or compatible tape drives. The floppy I/O address can be relocated to 480 different locations. 13 IRQ and 3 DMA channel options are available as well. Includes multiple power-down modes for reduced power use.

Connection to the floppy drives is via a header on the PWA. The floppy disk interface contains 48mA drivers and Schmitt trigger inputs on the drive interface.

Reference:	J6 (FLOPPY)
Connector Type:	male, 2 x 17, 0.100" centerline, straight
Connector Part Number:	AMP 1-103322-7 or equivalent

Table 2.13. Floppy Connector Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION
1	LOGIC-GROUND	2	DENSITY-SELECT*
3	N/C	4	N/C
5	LOGIC-GROUND[1]	6	N/C
7	LOGIC-GROUND	8	INDEX*
9	LOGIC-GROUND	10	MOTOR0*
11	LOGIC-GROUND	12	DISK-SELECT1*
13	LOGIC-GROUND	14	DISK-SELECT0*
15	LOGIC-GROUND	16	MOTOR1*
17	MEDIA-ID1*	18	DIRECTION
19	LOGIC-GROUND	20	STEP*
21	LOGIC-GROUND	22	WRITE-DATA*
23	LOGIC-GROUND	24	WRITE-ENABLE*
25	LOGIC-GROUND	26	TRACK00*
27	MEDIA-ID0*	28	WRITE-PROTECT*
29	LOGIC-GROUND	30	READ-DATA*
31	LOGIC-GROUND	32	HEAD-SELECT
33	N/C	34	DISK-CHANGE*

[1]: Pin 5 is *removed* as a key pin

I/O SUBSYSTEM

The I/O Subsystem is consists of a single component from SMC (Standard Microsystems Corp.). The FM519 uses the Plug and Play Compatible Ultra I/O Controller "FDC37C935", this device provides support for the ISA Plug-and-Play version 1.0a and includes the recommended functionality to support Windows '95. Through internal configuration registers, each of the FDC37C935's logical device's I/O address, DMA channel and IRQ channel may be programmed. There

are 480 I/O address location options, 13 IRQ options and 3 DMA channel options for each logical device.

The Ultra I/O device provides two (2) high speed NS16C550 compatible serial ports with send/receive 16 Byte FIFOs . One IR two pin port. One Multi-Mode Parallel Port with ChiProtect™ and ECP/EPP modes. And a Floppy/Tape Controller supporting up to 2.88MB transfer rates.

Serial Ports

The FM519 has two (2) NS16C550 AT-compatible serial ports configured as Data Terminal Equipment (DTE). The electrical characteristics are compliant with the *EIA-232-D Serial Communications Specifications*. The serial ports may be remapped above other installable serial ports or disabled through BIOS. As a minimum the first serial port (COM1) at J7 must be capable of remapping to COM3. The second serial port (COM2) at J8 must be able to be remapped to COM4. The serial ports I/O address can be relocated within 480 different locations. The default address for COM1, COM2, COM3 and COM4 are 3F8H, 338H, 2F8H and 238H respectively. 13 different IRQ options are available to the serial ports.

Connectors located on the rear panel of the system PWA are provided for external connection to the serial ports

Reference:	J7 (COM1)
Connector Type:	male, 9 pin metal shell D-SUB
Connector Part Number:	Amp 750529-3 or equivalent

Reference:	J8 (COM2)
Connector Type:	male, 2x5, 0.100” centerline, straight
Connector Part Number:	Amp 1-103322-5 or equivalent

Table 2.14. Serial Port Connector Pinout.

PIN	DESCRIPTION
1	DATA-CARRIER-DETECT (DCD)
2	RECEIVE-DATA (RXD)
3	TRANSMIT-DATA (TXD)
4	DATA-TERMINAL-READY (DTR)
5	LOGIC-GROUND
6	DATA-SET-READY (DSR)
7	REQUEST-TO-SEND (RTS)
8	CLEAR-TO-SEND (CTS)
9	RING-INDICATOR (RI)
10	SHELL-GROUND[1]
11	SHELL-GROUND[1]

1: Pins 10 and 11 (Shell Ground) are mounting holes connected to the metal connector housing on serial port 2. Not used on serial port 1.

Parallel port

The system PWA has a single bi-directional parallel port (EPP/ECP compatible). The parallel port is capable of being disabled or remapped to either the secondary LPT address or the tertiary LPT address through BIOS if other parallel ports are installed in the system. The parallel port I/O address can be relocated within 480 different locations. 3 DMA channels options and 13 different IRQ options are available to the parallel port.

A connector is located on the rear panel of the system PWA for the external connection to the port. The parallel port interface contains 12mA source output drivers on the drive interface, and incorporates ChipProtect circuitry for protection against damage due to printer Power-On.

Reference: J11 (PRINTER)
Connector Type: female, 25 pin metal shell D-SUB
Connector Part Number: AMP 750096-3 or equivalent

Table 2.15. Printer Port Connector Pinout

PIN	DESCRIPTION
1	STROBE*
2	PD0
3	PD1
4	PD2
5	PD3
6	PD4
7	PD5

8	PD6
9	PD7
10	ACKNOWLEDGE*
11	BUSY
12	PAPER-END (PE)
13	SELECT
14	AUTO-FEED*
15	ERROR*
16	INIT*
17	SELECT -IN*
18	LOGIC-GROUND
19	LOGIC-GROUND
20	LOGIC-GROUND
21	LOGIC-GROUND
22	LOGIC-GROUND
23	LOGIC-GROUND
24	LOGIC-GROUND
25	LOGIC-GROUND
26	SHELL-GROUND[1]
27	SHELL-GROUND[1]

1: Pins 26 and 27 are connector mounting holes connected to the metal connector housing.

Keyboard Interface

The system PWA has a PS/2-compatible keyboard interface. The shielded keyboard interface connector has a PS/2-compatible pinout and is located on the rear panel on the system PWA. To meet the requirements for UL compliance the Vcc pin (pin 4) is connected through a fuse prior to connection to the external connector.

Reference: J2 (KEYBOARD)
Connector Type: female, 6 pin metal shield mini-DIN
Connector Part Number: AMP 749231-1 or equivalent

Table 2.16. Keyboard Connector Pinout

PIN	DESCRIPTION
1	KEYBOARD-DATA
2	N/C
3	LOGIC-GROUND
4	KEYBOARD-Vcc
5	KEYBOARD-CLOCK
6	N/C
7	SHELL-GROUND[1]

8	SHELL-GROUND[1]
9	SHELL-GROUND[1]

1: Pins 7-9 are connector mounting hole pins connected to the metal connector housing

Mouse Interface

The system PWA has a PS/2-compatible mouse interface. The shielded mouse port can be disabled through SETUP. A connector, utilizing PS/2 pinouts, is located on the rear panel on the system PWA. To meet the requirements for UL compliance the Vcc pin (pin 4) was connected through a fuse prior to connection to the external connector.

Reference: J5 (MOUSE)
Connector Type: female, 6 pin metal shield mini-DN
Connector Part Number: AMP 749231-1 or equivalent

Table 2.17. Mouse Connector Pinout

PIN	DESCRIPTION
1	MOUSE-DATA
2	N/C
3	LOGIC-GROUND
4	MOUSE-Vcc
5	MOUSE-CLOCK
6	N/C
7	SHELL-GROUND[1]
8	SHELL-GROUND[1]
9	SHELL-GROUND[1]

1: Pins 7-9 are connector mounting hole pins connected to the metal connector housing.

Real-Time Clock

The integrated Real Time Clock (RTC) is DS12887/MC146818 compatible and provides the time of day clock, 100-year calendar with alarm features and is accurate to within 1 minute per month, it consumes less than 1 μA of standby current (Typ.). The (RTC) supports 256 bytes of battery backed Non-volatile CMOS memory in two banks of 128 bytes each, both banks being reserved for BIOS use. One bank of CMOS memory is used to maintain the clock and user-system-setting configuration parameters when the main system power is removed. The other bank (128 bytes) is lockable in 4x32 byte blocks and can be used to store and lock miscellaneous information.

The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also to prevent a lock-up situation the CMOS RAM values can be cleared to the system defaults by using the CLR CMOS jumper on the PWA.

Nonvolatile CMOS Memory Battery

An external coin-cell style battery provides power to the RTC and CMOS memory when system power is removed. The battery has an estimated lifetime of seven years and is socketed for easy replacement.

Reference:	BT1
Socket Type:	COIN TYPE

IR (Infra-Red) Support

The FM519 I/O subsystem incorporates an IR interface connector supporting the following industry standards; IrDA (HP-SIR), and ASK-IR. One header J24 (labeled IRDA) provides the interface allowing a two-way wireless communication port using infrared as the transmission medium. The user can transfer files to/from portable devices such as laptops, PDA's and printers using application software such as LapLink. The IrDA port shares the registers and logic block with COM2 port, once configured in the BIOS for IR a serial device in COM2 will stop transmitting.

IRDA Connector

A 1 x 6 straight header is available for a cable connection to the IR module.

Reference:	J24 (IRDA)
Connector Type:	1 x 6 male straight 0.100 centers
Connector Part Number:	AMP 103321-6

Table 2.18. Infrared “IrDA” Conn. Pinout

PIN	SIGNAL
1	+ 5 VOLTS
2	KEY
3	IR-RX
4	LOGIC-GROUND
5	IR-TX
6	CIR_RX

MISCELLANEOUS CONNECTORS

PC Speaker Connector

A 1 x 4 straight header (J18) is available to drive a chassis-mounted speaker if desired.

Reference: J18 (SPEAKER)
Connector Type: 1 x 4 male straight 0.100 centers
Connector Part Number: AMP 103321-4

Table 2.19. PC Speaker Conn. Pinout

PIN	SIGNAL
1	SPKRDAT
2	ON BOARD BUZZER
3	N/C
4	VCC

MODEM IN Connector

A 1 x 4 straight header (J12) is available to allow a speakerphone configuration when a Modem card is used in the system. The circuitry will allow the voice from a phone line coming through a Modem card to be sent to the external speakers. It will also send voice input from an external microphone through the Modem card and into the phone line.

Reference: J12 (MODEM IN)
Connector Type: 1 x 4 male straight 0.100 centers
Connector Part Number: AMP 103321-4

Table 2.20. MODEM IN Conn. Pinout

PIN	SIGNAL
1	LOGIC-GROUND
2	MODEM-MIC-OUT
3	LOGIC-GROUND
4	MODEM-SPKR-IN

Hard Drive LED Connector

A 1 x 2 straight header is available to the Hard Disk Drive LED on the front panel to indicate hard drive activity.

Reference: J27 (HD LED)
Connector Type: 1X2 male straight, .100 centers
Connector Part Number: AMP 103321-2 or equivalent

Table 2.21. HD Activity Indicator Pinout

PIN	SIGNAL
1	+ 5 V Pull-Up
2	HDACTIVE-

GREEN (Suspend/Resume) Connector

A 1 x 2 straight header is available for the suspend/resume function of the power management logic, it provides the system access to power management functions.

Reference: J19 (SUSPEND)
Connector Type: 1X2 male straight, .100 centers
Connector Part Number: AMP 103322-2 or equivalent

Table 2.22. Suspend/Resume Conn. Pinout

PIN	SIGNAL
1	LOGIC-GROUND
2	EXTERNAL SMI

RESET Connector

A 1 x 2 straight header is available for the suspend/resume function of the power management logic, it provides the system access to power management functions.

Reference: J25 (RESET)
Connector Type: 1X2 male straight, .100 centers
Connector Part Number: AMP 103322-2 or equivalent

Table 2.23. Reset Conn. Pinout

PIN	SIGNAL
1	RESET
2	LOGIC-GROUND

FAN Connector

A 1 x 3straight header is available for connecting a CPU Fan.

Reference: J21 (FAN)
Connector Type: 1X3 male straight, .100 centers
Connector Part Number: AMP 103322-3 or equivalent

Table 2.24. Fan Conn. Pinout

PIN	SIGNAL
1	GROUND
2	+5V
3	GROUND

POWER ON LED Connector

A 1 x 2 straight header is available for connecting an LED, which indicates whether the system is fully powered up or in suspend mode. The LED will be on when the system is fully powered up and flashing when the system is in suspend mode.

Reference: J22 (P/S-LED)
Connector Type: 1X2 male straight, .100 centers
Connector Part Number: AMP 103322-2 or equivalent

Table 2.25. Power On LED Conn. Pinout

PIN	SIGNAL
1	P/S-
2	+5V

3

Configuration

Product Configuration

The PWA component will be produced by BCM with the microprocessor soldered directly on the board. Therefore no jumpers need to be set for processor speed. The only user selectable jumper is the Password/CMOS Clear jumper.

DRAM Subsystem Configurations

Table 3.6. SIMMs Configurations

SIMM1	SIMM2	SIMM3	SIMM4	Total Memory
EMPTY	EMPTY	EMPTY	4MB	4MB
4MB	4MB	EMPTY	EMPTY	8MB
EMPTY	EMPTY	EMPTY	8MB	8MB
4MB	4MB	4MB	4MB	16MB
8MB	8MB	EMPTY	EMPTY	16MB
EMPTY	EMPTY	EMPTY	16MB	16MB
4MB	4MB	8MB	8MB	24MB
8MB	8MB	4MB	4MB	24MB
8MB	8MB	8MB	8MB	32MB
16MB	16MB	EMPTY	EMPTY	32MB
EMPTY	EMPTY	EMPTY	32MB	32MB
4MB	4MB	16MB	16MB	40MB
16MB	16MB	4MB	4MB	40MB
8MB	8MB	16MB	16MB	48MB
16MB	16MB	8MB	8MB	48MB
16MB	16MB	16MB	16MB	64MB
32MB	32MB	EMPTY	EMPTY	64MB
EMPTY	EMPTY	EMPTY	64MB	64MB
4MB	4MB	32MB	32MB	72MB
32MB	32MB	4MB	4MB	72MB
8MB	8MB	32MB	32MB	80MB
32MB	32MB	8MB	8MB	80MB
16MB	16MB	32MB	32MB	96MB

32MB	32MB	16MB	16MB	96MB
32MB	32MB	32MB	32MB	128MB
64MB	64MB	EMPTY	EMPTY	128MB

4

Operating Environments

Software

This product's software is referred to as "BIOS" (Basic Input and Output Subroutine), the BIOS resides as **firmware** in a non-volatile memory device using Flash technology. This technology gives the user the ability to be able to update the BIOS and accommodate changes to features or optimizations to better the performance of the system. The user need only to load a diskette with the new BIOS firmware and follow the manufacturer instructions to update the BIOS.

General

This product will have an Award Software, Inc. developed system Flash BIOS. The BIOS will have a menu driven SETUP utility. The specific features & implementation requirements are to be provided by the OEM Customer if so desired.

BIOS Setup

The SETUP Menu on your BIOS maybe slightly different than the one represented in here. Different OEMs will require certain user access to advanced functions while other OEMs may not allow the user any access at all. The exact BIOS Menu representation can be extracted from the BIOS supplied with your platform.

The Main Menu

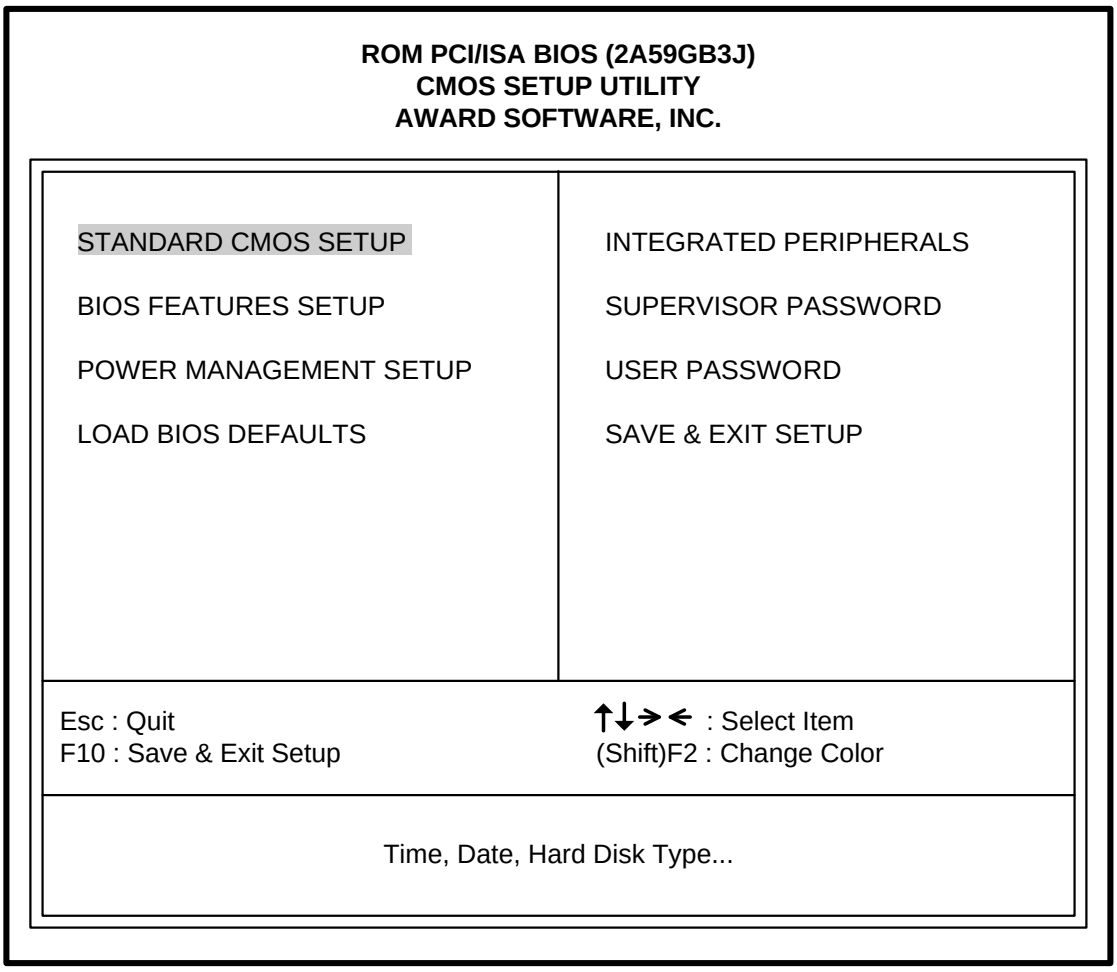
To start the Award BIOS CMOS Setup utility:

1. Turn on or reboot your system. The Award BIOS displays this message at the bottom of the screen:

   Press **DEL** to enter SETUP

2. Press the DELete Key to display the Main Menu, which looks like this:

Figure 4.1. BIOS Setup Main Menu



Main Menu Selections

The Main Menu Selections are as follows:

Table 4.1. Main Menu Selections

Standard CMOS Setup	Use this menu for basic system configuration, such as Date, Time, Hard Drive Parameters and Floppy Drive Parameters.
BIOS Features Setup	Use this menu to set certain BIOS Features available on your system's chipset.
Power Management Setup	Use this menu to configure Power-Management features.
Load BIOS Defaults	Use this to load the BIOS Defaults, except the Standard CMOS Setup
Integrated Peripherals	Use this menu to configure the Onboard peripherals, such as Serial and Parallel Ports and Hard Drive and Floppy Drive Controllers.
Supervisor Password	Setting a Supervisor Password restricts access to the BIOS Setup menus
User Password	Setting a User Password restricts access to the BIOS Setup menus or the System
Save & Exit Setup	Save all changes to CMOS and Exit the Setup Utility

Use the "←↑→↓" arrow keys to make a selection.

Standard CMOS Setup

You can make the following selections on the Standard CMOS Setup Menu.

Figure 4.1.1 Standard CMOS Setup

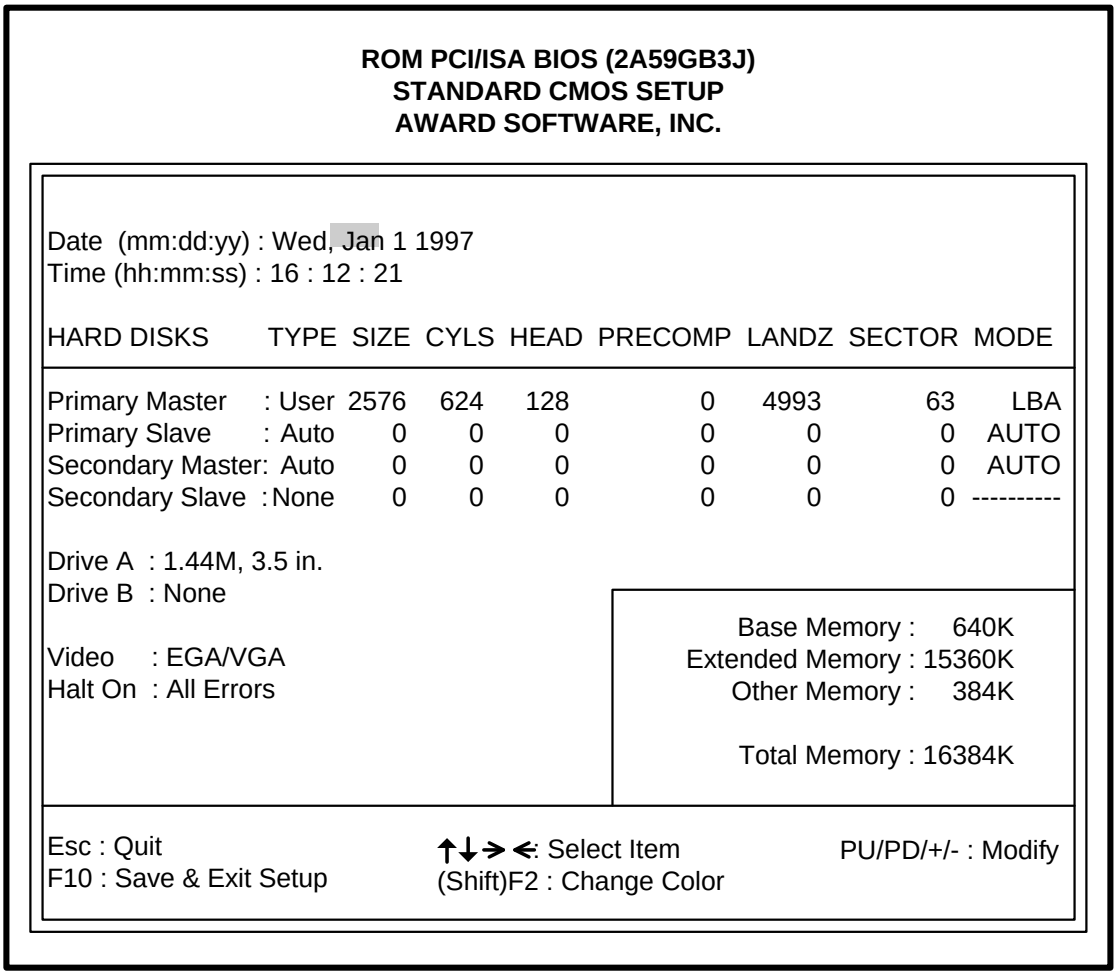


Table 4.1.1. Standard CMOS Setup

Feature	Options	Description
Date	MM/DD/YYYY	Set the system date.
Time	HH/MM/SS	Set the system time.
Primary Master TYPE Primary Slave TYPE Secondary Master TYPE Secondary Slave TYPE	Auto User None 1 - 45	'Auto' autotypes the drive at each boot. 'User' prompts the user to fill in remaining fields. 'None' indicates no drive is attached. '1 - 45' fills in all remaining fields with values for predefined disk types.
SIZE	N/A	Indicates the Size of the Hard Drive
CYLS∗	1 - 16,384	Number of Cylinders
HEAD∗	1 - 16	Number of read/write Heads
PRECOMP∗°	N/A	Obsolete
LANDZ∗°	N/A	Obsolete
SECTOR∗	1 - 63	Number of sectors per track
MODE	AUTO NORMAL LBA LARGE	'AUTO' will automatically select which mode to use. 'NORMAL' can be used for drive smaller than 514MB. 'LBA' and 'LARGE' can be used for drives larger than 514MB.
Disk A: Disk B:	360KB, 5 ¼" 1.2MB, 5 ¼" 720KB, 3 ½" 1.44M, 3 ½" 2.88MB, 3 ½" None	Select the type of floppy-disk drive installed in your system.
Video	Mono EGA/VGA CGA 40 CGA 80	Select the default video device
Halt On	No Errors All, But Keyboard All, But Diskette All, But Disk/Key All Errors	System displays the error found and 'Press F1 to continue, DEL to enter Setup', unless disabled.
Base Memory	N/A	Displays amount of conventional memory detected during bootup
Extended Memory	N/A	Displays the amount of extended memory detected during bootup
Other Memory	N/A	Displays the amount of other memory detected during bootup
Total Memory	N/A	Displays the total amount of memory detected during bootup

° IDE drives do not require setting Landing Zone and Write Precomp.

∗ These settings can only be changed when the Hard Disk Type is set to 'USER'.

WARNING: Incorrect settings can cause your system to malfunction.

BIOS Features Setup

You can make the following selections on the BIOS Features Setup Menu.

Figure 4.1.2 BIOS Features Setup

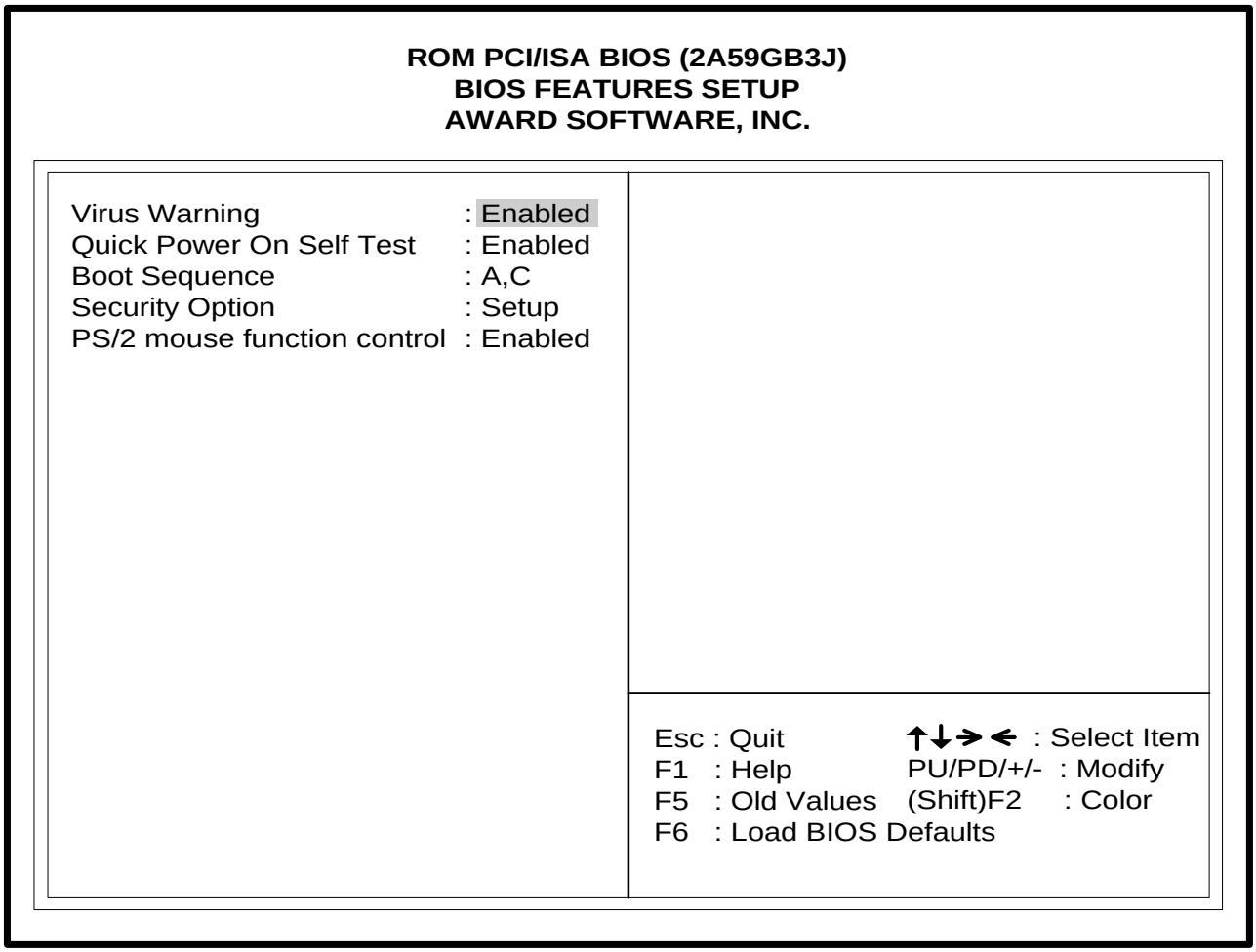


Table 4.1.2 BIOS Features Setup

Feature	Options	Description
Virus Warning	Enabled Disabled	If 'Enabled', a warning message will appear on the screen when any attempt is made to write to the boot-sector of the Hard Disk Drive.
Quick Power On Self Test	Enabled Disabled	If 'Enabled', the system will shorten or skip certain checks during the Power On Self Test (POST). The system will boot more quickly.
Boot Sequence	A,C C,A C,CDROM,A CDROM,C,A C only	The BIOS attempts to load the Operating System from the disk drives in the sequence selected here.
Security Option	Setup System	When 'Setup' is selected, the system will neither boot nor allow access to the CMOS Setup, without entering the correct password. When 'System' is selected, the system will boot, but access to the CMOS Setup is restricted by password.
PS/2 Mouse Function Control	Enabled Disabled	Enables or Disables the on-board PS/2 Mouse functionality.

Power Management Setup

Selecting "Power Management Setup" from the Main Menu displays a menu like the one shown here.

Figure 4.1.3 Power Management Setup

ROM PCI/ISA BIOS (2A59GB3J)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	: Max Saving
PM Control by APM	: Yes
Video OFF Method	: V/H SYNC+Blank
MODEM Use IRQ	: 3
Doze Mode	: 1 Min
Standby Mode	: 1 Min
Suspend Mode	: 1 Min
HDD Power Down	: 1 Min

** Wake Up Events in Doze & Standby**

IRQ3 (Wake-Up Event)	: ON
IRQ4 (Wake-Up Event)	: ON
IRQ8 (Wake-Up Event)	: ON
IRQ12(Wake-Up Event)	: ON

** Power Down & Resume Events **

IRQ3	(COM 2)	: ON
IRQ4	(COM 1)	: ON
IRQ5	(LPT 2)	: OFF
IRQ6	(Floppy Disk)	: OFF
IRQ7	(LPT 1)	: OFF
IRQ8	(RTC Alarm)	: OFF
IRQ9	(IRQ2 Redir)	: OFF
IRQ10	(Reserved)	: OFF
IRQ11	(Reserved)	: OFF
IRQ12	(PS/2 Mouse)	: ON
IRQ13	(Coprocessor)	: OFF
IRQ14	(Hard Disk)	: ON
IRQ15	(Reserved)	: OFF

Esc : Quit	↑↓→← : Select Item
F1 : Help	PU/PD/+/- : Modify
F5 : Old Values	(Shift)F2 : Color
F6 : Load BIOS Defaults	

Table 4.1.3 Power Menu Selections

Feature	Options	Description
Power Management Mode	Disable Min Saving User Define Max Saving	'Max' and 'Min' set power-management options with pre-defined values. Select 'User Define' to make your own selections from the following fields. Disabled turns off all power management.
PM Control by APM	Yes No	When 'Yes' is selected the Power Management features are controlled by an advanced operating system such as Windows95®. When 'No' is selected, the BIOS will control power management.
Video Off Method	Blank Screen V/H SYNC+Blank DPMS	When 'Blank Screen' is selected, the system will only blank the screen when going into power saving mode. When 'V/H Sync+Blank' is selected, the system will also turn off the V-SYNC and H-SYNC signals. 'DPMS' mode can only be used by video card that adhere to the DPMS Standard.
Modem Use IRQ	NA, 3, 4, 5, 7, 9, 10, 11	Enter the Interrupt that is used by the modem, if one is installed. Select 'NA' if no modem is installed
Doze Mode Standby Mode Suspend Mode	Disable 1 min 2 min 4 min 6 min 8 min 10 min 20 min 30 min 40 min 1 Hour	Time of inactivity required to enter the next consecutive power saving mode. These selections are only available when the above Power Management feature is set to 'User Define'
HDD Power Down	Disable 1 - 15 Min	Time without any disk access, before the hard drive goes into standby mode (i.e. motor turns off).
Wake Up events in Doze and Standby IRQ 3, 4, 8, 12	OFF ON	When the system is in Doze or Standby mode, accessing the enabled IRQ turns the system back to full power mode.
Power Down and Resume Events IRQ 3 - 15	OFF ON	Any activity on the enabled IRQ will reset the Power Management Timers to 0. If the system is in Power Saving Mode, accessing the enabled IRQ turns the system back to full power

Load BIOS Defaults

This feature allows the CMOS Settings to be reset to the original default values. The values in the Standard CMOS Setup Menu, such as date, time and disk drive parameters are unaffected.

Integrated Peripherals

Selecting "Integrated Peripherals" from the Main Menu displays a menu like the one shown here.

Figure 4.1.4 Integrated Peripherals Menu

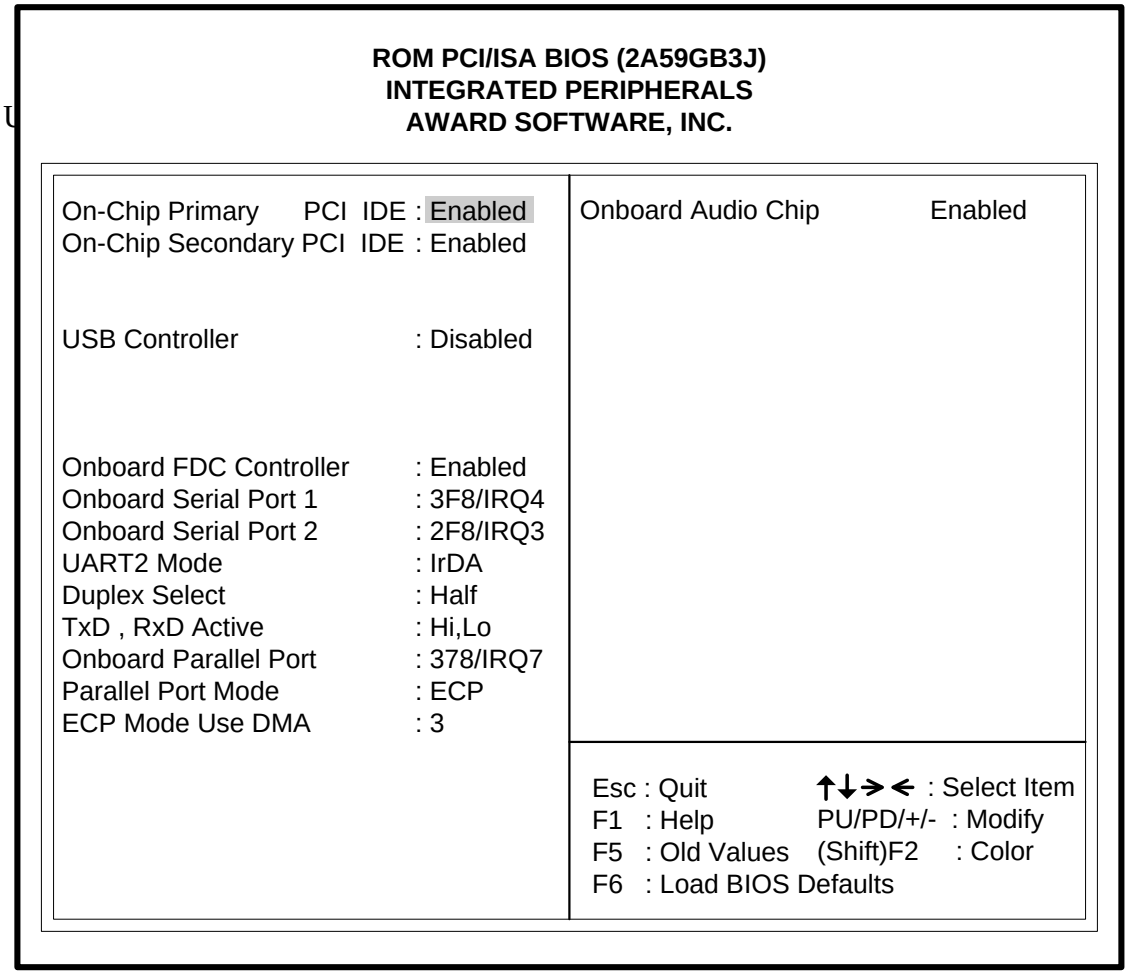


Table 4.1.4 Integrated Peripherals Selections

Feature	Options	Description
On-Chip Primary & Secondary PCI IDE	Enabled Disabled	Enable or Disable the corresponding on-board IDE adapter.
USB Controller	Enabled Disabled	Enable or Disable the on-board Universal Serial Bus (USB) controller
Onboard FDC Controller	Enabled Disabled	Enable or Disable the on-board Floppy Disk Drive controller
Onboard Serial Port 1	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3 Auto	Disable or Enable the first onboard serial port. 3F8 through 2E8 correspond to Com1 through Com4 assignments respectively.
Onboard Serial Port 2	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3 Auto	Disable or Enable the second onboard serial port. 3F8 through 2E8 correspond to Com1 through Com4 assignments respectively.
UART2 Mode	Standard IrDA ASK-IR	Select mode for the second serial port. 'Standard' is used for normal serial communications. 'IrDA' is used for Infra-Red communications at a rate of up to 115 kBaud. ASK-IR is used for Infra-Red communication at up to 19.2kBaud.
Duplex Select	Half Full	Select 'Half' or 'Full' duplex to match the specification of the IR capable peripheral that is being used.
TxD, RxD Active	Lo,Lo Hi,Hi Hi,Lo Lo,Hi	Sets the transmit and receive active level, i.e. 'Hi,Lo' means that the transmit output is active high (+V) and the receive input is active low (Logic Ground)
Onboard Parallel Port	Disabled 3BC/IRQ7 378/IRQ7 278/IRQ5	Disable or Enable the Parallel Port. 3BC, 378, 278 correspond to printer ports LPT3, LPT2, LPT1 respectively.
Parallel Port Mode	Normal EPP1.7+SPP ECP+EPP1.7 SPP EPP1.9+SPP ECP ECP+EPP1.9	'Normal' can be selected when the port is used for printer only. The Enhanced Parallel Port (EPP) protocol is meant to be used with peripherals such as CD ROM and Tape Backup. The Extended Capabilities Port (ECP) protocol is meant to be used with multi-function peripherals, such as a Fax/Printer/Modem device.
ECP Mode used DMA	1, 3	Select the Dynamic Memory Address (DMA) channel to be used by the parallel port. Only available when ECP mode is selected.
Onboard Audio Chip	Enabled Disabled	Enable or Disable the audio chip on the motherboard.

Supervisor Password

Select a supervisor password to prevent access to the CMOS Setup Utility program without entering the proper password. If the security option in the BIOS Features Setup is set to ‘System’, a password must also be entered before the system will boot.

User Password

Select a user password to prevent access to the CMOS Setup Utility program without entering the proper password. If the security option in the BIOS Features Setup is set to ‘System’, a password must also be entered before the system will boot. If a supervisor password is also set up the CMOS Setup Utility program will be unavailable unless the supervisor password is entered.

Save & Exit Setup

This feature allows the changes to be made to the CMOS setup to be saved. The system will resume booting after a successful save.

Operating Systems

The following operating system are required to be tested prior to First Customer Shipment (FCS):

* Windows ‘95
* Netware 3.12
* DOS 6.22
* Netware 4.0

Performance

The benchmarks used to qualify performance include, but are not limited to:

- Winstone96/97 Ver. 1.0
- ZD Labs WINBENCH & WINMARK 96/97 V1.0
- Norton SI version 8.0 and 9.0
- Landmark System Speed Test 2.0

The following table is an expected minimum performance for FM519 systems under several of the "common" user benchmarks. The stated benchmarks are for the 200MHz Pentium P55C MMX Processor using 32MB of main system memory with 256KB of external Pipeline Burst cache and a Quantum 1280MB HD in Mode 4. The Video mode is set to 800x600 at 256 colors.

Table 4.6. Benchmark Figures

WinBench97 V1	CPU mark 16	CPU mark 32	H/G disk (kb/s)	H-G mark	
WinStone97 V1	H-E app	H-E Image	Business-D	Business-P	Business-W
WinStone32	Overall	Graphic/DTP	DataBase	Word P/S	
WinBench96 V1	Overall	CPU mark 16	CPU mark 32	Video mark	Disk mark
WinStone96	Overall	Graphic/DTP	DataBase	Spreadsheet	Word P/S
Norton 9.0	Bench Mark				
Norton 8.0	CPU	Disk Speed	Overall		
Landmark	CPU	FPU	Video		

Compatibility

BCM will supply necessary information and resources to assist the customer in the FM519 product qualification testing. The product is designed for compatibility and shall be tested to the requirements set forth in the **FM519 System Compatibility Test Plan**.

5

Electrical, Environmental and Mechanical Specifications

This section specifies Electrical and Environmental parameters for the FM519 motherboard and describes its Mechanical characteristics.

Absolute Maximum Ratings

Stresses beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only).

Table 5.1. Absolute Maximum Ratings

Operating Temperature	0°C to + 55°C
Storage Temperature	-55°C to + 150°C
Voltage on any Signal with Respect to VSS	-0.3 to Vcc +0.3 V
Supply Voltage with Respect to VSS	-0.3 to +5.5 V

The topics in this section specify the normal operating conditions for the FM519 motherboard. Exposure to absolute maximum rating conditions for extended periods may affect the system reliability.

Electrical

FM519 DC specifications are summarized here, for motherboard signaling environment, power connectors and 5V power budget. Refer to PCI Local Bus Specification Rev. 2.0, and ISA Bus Specification for PCI and ISA DC and AC electrical specifications. Refer also to the documentation for ASIC devices used on the FM519 motherboard.

DC Specifications for 5V and 3.6V Signals

The following tables, show the required DC specifications for 5V and 3.6V CPU bus signaling environment.

Table 5.2. 5 Volt DC Specifications

Symbol	Parameter	Condition	Min	Max	Units
Vcc	Supply Voltage		4.75	5.25	V
TA	Operating Temperature	Still Air	0	55	°C
Vih	Input High Voltage		2.2	Vcc +1.2	V
Vil	Input Low Voltage		-1.2	0.8	V
Iih	Input High Current	Vin = 2.7		1.0	mA
Iil	Input Low Current	Vin = 0.5		-1.6	mA
Voh	Output High Voltage	Ioh, max Vcc, min	2.4		V
Vol	Ouput Low Voltage	Iol, max Vcc, min		0.55	V

Table 5.3. 3.6 Volt DC Specifications

Symbol	Parameter	Condition	Min	Max	Units
Vcc3	Supply Voltage		3.00	3.6	V
Vih	Input High Voltage		0.475 x Vcc3	Vcc +0.5	V
Vil	Input Low Voltage		-0.5	0.325 x Vcc3	V
Iih	Input High Leakage Current	Vin = 2.7		+/- 10	OA
Iil	Input Low Leakage Current	Vin = 0.5		+/- 10	OA
Voh	Output High Voltage	Iout = -0.5 mA	0.9 x Vcc3		V
Vol	Ouput Low Voltage	Iout = -1.5 mA		0.1 x Vcc3	V

Power Supply

Power Supply Connectors

The input power is supplied via a pair of power supply connectors on the system PWA. The connectors are positioned end-to-end to create a single row (1x12).

Reference: J1
Connector Type: male, 1x12, .156 centers
Connector Part Number: MOLEX 87218-1204 / AMP 6440445-6

Table 5.4. Power Supply Connector

PIN	DESCRIPTION
1	POWER GOOD
2	+5VDC
3	+12VDC
4	-12VDC
5	GROUND
6	GROUND
7	GROUND
8	GROUND
9	-5 VDC
10	+5VDC
11	+5VDC
12	+5VDC

NOTE: The J1 shell may be keyed, per customer's request, to allow proper installation of the mating connectors.

Input Power Budget

The +5V current available reflects the rating of the power connector. The Power itself may deliver more so the system integrator must be sure that the total load does not exceed the system power supply or board power connector rating, whichever is less. The rating of the ISA slots is 4.5A per slot. The ISA specification recommends supporting an average of 3.0A per slot. The average current consumption may not exceed 3A per slot. The system integrator must also guarantee that worst-case power consumption does not exceed the maximum allowed by the motherboard power connector.

Table 5.5. FM519 Motherboard Power Budget

Voltage		**Current Load(A)**	
Input	**Tolerance**	**Minimum**	**Maximum**
-12V	+/-5%	0.0	0.1
-5V	+/-5%	0.0	0.1
+5V	+/-5%	3.0	8.0
+12V	+/-5%	0.2	0.8

Environmental

The FM519 motherboard is intended for use in a Class B environment (residential). The following table summarizes environmental limits for the FM519, operating and non-operating.

Table 5.6. Environmental Specifications

Temperature	**Specification**
Non-operating	-40^0 C to 70^0 C
Operating Temperature	0^0 C to 55^0 C
Thermal Map	Must not exceed maximum IC junction temperature as specified in the component data sheets (CPDs).
Thermal Shock	**Specification**
Non-operating	-40^0 C to 70^0 C
Humidity	**Specification**
Non-operating	92% RH at $+55^0$ C
Operating	85% RH at $+55^0$ C
Vibration	**Specification**
Non-operating	Random input, 0.01 g2/Hz at 5Hz, sloping to 0.02 g2/Hz at 20Hz and maintaining 0.02 g2/Hz from 20Hz to 500Hz
Shock	**Specification**
Non-operating	50g, 11msec, 1/2 sine
Operating	Not applicable
Altitude	**Specification**
Non-operating	50K feet (pressure altitude)
Operating	10K feet (pressure altitude)
ESD	**Specification**
Operating	Indirect (radiated) only. Test to 15KV with limited errors and to 25KV with no damage.
EMI	**Specification**
Operating	Required to meet EMI emission requirements, tested as part of the system.

Reliability Specification

The following table lists the hard MTBF for the motherboard. A hard failure indicates that a permanent or repeatable failure that can be readily remedied by replacing the faulty part with a good one. The listed MTBF is for the motherboard without a CPU or memory components.

Table 5.7. Motherboard MTBF

Configuration	MTBF	Temperature
With Audio	198,316 Hours	35 ^{o}C
Without Audio	227,737 Hours	35 ^{o}C
With Audio	153,390 Hours	50 ^{o}C
Without Audio	175,684 Hours.	50 ^{o}C

Mechanical

System Interfaces

User-Accessible Sockets

The following user accessible sockets are located on the top of the system PWA:

Table 5.9. Accessible Sockets

SIMM1 - 4	SIMM sockets

User-accessible Connectors

The following user-accessible connectors are located on top of the system PWA:

Table 5.10. Accessible Connectors

NAME	REFERENCE
J9 (CD-IN)	CD Audio input connector
J10 (GAME)	Joystick header
J1 (POWER)	Power supply connector header
J8 (COM2)	Serial Port 2 header
J27 (HD LED)	Hard drive activity indicator
J21 (FAN)	CPU Cooling Fan connector
J22 (POWER LED)	Front panel Power LED connector
J18 (SPEAKER)	Speaker Connector
J25(RESET)	Reset Switch connector
J19(SUSPEND)	Suspend Switch connector
J13	Microphone In header
J15	Line Out header
BT1 (EXT BATT)	External CMOS Battery Connector
J4, J3 (IDE PRIMARY & IDE SECONDARY)	IDE Hard disk drive interface headers
J24(IRDA)	IR Interface connector
J6 (FLOPPY)	Floppy disk drive interface header

Back-Panel Interfaces

The following interface connections are located on the rear panel of the system PWA:

Table 5.11. Back-Panel Interfaces

J2	Keyboard connector

J5	PS/2 Mouse connector
P1	Monitor connector
J20	TV Output – RCA Jack
J21	TV Output – S-Video connector
J7	COM 1 port connector
J12	Microphone In connector
J14	Line Out Connector
J11	Parallel port connector

Manufacturability/Serviceability

FM519 is designed to be both easy to manufacture and service. The items specifically related to the system PWA are:

- Connector location & labeling
- Jumper location & labeling
- PWA bar code label (part number and revision)
- Flash BIOS Memory location & socket
- SIMM sockets labeling & location

Regulatory

BCM will supply information and resource to assist in the FM519 product qualification testing for compliance with the regulatory agency approvals.

BLANK

Appendix A - PWA Layout