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Customer Support Dept.
April 1, 2003

3DK38124
USER MANUAL

FOR H8/38124 ON-CHIP FLASH MICROCONTROLLER

Warning

Check the silkscreen around the power jack (J9) for the minimum and maximum voltage input levels for this 3DK.

Always use a centre positive supply for this board.

DO NOT USE AN E6000 POWER SUPPLY with this 3DK

Preface

Cautions

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Document Information

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Version: 1

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Website: http://www.eu.renesas.com/

Table of Contents

1. Power Requirements

All 3DK boards are centre positive with a 2.5mm barrel power jack.
The diode, D1 provides reverse polarity protection.
A 9V, centre positive supply is suitable for use with this board.

Warning
Check the silkscreen around the power jack (J9) for the minimum and maximum voltage input levels for this 3DK.
The 3DK is neither under nor over voltage protected.
Always use a centre positive supply for this board.
DO NOT USE AN E6000 POWER SUPPLY with this 3DK

2. Power – Up Behaviour

The 3DK board has code pre-programmed into the Renesas microcontroller. On powering up the board, the red user LEDs will start to flash. Switches 2 and 3 as well as the potentiometer can be used to modify the LED flashing pattern.

3. Purpose

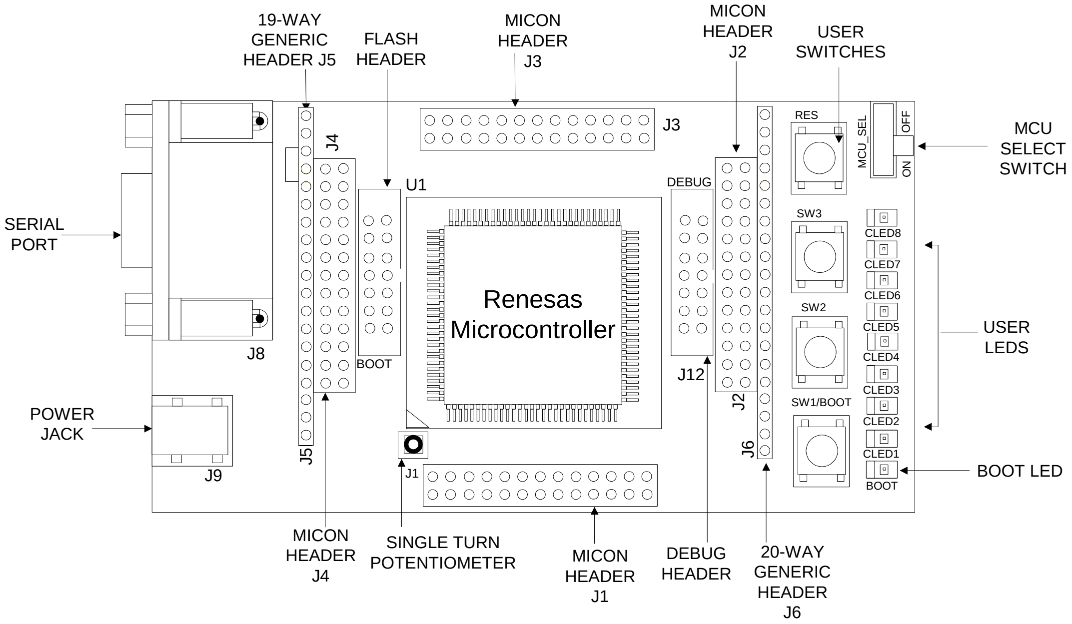
This 3DK board is an evaluation tool for Renesas microcontrollers.
Features include:

a. Renesas Microcontroller Programming
b. User Code Debugging
c. User Circuitry such as Switches, LEDs and potentiometer(s)
d. User or Base Board Connectivity

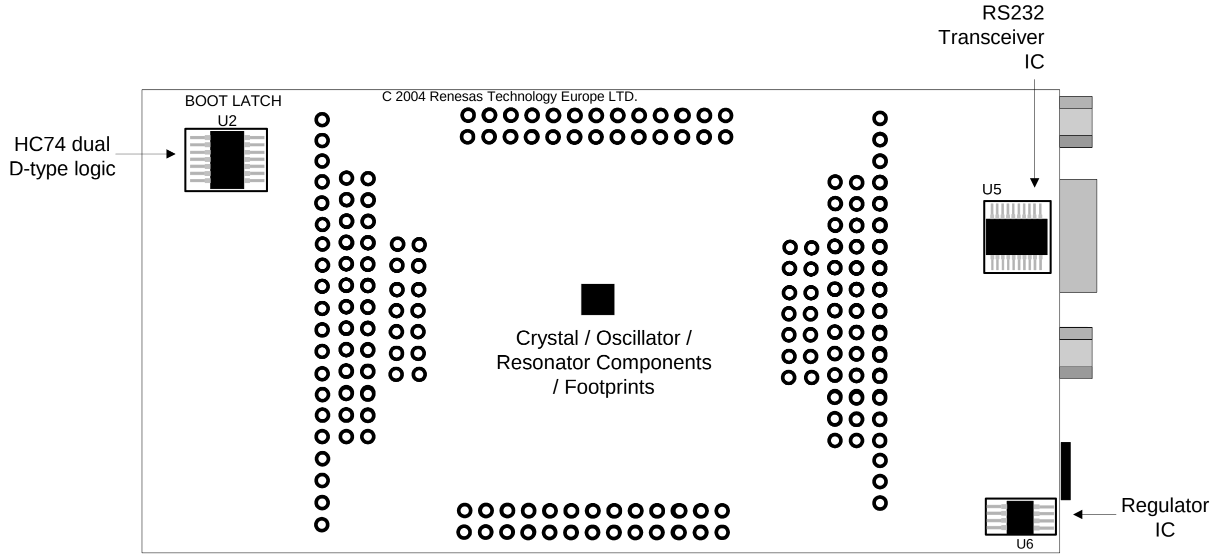
The 3DK board contains all the circuitry required for microcontroller operation.

4. Board Layout

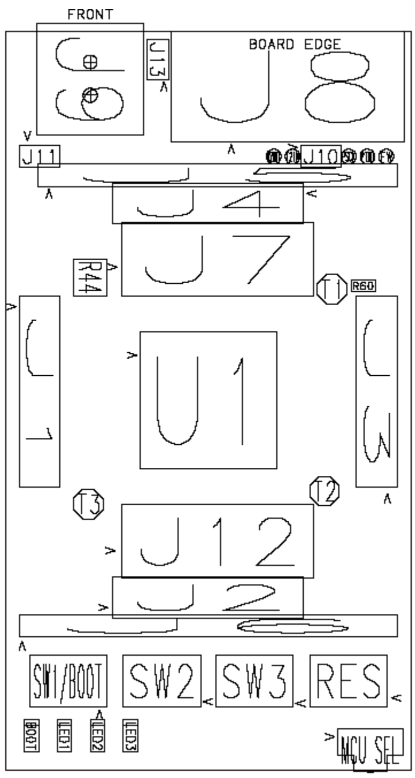
The following diagram shows the component layout top layer component of the board.
Note: The diagram below is for illustrative purposes and does not accurately reflect the 3DK detailed in this manual.



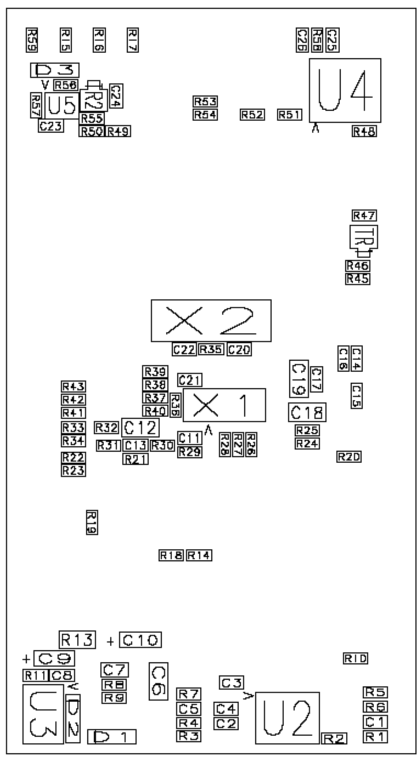
The following diagram shows the component layout bottom layer component of the board. Note: The diagram below is for illustrative purposes and does not accurately reflect the 3DK detailed in this manual.



PCB Component Placing Top

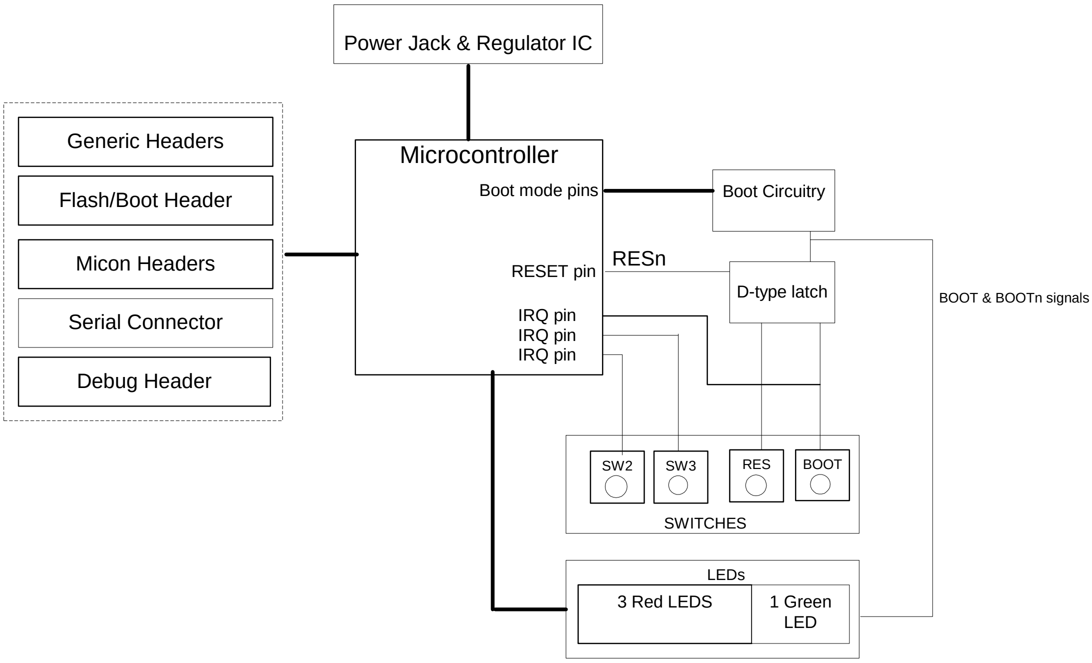


PCB Component Placing Bottom



5. BLOCK DIAGRAM

Diagram 5.1 is representative of the 3DK components and their connectivity.



6. USER CIRCUITRY

6.1. SWITCHES

There are four switches located on the 3DK. These are:

Switch	Function	Microcontroller
SW1/BOOT	This switch is used in conjunction with the RES switch to place the device in BOOT mode.	IRQ0 (Port 4 –3)
SW2	This switch is connected via a 0R link to an IRQ line capable of waking up the microcontroller device from sleep mode.	IRQ4 (Port 1 –4)
SW3	This switch is connected via a 0R link to another IRQ line capable of waking up the microcontroller device from sleep mode.	IRQ3 (Port 1 – 7)
RES	This switch when pressed resets the 3DK microcontroller.	RESn

NB. Refer to schematic for detailed connectivity information.

6.2. LEDS

There are four LEDs on the 3DK board. The green BOOT LED indicates the device is in boot mode when lit. The three red LEDs are connected to an IO port and will light when their corresponding port pin is set low.
Table 6-1, below, shows the LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As shown on silkscreen)	Microcontroller Port Pin function	Microcontroller Pin Number
CLED1	Port 9 – 0	54
CLED2	Port 9 – 1	55
CLED3	Port 9 – 2	56

Table 6-1:LED Port

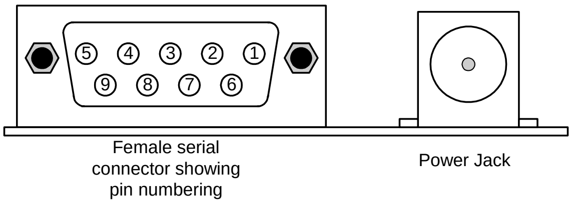
6.3. SERIAL PORT

The microcontroller programming serial port (SCI3) is connected to the D–type connector J8 via an RS232 transceiver.
The serial baud rates supported by this 3DK are shown below. Note: these values are calculated from the frequency value of the main oscillating source fitted by default on this 3DK.

Baud Rate Register Settings for Serial Communication Rates												
Values are calculated for 9.8304MHz clock												
SMR Setting:	**0**			**1**			**2**			**3**		
Comm. Baud	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**
110	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	86	110.3	0.31	21	109	-0.83
300	Invalid	Invalid	Invalid	127	300	0.00	31	300	0.00	7	300	0.00
1200	127	1200	0.00	31	1200	0.00	7	1200	0.00	1	1200	0.00
2400	63	2400	0.00	15	2400	0.00	3	2400	0.00	0	2400	0.00
4800	31	4800	0.00	7	4800	0.00	1	4800	0.00	Invalid	Invalid	Invalid
9600	15	9600	0.00	3	9600	0.00	0	9600	0.00	Invalid	Invalid	Invalid
19200	7	19200	0.00	1	19200	0.00	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
38400	3	38400	0.00	0	38400	0.00	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
57600	2	51200	-11.11	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
115200	0	153600	33.33	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid

Table 6-2 : BRR Settings

This serial port may be used as a debugging communication port or as a normal serial communication port when the device is in user mode.



6.4. JUMPERS

Table 6-3 below describes the function of the 2-Pin jumpers contained on this 3DK board.

2-Pin Jumper Settings				
Reference	Jumper Function	Fitted	Alternative (Removed)	Footprint for jumper only/Jumper pins fitted
J10	RX Disable	PRXD from the RS232 device to U1 is enabled. This enables serial port communication.	Disabled. This allows the FDM to program the microcontroller	Jumper pins fitted
J11	UVCC power Measurement	Bypasses R11, a 1206 0R resistor, for current measurement	R11 must be fitted to power UVCC	Footprint only

Table 6-4: 2-Pin jumpers

7. OSCILLATOR SOURCES

A crystal resonator is fitted on the 3DK and used to supply the main clock input to the Renesas microcontroller. Table 7-1 details the oscillators that are fitted on this 3DK:

Component	Details		
Crystal	Yes	9.8304MHz	38400
Subclock	Yes	32.768 kHz	N/A

Table 7-1: Oscillators / Resonators

Warning: When replacing the default oscillator with that of another frequency, the FDT programming kernels supplied will need rewriting. The supplied HMON debugging monitor will not function. The user is responsible for code written to support operating speeds other than the default. See the HMON user manual for details of making the appropriate modifications in the code to accommodate different operating frequencies.

8. MODES

The 3DK supports User mode and Boot mode. User mode may be used to run user code, while Boot mode may be used to program the Renesas microcontroller with program code and to debug code.
To enter boot mode, the mode pins are held in their boot states while reset is pressed and released. The BOOT LED will be illuminated to indicate that the microcontroller is in boot mode.

8.1. BOOT MODE

The boot mode settings for this 3DK are shown in Table 8-1 below:

TEST	NMI	P36	LSI State after Reset End
0	1	X	User Mode
0	0	1	Boot Mode

Table 8-1: Mode pin settings

8.2. USER MODE

For the device to enter User Mode, reset must be held active while the microcontroller mode pins are held in states specified for User Mode operation. 100K pull up and pull down resistors are used to set the pin states during reset.
The H8/38124 supports only normal mode, which has a 64-kbyte address space.

9. PROGRAMMING METHODS

The Flash ROM on the microcontroller can be programmed when the device is in Boot mode. Once in boot mode, the bootloader program stored in the microcontroller executes and attempts a connection with a host (for example, a PC). The host, on establishing a connection with the microcontroller, may then transmit program data to the microcontroller via the appropriate programming port.

Table 9-1 below shows the programming port for this Renesas Microcontroller and its associated pins

Programming Port Table – Programming port pins and their 3DK signal names		
SCI3	TXD, PIN 71	RXD_1, PIN 70
3DK Signal Name	PTXD	PRXD

Table 9-1: Serial Port Boot Channel

9.1. BOOT PROGRAMMING

The microcontroller must enter boot mode for programming, and the programming port must be connected to a host for program download. To execute the boot transition, and allow programs to download to the microcontroller, the user must perform the following procedure:

1. Connect a 1:1 serial cable between the host PC and the 3DK board
2. Depress the BOOT switch and keep this held down
3. Depress the RESET switch once, and release
4. Release the BOOT switch

9.2. FDM HEADER

This 3DK does not support the FDM.

9.3. E7 HEADER

The Renesas E7 Debugger is a tool for debugging Renesas microcontrollers, available separately from Renesas. The E7 utilises SCI4 on the microcontroller. The device may be debugged and programmed using the E7.

9.4. OFF-BOARD PROGRAMMING

All 3DKs are capable of programming an alternative microcontroller on a secondary board. The user is responsible for providing this second board containing the alternative microcontroller, its supporting circuitry and an FDM or FoUSB header for the microcontroller.

To program the alternative microcontroller, the user should perform the following steps

- Connect a cable between the 3DK programming header and that located on the secondary board.
- Slide switch MCU_SEL to the off-board programming position (OFF). This holds the microcontroller on the 3DK in reset, preventing it from being programmed.

10. HEADERS

10.1. MICON HEADERS

Table 10-1 to Table 10-4 shows the micon headers and their corresponding microcontroller connections. The header pins connect directly to the micon pin unless otherwise stated.

J1 Pin	Circuit Net Name	U1 pin number	J1 pin number	Circuit Net Name	U1 pin number
1	CON_AVCC (AVCC via a 0R link)	1	2		2
3		3	4		4
5		5	6		6
7	CON_X2 (X2 via a 0R link)	7	8	CON_X1 (X1 via a 0R link)	8
9	CON_OSC2 (OSC2 via a 0R link)	9	10	CON_OSC1 (OSC2 via a 0R link)	10
11		11	12		12
13		13	14		14
15		15	16		16
17		17	18		18
19		19	20		20

Table 10-1: J1

J2 Pin	Circuit Net Name	U1 pin number	J2 pin number	Circuit Net Name	U1 pin number
1		21	2		22
3		23	4		24
5		25	6		26
7		27	8		28
9		29	10		30
11		31	12		32
13		33	14		34
15		35	16		36

17		37	18		38
19		39	20		40

Table 10-2: J2

J3 Pin	Circuit Net Name	U1 pin number	J3 pin number	Circuit Net Name	U1 pin number
1		41	2		42
3		43	4		44
5		45	6		46
7		47	8		48
9		49	10		50
11		51	12		52
13		53	14		54
15		55	16		56
17	CON_PIN57 (PIN57 via a 0R link)	57	18		58
19		59	20		60

Table 10-3: J3

J4 Pin	Circuit Net Name	U1 pin number	J4 pin number	Circuit Net Name	U1 pin number
1		61	2		62
3		63	4		64
5		65	6		66
7		67	8		68
9		69	10		70
11		71	12		72
13		73	14		74
15		75	16		16
17		77	18		78
19		79	20		80

Table 10-4: J4

10.2. Generic Headers

Table 10-5 below shows the generic header connections

19 way generic Header				20 way generic Header			
Pin Number	Generic Header Name	3DK Signal Name	Micon Pin	Pin Number	Generic Header Name	3DK Signal Name	Micon Pin
1	Supply	Supply	N/A	1	IOPORT_TXD	IOPORT_TXD	N/A
2	Xin	CON_OSC1	10*	2	IOPORT_RXD	IOPORT_RXD	N/A
3	Vcc	VCC1	N/A	3	IOPORT_T1	IOPORT_T1	63
4	Vss	GROUND	N/A	4	IOPORT_T2	IOPORT_T2	62
5	Vcc	VCC2	N/A	5	IOPORT_T3	IOPORT_T3	67
6	Vss	GROUND	N/A	6	IOPORT_T4	IOPORT_T4	68
7	AVcc	AVCC	52	7	IOPORT_U	Not Connected	NC
8	AVss	AVSS	53	8	IOPORT_V	Not Connected	NC
9	Vref	VREF	N/A	9	IOPORT_W	Not Connected	NC
10	AN_0	PIN77	77	10	IOPORT_0	IOPORT_0	54
11	AN_1	PIN78	78	11	IOPORT_1	IOPORT_1	55
12	AN_2	PIN79	79	12	IOPORT_2	IOPORT_2	56
13	AN_3	PIN80	79	13	IOPORT_3	Not Connected	NC
14	DAC0	Not Connected	80	14	IOPORT_4	Not Connected	NC
15	DAC1	Not Connected	NC	15	IOPORT_5	Not Connected	NC
16	SCL	Not Connected	NC	16	IOPORT_6	Not Connected	NC
17	SDA	Not Connected	NC	17	IOPORT_7	Not Connected	NC
18	CTX	Not Connected	NC	18	/Reset	RESn	12
19	CRX	Not Connected	NC	19	/NMI	IOPORT_INT	N/A

20	V_{SS}	GROUND	N/A

Table 10-5: Generic Headers

* Connected via a DNF 0R Link, refer to schematic for further details.

11. CODE DEVELOPMENT

11.1. OVERVIEW

Note: For all code debugging using Renesas software tools, the 3DK board must be connected to a PC serial port via a serial cable.

The HMON embedded monitor code is modified for each specific 3DK Renesas Microcontroller. HMON enables HEW to establish a serial connection to the 3DK microcontroller, and control code execution on the microcontroller. The HMON embedded monitor code must be compiled with user software and downloaded to the 3DK, allowing the users' code to be debugged within HEW. The board must be operated in BOOT mode during debugging.

11.2. MODE SUPPORT

The HMON library is built to support Normal Mode only. The Device supports only Normal Mode.

11.3. BREAKPOINT SUPPORT

The monitor has an address break controller with one break channel, therefore one breakpoint can be located in ROM. Code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM.

Due to a limitation of the internal address break controller, a breakpoint set in ROM will execute the instruction at the breakpoint and stop on the subsequent op-code. The break controller only functions in BOOT mode.

11.4. CODE LOCATED IN RAM

Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

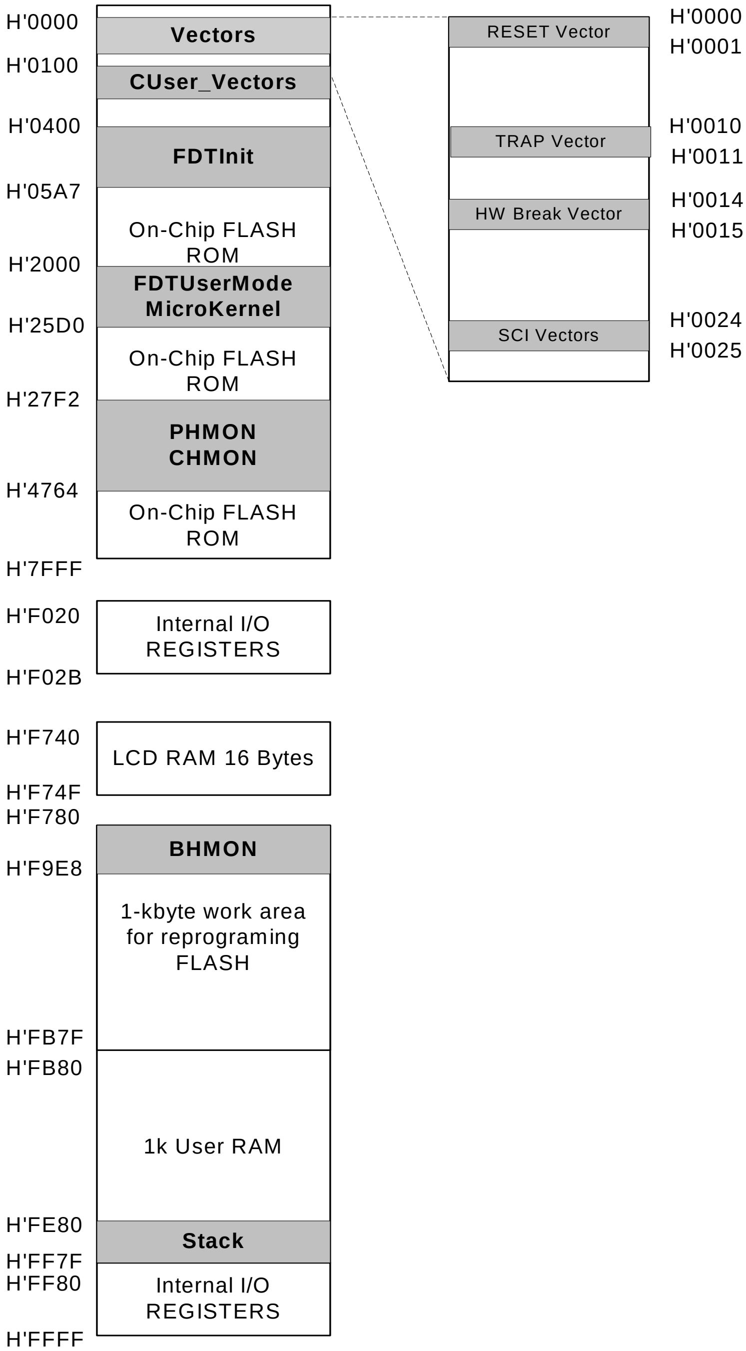
11.5. HMON CODE SIZE

HMON is built along with the debug code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Startup of HMON	H' 0000 0000	2
TRAP_VECTORS	TRAPA Instruction Vector (Vector 8) Required by HMON to create Breakpoints in RAM	H' 0000 0010	2
HW_BREAK_VECTORS	HMON Break Controller (Vector 10) Required by HMON to create Breakpoints in ROM	H' 0000 0014	2
SCI_VECTORS	HMON Serial Port Vectors (Vector 18) Used by HMON when EDK is configured to connect to the default serial port.	H' 0000 0024	2
PHMON	HMON Code	H' 0000 27f2	1e92
CHMON	HMON Constant Data	H' 0000 4684	e1
BHMON	HMON Uninitialised data	H' 0000 f780	1fd
FDTInit	FDT Init Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0000 0400	1a8
FDTUserModeMicroKernel	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0000 2000	5d1
CUser_Vectors	Pointer used by HMON to point to the start of user code.	H' 0000 0100	2

11.6. Memory Map

The memory map shown in this section visually describes the locations of program code sections related to HMON, the FDT kernels and the supporting code within the ROM/RAM memory areas of the microcontroller.



11.7. Baud Rate Setting

HMON is initially set to connect at 38400 Baud. The value set in the baud rate register for the microcontroller must be altered if the user wishes to change either the serial communication baud rate of the serial port or the operating frequency of the microcontroller. This value is held in the HMONserialconfiguser.c file, as SCI_CFG_BRR (see the Serial Port section for baud rate register setting values). The project must be re-built and the resulting code downloaded to the microcontroller once the BRR value is changed. Please refer to the HMON User Manual for further information.

11.8. Interrupt Usage

Because HMON uses the serial port, interrupts using a higher priority cannot be used while debugging. In practice this means that only the ADC interrupt can be used reliably during debugging.

11.9. Additional Information

For details on how to use High-performance Embedded Workshop (HEW), with HMON, refer to the HEW manual available on the CD or from the web site.

For information about the H8/38024-H8/38124 series microcontrollers refer to the H8/38024 *Series Hardware Manual*

For information about the H8/38124 assembly language, refer to the H8 *Series Programming Manual*

Further information available for this product can be found on the Renesas web site at:

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