NEC

Customer Notification

V850ES/Fx2

32-bit Single-Chip Microcontrollers

Operating Precautions

μPD70F323x,
μPD70323x,
μPD70F323xA,
μPD70323xA,
μPD70F323xB

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(A) Table of Operating Precautions

No.	Outline		μPD70F323x, μPD70323x		
		Rev.			
		Rank[Note]	K	E	
1	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗	
2	Stand-by Mode Release (Specification change notice)		✗	✗	
3	Undefined Voltage Level on Analog ports (Specification change notice)		✗	✗	

✓ :Not applicable

✗ :Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD70F323xA, μPD70323xA		
		Rev.			
		Rank[Note]	K		
1	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗		
2	Stand-by Mode Release (Specification change notice)		✓		
3	Undefined Voltage Level on Analog ports (Specification change notice)		✗		

✓ : Not applicable

✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD70F323xB		
		Rev.			
		Rank[Note]	K		
1	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗		
2	Stand-by Mode Release (Specification change notice)		✓		
3	Undefined Voltage Level on Analog ports (Specification change notice)		✓		

✓ : Not applicable

✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	AFCAN: Sleep Mode Wakeup (Specification change notice)

1. Description

When the AFCAN macro is set into SLEEP mode, it can be waken up by CAN bus activity.
This waking up is asynchronous to the operation of the macro and the CPU. By configuration setting, a WAKEUP interrupt can be generated by the AFCAN macro on the wakeup event.
While the interrupt is generated asynchronously, the AFCAN macro may need another dominant edge on the CAN bus, or software clearing of the SLEEP mode, in order to restart its synchronous operation.
During the time, after the interrupt already has been indicated, and before the CAN macro has restarted its synchronous operation, the registers of the AFCAN macro will not operate, because the AFCAN macro still remains in SLEEP mode. This time we will refer to as “wakeup dead time” in the following context.
To resolve from the *wakeup dead time*, software and/or hardware measures are required.

2. Exclusions

This Operating Precaution is **only applicable** to applications, which are fulfilling at least one of the following three conditions:

- SLEEP Mode of AFCAN is used **and** the possibility to wake up AFCAN by CAN-Bus events is given (see remark 1 below).
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see remark 2 below) **and**
  - after waking up from SLEEP mode of the AFCAN macro, the application software does **not** wait until the SLEEP mode is released by polling the CnCTRL (PSMODE) register, before continuing operation with the AFCAN macro (see remark 3 below) **and**
  - the CPU can reach instructions, where AFCAN registers are accessed while the AFCAN macro is still in SLEEP mode, due to the missing waiting condition.
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see remark 2 below) and
  - after waking up from SLEEP mode of the AFCAN macro, the CAN Bus Transceiver generates a **long-lasting or permanent dominant level** to the CRXD input of the AFCAN macro, instead of the propagated CAN-Bus level.

Remarks: 1. If the CAN-Bus Transceiver does not propagate the CAN-Bus signal, while the AFCAN macro is in SLEEP mode, and also does not forward a wakeup signal to CRXD, **this Operating Precaution is not applicable**.

2. The clock supply to the AFCAN macro can be stopped, depending on the features of the device, and the system design of the application. If the clock supply to the AFCAN macro is stopped, while a wakeup condition occurs, **this Operating Precaution is not applicable**.

3. The maximum waiting time for this loop can be up to 10 bits of the CAN-Bus Baudrate.
Waiting while retrying to clear CnINTS (Bit 5) can be used alternatively.

All other applications are not affected by this Operating Precaution.

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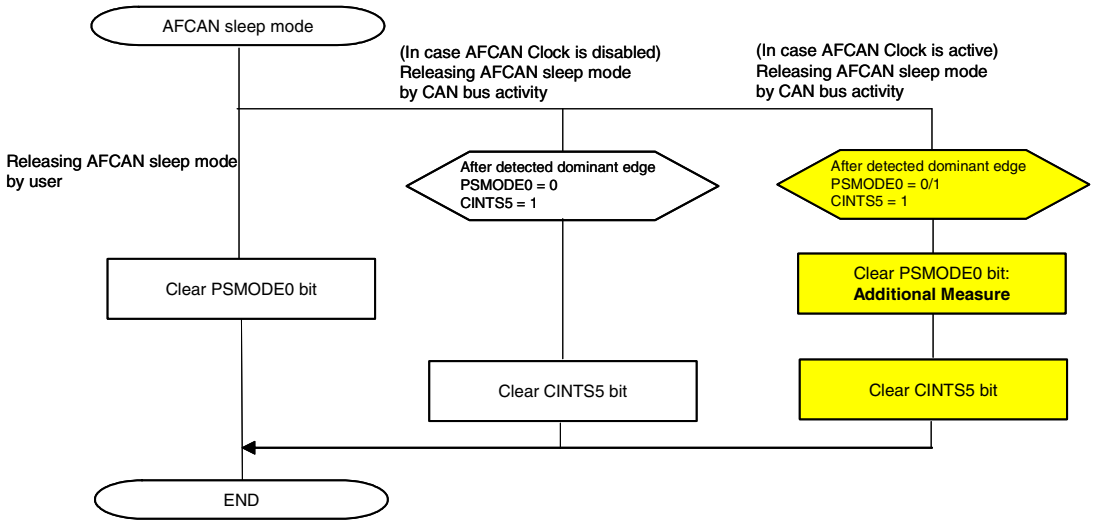
3. Application Dependency

3.1 Overview

The following flowchart illustrates, how and whether additional measures have to be taken in software, to avoid the *wakeup dead time*.

Figure: Additional Measures in case AFCAN clock is active when waking up



3.2 Not affected Applications

3.2.1 Applications not using SLEEP mode

If SLEEP mode is not used, **this Operating Precaution is not applicable.**

3.2.2 Applications waking up from SLEEP mode by User Request only

If there is no condition, when SLEEP mode can be left by CAN-Bus activity, but only on User Request (by clearing the PSMODE flag by software), **this Operating Precaution is not applicable**.

3.2.3 Applications using a CPU Power Save Mode

If the clock to the AFCAN macro is disabled, while it is waken up from SLEEP mode, **this operating precaution is not applicable**.
This means, if the user selects a power save mode of the target device, which switches off the clock of the AFCAN macro, immediately after it had been set into SLEEP mode, like the CPU STOP mode, the precaution needs not to be considered.
This is associated with the software improvement hints below.

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3.3 Affected Applications

3.3.1 Applications not waiting until SLEEP mode is left

If bus transceivers are used in conjunction with AFCAN, which will propagate the CAN bus signal to AFCAN permanently (not switched off or not in power saving modes), or, if bus transceivers are used in conjunction with AFCAN, which will propagate the unmodified CAN-Bus signal when waking up from a power save mode, the wakeup dead time lasts from the first recessive-to-dominant edge of the CAN-Bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN-Bus signal.
The worst case (maximum length) of the wakeup dead time, is given by the CAN bus speed and the rule of the CAN bus about the frequency of recessive-to-dominant edges. Given by the stuffing rule, at least every 10 bits, a recessive-to-dominant edge must occur.
If during the wakeup dead time, the CPU waits until the SLEEP mode is indicated to be cleared (either by polling the PSMODE flag, or by retrying to clear CnINTS[5]), **this operating precaution is not applicable**. In this case, the improvement hint according to 4.2.2 is followed implicitly.
If during the wakeup dead time, the CPU does not perform any access to the AFCAN macro in any case, **this operating precaution is not applicable**.

3.3.2 Applications using Bus Transceivers generating long-lasting dominant CAN-Bus Signals

If bus transceivers are used in conjunction with AFCAN, which *generate a permanent or long-lasting dominant level* when waking up from a power save mode, the operating precaution must be considered in any case.
In this case, the wakeup dead time lasts from the first recessive-to-dominant edge of the CAN bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN bus signal, depending on the behaviour of the CAN bus transceiver.
If no further dominant edge on the CAN bus occurs (in case of some CAN transceivers, which only provide one single edge on waking up), the time until SLEEP mode is left may become endless. Therefore, the waking up procedure of AFCAN regarding software, must be adjusted according to 4.1.1.

4. Software Improvement Hints

4.1 Recommended WAKEUP Handling by Software

4.1.1 Clearing the SLEEP Mode by Software

Within the WAKEUP interrupt routine, before accessing any other register or area of AFCAN, the SLEEP mode can be canceled by software, followed by a clearance of the WAKEUP interrupt flag.
Doing so, the AFCAN macro will start its synchronous operation right after these accesses.
In the following C-code example, replace the objects in “<>” brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User’s Manual.

```
WAKEUP INTERRUPT VECTOR -->
                        <CnCTRL_PSMODE> = 0;     /* Clear SLEEP Mode */
                        <CnINTS_CINTS5> = 1;     /* Clear INTS5      */
                        ...
                        /* following other parts of interrupt routine */
                        ...
```

Remark: Clearing INTS5 is required to get another WAKEUP interrupt anyway, by specification.

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4.2 Other WAKEUP Handling Hints

4.2.1 Switching off the Clock Supply to AFCAN, while in SLEEP Mode

If the clock supply to the AFCAN macro is stopped, while it is in SLEEP mode, the synchronisation of the WAKEUP works without any restriction. To achieve this, the documentation of clock controlling unit of the target device should be consulted. Usually this is performed by setting the STOP mode of the CPU of the target device.
However, the user has to consider, that there must not be any WAKEUP condition (dominant level on the CAN-Bus), while the software is executing between setting SLEEP mode and stopping the AFCAN clock.

4.2.2 Using a Waiting Loop within the WAKEUP interrupt routine

Within the WAKEUP interrupt routine, create a waiting loop, which tests the capability of clearing the WAKEUP interrupt flag within AFCAN, by checking the actual power save mode.
In the following C-code example, replace the objects in “<>” brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User’s Manual.

```
do
{
      AFCAN_SleepStatus = <CnCTRL_PSMODE>

      if( AFCAN_SleepStatus != 0 )
      {
      /* macro is still in SLEEP mode (waiting for latency time) */
      <CnINTS_CINTS5> = 1;    /* repeated trying to clear CINTS5 */
      }

} while( AFCAN_SleepStatus != 0 );
```

This improvement hint **cannot be applied**, if a CAN-Bus-Transceiver is attached to AFCAN, which generates a permanent or long-lasting dominant level to the FCRXDn receive input pin, if a wakeup condition occurs. Missing another dominant edge on the bus, the synchronisation will not happen, and the loop could run endlessly.

4.2.3 Using INIT Mode instead of SLEEP Mode

In this case, the waking up by CAN-bus activity must be performed via another free external interrupt. The CAN receive signal must be distributed on the FCRXDn pin, and to another external interrupt pin in parallel.
Using this external interrupt, the AFCAN macro can be restored into the previous operation mode. This implementation will not use the SLEEP mode of AFCAN at all, and use the INIT mode instead.

No. 2	Stand-by Mode Release (Specification change notice)

Description:

If a stand-by mode request and a wake-up event coincide with the same timing, the µC may enter the power save mode in a way that the power save mode can be released by Reset (external or internal) only.
This happens only if the stand-by mode request and the wake-up event occur within a timing window of 0.46 nsec width.

The term “stand-by mode” of the above description refers to all stand-by modes which are selected by the Power Save Control Register (PSC).
The term “wake-up event“ of the above description refers to any event which is configured to release the microcontroller from a stand-by mode. This can be any unmaskable or unmasked maskable interrupt (internal or external) except reset.

Affected stand-by modes are:
- Idle1 Mode,
- Idle2 Mode,
- Sub-Idle Mode and
- Stop Mode

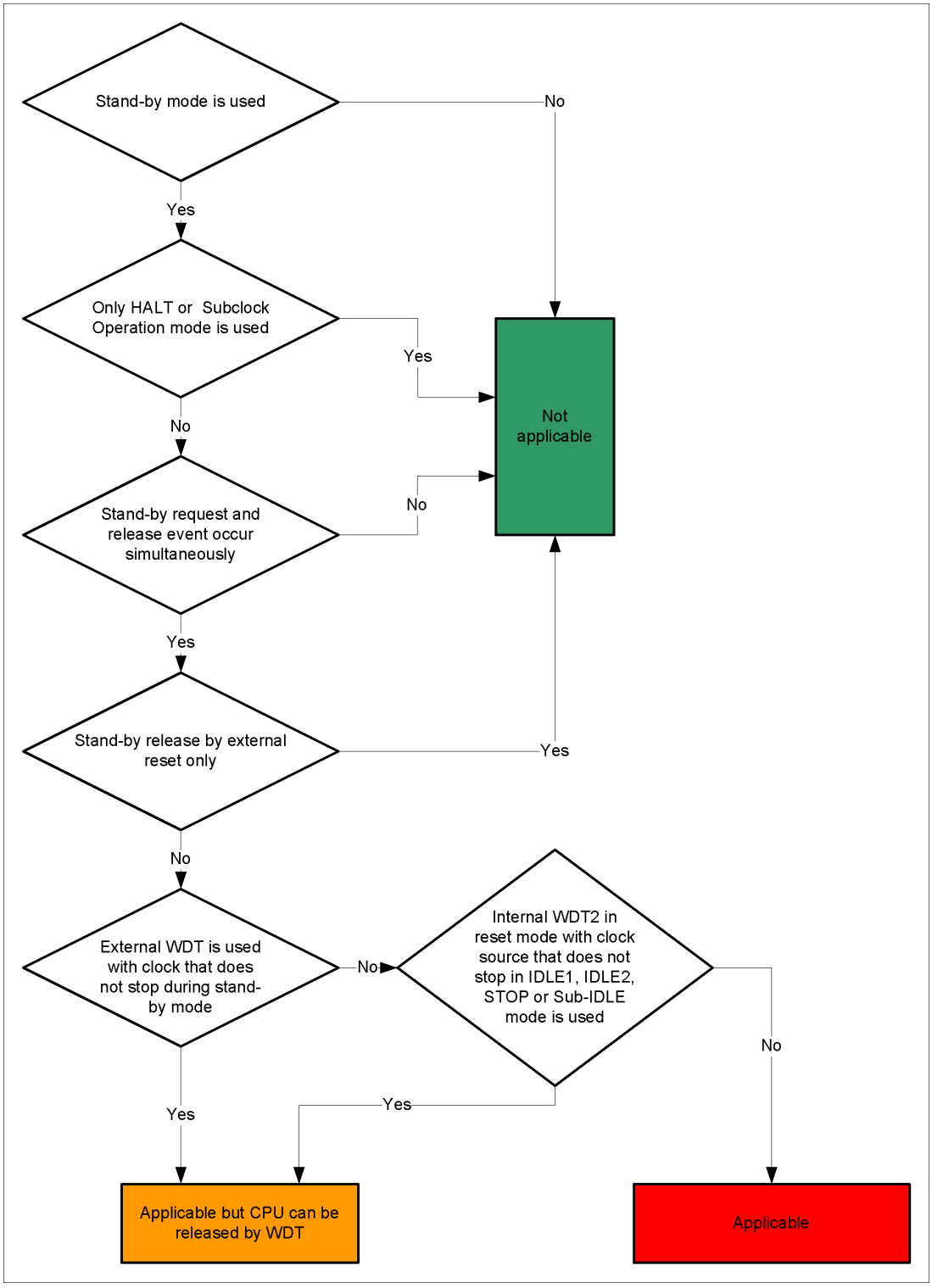
Not affected stand-by mode:
- Halt Mode

Please see the flowchart on the following page.

No. 2	Stand-by Mode Release (Specification change notice)

Description (continued):

Please see the following flowchart to check if the described behaviour might be relevant for a particular application:



No. 3	Undefined Voltage Level on Analog ports (Specification change notice)

Description:
An undefined voltage level in the range of GND to AVREF0 may be output on one of the analog ports (ANIn **NOTE**) after power-on.
In case of utilizing as I/O port functions, the undefined voltage level may be seen continuously until the next power-on.

The input or output port function may not operate as expected since the input voltage from external circuits or output voltage from the I/O port of this device may be altered due to this behaviour. Depending on the supply voltage and the external circuitry a maximum input or output current of 11.8 mA can occur (e. g. in case of supply voltage = 5.5 V and external connection to GND).

NOTE:
n = 0 to 9 for V850ES/FE2
n = 0 to 11 for V850ES/FF2
n = 0 to 15 for V850ES/FG2
n = 0 to 23 for V850ES/FJ2

Workaround:
The described behaviour disappears when the ADC is enabled at least once after power-on. Therefore the ADC should be enabled at least once even if the ADC is not used in the application. The ADC is enabled by setting the ADA0CE bit of the ADA0M0 register to 1.

(C) Valid Specification

Item	Date pulished	Document No.	Document Title
1	November 2005	U17830EE1V0UM00	V850ES/Fx2 Hardware (User's Manual)
2	December 2005	U17830EE1V0X000	Errata Sheet for V850ES/Fx2 Hardware (User's Manual)
3	November 2004	U17834EE1V0DS00	Data Sheet for V850ES/FE2
4	April 2006	U17833EE3V0DS00	Data Sheet for V850ES/FF2
5	November 2005	U17832EE1V0DS00	Data Sheet for V850ES/FG2
6	November 2005	U17831EE1V0DS00	Data Sheet for V850ES/FJ2
7	February 2010	U15943EJ4V0UM00	V850ES Architecture (User's Manual)

(D) Revision History

Item	Date pulished	Document No.	Comment
1	August 2006	TPS-HE-B-2590	New List
2	October 2006	U18385EE3V0IF00	Added item 2, added No. 7 to section “Valid Specification”
3	December 2006	U18385EE3V1IF00	Added mask rank “E”
4	May 2007	U18385EE4V0IF00	Added µPD70F323xA, µPD70323xA
5	October 2008	U18385EE5V0IF00	Added item 3
6	March 2010	U18385EE6V0IF00	Added µPD70F323xB