

# Theory of High Power Loadpull Characterization for RF and Microwave Transistors

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## Introduction

In both portable and infrastructure wireless systems the power amplifier often represents the largest single source of power consumption in the radio. While the implications of this are obvious for portable applications, manifested as talk-time, it is also important for infrastructure applications due to thermal management, locatability limitations, and main power limitations. Significant effort is devoted toward developing high-performance RF and microwave transistors and circuits to improve power amplifier efficiency. In the former case, an accurate and repeatable characterization tool is necessary to evaluate the performance of the transistor. In the latter case, it is necessary to determine the source and load impedance for the best trade-off in overall performance. Load-pull is presently the most common technique, and arguably the most useful for carrying out these tasks. In addition, load-pull is also necessary for large-signal model development and verification.

Load-pull as a design tool is based on measuring the performance of a transistor at various source and/or load impedances and fitting contours, in the gamma-domain, to the resultant data; measurements at various bias and frequency conditions may also be done. Several parameters can be superimposed over each other on a Smith chart and trade-offs in performance established. From this analysis, optimal source and load impedances are determined.

Load-pull can be classified by the method in which source and load impedances are synthesized. Since the

complex ratio of the reflected to incident wave on an arbitrary impedance completely characterizes the impedance, along with a known reference impedance, it is convenient to classify load-pull by how the reflected wave is generated.

The simplest method to synthesize an arbitrary impedance is to use a stub tuner. In contrast to early load-pull based on this method, contemporary systems fully characterize the stub tuner a priori, precluding the need for determining the impedance at each load-pull state<sup>1</sup>. This results in a significant reduction in time and increases the reliability of the system. This method of load-pull is defined as passive-mechanical. Passive-mechanical systems are capable of presenting approximately 50:1 VSWR, with respect to 50  $\Omega$ , and are capable of working in very high power environments. Repeatability is better than -60 dB. Maury Microwave and Focus Microwave each develop passive-mechanical load-pull systems<sup>2, 3</sup>. For high-power applications, e.g., > 100 W, the primary limitation of passive-mechanical systems is self-heating of the transmission line within the tuner, with the resultant thermally induced expansion perturbing the line impedance.

Solid-state phase-shifting and attenuator networks can also be used to control the magnitude and phase of a reflected wave, thereby effecting an arbitrary impedance. This approach has been pioneered by ATN Microwave<sup>4</sup>. These systems can be based on a lookup table approach, similar to the passive



mechanical systems, or can use a vector network analyzer for real-time measurement of tuner impedance. Like all passive systems, the maximum VSWR is limited by intrinsic losses of the tuner network. Passive solid-state systems, such as the ATN, typically exhibit a maximum VSWR of 20:1 with respect to 50  $\Omega$ . These systems are ideally suited for medium power applications and noise characterization (due to the considerable speed advantage over other types of architectures).

Tuner and fixture losses are the limiting factor in achieving a VSWR in excess of 50:1 with respect to 50  $\Omega$ . This would be necessary not only for characterization of high-power transistors, but also low power transistors at millimeter-wave frequencies, where system losses can be significant. In these instances, it is possible to synthesize a reflected wave by sampling the wave generated by the transistor traveling toward the load, amplifying it, controlling its magnitude and phase, and reinjecting it toward the transistor. Systems based on this method are defined as active load-pull. Although in principle active load-pull can be used to create very low impedance, the power necessary usually limits the application of this method to millimeter-wave applications<sup>5, 6</sup>. Because active load-pull systems are capable of placing any reflection coefficient on the port being pulled (including reflections greater than unity) these systems can be very unstable and difficult to control. Instability in a high-power load-pull system can lead to catastrophic failure of the part being tested.

The present chapter is devoted to discussing the operation, setup, and verification of load-pull systems used for characterization of high-power transistors used in wireless applications. While the presentation is general in that much of the discussion can be applied to any of the architectures described previously, the emphasis is on passive-mechanical systems. There are two reasons for limiting the scope. The first reason is that passive-solid-state systems are usually limited in the maximum power incident on the tuners, and to a lesser extent, the maximum VSWR the tuners are capable of presenting. The second reason is that currently there are

no active load-pull systems commercially available. Further, it is unlikely that an active load-pull system would be capable of practically generating the sub 1  $\Omega$  impedances necessary for characterization of high-power transistors.

The architecture of the passive-mechanical system is discussed first, with a detailed description of the necessary components for advanced characterization of transistors, such as measuring input impedance and ACPR<sup>7</sup>. Vector network analyzer calibration, often overlooked, and the most important element of tuner characterization, is presented next. Following this, tuner, source, and load characterization methods are discussed. Fixture characterization methods are also presented, with emphasis on use of pre-matching fixtures to increase tuner VSWR. Finally, system performance verification is considered.

## System Architecture for High Power Loadpull

**Figure 1** shows a block diagram of a generalized high-power automated load-pull system, although the architecture can describe any of the systems discussed in the previous section. Sub-harmonic and harmonic tuners are also included for characterization of out-of-band impedances<sup>8</sup>. The signal sample ports are used to measure the incident and reflected voltage waves at the source-tuner interface and the incident voltage wave at the load. The signals at each of these ports are applied to the equipment necessary to make the measurements the user desires. Each of these blocks is described subsequently.

The source block of **Figure 1** usually includes all of the components necessary for generating the signal, leveling its power, providing gate/base bias for the device under test, and providing robust sampling points for the measurement equipment. **Figure 2** shows the details of a typical source block. For flexibility and expediency in applying arbitrarily modulated signals, an arbitrary waveform generator and vector signal source are shown. The signal is

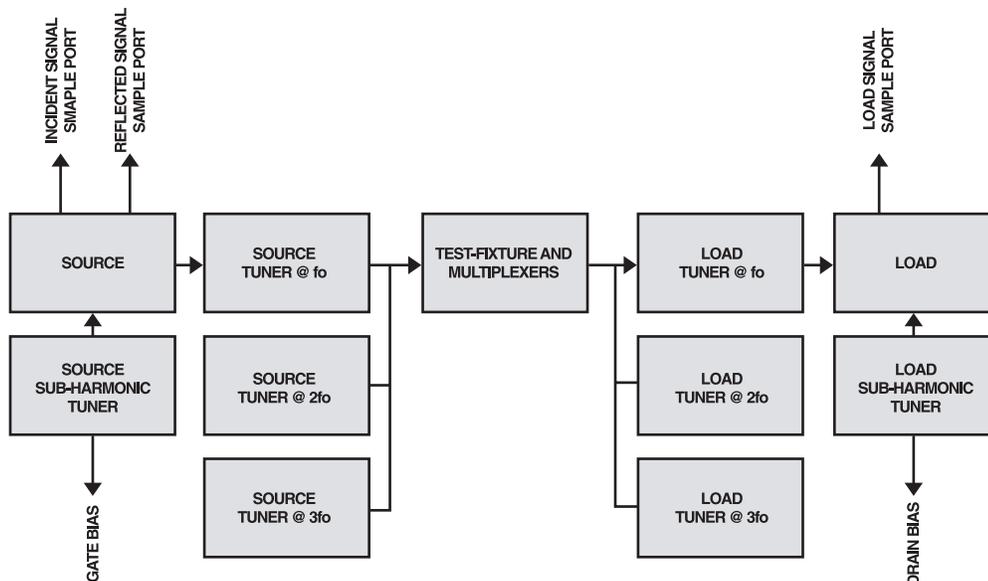


Figure 1. Block Diagram of a Generalized High-Power Loadpull System, Illustrating the Source, Tuners, Test Fixture, and Load. The Incident, Reflected, and Load Signals are Sampled at the Three Sampling Points Shown. Also Shown, Though not Necessary, are Harmonic and Sub-harmonic Tuners.

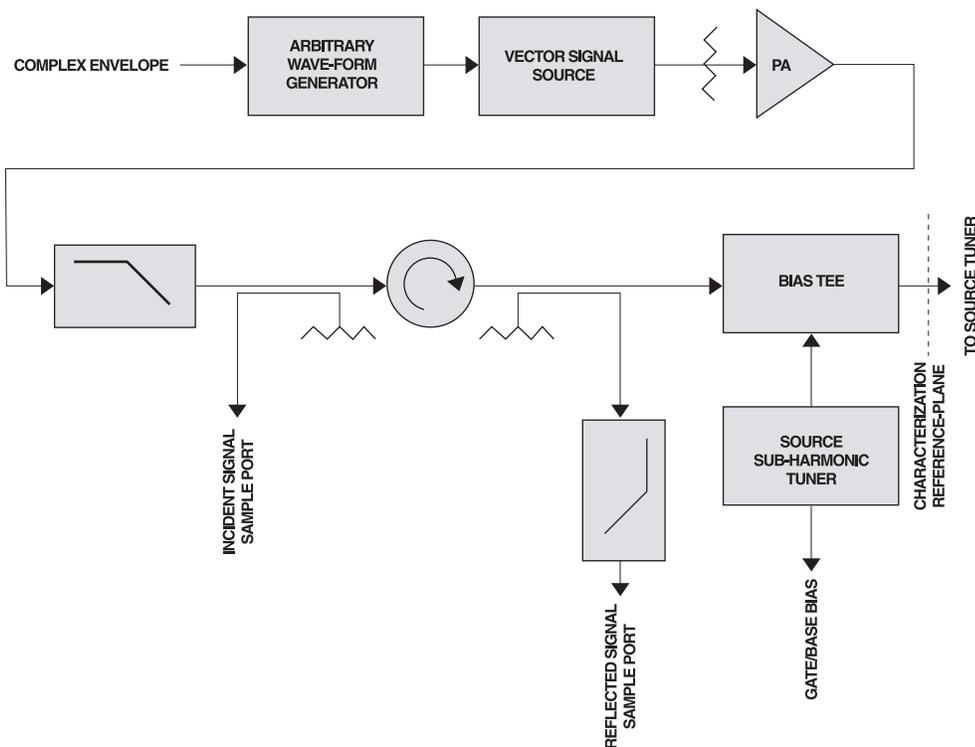


Figure 2. Detail of the Source Portion of Figure 1.



typically created using MATLAB, and can represent not only digitally modulated signals, but also the more conventional two-tone signal. The signal is applied to a reference PA, which must be characterized to ensure that it remains transparent to the DUT; for high-power applications this is often a 50 W to 100 W PA.

Following the reference PA is a low-pass filter to remove harmonics generated from the source and/or reference PA. Next are the sampling points for the incident and reflected waves, which is done with two distinct directional couplers. Since the source tuner may present a high reflection, a circulator to improve directivity separates each directional coupler; the circulator also protects the reference PA from reflected power. The circulator serves to present a power-invariant termination for the source tuner, the impedance of which is critical for sub  $1 \Omega$  load-pull. The bias-tee is the last element in the source block, which is connected to the gate/base bias source via

a low-frequency tuner network for sub-harmonic impedance control. Since the current draw of the gate/base is typically small, remote sensing of the power supply can be done directly at the bias-tee.

Although components within the source block may have type N or 3.5mm connectors, interface to the source tuner is done with an adapter to an APC7mm connector. This is done to provide a robust connection and to aid in the VNA characterization of the source block. Depending on the measurements that are to be made during load-pull, a variety of instruments may be connected to the incident and reflected sample ports, including a power meter and VNA. The former is required for real-time leveling and the latter for measuring the input impedance to the DUT<sup>9</sup>.

The load block of **Figure 1** usually includes a port for sampling the load signal of the DUT and the padding and filtering necessary to interface the load signal to a power sensor. **Figure 3** shows the details of a

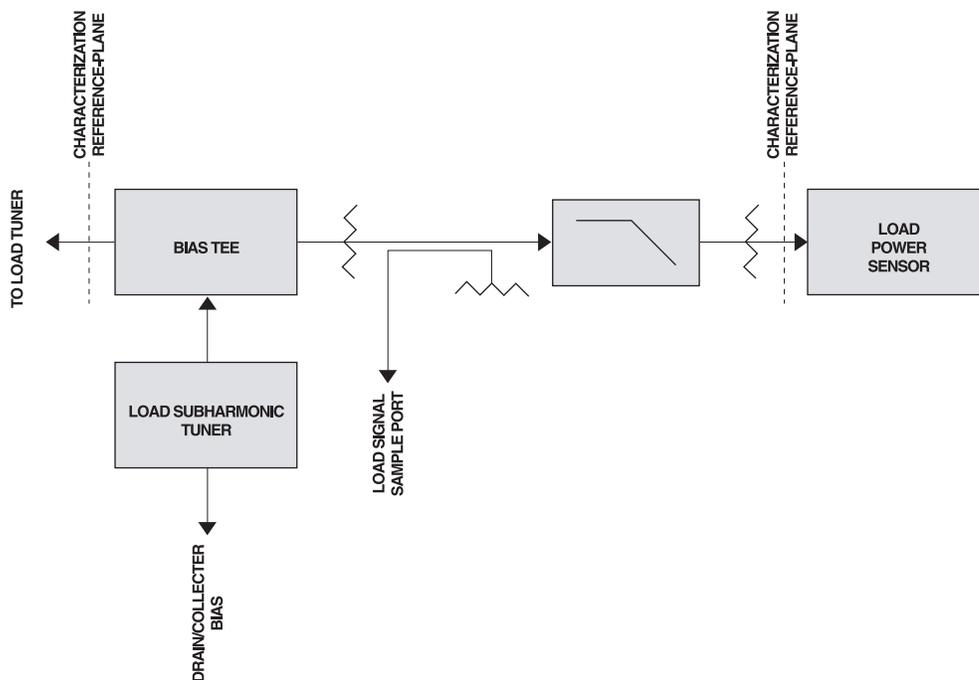


Figure 3. Detail of the Load Portion of Figure 1.



typical load block. The bias-tee comes first. Although remote-sense can be sampled here, in situations where significant current is required, the remote-sense should be sampled directly on the DUT test fixture. For a load-pull system capable of 100 W average power, the attenuator following the bias-tee should be appropriately rated and exhibit at least 30 dB attenuation.

The load signal is sampled at a directional coupler after the high-power pad. A spectrum analyzer is often connected at this port, and it may be useful to use a low coupling factor, e.g., -30 dB, to minimize the padding necessary in front of the spectrum analyzer. This results in an optimal dynamic range of the system for measuring ACPR. Following the directional coupler is a low-pass filter, to remove harmonics,<sup>1</sup> which is followed by another attenuator. This attenuator is used to improve the return loss of the filter with respect to the power sensor. As with the source block, interface to the load tuner and power sensor are done with APC7mm connectors to improve robustness and power-handling capability.

The DUT test-fixture is used to interface the source and load tuners to a package. For cost and package de-embedding reasons, it is useful to standardize on two or three laboratory evaluation packages. For hybrid circuit design, it is useful to design a test fixture with feeds and manifolds identical to those used in hybrid to mitigate de-embedding difficulties. The collector/drain side of the test fixture should also have a sampling port for remote sensing of the power supply.

After the load-pull system has been assembled, it is recommended that the maximum expected power be applied to the system and changes in impedance be measured due to tuner self-heating. This may be significant where average powers exceed 100 W or peak powers exceed several hundred watts. Any impedance change will establish the upper power limit of the system with respect to impedance accuracy.

## **Characterization of System Components**

Each of the blocks described in the previous section must be characterized using s-parameters in order for a load-pull system to function properly. In this section, the characterization procedure for each of the sections of **Figure 1** is described, with emphasis on calibration of the vector network analyzer and the characterization of the transistor test fixture. Two-tier calibration and impedance re-normalization are considered for characterizing quarter-wave pre-matching test fixtures.

### **Vector Network Analyzer Calibration Theory**

Due to the extremely low impedances synthesized in high-power loadpull, the vector network analyzer (VNA) calibration is the single most important element of the characterization process. Any errors in the measurement or calibration, use of low quality connectors, e.g., SMA or type N, or adoption of low performance calibration methods, e.g., SOLT, will result in a significant reduction in accuracy and repeatability. Only TRL calibration should be used, particularly for tuner and fixture characterization. Use of high-performance connectors is preferred, particularly APC7mm, due to its repeatability, power handling capability, and the fact that it has a hermaphroditic interface, simplifying the calibration process.

Vector network analysis derives its usefulness from its ability to characterize impedance based on ratio measurements, instead of absolute power and phase measurements, and from its ability to characterize and remove systematic errors due to nonidealities of the hardware. For a complete review of VNA architecture and calibration theory, the reader is encouraged to review notes from the annual ARFTG Short-Course given in November of each year<sup>10, 11</sup>.

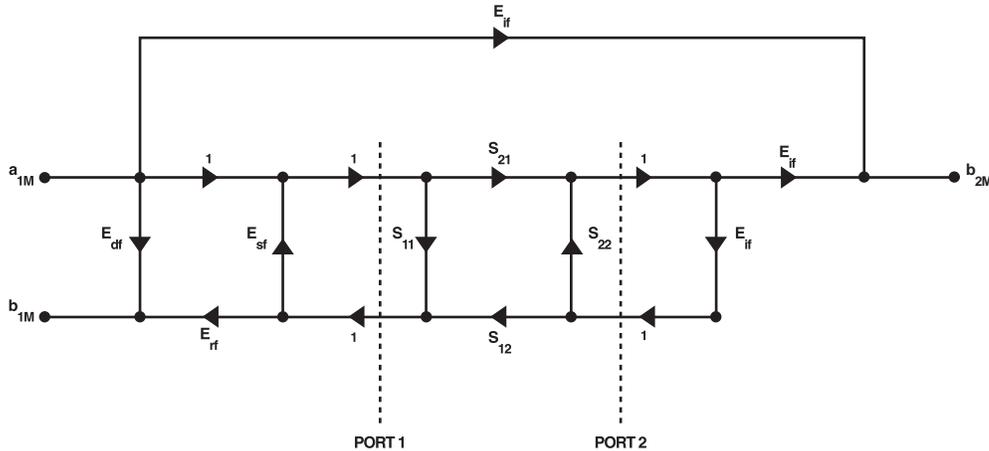


Figure 4. Signal Flow Graph of the Forward Direction of a Typical VNA.

Figure 4 shows a signal-flow graph of the forward direction of a common VNA architecture, where six systematic error terms are identified. An identical flow-graph exists for the reverse direction, with six additional error terms. Consider the situation where it is required to measure an impedance that exhibits a near total reflection, such as a load tuner set for  $1 \Omega$ . Assuming a  $50 \Omega$  reference impedance, nearly all of the incident power is reflected back toward the VNA, along with a phase shift of  $180^\circ$ . Consider what happens when the reflected wave is sampled at the VNA, denoted as  $b_{1M}$  in Figure 4. If there is any reflection of the reflected wave incident at the VNA, an error will occur in measuring the actual impedance of the load. The ability of a VNA to minimize this reflected power is characterized by its residual source match, which is the corrected source impedance looking into the VNA. The uncorrected source impedance looking into the VNA is characterized by the  $E_{sr}$  term in the flow graph of Figure 4.

Continuing with this example, Figure 5 shows a plot of the upper bound on apparent load impedance versus the residual source match (with respect to a reference impedance of  $50 \Omega$  and an actual impedance of  $1 \Omega$ ). For simplicity, it is assumed that the residual source match is in phase with the reflected signal.

Also shown are typical residual source match performance numbers for an HP8510C using an

HP8514B test set. From this graph it is clear that use of low-performance calibration techniques will result in latent errors in any characterization performed using a DUT with reflection VSWR near 50:1. Using a 3.5 mm SOLT calibration can result in nearly 20% uncertainty in measuring impedance. Note that TRL\*, the calibration method available on low-cost VNAs, offers similar performance to 3.5 mm SOLT, due to its inability to uniquely resolve the test-set port impedances. This limitation is due to the presence of only three samplers instead of four, and does not allow switch terms to be measured directly. For this reason, it is recommended that three-sampler architectures not be used for the characterization process.

Similar arguments can be made for the load reflection term of Figure 4, which is characterized by the residual load match error term. Identical error terms exist for the reverse direction too, so that there are a total of four error terms that are significant for low impedance VNA calibration.

TRL calibration requires a thru line, a reflect standard (known only within  $\lambda/4$ ), and a delay-line. The system reference impedances will assume the value of the characteristic impedance of the delay-line, which if different from  $50 \Omega$ , must be appropriately re-normalized back to  $50 \Omega$ <sup>12, 13, 14, 15</sup>. TRL calibration can be done in a variety of media, including APC 7 mm coaxial waveguide, rectangular/cylindrical

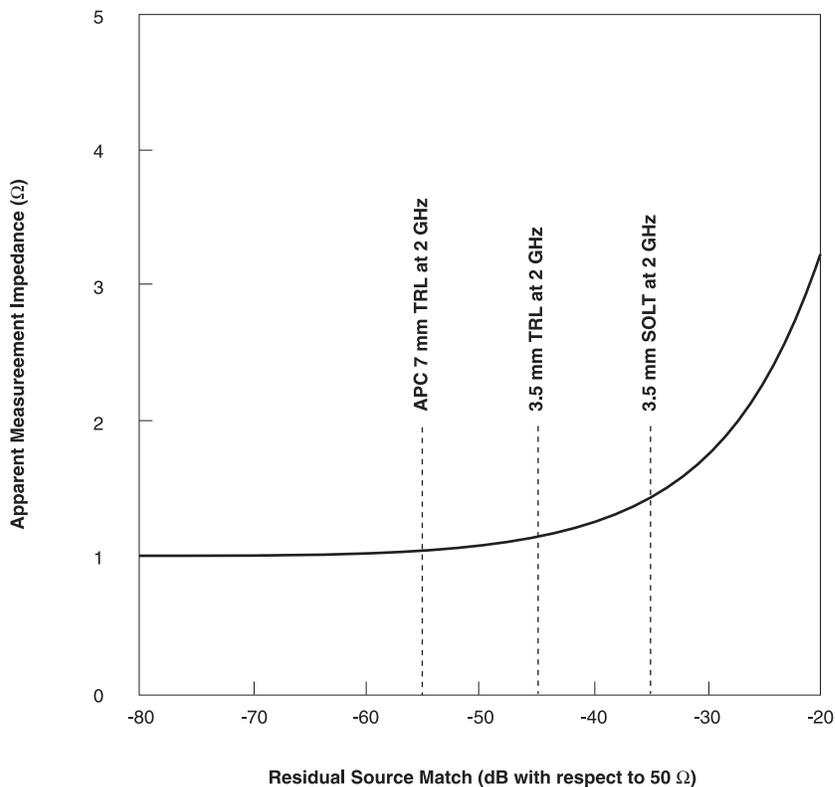


Figure 5. The Influence of Residual Source Match on the Ability of a VNA to Resolve a 1 Ω Impedance with a 50 Ω Reference Impedance. The Calibration Performance Numbers are Typical for an HP 8510C with an 8514B Test Set Operating a 2 GHz.

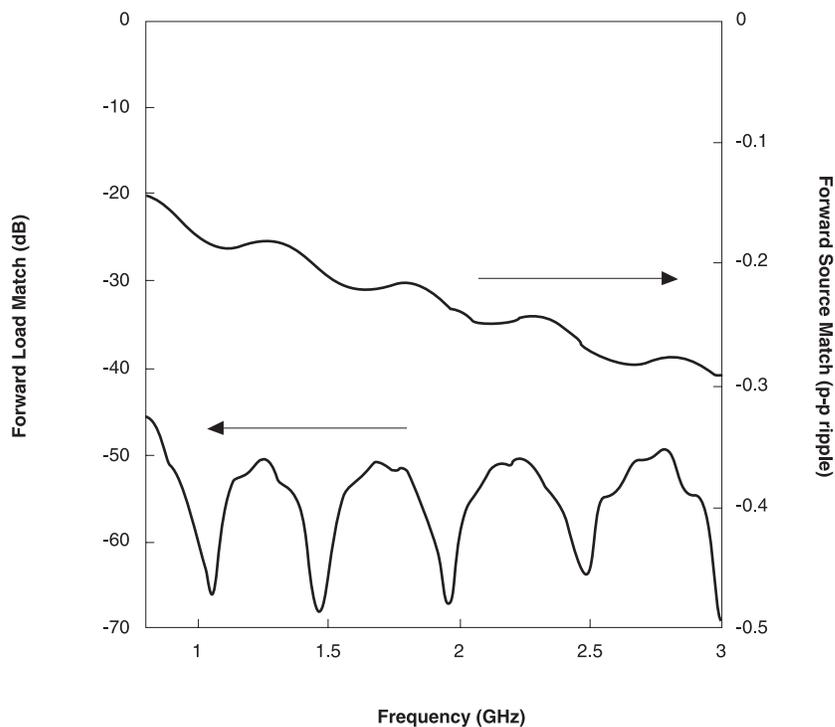


Figure 6. Typical Response of an APC7mm TRL Calibration Using an Offset Short and Delay Line to Extract Source Match and Load Match, Respectively. This Data was Taken from an HP 8510C with an HP 8514B Test Set.



waveguide, microstrip, and stripline. Calibration verification standards, which must be used to extract the residual error terms described above, are also easily fabricated. **Figure 6** shows the residual forward source and load match response of an APC 7mm calibration using an HP8510C with an HP8514B test set. These were obtained with a 30 cm offset-short airline and 30 cm delay-line, respectively<sup>16,17,18</sup>. The effective source match is computed from the peak-peak ripple using

$$E_{sf} = 10 * \log_{10} \left[ \frac{1 - 10^{-\frac{p-p \text{ ripple}}{20}}}{1 - 10^{-\frac{p-p \text{ ripple}}{20}}} \right] \quad (4.47)$$

where it is seen that better than -53 dB source match is obtained across the band. Due to finite directivity, 6 dB must be subtracted from the plot showing the delay-line response, indicating that better than -56 dB load match is obtained except near the low end of the band. Calibration performance such as that obtained in **Figure 6** is necessary for accurate tuner and fixture characterization, and is easily achievable using standard TRL calibration.

For comparison purposes, **Figures 7** and **8** show forward source and load match for 3.5 mm TRL and SOLT calibration, respectively. Here it is observed that the source match of the 3.5 mm TRL calibration has significantly degraded with respect to the APC 7 mm TRL calibration and the 3.5 mm SOLT calibration has significantly degraded with respect to the 3.5 mm TRL calibration.

Proper VNA calibration is an essential first step in characterization of any component used for high power load-pull characterization, and is particularly important for tuner and fixture characterization. All VNA calibrations should be based on TRL and must be followed by calibration verification to ensure that the calibration has been performed properly and is exhibiting acceptable performance, using the results of **Figure 6** as a benchmark. Averaging should be set to at least 64. Smoothing should in general be turned off in order to observe any resonances that might

otherwise be obscured. Although APC 7 mm is recommended, 3.5 mm is acceptable when used with a TRL calibration kit. Under no circumstances should type-N or SMA connectors be used, due to phase repeatability limitations and connector reliability limitations.

## ***S-parameter Characterization of Tuners***

Tuner characterization begins with proper calibration of the VNA, as described in the previous section.

It is suggested at this point that any adapters on the tuner be serialized and alignment marks made to ensure that in the event of removal, they can be replaced in their original positions. Replacement of an adapter, for any reason, will require a new tuner characterization. Tuners should be leveled using a bubble level and should be positioned such that the VNA test-port cables are not flexed. Proper torquing of all connector interfaces is essential. Since the tuner files usually consist of a small number of frequencies with respect to the number of frequencies present in a typical VNA calibration, it is appropriate to increase the number of averages to 128 or 256.

It is generally most useful to characterize a tuner without any additional components attached, such

as a bias-tee, in order to maintain maximum flexibility in the use of the tuner subsequent to the characterization. For tuners that are being characterized for the first time, it is recommended that they be fully evaluated for insertion loss, minimum and maximum VSWR, and frequency response to ensure they are compliant with the manufacturer's specifications.

After characterization the tuner file should be verified by setting the tuner for arbitrary impedances near the center and edge of the Smith chart over  $2\pi$  radians. The error should be less than 0.2% for magnitude and 0.1° for phase. Anything worse than this may indicate a problem with either the calibration (verify it again) or the tuner.

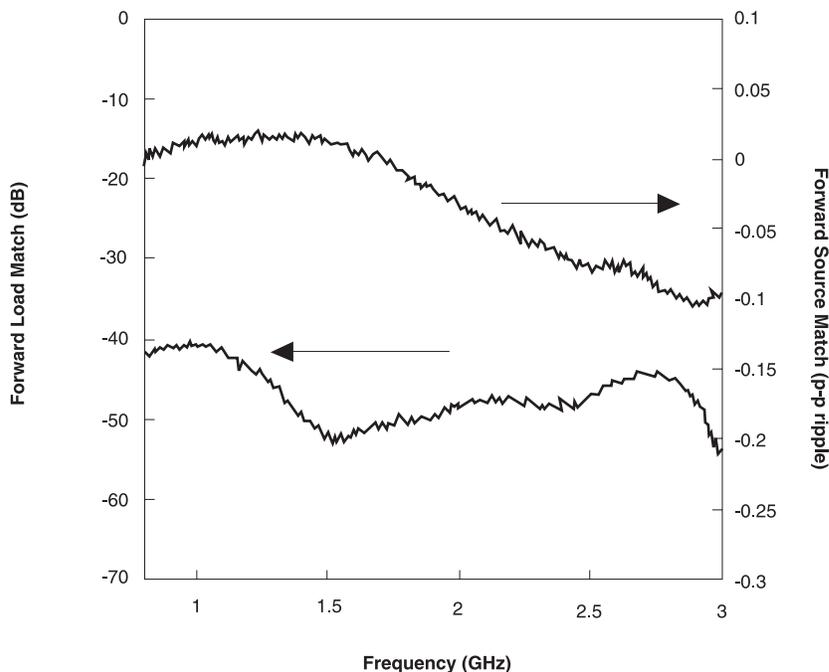


Figure 7. Typical Response of a 3.5mm TRL Calibration Using an Offset Short and Delay Line to Extract Source Match and Load Match, Respectively. This Data was Taken From an HP 8510C with an HP 8514B Test Set.

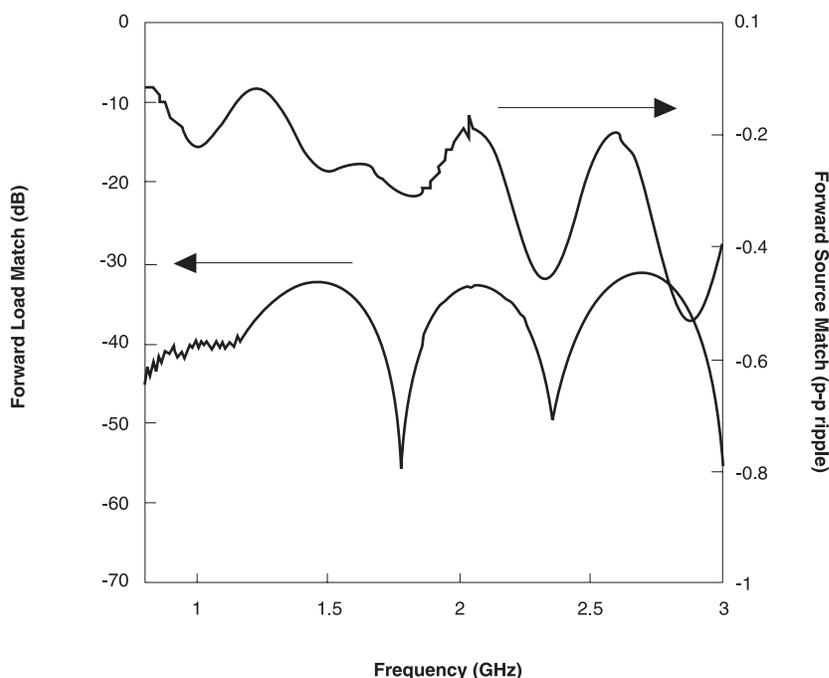


Figure 8. Typical Response of a 3.5mm SOLT Calibration Using an Offset Short and Delay Line to Extract Source Match and Load Match, Respectively. This Data was Taken from an HP 8510C with an HP 8514B Test Set.



## S-parameter Characterization of System Components

Characterization of system components consists of creating one-port and two-port s-parameter files of the source block and load block, as shown in **Figures 1 and 2**, respectively. Each of these figures show suggested reference-planes for characterization of the network. Since the reflection coefficient of each port of the source and load blocks is in general small with respect to that exhibited by tuners, the VNA3 calibration is not as critical<sup>2</sup> as it is for tuner characterization. Nevertheless, it is recommended to use the same calibration as used for the tuner characterization and to sweep a broad range of frequencies to eliminate the possibility of characterization in the future at new frequencies.

If possible, each component of the source and load blocks should be individually characterized prior to integration into their respective block. This is particularly so for circulators and high-current bias tees, which tend to have limited bandwidth. The response of the source and load block should be stored for future reference and/or troubleshooting.

## Fixture Characterization to Increase System VSWR

In the beginning of this section it was indicated that high-power load-pull may require source and load impedances in the neighborhood of  $0.1 \Omega$ . This does not mean that the DUT may require such an impedance as much as it is necessary for generating closed contours, which are useful for evaluation of performance gradients in the gamma domain. A very robust and simple method of synthesizing sub  $1 \Omega$  impedances is to use a quarter-wave pre-matching

network characterized using numerically well-defined two-tier calibration methods. To date, use of quarter-wave pre-matching offers the lowest impedance, though it is limited in flexibility due to bandwidth restrictions. Recently, commercially available passive mechanical systems cascading two tuners together have been made available offering octave bandwidths, though they are not able to generate impedances as low as narrow band quarter-wave pre-matching. In this section, a robust methodology for designing and characterizing a quarter-wave pre-matching network capable of presenting  $0.1 \Omega$  at 2 GHz is described<sup>16,18</sup>. It is based on a two-tier calibration with thin film gold on alumina substrates (quarter-wave pre-matching networks on soft substrates are not recommended due to substrate variations and repeatability issues over time).

The theory of quarter-wave pre-matching begins with the mismatch invariance property of lossless networks<sup>19</sup>. Consider the quarter-wave line of characteristic impedance  $Z_{ref}$  shown in **Figure 9**. This line is terminated in a mismatch of VSWR<sub>load</sub> with an arbitrary phase. The reference impedance of VSWR load is  $Z_L$ . The mismatch invariance property of lossless networks shows that the input VSWR is identical to the load VSWR, but it is with respect to the quarter-wave transformed impedance of  $Z_L$ . Thus, the minimum achievable impedance, which is real valued, is the impedance looking into the quarter-wave line when it is terminated in  $Z_L$  divided by VSWR load. This is expressed as

$$R_{in,min} = \frac{Z_{ref}^2}{Z_L \cdot VSWR_{load}} \quad (4.48)$$



**Figure 9. Network to Describe the Mismatch Invariance Property of Lossless Networks.**



Suppose it is desired to synthesize a minimum impedance of  $0.1 \Omega$ , which might be required for characterizing high power PCS and UMTS LDMOS transistors. If a typical passive-mechanical tuner is capable of conservatively generating a 40:1 VSWR, then the input impedance of the quarter-wave line must be approximately  $4 \Omega$ , requiring the characteristic impedance of the quarter-wave line to be approximately  $14 \Omega$ , assuming a  $Z_L$  of  $50 \Omega$ . To the extent that the minimum impedance deviates from the ideal is directly related to fixture losses. Thus, the importance of using a low-loss substrate and metal system is apparent.

Full two-port characterization of each fixture side is necessary to reset the reference plane of each associated tuner. Several methods are available to do this, including analytical methods based on approximate closed-form expressions, full-wave analysis using numerical techniques, and employment of VNA error correction techniques<sup>20, 21, 22</sup>. The first method is based on approximations that have built-in uncertainty, as does the second method, in the form of material parameter uncertainty. The third method is entirely measurement based, and relies on well-behaved TRL error correction mathematics to extract a two-port characterization of each fixture half from a two-tier calibration. More importantly, using verification standards, it is possible to quantify the accuracy of the de-embedding, as described in the section on VNA calibration.

Using the error-box formulation of the TRL calibration it is possible to extract the two-port characteristics of an arbitrary element inserted between two reference planes of two different calibrations<sup>11</sup>. The first tier of the calibration is usually done at the test-port cables of the VNA. The second tier of the calibration is done in the media that matches the implementation of the test fixture, which is usually microstrip. **Figure 10** illustrates the reference-plane definitions thus described. The second tier of the calibration will have its reference

impedance set to the impedance of the delay standard, which is the impedance of the quarter-wave line. Although there are many methods of determining the characteristic impedance of a transmission line, methods based on estimating the capacitance per unit length and phase velocity are well suited for microstrip lines<sup>12, 15</sup>. The capacitance per unit length and phase velocity uniquely describe the quasi-TEM characteristic impedance as

$$Z_0 = \frac{1}{v_p C} \quad (4.49)$$

Once the characteristic impedance of the delay-line is known, the s-parameters can be re-normalized to  $50 \Omega$  to make them compatible with the  $50 \Omega$  reference impedance that most automated load-pull systems use<sup>2, 3, 15</sup>.

**Figure 11** shows the forward source and load match of the second tier microstrip calibration used in the pre-matching fixture described in References 16 and 18. This fixture was intended to present  $0.1 \Omega$  at 2 GHz with extremely high accuracy. From the verification data, the resultant source match is better than  $-45$  dB across the band and the resultant load match is better than  $-52$  dB across the band. Comparing these results with **Figure 5** shows that the uncertainty is very low.

A significant advantage of using a transforming network to increase system VSWR, whether it be a quarter-wave line or an additional cascaded tuner, is that the two-port characterization of each element is done at manageable impedance levels. Characterization of a tuner presenting a 50:1 VSWR in direct cascade of a quarter-wave pre-match network would result in a significant increase in measurement uncertainty since the VNA must resolve impedances near  $0.1 \Omega$ . Segregating the characterization process moves the impedances that must be resolved to the  $1 \Omega$  to  $2 \Omega$  range, where the calibration uncertainty is considerably smaller.

The final step of the fixture verification process is to verify that the two-tier calibration has provided the

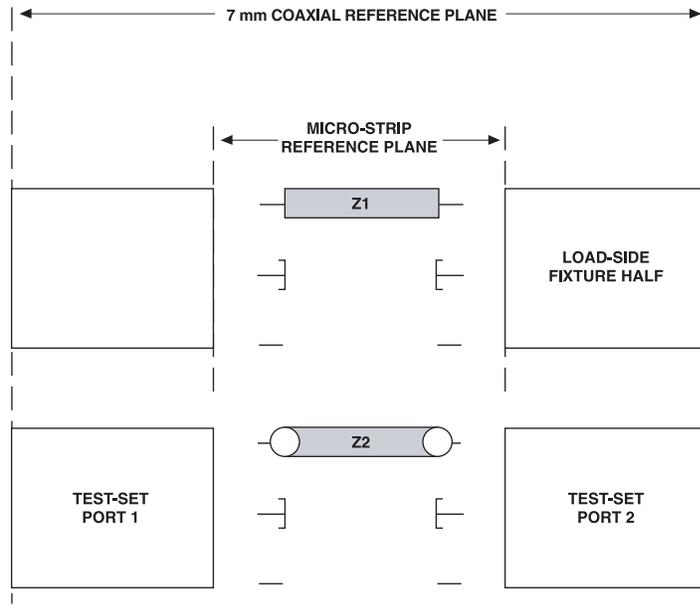


Figure 10. Reference Plane Definitions for a Two-tier Calibration used for Fixture Characterization. The First Tier is based on a TRL APC7mm Calibration and the Second Tier is based on a Microstrip TRL Calibration.

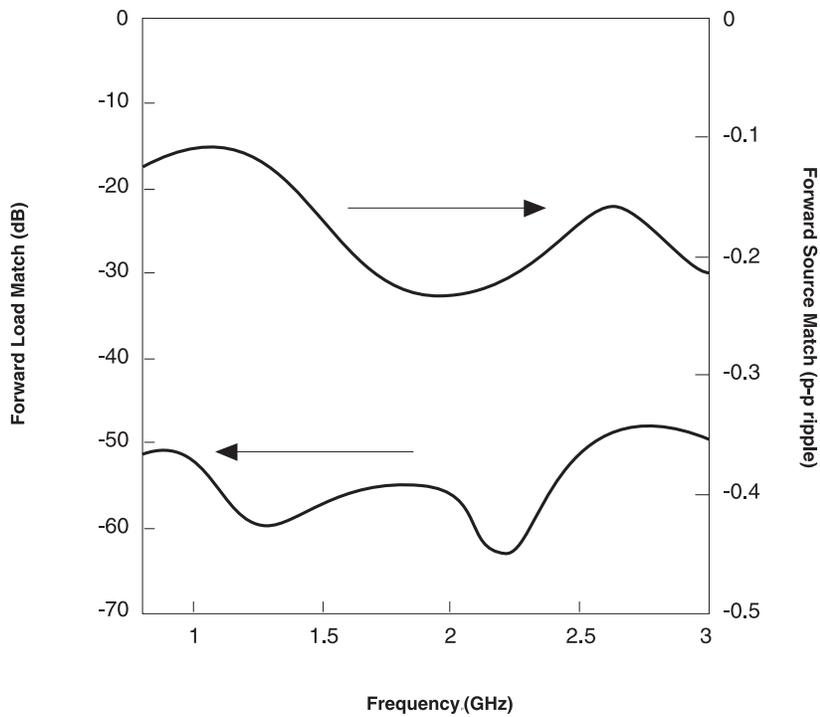
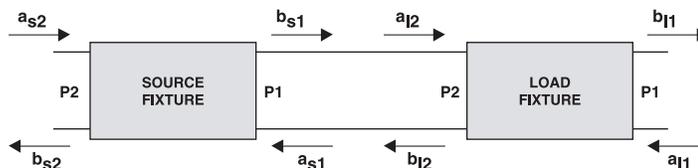


Figure 11. Microstrip TRL Calibration Using an Offset Short and Delay Line to Extract Source Match and Load Match, Respectively. This Data was taken from an HP 8510C with an HP 8514B Test Set.



**Figure 12. Port and Traveling Wave Definitions for Cascading the Source Fixture and Load Fixture to Examine the Accuracy of the Two-tier Calibration Fixture Characterization.**

correct two-port s-parameter description of each fixture half **Figure 12** shows each fixture half cascaded using the port definitions adopted by NIST Multical™<sup>15</sup>. With microstrip, an ideal thru can be approximated by butting each fixture half together and making top-metal contact with a thin conductive film. When this is not possible, it is necessary to extract a two-port characterization of the thru. The cascaded transmission matrix is expressed as

$$\begin{bmatrix} A_{11} & B_{12} \\ C_{21} & D_{22} \end{bmatrix}_{\text{cascade}} = \begin{bmatrix} A_{11} & B_{12} \\ C_{21} & D_{22} \end{bmatrix}_{\text{source}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}_{\text{thru}} \begin{bmatrix} A_{11} & B_{12} \\ C_{21} & D_{22} \end{bmatrix}_{\text{load}} \quad (4.50)$$

where the middle matrix of the right-hand side is the transmission matrix of a lossless zero phase-shift thru network. Converting the cascade transmission matrix back to s-parameter form yields the predicted response of the cascaded test-fixture, which can then be compared to the measurements of the cascade provided by the VNA.

**Figure 13** shows the measured and predicted cascade magnitude response of a typical PCS quarterwave pre-matching fixture based on an 11 Ω quarter-wave line; the phase is shown in **Figure 14**<sup>16, 18</sup>. The relative error across the band is less than 0.1%. This type of fixture characterization performance is necessary to minimize error for synthesizing sub 1 Ω impedances.

## System Performance Verification

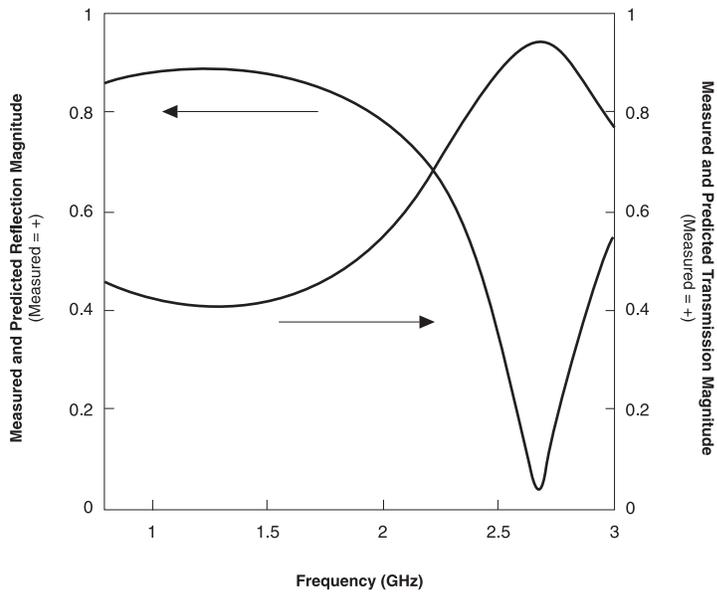
Just as verification of VNA calibration is essential, so too is verification of overall load-pull system performance essential. Performance verification can be done with respect to absolute power or with

respect to power gain. The former is recommended only occasionally, for example when the system is assembled or when a major change is made. The latter is recommended subsequent to each power calibration. Each of the methods will be described in this section.

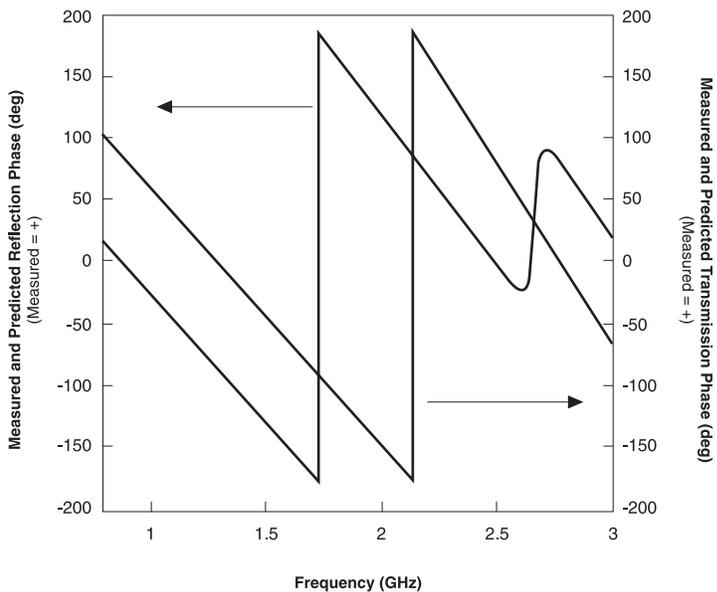
Absolute power calibration is done by applying a signal to the source tuner via the source block of **Figure 2**. After appropriately padding a power sensor, it is then connected to DUT side of the source tuner and, with the tuners set for 1:1 transformation, the resultant power is compared to what the overall cascaded response is expected to be.

This procedure is repeated for the load tuner except that the signal is injected at the DUT side of the load tuner and the power sensor is located as shown in **Figure 3**. Splitting this verification in two steps assists in isolating any issues with either the source or load side. It is also possible to vary the impedance of each tuner and calculate what the associated available gain or power gain is, although this step is more easily implemented in the power gain verification.

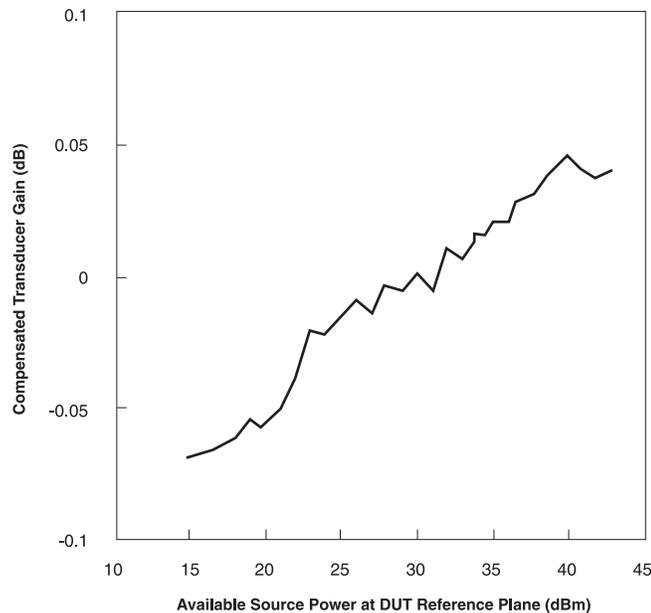
Power gain verification starts with a two-port characterization of a known mismatch standard. The simplest way to implement this standard is to use one of the tuners, and then set the other tuner for the conjugate of this mismatch. In this case, the mismatch standard is an ideal thru, similar to the one used in fixture verification described in the previous section. Since it is unlikely that both the source and load tuners would have identical impedance domains, the



**Figure 13. Forward Reflection and Transmission Magnitude Comparison of Measured and Cascaded Fixture Response. The Error is so Small the Curves Sit on Top of Each Other.**



**Figure 14. Forward Reflection and Transmission Phase Comparison of Measured and Cascaded Fixture Response. The Error is so Small the Curves Sit on Top of Each Other.**



**Figure 15. Measured Transducer Gain under the Condition of Conjugate Match with Mismatch Loss Compensation Included.**

measured loss must be compensated to arrive at actual loss. To compensate for this, the mismatch loss is computed as

$$G_{mm} = 10 \log_{10} \left[ \frac{\left( (1 - |\Gamma_s|^2) (1 - |\Gamma_l|^2) \right)}{|1 - \Gamma_s \Gamma_l|^2} \right] \quad (4.51)$$

where  $\Gamma_s$  and  $\Gamma_l$  are the source and load reflection coefficients, respectively, looking back into each tuner. **Figure 15** shows a typical response of an entire cascade, including the quarter-wave pre-matching network. A transducer gain response boundary of +0.1 dB is typical, and +0.2 should be considered the maximum.

## Summary

Load-pull is a valuable tool for evaluating high-power RF and microwave transistors, designing power amplifiers, and verifying large-signal model performance and validity domains. To enhance the reliability of the data that a load-pull system provides, it is essential that high performance VNA calibration techniques be adopted. Further, as emphasized in the present section, treating each section of the

loadpull separately is useful from a measurement perspective and from a problem resolution perspective. In the former case, it was shown that measuring quarter-wave pre-matching networks and tuners separately reduces the uncertainty of the calibration. In the latter case, it was shown that characterization of each section individually allows its performance to be verified prior to integrating it within the entire system.

The central theme of this section has been the VNA and its associated calibration. Due to the extremely low impedances synthesized in high-power loadpull, the VNA calibration is the single most important element of the characterization process. Any errors or uncertainty encountered in the VNA calibration will be propagated directly into the loadpull characterization files and may result in erroneous data, particularly if system performance verification is not performed.

To present the sub 1  $\Omega$  impedances necessary for evaluation of high-power transistors, transforming networks are required. These can be implemented using an impedance transforming



network, such as a quarter-wave line, or by cascading two tuners together. The former offers the highest VSWR at the expense of narrow bandwidth, while the latter is in general more flexible. In either case, high performance and reliable characterization methods are necessary to attain the best possible results for using loadpull as a verification and design tool.

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Kerry Burger (Philips), Mike Majerus (Motorola), and Gary Simpson and Jon King (Maury Microwave) have, in many ways, influenced the content of this section. Their support and friendship is happily acknowledged.

## Notes

- <sup>1</sup> Although a filter is not necessary, characterization of a DUT in significant compression will result in the average power detected by the power sensor including fundamental and harmonic power terms. When the DUT is embedded into a matching network, the matching network will usually attenuate the harmonics; thus, inclusion of the low pass filter more closely approximates the performance that will be observed in practice.
- <sup>2</sup> If the magnitude of the reflection coefficient approaches the residual directivity of the VNA calibration, then errors may occur.

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