PLL Frequency Synthesizer Evaluation Kit

PE3291-EK

User's Manual

Table of Contents

Peregrine Semiconductor Corp. Life Support Policy

Peregrine Semiconductor Corp. products are not intended for use in life-critical situations, or as critical components in life-support devices or systems.

Life-support devices or systems are defined as devices or systems that are intended for surgical implant into the body, or that support or sustain life, and whose failure to perform when used in accordance with the instructions provided by the manufacturer, might result in injury to the user.

This device is intended for use only in a research and development environment. It has not been tested for compliance with FCC regulations regarding interference with radio frequency energy. It might cause harmful interference with radio communications. The user assumes responsibliity for any interference caused by this device.

General Design Considerations for the PE3291 Evaluation Kit

The PE3291-EK is a self contained dual PLL synthesizer on a 3.1″ x 3.1″ surface mount circuit board. Externally it requires only power supplies, a reference frequency source and a three-wire serial data programmer to make an operating dual frequency synthesizer. The board demonstrates the features and superior performance provided by Peregrine's unique PLL topology and UTSi process. The combination of superior phase noise and outstanding spurious output levels are achieved by the incorporation of on-chip spurious compensation circuitry within a low noise fractional-N architecture. The UTSi process, with its insulating substrate, provides excellent isolation between the two PLLs on the chip. The technology also minimizes current consumption by allowing the user to choose the optimal trade off between speed and power.

The PE3291 has internal fractional spurious compensation. This compensation along with a standard second order loop filter should limit the fractional spurs to -70 dBc or less. The compensation requires no external components, tuning, or software commands. No special circuit or layout features are needed on the demonstration board to fully utilize the fractional spur compensation. The fractional spur compensation may cause stability problems if loop bandwidths of more than 10% of the step size are used. The loop filter is a standard second order passive filter, keeping in mind that N is calculated using the output frequency divided by the comparison frequency, not the output frequency divided by the step size. Example: for f_{out} = 950 MHz, $f_{compare}$ = 800 KHz, and f_{step} = 25 KHz, we have N = 950 / 0.8 = 1187.5. Pads are provided on the board for installing additional components to make a 3rd order loop filter if desired.

Special layout features are employed in the PE3291 demonstration board to maximize the isolation between sections allowed by the fully insulating substrate of the PE3291. The power supplies for the two VCOs are isolated and brought out to separate pins on the board. This provides additional isolation and allows use of common 3 or 5 volt VCOs with the 3.6 volt maximum PE3291.

The outputs of the VCOs and the reference frequency input are via SMA jacks. The power supply inputs are configured for standard .100″ center header pins. A test point is set for the f_oLD output which can be connected to a SMA jack through a jumper.

Applications Support

If you have a problem with your evaluation kit or the software, or if you have applications questions, call (858) 455-0660 and ask for Applications Support. You may also contact us by fax or e-mail:

Fax   (858) 455-0770

E-Mail   help@peregrine-semi.com

FCC Labeling Requirement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Hardware Installation

Equipment Needed

Computer
- Intel CPU or equivalent (386 or later)
- 640 kB RAM
- Microsoft Windows 95/98
- Parallel port (LPT1)
- Mouse (Microsoft or compatible)

Power Supply
- 3 VDC at 3 mA or less for PLL
- 5 VDC at 31mA for VCO2
- 4.5 VDC at 7 mA for VCO1

Test Equipment
- Spectrum analyzer: HP 8561E or similar (phase noise and spurious output measurement)

CAUTION: The PE3291-EK circuit contains components that might be damaged by exposure to voltages in excess of the specified supply voltage including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals or signal inputs or outputs.

Setting Up Hardware

The primary test setup uses a spectrum analyzer to measure center frequency, output power, spurious outputs, crosstalk and phase noise. The configuration used to test the PE3291-EK at our facility is shown in Figure 1. The detailed connections are shown in Figures 2 and 3. The board layout is shown in Figure 4 and Figure 5 for PE3291 in BCC package and in TSSOP package, respectively.
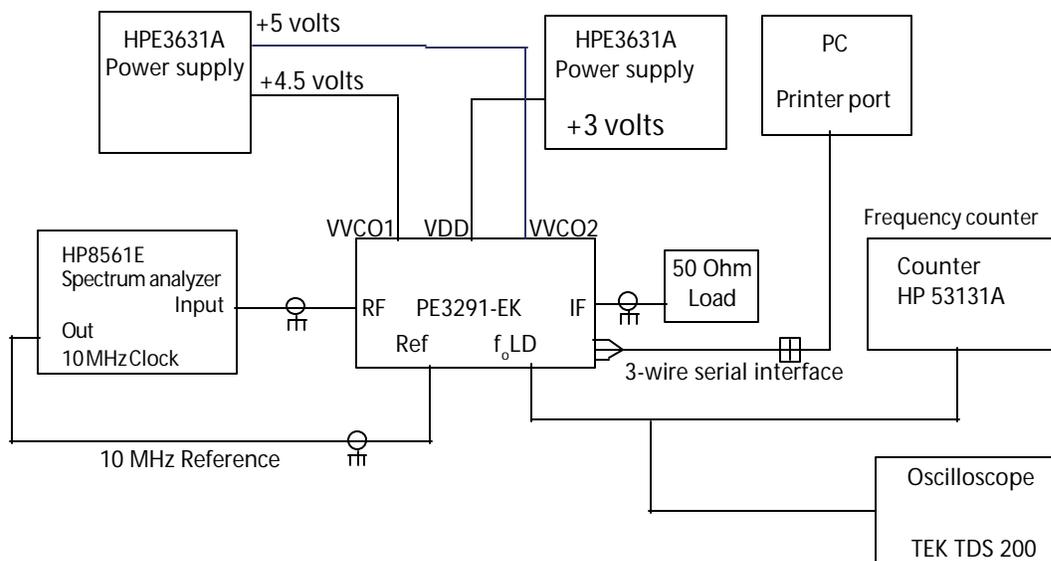

Figure 1: PE3291 Evaluation Board Test Configuration

Connecting Power Supplies and Test Equipment

Connect the PE3291-EK to suitable power supplies as shown in Figs. 2 and 4. The VDD to the PE3291 will require +3 volts. Although the Vvco1 VDD will require +3.8 volts only, the actual supply will be 4.5 volts to compensate the voltage drop across a 100-Ohm resistor in the power supply line. The Vvco2 supply will be +5 volts for the recommended VCOs. Connection can be made using dedicated wires soldered into the supply holes or polarized pin plugs as called out in the parts list.

Since the internally generated biases are used to power the prescalers, Pins 6 (VDD1) and 15 (VDD2) must be grounded or connected to VDD. Grounding has been done by soldering a jumper of (0 ohm resistor) at C9 and C12 pads in this EK board.

When using a 5 volt VCO, note that the maximum tuning voltage from the PE3291 will be 2.5 volts, and the tuning range of the VCO will be restricted on the high frequency end of the specified frequency range of the VCO.

Connect the PE3291-EK to a spectrum analyzer or frequency counter using coaxial cable as shown in Fig. 2.
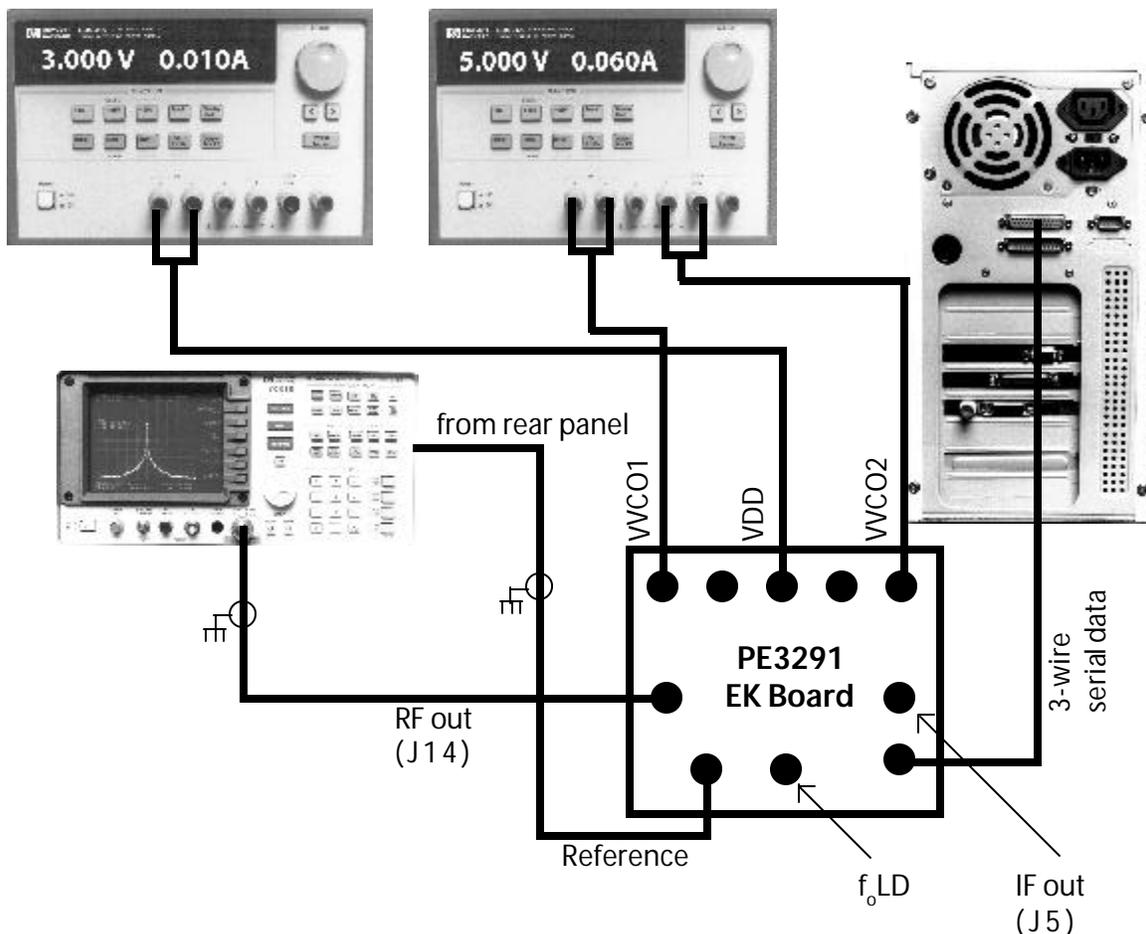

Figure 2 - Connecting the PE3291-EK to the computer's parallel port, the power supplies, and spectrum analyzer.

Connecting the Serial Interface

Connect the PE3291-EK to the computer's parallel port using a cable constructed as shown in *Fig. 3*. **It is not necessary to power down the computer when connecting or disconnecting the PE3291-EK.**

J3

```
  1 ──── Clock ──────── 2
  2 ──── Data ───────── 3
  3 ──── LE ─────────── 4                    DB25
  4 ──── Ground ────── 18                    Male Connector
```

Cable Connector
Female 0.100" centers
Single row, 4 positions

5
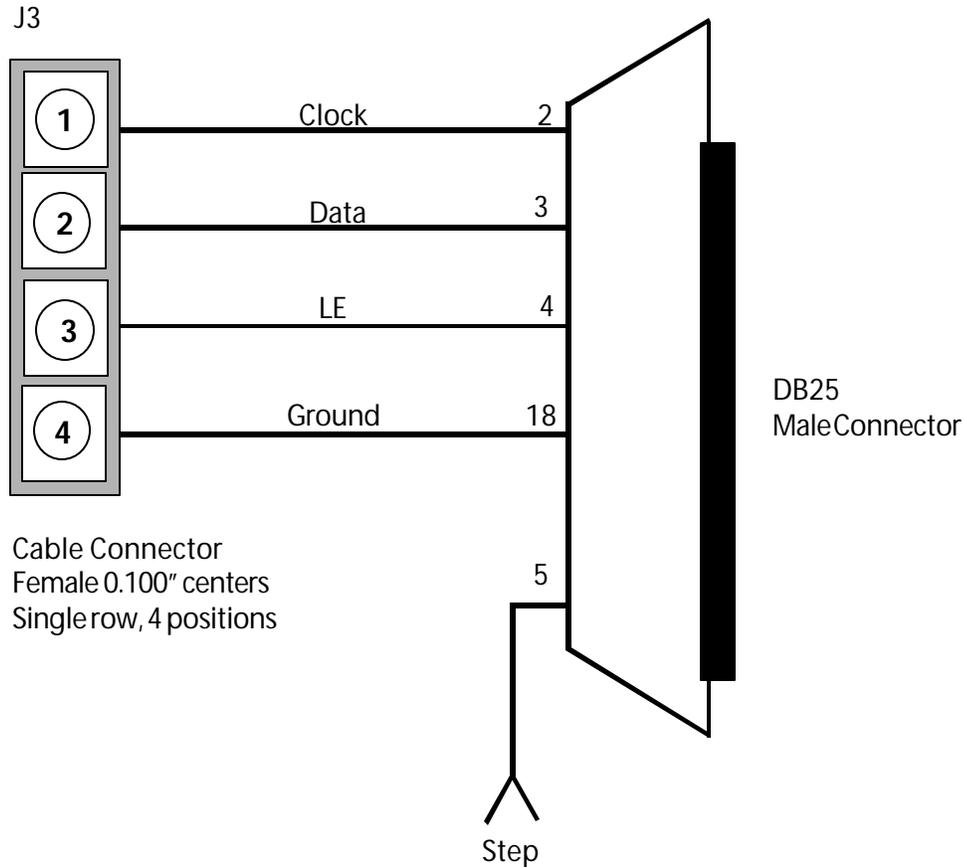
Step

Figure 3

The PE3291 demonstration software outputs a standard three-wire serial bus command plus ground from pins 2, 3, 4 and 18 of the printer port of the computer. The "Step" function is used as a trigger for single event measurements such as lock time (see page 27). The "Step" function is carried on pin 5 of the printer port and goes high with the LOAD ENABLE pulse of the PLL1 main programming word. The software normally transmits all four programming words, with the PLL1 main divider control word being the third word sent.

PE3291 Evaluation Board Layout and Parts Placement

Vvco1

+4.5V Input

+3V PLL Input

+5V Input For VCO2

N/C

RF Out

IF Out

N/C

Ref In

Serial Input

Figure 4. PE3291 Evaluation Board Layout and Parts Placement for PE3291 in BCC Package.
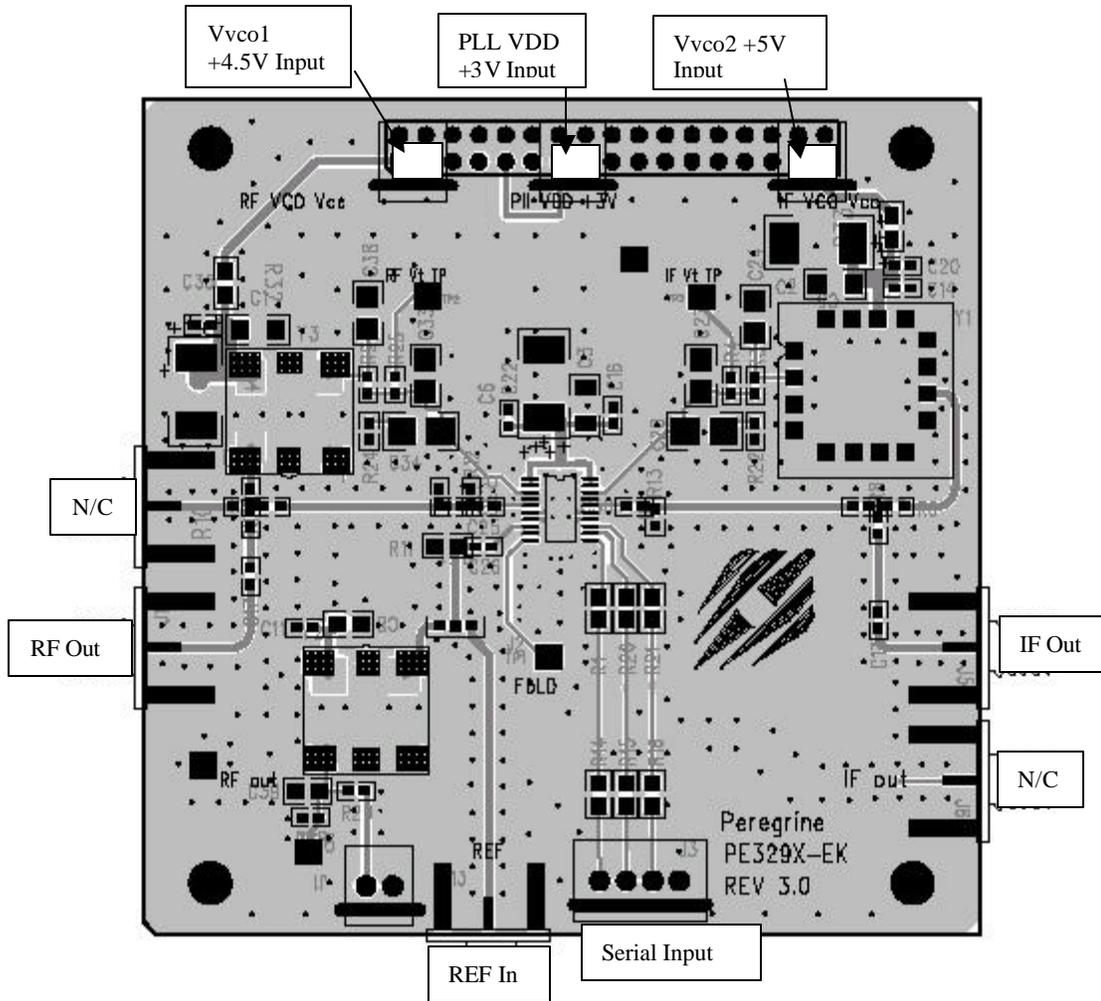
Figure 5. PE3291 Evaluation Board Layout and Parts Placement for PE3291 in TSSOP Package.

Parts List for PE3291 EK Board

* Reference Bill of Materials included in evaluation kit.

Source List For VCO

Micronetics Wireless
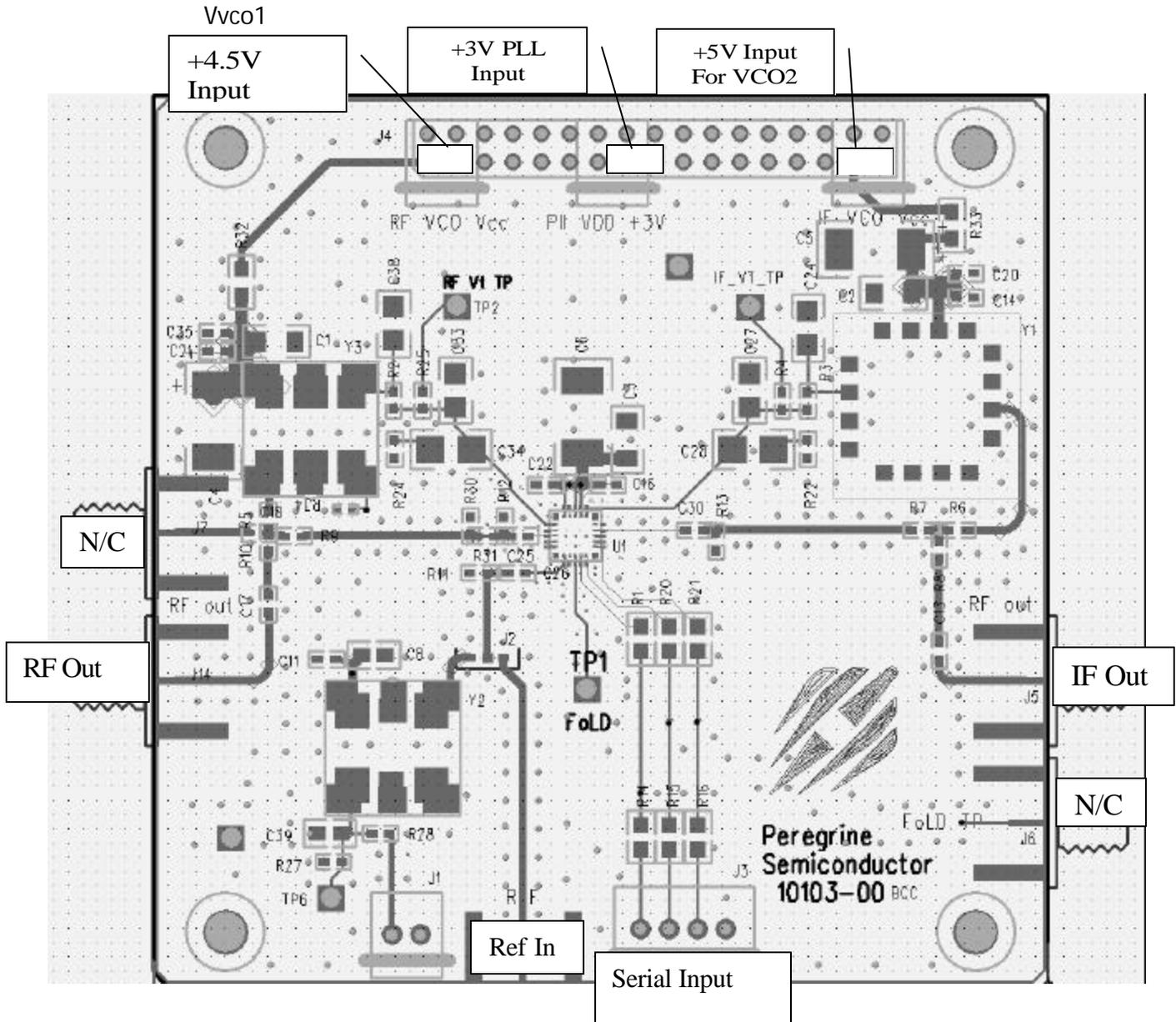26 Hampshire Drive
Hudson, NH 03051
(603) 883-2900
Fax (603) 882-8987
Customer hotline (800) 963-3382

Synergy Microwave Corp.
201 McLean Blvd.
Paterson, NJ 07504
(201) 881-8800
Fax (201) 881-8361

Z-Communications, Inc.
9939 Via Pasar
San Diego, CA 92126
(619) 799-5695
Fax (609) 799-7743

Fujitsu Media Devices of America, Inc.
50 Rio Robles
San Jose, CA 95134

Emhiser Micro-Tech
2705 Old Highway 40 West
P. O. Box 708
Verdi, NV 89439
(702) 345-0461
Fax (702) 345-2484

Vari-L
11101 East 51st Avenue
Denver, CO 80239
(303) 371-1560
Fax (303) 371-0845

Murata
Marketing Communications
2200 Lake Park Drive
Smyrna, Georgia 30080
(800) 831-9172
Fax (700) 436-3030
(Note: Murata VCOs use a non-standard footprint)

Princeton Electronic Systems
P.O. Box 8627
Princeton, NJ 08543

Software

Section

Software Introduction

Description

The PE3291-EK software runs under Microsoft Windows 95/98. It provides a conve-
nient means of initializing and controlling the PE3291-EK board. The user can enter
frequencies directly, enter division values directly as decimal, hexadecimal, or
binary numbers, and set individual control register bits directly in a register-map
window. The program calculates register values from user-specified frequencies
and performs range-checking on all values. The program communicates with the
PE3291-EK through a standard PC parallel port (LPT1, 2, or 3). The user can save the
PE3291-EK control settings as files for easy recall at any time.

Getting Help

This *User's Manual* covers all of the functions of the PE3291-EK program. The
program uses well-established Windows user-interface conventions and is often
self-explanatory. Still, we recommend that you read through this manual before
using the program.

Internet

Software upgrades, frequently asked questions, and applications information can
be found on Peregrine's website at http://www.peregrine-semi.com.

Customer Support

Our Applications Engineering staff will be happy to answer any questions you
might have about using the PE3291 or other Peregrine Semiconductor Corp.
products. Contact us at **(858) 455-0660**.

You may also contact us by fax or e-mail:

Fax:	**(858) 455-0770**
E-Mail:	**help@peregrine-semi.com**

Setup

Screen Shots

All screen images used in this manual are from Windows 95. The appearance of the windows on your system might differ somewhat from the images in this manual, depending on the version of Windows and type of display you are using.

System requirements

To run the PE3291-EK software, your system should meet the following *minimum* requirements:
- Microsoft Windows 95/98
- Intel 386 CPU or later
- 4 megabytes of RAM
- Standard or enhanced parallel port (LPT1, LPT2, or LPT3)

Installation Windows 95/98

1. The PE3291-EK software con be downloaded from the Peregrine Web site http://www.peregrine-semi.com or copied from the Peregrine CD.

   a. To download the software from the Web site, click **Products, PE3291 - 1.2 GHz/550 MHz** in the **Phase Locked Loops** section, and **Evaluation Board Software** in the **Evaluation Kit Documentation** section. Download the **3291.exe** file to an empty directory of your hard disk and double-click it. Two new files, **3291_disk1.exe** and **3291_disk2.exe,** will be generated.

   b. To copy the software from the Peregrine CD, click **Evaluation Kit Documentation, PE3291 - 1.2 GHz/550 MHz,** and then **Evaluation Board Software.** Choose the option of "Save and run the **3291.exe** file in your hard disk" or "Run it from CD". Either way, two new files, **3291_disk1.exe** and **3291_disk2.exe,** will be generated.

2. Click the **PE3291_disk1.exe** and **PE3291_disk2.exe** to unzip them.

3. Click the **setup.exe** file to start setup procedure. Follow the instructions on the screen.

Operation

Overview

This section describes how to use all of the features of the PE3291-EK software to control the PE3291-EK board. Since the PE3291-EK software uses a standard three-wire interface, it can also be used to control customer-designed breadboards or modified PE3291-EK boards. The PE3291-EK program performs range checking on values entered by the user or calculated by the program, and warns the user if certain limits are exceeded. The error messages are advisory; the program will permit the user to enter values outside the normal operating range of the PE3291.

Basic Operation

Three types of screen can be used to set the frequency of the PLLs. These are the **Frequency Input Loop** screens, which accepts frequency values, the **Loop Block Diagram** screens, which accept numbers to directly program the count registers, and the **Register Map** screen, which allows the binary control words to be set directly into the programming word registers.

If the **Frequency Input Loop** screens or the **Loop Block Diagram** screens are used to program the PLL then a third screen, the **Control Bits** screen must be used to set the output state of the PLL and the function of the f_oLD pin. For the PE3291 the control bits screen also sets the FlexiPower function of the prescalers.

If the **Register Map** screen is used to set the PLLs the control bits can be set directly in the **Register Map** screen.

The different screens can be accessed with the View menu from any window. The Control Bits screen can be accessed from the Options menu.

Setting the Operating Frequency of the PLLs

The PE3291 is a dual PLL synthesizer IC. The 1.2 GHz PLL (PLL 1 or RF PLL) and the 550 MHz PLL (PLL 2 or IF PLL) are programmed separately. Each PLL requires two programming words. The programming words can be generated in one of three ways.

1. Programming with the "Frequency Input Loop" Screens

The reference frequency, output frequency, step size, step number and comparison frequency can be specified on the **Frequency Input Loop** screens (*Figure 6*). Go to **View** on the main menu and select **Frequency Input Loop 1**.

Figure 6

Note that the **Frequency Input Loop 1** and the **Frequency Input Loop 2** screens are identical in appearance and function except that the prescaler for Loop 1 is a divide by 32/33, and the prescaler for Loop 2 is a divide by 16/17.

The **Frequency Input** screens are the basic method for programming the PLLs. These screens allow you to enter the *reference frequency (fr)*, *starting frequency*, *step size*, *step number*, *maximum fractionality*, and *comparison frequency (fc)* or reference *divider ratio* (*R*) value.

Programming with the "Frequency Input Loop", continued

From these entered values, the software will calculate the values for the boxes in green. When *fc* is changed, the software will recalculate the value of *R*, and vice versa.

When both **Frequency Input Loop** screens have been programmed to the desired *fin. Calc.*, the settings from both screens can be sent to the output port by clicking on **Send** at the bottom of either **Frequency Input Loop** screen or by typing **Alt S**.

There are a number of conditions for correct operation of the PE3291.

1. *fr* must be an integer multiple of *fc*. (i.e. *R* must be an integer)
2. *fr* must be an integer multiple of *Step Size*
3. *Step Size* must be equal to *fc* divided by 1, 2, 4, 8, 16, or 32.
4. *Step Number* must produce a calculated value for *F* which is compatible with *Max. fractionality.*
   - $F = 0$ for any Max. fractionality.
   - F = any value for Max. fractionality of 32.
   - F = even values for Max. fractionality of 16.
   - F = multiples of 4 for Max. fractionality of 8.
   - F = multiples of 8 for Max. fractionality of 4.
   - F = multiples of 16 for Max. fractionality of 2.
   - $F = 0$ for Max. fractionality of 1.

5. The desired output frequency must be achievable.
   - A. The desired output frequency (*fin. Spec.*) will be calculated as:
     1) (*Starting freq.*) + (*Step Size* X *Step Number*).
   - B. The closest achievable frequency (*fin. Calc.*) will be calculated as:
     1) $(32 \times M1 + A1 + F1/32) \times fc1$ for the Loop 1 screen
     2) $(16 \times M2 + A2 + F2/32) \times fc2)$ for the Loop 2 screen
   - C. *fin. Spec.* and *fin. Calc.* must match or an error message will be displayed.

Failure to meet any of these conditions will result in an error message in the dialog box under the **Inputs** window.

Input the numbers in the clear boxes by clicking on the box and typing the values in. Enter the values by moving to another box, clicking outside the box, clicking **Send** or hitting the enter key. For the *Step Number*, you may type the value into the box or use the up and down buttons to increment or decrement the value by 1. The *Max Fractionality* is input by clicking on the box to show its pull down list and then clicking on the desired *Max Fractionality* on the list.

Programming with the "Frequency Input Loop", continued

The user must provide *fr*. This is the reference frequency available from your reference source. The external reference is supplied to the input of both reference counters in the PE3291. The user must then specify either *fc* or *R*. The program will calculate the remaining term. If you change *fc* or *R*, the program will recalculate the other term to fit. If you specify a value for *fc* that cannot be generated by dividing *fr* by an integer between 3 and 511, there will be an error message, "*fr* is not an integer multiple of *fc*."

The *Starting freq*, *Step Size*, and *Step Number* are provided by the user. The program will calculate *fin Spec.* = *Starting freq* + (*Step Size* X *Step Number*). The program will then generate *fin Calc.* as the closest value that can be achieved using integer values for *M*, *A*, and *F*. If *fin Spec.* cannot be achieved using integer values of *M*, *A*, and *F*, there will be an error message, "Cannot achieve specified fin."

> In general, the step size should be chosen as *fc/Max fractionality*. Failure to do so will lead to numerous non-achievable *fin Spec.* values.

> In general, the *Starting frequency* should be an integer multiple of the *Step Size*. Failure to do so will usually lead to numerous non-achievable *fin Spec.* values.

Max fractionality is set by choosing 1, 2, 4, 8, 16, or 32 from the pull down list for *Max Fractionality* on the **Frequency Input Loop** screen. If the calculated value for *F* is not zero or a multiple of 32/ *Max fractionality*, the error message "Max fractionality exceeded" will appear.

The values of *M*, *A*, and *F* cannot be entered directly in the **Frequency Input Loop 1** screen. If you wish to enter these values directly, see the "Programming With the Loop Block Diagram Screen" below.

PLL 2 is programmed by going to **View** on the main menu and selecting **Frequencey Input Loop 2**. Follow the same steps as shown above for setting the operating frequency of PLL1.

2. Programming with the Loop Block Diagram Screen

The count numbers for the *A, F, M,* and *R* counters can be input into the **Block Diagram** screen *(Figure 7).*

 Note that the **Loop 1 Block Diagram** and the **Loop 2 Block Diagram** screens are identical in appearance and function except that the prescaler block for Loop 1 shows a divide by 32/33 , and the prescaler block shown for Loop 2 is a divide by 16/17.

The **Loop Block Diagram** screens allow the user to input the values for *A, F, M,* and *R* (the numbers shown in green) directly to the registers. The values for *fin. Calc.* and *fc* (shown in black) can be changed only by changing *A, F, M,* or *R,* or by going to the **Frequency Input** screen. If the resulting values of *fin. Calc.* or *fc* result in an error condition , the number will display in red in the **Loop Block Diagram** screen. If the resulting value of *fin. Calc.* does not agree with the *fin. Spec.* from the **Frequency Input** screen, the number will appear in red in the **Loop Block Diagram** screen.
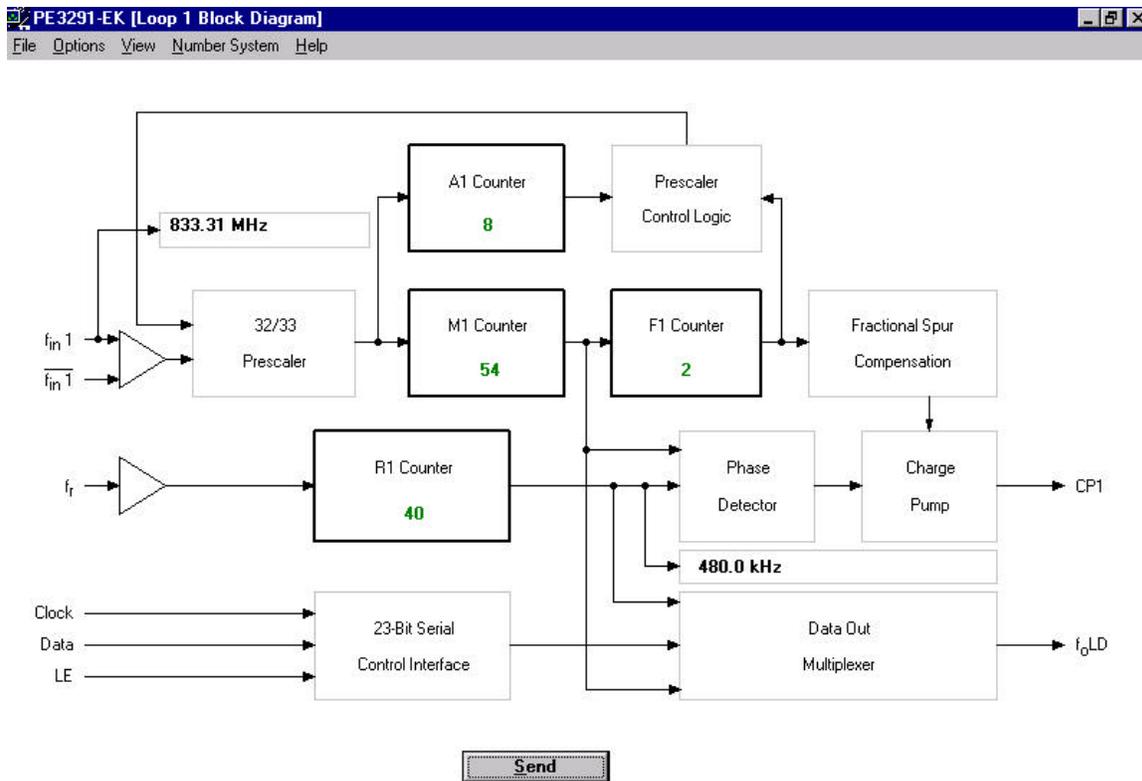

Figure 7

Programming with the "Loop Block Diagram", continued

When a **Loop Block Diagram** screen is open, the **Number System** window is active on the main menu bar. This allows input and viewing of *A, F, M,* and *R* in decimal, hex, or binary by clicking on **Number System** to pull down the menu and choosing the desired numbering system. The default setting will be in decimal.

The **Loop Block Diagram** screen is useful when you have already calculated the register values or when you wish to view the register values calculated by the program in a more intuitive format.

To program Loop 1, go to **View** on the main menu and select **Loop 1 Block Diagram** (*Fig. 7*). In this screen you can specify the count value of the *A, F, M,* and *R* counter registers for Loop 1. The *A, F, M,* and *R* values can be entered and displayed in decimal, hexadecimal, or binary format.

The value of *fr* must be specified in the **Frequency Input Loop 1** screen. The values of *A, F, M,* and *R* from the **Loop 1 Block Diagram** will be transferred to the **Frequency Input Loop 1** screen and used to calculte *fin Calc*. If the choices of *A, F, M,* or *R* entered in the **Loop 1 Block Diagram** cause an error message in the the **Frequency Input Loop 1** screen, the value for $f_{in}1$ displayed in the **Loop 1 Block Diagram** will appear in red.

> Note: If *R1* is changed in the **Loop 1 Block Diagram,** the comparison frequency (output of the R1counter) in the **Loop 1 Block Diagram** screen will change to the new calculated value.

3. Programming with the Register Map screens

The **Register Map** (*Figure 8*) view allows you to set the state of any accessible bit in the registers of the PE3291. Bits that you can set are green. Fixed or reserved bits are gray.

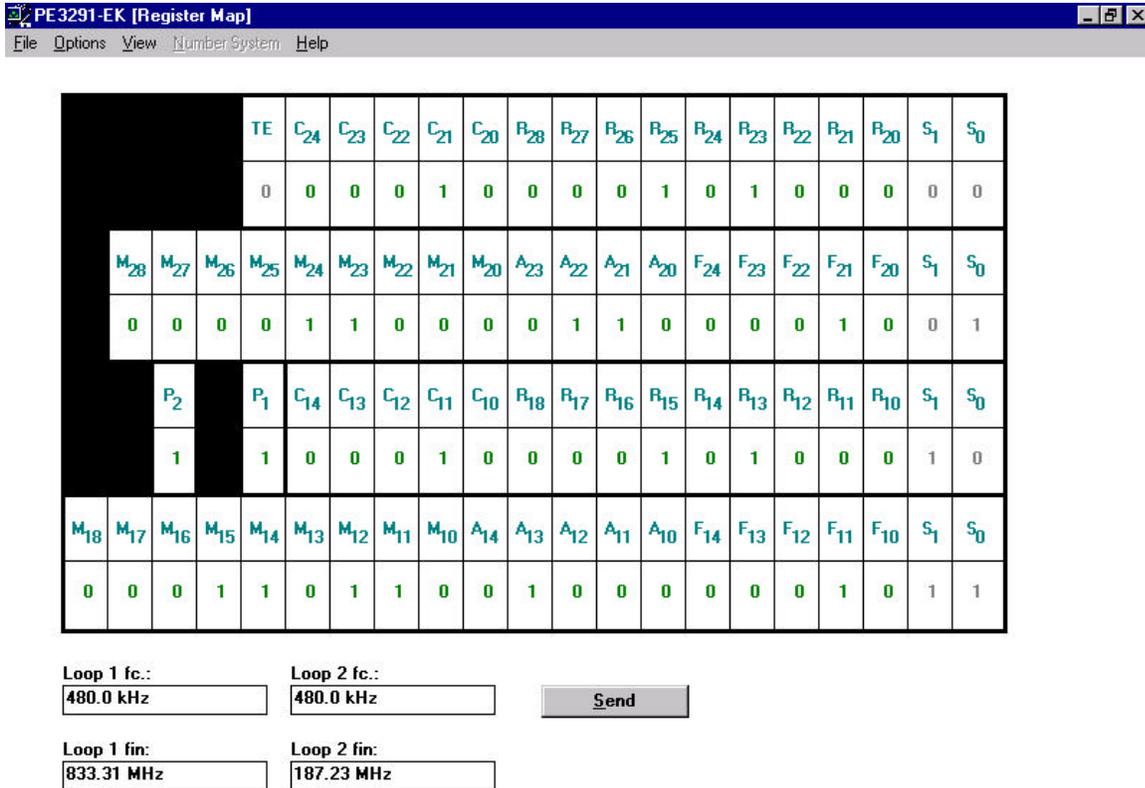Go to **View** on the main menu and select **Register Map**.

Figure 8

Place the cursor on the bit that you want to change and press the 0 or 1 keys to change the value. In this view, the program recognizes changes immediately. It is not necessary to move the cursor to enter the new value. The control bits for the PE3291 can be entered directly in the **Register Map** view to turn the individual PLLs on or off, control the f_oLD output and set the charge pump **Output Options**.

Once the desired bits are entered click on **Send** to program the PE3291. You can use this feature with the **Send Continuous** mode to change individual bits while automatically updating the PE3291.

Programming the Control Bits Window

When the PLL frequency is set using either the **Frequency Input Loop** screens or the **Loop Block Diagram** screens, the settings for the **Loop Output Options** must be set using the **Control Bits** window. (*Figure 9*)

Go to **Options** in the main menu and click on **Control Bits** to display the **Control Bits** window. Click on any f_o**LD Control** button to choose that output function for the f_oLD pin. The **Loop Output Options** are toggled by clicking on the function buttons. The **On** button toggles the entire PLL on or off. The **Invert** button sets the charge pump of that loop to invert the current sink and source relationship. The **Hi-Z** button turns the charge pump for that loop off, creating a high impedance at the charge pump output.

Click on one of the **Prescaler FlexiPower Setting** buttons to control the prescaler function.

When the f_o**LD Control**, both **Loop Output Options**, and the **Prescaler FlexiPower Setting** are set to the desired states, click on **Ok** to transfer the new states to the control word registers and close the window.
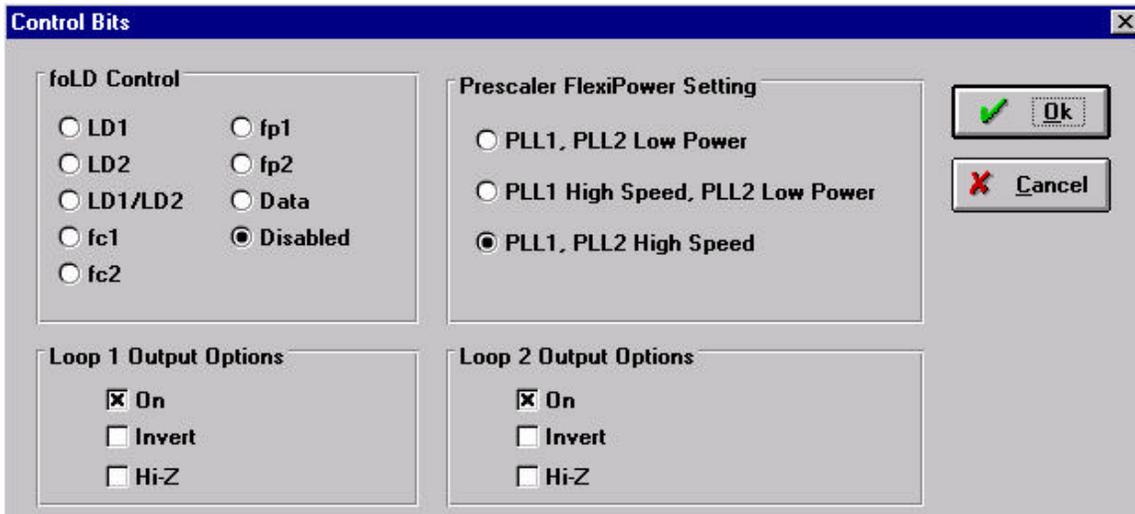

Figure 9

Configuration Files

All of the register values and control states can be saved as files. Later, you can reload a saved configuration to restore the PE3291-EK to a particular state without having to re-enter all of the values.

Saving Configurations

From the **File** menu, choose **Save Settings As**.
In the **Save As** dialog box, select a directory and enter a file name, then click **OK**.

Loading Configurations

From the **File** menu, choose **Load Settings**.
In the **Open** dialog box, select a directory and a file, then click **OK**.
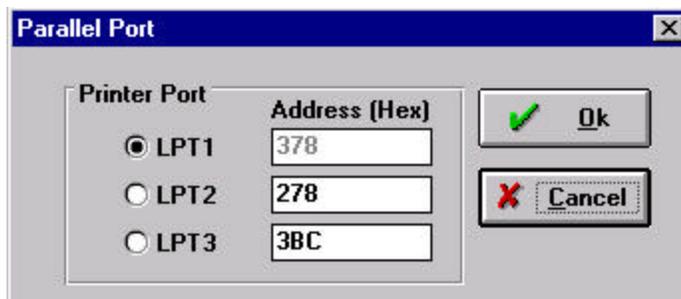
Printer Port Screen

Figure 10

The default output of the PE3291-EK software is through the LPT1 printer port as shown in Figure 10. If you wish to use a different port to control the PE3291, go to **Options,** click on **Parallel Port** and click on the button for the port you wish to use. Click on **OK** to set the output to the selected port. The data will now be sent out through the new selected port when you click on **Send**.

Measuring Lock Time

The PE3291 software has two modes for use in measuring the lock time of PLL1.

The **Toggle** mode allows switching repeatedly back and forth between two chosen frequencies. This is well suited to checking the coarse frequency acquisition by monitoring the tuning voltage of a synthesizer using an oscillo-scope, or when using a mixer and oscilloscope to measure the phase differ-ence between a PLL already locked on frequency, and the experimental PLL. The standard programming mode is more useful when measuring the lock up time as a one-shot event using a Modulation Domain Analyzer or similar instrument.

To use **Toggle Mode** click on **Options** to pull down the menu and then click on **Toggle Mode**. Click on **Options** again. You will now see that the **Repeti-tion Rate** and **Toggle Setting** options are available.

Click on **Repetition Rate**. The **Repetition Rate** window will ask you to set a number for the delay time. The actual time period represented by this num-ber will be machine dependent. You will have to experiment to determine the delay number needed to give the desired time between stepping events for your computer.

Click on **Toggle Setting**. The **Toggle Setting** window will ask you to chose the number of step sizes you wish to jump at each toggle event. The output frequency will toggle between the specified frequency (**fin Spec.**) in the **Frequency Input Loop 1** screen and a frequency that is the set number of steps above or below the starting frequency. A step is defined by the **Step Size** entry of the **Inputs** box of the **Frequency Input Loop 1** view. As an example if we set the **Starting Frequency** to 824.0 MHz, the **Step Size** to 25 KHz and the **Step Number** to 1, we will get an **fin Spec.** of 824.025 MHz. A **Toggle Setting** of 5 steps will then cause the frequency to toggle between 824.025 MHz and 824.150 MHz. A **Toggle Setting** of -5 steps will cause the frequency to toggle between 824.025 MHz and 823.900 MHz.

When the **Toggle Mode** is used, the software sends only the programming word for the PLL1 main divider. The rising edge of the Load Enable pulse can be used as a start signal for measuring lock up time. The Load Enable pulse is

Measuring lock time, continued

present on Pin 4 of the DB25 connector, Pin 3 of J3 (see Fig. 3, Page 9), and Pin 14 of the BCC IC or Pin 13 of the TSSOP IC. When done as a one-shot event there is no way to distinguish between jumping to the toggle frequency and jumping back to the specified frequency.

To use the standard programming mode to measure lock time as a single event with a Modulation Domain Analyzer, an output for use as the trigger has been provided on pin 5 of the DB25 connector. When the standard programming mode is used the software always sends all four programming words. The word for the PLL1 main divider is the third word in the series. This makes it difficult to use the Load Enable pulse as the trigger for measuring lock time. The output provided on pin 5 of the DB25 connector gives a pulse which is synchronous with the PLL1 main divider Load Enable pulse. This output is labeled "step" (see Fig. 3, Page 9). This signal is not available on the PE3291 board. It must be taken from the DB25 connector.

Test Results

Four test plots are normally enclosed, 2 for each PLL.
The test data will be measured with the following parameter:

Reference freq.: 19.2 MHz

Prescaler Flexi Power Setting: Low Power for both PLLs.

	PLL1	PLL2
fr (Reference freq.) (MHz):	19.2	19.2
Starting frequency (MHz):	833.31	187.23
Step size (KHz):	30	30
Step number:	0	0
Max fractionality:	16	16
fc (comparison frequency) (KHz):	480	480
R	40	40
M	54	24
A	8	6
F	2	2
N	1736+2/32	390+2/32