TQ-Minimodul

TQM167UL

mit

Microcontroller SAB-C167

Hardware - Manual

Hardware Manual for:

TQM167UL Rev100
Rev101

Contents

1. Introduction

Top Quality embedded Microcontroller Systems

High integration and high reliability are what set the TQ-Components industrial microcontroller modules apart from the rest. TQ-Components Minimodules from credit-card to half credit-card size are unbeatable in various applications. With an ever-expanding product line and clear technology migration path, TQ-Components offers OEMs uncompromising excellence in microcontroller modules. In a variety of industrial measurement, process regulation and control developments engineers confronted with the task of developing a complex monitoring / control system under time constraints are the prime beneficiaries of our microcontroller devices. Compare the advantage of the implementing a TQ-Components module to the total cost of a completely new circuitry design.

Time to market

TQ-Components microcontroller modules provide a drop-in CPU solution, with complete CPU kernel functionality on board. This enables engineers to take a project from concept to prototype or market in weeks, rather than in months or longer.

Reliability

TQ-Components modular embedded microcontroller Minimodules have proven to be reliable and rugged in numerous demanding and critical applications. Our highly knowledgeable team of electronic engineers has wide experience in designing embedded microcontroller Modules. The team‘s commitment to quality and reliability is evident throughout the whole TQ-Components product line.

Upgradability

Thanks to the flexibility of TQ’s product architectures, you will be able to enhance your products by taking advantage of a new technology as when it becomes available. Our products offer a migration path so you can upgrade features or performance without major redesign.

TQ-Minimodules offers you ...

☑ **Best price-performance relationship**

- uncompromising use of most modern production-technology
- low price through high production quantity
- Customised Versions on requests

☑ **Maximum performance on small footprint**

- double-sided SMT Technology
- Fine Pitch Multilayer Printed Circuit Boards
- using latest chip technology
- using latest Flash Memory technology

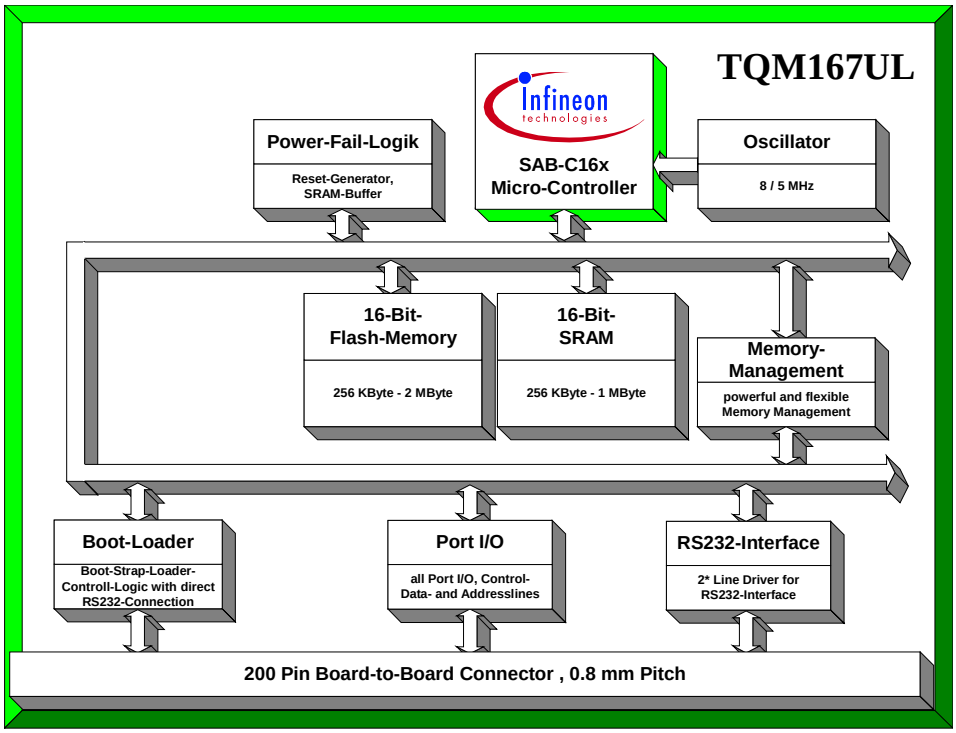
☑ **save time and money in your development**

- complete CPU kernel functionality on board
- immediate start through particular monitor-program
- works with most modern Software Development Tools such as compilers and debuggers
- Design-In Support through the manufacturer

☑ **save time and money in your production and service**

- Download-Function for development, production and service
- simple Firmware-Updates through Download-Function
- Download over Standard RS232-Interface without additional switches and jumpers
- Service-friendly modular construction

2. Block-Diagram:



2.1 Microcontroller SAB-C167CR-LM / SAB-C167CS-32FM

- High Performance 16 Bit-CPU
- 100 ns Instruction Cycle Time at 20 MHz CPU
- Up to 16 MByte Linear Address Space for Code and Data
- On-Chip CAN Interface (Version 2.0B) (1x SAB-C167CR-LM / 2x SAB-C167CS-32FM)
- 16-channel 10-bit A/D Converter
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with five 16-bit Timers
- Programmable Watchdog Timer
- Two Serial Channels (Synchronous/Asynchronous and High-Speed Synchronous)
- On-Chip Bootstrap Loader

Details see Siemens / Infineon User's Manual SAB-C167

2.2 Memory

2.2.1 Flash-Memory

- 256 kByte to 2 MByte
- organisation, 128k*16, 256k*16 or 512k*16, 1M*16,
- 90 or 70 ns access time
- on Board programmable
- Standard: 1 MByte

2.2.2 SRAM-Memory

- 256 kByte to 1MByte
- organisation 2*128k*8, 2*512k*8,
- 55 ns access time
- external battery backup
- Standard: 256 kByte

2.3 Reset-Logic

- CPU internal Watchdog
- Power-Fail Logic with MAX808

2.4 Interface

2.4.1 Serial-Interface

- one internal asynchronous (integrated in the processor)
  - with RS232 Driver as RxD0# and TxD0#
  - used unbuffered as RxD0 and TxD0
- one internal synchronous (integrated in the processor)

2.4.2 CAN-Interface

- Up two internal CAN-Interfaces (integrated in the processor)

2.4.3 Bus-Interface

- Port I/O, Control- Data- and Addresslines
- No Bus Drivers

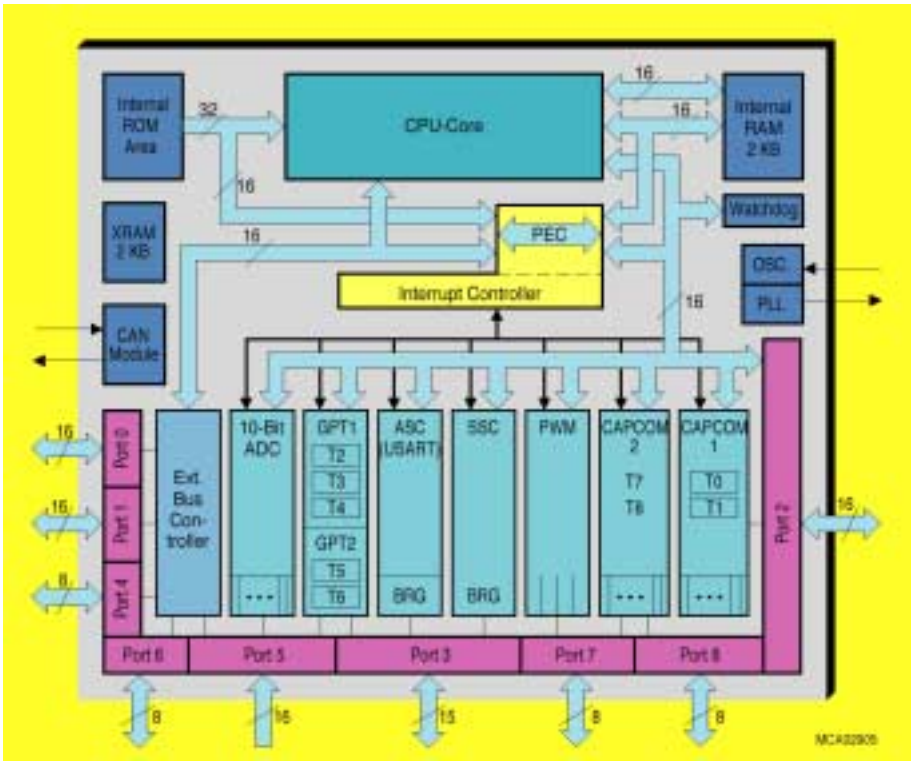
2.4.4 Internal Bootstrap Loader

- Download via serial Interface
- Powerful Download Tools
- Download to SRAM or Flash

2.5 Internal LED

The LED installed on the top of the module is connected to the reset output RSOUT# of the module. It lights when RSOUT# is active, i.e. until the EINIT command has been executed after a reset.

3. Microcontroller



- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- Enhanced Boolean Bit Manipu-lation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Clock Generation via on-chip PLL or via direct clock-input
- Up to 16 MBytes Linear Address Space for Code and Data
- 4/11 KBytes On-Chip SRAM (2/3 KB Internal RAM, 2/8 KBytes Extension RAM) (167CR/167CS)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-bit or 16-bit External Data Bus
- Five Programmable Chip-Select Signals
- Hold- and Hold-Acknowledge Bus Arbitration Support
- 1024 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40 ns
- 16/24-Channel 10-bit A/D Converter with 9.7/7.8 µs Conversion Time (167CR/167CS)
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with five 16-bit Timers
- Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- On-Chip CAN Interface 2.0 B active with 15 Message Objects (Full-CAN/Basic-CAN) (1* at SAB-C167CR / 2* at SAB-C167CS)
- Programmable Watchdog Timer
- Up to 111 General Purpose IO Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader

Details see Siemens / Infineon User's Manual SAB-C167CR / SAB-C167CS

4. Memory

The TQM167UL offers very flexible and simple ways to handle the memory configuration.

The processor provides 5 free programable Chip Selects to access the respective components. This allows a completely open memory configuration of the Minimodule.

The memory management is described in detail in Section 4.3.

4.1 Flash-Memory

4.1.1 Flash-Memory structure

The non-volatile memory of the module is implemented with one 16-bit flash EPROM with variable storage capacity. Depending on the version of the module this results in a possible memory space of 128K*16, 256k*16, 512K*16 or 1M*16 representing a memory capacity of 256 kByte, 512 kByte, 1 MByte or 2 Mbyte. The module TQM167UL is available with a maximum non-volatile memory of 2 MByte.

For exact technical data of the applied memory chips, please refer to the refering data sheets.

Details on programming are to be found in Section 4.1.2

The following memory configurations are possible:

Flash1	Capacity:	Address space:
256 kByte	256 kByte	128k x 16
512 kByte	512 kByte	256k x 16
1 MByte	1 Mbyte	512K x 16
2 Mbyte	2 Mbyte	1 M x 16

4.1.2 Flash EPROM BUSCON

The BUSCON depends on the memory access time, the multiplexed or demultiplexed data bus mode and latched or unlatched programmed Chip Selects.

The following configurations are possible:

BUSCON 0		
	CS - Mode	
Bus type	Latched CSCFG = 0	unlatched CSCFG = 1
70ns demultiplexed	**04BEh** (1 WS) 150ns	**04BFh** (0 WS) 100ns
90ns demultiplexed	**04BEh** (1 WS) 150ns	**04BEh** (1 WS) 150ns

☞ *Example: (70ns Flash EPROM, demultiplexed Bus, CSCFG =0)*

Field in BUSCON:	Value:	Delay:
MCTC [BUSCON 0.0...3]	1110b	1 Waitstate
RWDC [BUSCON 0.4]	1b	
MTTC [BUSCON 0.5]	1b	No Delay

The associated C command:

➔ BUSCONx = 04BEh

4.2 SRAM-Memory

4.2.1 SRAM-Memory structure

The SRAM of the module is implemented with two 8-bit wide SRAMs with a memory space of max 512k*16, representing a memory capacity of max. 1 MByte. The SRAM can be connnected to Vbat to avoid possible data loss.

For exact technical data of the applied memory chips, please refer to the refering data sheets.

Details on programming are to be found in Section 4.2.2

The following memory configurations are possible:

SRAM1	SRAM2	Capacity:	Address space:
128 KByte	128 KByte	256 KByte	128K x 16
512 KByte	512 KByte	1MByte	512K x 16

4.2.2 SRAM access times

The SRAMs have a maximum access time of 55ns. Using the fields MCTC (Memory Cycle Time Control), MTTC (Memory Tri-State Time Control) and RWDC (Read/Write Delay Control) of the respective BUSCON register sets up access time.
The BUSCON depends on the memory access time, the multiplexed or demultiplexed data bus mode and latched or unlatched programmed Chip Selects.

The following configuration is possible:

BUSCON 1		
	CS - Mode	
Bus type	**Latched** **CSCFG = 0**	**unlatched** **CSCFG = 1**
55ns demultiplexed	**04BEh** (1 WS) 150ns	**04BFh** (0 WS) 100ns

☞ *Example: (55ns SRAM memory, demultiplexed Bus, CSCFG =0)*

Field in BUSCON:	Value:	Delay:
MCTC [BUSCON 0.0...3]	1110b	1 Waitstate
RWDC [BUSCON 0.4]	1b	
MTTC [BUSCON 0.5]	1b	No Delay

The associated C command:

➔ BUSCONx = 04BEh

4.3 Memory Management

This section contains all details for the correct usage of the onboard memory of the module. The memory management can entirely be implemented by software.

4.3.1 Principle of operation

The microcontroller SAB-C167CR/CS is equipped with 5 free programmable Chip Selects. For each address block allocated to a Chip Select output, it is also possible to select an individual configuration of the system bus. For this, the bus type, bus width, wait states and also the memory block can be allocated to a CS signal.

CS0 addresses all memory blocks of the addressable range not allocated to CS1-CS4. This makes it possible to manage non-sequential memory blocks without further measures. After a reset, the Chip Select lines CS1-CS4 of the processor are inactive. In this case, CS0 is active for the entire memory range.

To allow programs in the flash EPROM to be started, CS0 is used to address these memory chips after a reset.

4.3.2 Chip Select allocation

The memory configuration applicable in most cases is installed as default by the manufacturer:

- CS0 addresses the flash EPROMs,
- CS1 the SRAMs.

For programming, please refer to Section 4.3.4 of this description.

Standard settings by TQ-Components:

Control line	Connected chip		
CS0#	On-board flash EPROM		
CS1#	On-board SRAM		
CS2#	external CS-Signal		
CS3#	external CS-Signal		
CS4#	external CS-Signal		
CS0#	Reset configuration	000000_h- $FFFFFF_h$	Flash EPROM

4.3.3 Programming of the Chip Select lines

The Chip Select lines are programmed by software via the registers BUSCON0..4 and ADDRSEL1..4.

The BUSCON registers define the hardware configuration of the system bus, the ADDRSEL registers the size of the memory.

BUSCON registers:

The BUSCON registers are adjustable by software. They are not pre-set via the BUSCON0 register.

The following parameter can be set individually through the BUSCON registers for each memory block. It will be initialised with the corresponding CS lines:

- Bus width:
  The system bus can be selected with a width of 8 or 16 bits. If an 8-bit bus is selected, first the Low byte and then the High byte are transferred through the data lines D0-D7.
- Bus type:
  This allows the selection of a non-multiplexed bus.
- Wait states:
  Up to 15 wait states, memory tristates and a R/W delay can be specified.
- Miscellaneous:
  The length of the ALE signal and the functions of RD# and WR# can also be influenced here.

The exact programming is to be found in the Microprocessor manual.

ADDRSEL registers:

The separation of the memory range is realised using the ADDRSEL registers. Thus the starting address of the memory block and the memory size must be specified:

ADDRSELx:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Range Start Address												Range Size Selection			

- **Range Start Address (RGSAD):**
  specifies the starting address of the memory block for the respective CS line (only integer multiples of the adjusted block size (RGSZ) are valid for the starting address; see table).
- **Range Size Selection (RGSZ):**
  Specifies the memory size as shown in the table below.

The following table is intended to simplify programming.

RGSZ:	Memorysize	RGSAD:	Startaddress
0 0 0 0	4 Kbyte	$RRRRRRRRRRRR_b$	$RRRRRRRRRRRR_b$ * 4KByte
0 0 0 1	8 Kbyte	$RRRRRRRRRRRx_b$	$RRRRRRRRRRR0_b$ * 4KByte
0 0 1 0	16 Kbyte	$RRRRRRRRRRxx_b$	$RRRRRRRRRR00_b$ * 4KByte
0 0 1 1	32 Kbyte	$RRRRRRRRRxxx_b$	$RRRRRRRRR000_b$ * 4KByte
0 1 0 0	64 Kbyte	$RRRRRRRRxxxx_b$	$RRRRRRRR0000_b$ * 4KByte
0 1 0 1	128 Kbyte	$RRRRRRRxxxxx_b$	$RRRRRRR00000_b$ * 4KByte
0 1 1 0	256 Kbyte	$RRRRRRxxxxxx_b$	$RRRRRR000000_b$ * 4KByte
0 1 1 1	512 Kbyte	$RRRRRxxxxxxx_b$	$RRRRR0000000_b$ * 4KByte
1 0 0 0	1 MByte	$RRRRxxxxxxxx_b$	$RRRR00000000_b$ * 4KByte
1 0 0 1	2 MByte	$RRRxxxxxxxxx_b$	$RRR000000000_b$ * 4KByte
1 0 1 0	4 MByte	$RRxxxxxxxxxx_b$	$RR0000000000_b$ * 4KByte
1 0 1 1	8 MByte	$Rxxxxxxxxxxx_b$	$R00000000000_b$ * 4KByte
Rest:	Not defined		

R: used bit; x: unused bit

Example:

ADDRSEL4 = 1A42h; (= 0001 1010 0100 0010_b)

Specifies a 16 KByte block of memory from address $1A4000_h$ for access to external memory.

4.3.4 Programming the SYSCON registers

The TQM167UL takes the Byte access to the 16 Bit Bus with the Signals WRL# and WRH#.
WRL# will be active, when you write to the lowest Byte (LBS).
Therefore Bit **WRCFG** in the SYSCON will be setted.

➔ WRCFG = 1

The SAB-C167 can use the Chip Select Signals on two different Modes.

4.3.4.1 Latched CS# Modus

After the ALE Signal lost his value the CS# - Signals change his level.
Therefore this Modus shows a clear but a slow Bustiming.

4.3.4.2 Unlatched CS# Modus

The CS# -Signals changing together with the Addresslines his level. The Bustiming is fast. Therefore it could be that we have on the CS# lines some Spikes between the bus access times. The Spikes takes no effect on theTQM167UL. Please be careful with your own Peripheries.

Details see Siemens / Infineon User's Manual SAB-C167CR / SAB-C167CS

4.3.5 Programming the flash EPROMs

Bit A0 of the flash EPROM is connected to A1 of the address bus. Therefor the Flash EPROM an be programmed only wordwise. During programming the addresses which are used has to be doubled.

If the Flash EPROM should be programmed bytewise following procedure should be used:

1. Read out the data word which has the byte that should be changed
2. Change the byte
3. Write back the data word.

☞ *Example:* Word Program

	1st Buscycle		2nd Buscycle		3rd Buscycle		4th Buscycle	
	Addrerss	Data	Address	Data	Address	Data	Address	Data
Standard	5555h	00AAh	2AAAh	0055h	5555h	00A0h	PA	Data
TQM167	AAAAh	00AAh	5554h	0055h	AAAAH	00A0h	PA	Data

PA: the address to be programmed is equal in both cases.

4.3.6 Examples of memory configurations

The Examples are configured with 70ns FLASH and demultiplexed BUS

4.3.6.1 Memory allocation used by the monitor Program MON16U and C166Mon (Keil)

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-1FFFFFh	SRAM	1	04BFh	0009h
200000h-3FFFFFh	Flash-EPROM	0	04BFh	--------
400000h-4FFFFFh	External Memory	2	060Dh	4008h
500000h-5FFFFFh	External Memory	3	048Eh	5008h

4.3.6.2 Memory allocation after download to the RAM

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-1FFFFFh	SRAM	1	04BFh	0009h
200000h-3FFFFFh	Flash-EPROM	0	04BFh	--------

These are two concrete proposals of memory configurations which ensure stable operation:

Variant for a program in flash memory
Variant for a program in SRAM

5. Interface

5.1 Serial Interface

The module is equipped with three serial interfaces:

- one internal asynchronous (integrated in the processor)
- one internal synchronous (integrated in the processor)

5.1.1 Internal asynchronous interface

Initialisation:

The internal asynchronous interface operates directly with the processor clock. For programming, please refer to the initialisation recommended in the manual.

Hardware configuration:

The interface is equipped with two connections on the module:

- Unbuffered as RxD0# and TxD0#.
- With RS232 driver as RxD0 and TxD0.

5.1.2 Internal synchronous interface

Initialisation:

See Section 5.1.1

Hardware configuration:

The conductors of the synchronous interface are connected to port 3 and can be used without limitations. This Interface can be used up to 5 MBaud.

P3.8 MRST
P3.9 MTSR
P3.13 SCLK

5.2 CAN - Interface

- Unbuffered as CAN1-RxD and CAN1-TxD and CAN2-RxD and CAN2-TxD.

5.3 Bus - Interface

All Port I/O, Control- Data- and Addresslines are available and connected to X1 and X2.

For Pin Configuratin, please refer to Section 0 of this description.

5.4 Internal bootstrap loader

The installed processor is equipped with a bootstrap loader which, in conjunction with the periphery implemented in the module, makes programming of the EPROMs unnecessary.

The downloading of a program to the module can be performed via the serial interface

In this way, programs can be downloaded from a PC without additional hardware, either to the SRAM or to the flash EPROM.

Because the internal bootstrap loader of the processor can only process 32 bytes, it is necessary to transfer programs in several blocks into the memory of the module.

Functional sequence:

1. To activate the bootstrap loader, a reset must first be initiated (RTS and DTR active = 1).
2. The reset is enabled after approx. 10 ms, the DTR line remains active.
3. The processor then enters the bootstrap loader mode and waits for a Null byte transmitted via ASC0.
4. The processor then returns an acknowledgement byte ($A5), which can be used to identify the processor.
5. 32 bytes are then transmitted by the PC, which are loaded directly into the internal RAM of the processor.

To allow convenient downloading of programs with larger memory requirement, TQ has developed the program BOOT16x (DOS Version) and TQLoad (Windows Version).

The program BOOT16x provides user-friendly control of the entire loading operation.

More detailed explanations and examples of this are to be found in the Software Manual.

The following signal lines of the serial interface are used (by the PC) for the download:

TQM167			PC (DSUB-9)		PC (DSUB-25)	
Signal	Pin		Pin	Signal	Pin	Signal
RESINS#	X1-52	↔	7	RTS	4	RTS
TXD0	X1-55	↔	2	RxD	3	RxD
GND	X1-2	↔	5	GND	7	GND
GND	X1-40	↔	5	GND	7	GND
BOOTSTR#	X1-53	↔	4	DTR	20	DTR
RXD0	X1-56	↔	3	TxD	2	TxD

6. Pin Configuration

This chapter describes the function of the TQM167UL connections.

6.1 CPU Pins

Signal	CPU-Pin	Module-Pin	Type	Description
P0L.0 / AD0	100	X1-32	I/O	P0L.0 – direct connected buffered
P0L.1 / AD1	101	X1-31	I/O	P0L.1 – direct connected buffered
P0L.2 / AD2	102	X1-30	I/O	P0L.2 – direct connected buffered
P0L.3 / AD3	103	X1-29	I/O	P0L.3 – direct connected buffered
P0L.4 / AD4	104	X1-28	I/O	P0L.4 – direct connected buffered
P0L.5 / AD5	105	X1-27	I/O	P0L.5 – direct connected buffered
P0L.6 / AD6	106	X1-26	I/O	P0L.6 – direct connected buffered
P0L.7 / AD7	107	X1-25	I/O	P0L.7 – direct connected buffered
P0H.0 / AD8	108	X1-24	I/O	P0H.0 – direct connected buffered
P0H.1 / AD9	111	X1-23	I/O	P0H.1 – direct connected buffered
P0H.2 / AD10	112	X1-22	I/O	P0H.2 – direct connected buffered
P0H.3 / AD11	113	X1-21	I/O	P0H.3 – direct connected buffered
P0H.4 / AD12	114	X1-20	I/O	P0H.4 – direct connected buffered
P0H.5 / AD13	115	X1-19	I/O	P0H.5 – direct connected buffered
P0H.6 / AD14	116	X1-18	I/O	P0H.6 – direct connected buffered
P0H.7 / AD15	117	X1-17	I/O	P0H.7 – direct connected buffered
P1L.0 / A0 / AN16	118	X2-19	I/O	P1L.0 - direct connected buffered
P1L.1 / A1 / AN17	119	X2-20	I/O	P1L.1 - direct connected buffered
P1L.2 / A2 / AN18	120	X2-21	I/O	P1L.2 - direct connected buffered
P1L.3 / A3 / AN19	121	X2-22	I/O	P1L.3 - direct connected buffered
P1L.4 / A4 / AN20	122	X2-23	I/O	P1L.4 - direct connected buffered
P1L.5 / A5 / AN21	123	X2-24	I/O	P1L.5 - direct connected buffered
P1L.6 / A6 / AN22	124	X2-25	I/O	P1L.6 - direct connected buffered
P1L.7 / A7 / AN23	125	X2-26	I/O	P1L.7 - direct connected buffered
P1H.0 / A8	128	X2-27	I/O	P1H.0 - direct connected buffered
P1H.1 / A9	129	X2-28	I/O	P1H.1 - direct connected buffered
P1H.2 / A10	130	X2-29	I/O	P1H.2 - direct connected buffered
P1H.3 / A11	131	X2-30	I/O	P1H.3 - direct connected buffered
P1H.4 / A12 / CC24IO	132	X2-31	I/O	P1H.4 - direct connected buffered
P1H.5 / A13 / CC25IO	133	X2-32	I/O	P1H.5 - direct connected buffered
P1H.6 / A14 / CC26IO	134	X2-33	I/O	P1H.6 - direct connected buffered
P1H.7 / A15 / CC27IO	135	X2-34	I/O	P1H.7 - direct connected buffered
P2.0 / CC0IO	47	X2-72	I/O	Port P2.0 – direct connected
P2.1 / CC1IO	48	X2-73	I/O	Port P2.1 – direct connected
P2.2 / CC2IO	49	X2-74	I/O	Port P2.2 – direct connected
P2.3 / CC3IO	50	X2-75	I/O	Port P2.3 – direct connected
P2.4 / CC4IO	51	X2-76	I/O	Port P2.4 – direct connected
P2.5 / CC5IO	52	X2-77	I/O	Port P2.5 – direct connected
P2.6 / CC6IO	53	X2-78	I/O	Port P2.6 – direct connected
P2.7 / CC7IO	54	X2-79	I/O	Port P2.7 – direct connected
P2.8 / CC8IO / EX0IN	57	X2-80	I/O	Port P2.8 – direct connected
P2.9 / CC9IO / EX1IN	58	X2-81	I/O	Port P2.9 – direct connected
P2.10 / CC10IO / EX2IN	59	X2-82	I/O	Port P2.10 – direct connected
P2.11 / CC11IO / EX3IN	60	X2-83	I/O	Port P2.11 – direct connected
P2.12 / CC12IO / EX4IN	61	X2-84	I/O	Port P2.12 – direct connected
P2.13 / CC13IO / EX5IN	62	X2-85	I/O	Port P2.13 – direct connected

P2.14 / CC14IO / EX6IN	63	X2-86	I/O	Port P2.14 – direct connected
Signal	CPU-Pin	Module-Pin	Type	Description
P2.15 / CC15IO / EX7IN / T7IN	64	X2-87	I/O	Port P2.15 – direct connected
P3.0 / T0IN	65	X1-78	I/O	Port P3.0 – direct connected
P3.1 / T6OUT	66	X1-77	I/O	Port P3.1 – direct connected
P3.2 / CAPIN	67	X1-76	I/O	Port P3.2 – direct connected
P3.3 / T3OUT	68	X1-75	I/O	Port P3.3 – direct connected
P3.4 / T3EUD	69	X1-74	I/O	Port P3.4 – direct connected
P3.5 / T4IN	70	X1-73	I/O	Port P3.5 – direct connected
P3.6 / T3IN	73	X1-72	I/O	Port P3.6 – direct connected
P3.7 / T2IN	74	X1-71	I/O	Port P3.7 – direct connected
P3.8 / MRST	75	X1-70	I/O	Port P3.8 – direct connected
P3.9 / MTSR	76	X1-69	I/O	Port P3.9 – direct connected
P3.10 / TxD0#	77	X1-68	O	Port P3.10 – direct connected Connected to RS232 driver
P3.11 / RxD0#	78	X1-67	I	Port P3.11 – direct connected Connected to RS232 driver
WRH#	79	X1-66	O	WRH# - direct connected
P3.13 / SCLK	80	X1-65	O	Port P3.13 – direct connected
P3.15 / CLKOUT / FOUT	81	X1-63	O	Port P3.15 – direct connected
P4.0 / A16	85	X1-47	O	Port P4.0 – direct connected Used as Address Line for 2 MB Flash
P4.1 / A17	86	X1-46	O	Port P4.1 – direct connected Used as Address Line for 2 MB Flash
P4.2 / A18	87	X1-45	O	Port P4.2 – direct connected Used as Address Line for 2 MB Flash
P4.3 / A19	88	X1-44	O	Port P4.3 – direct connected Used as Address Line for 2 MB Flash
P4.4 / A20 / CAN2_RxD[167CS]	89	X1-43	O	Port P4.4 – direct connected Used as Address Line for 2 MB Flash
P4.5 / A21 / CAN1_RxD[167CR]	90	X1-42	O	Port P4.5 – direct connected
P4.6 / A22 / CAN1_TxD[167CR]	91	X1-41	O	Port P4.6 – direct connected
P4.7 / A23 / CAN2_TxD[167CS]	92	X1-38	O	Port P4.7 – direct connected
P5.0 / AN0	27	X2-101	I	Port P5.0 – direct connected
P5.1 / AN1	28	X2-102	I	Port P5.1 – direct connected
P5.2 / AN2	29	X2-103	I	Port P5.2 – direct connected
P5.3 / AN3	30	X2-104	I	Port P5.3 – direct connected
P5.4 / AN4	31	X2-105	I	Port P5.4 – direct connected
P5.5 / AN5	32	X2-106	I	Port P5.5 – direct connected
P5.6 / AN6	33	X2-107	I	Port P5.6 – direct connected
P5.7 / AN7	34	X2-108	I	Port P5.7 – direct connected
P5.8 / AN8	35	X2-109	I	Port P5.8 – direct connected
P5.9 / AN9	36	X2-110	I	Port P5.9 – direct connected
P5.10 / AN10 / T6EUD	39	X2-111	I	Port P5.10 – direct connected
P5.11 / AN11 / T5EUD	40	X2-112	I	Port P5.11 – direct connected
P5.12 / AN12 / T6IN	41	X2-113	I	Port P5.12 – direct connected
P5.13 / AN13 / T5IN	42	X2-114	I	Port P5.13 – direct connected
P5.14 / AN14 / T4EUD	43	X2-115	I	Port P5.14 – direct connected
P5.15 / AN15 / T2EUD	44	X2-116	I	Port P5.15 – direct connected

Signal	CPU-Pin	Module-Pin	Type	Description
P6.0 / CS1#	1	-	I/O	Port P6.0 – not connected only internal
P6.1 / CS1#	2	-	I/O	Port P6.1 – not connected only internal
P6.2 / CS2#	3	X2-38	I/O	Port P6.2 – direct connected[CS2#]
P6.3 / CS3#	4	X2-39	I/O	Port P6.3 – direct connected
P6.4 / CS4#	5	X2-40	I/O	Port P6.4 – direct connected
P6.5 / HOLD#	6	X2-41	I/O	Port P6.5 – direct connected
P6.6 / HLDA#	7	X2-42	I/O	Port P6.6 – direct connected
P6.7 / BREQ#	8	X2-43	I/O	Port P6.7 – direct connected
P7.0 / POUT0	19	X2-52	I/O	Port P7.0 – direct connected
P7.1 / POUT1	20	X2-53	I/O	Port P7.1 – direct connected
P7.2 / POUT2	21	X2-54	I/O	Port P7.2 – direct connected
P7.3 / POUT3	22	X2-55	I/O	Port P7.3 – direct connected
P7.4 / CC28IO	23	X2-56	I/O	Port P7.4 – direct connected
P7.5 / CC29IO	24	X2-57	I/O	Port P7.5 – direct connected
P7.6 / CC30IO	25	X2-58	I/O	Port P7.6 – direct connected
P7.7 / CC31IO	26	X2-61	I/O	Port P7.7 – direct connected
P8.0 / CC16IO	9	X2-44	I/O	Port P8.0 – direct connected
P8.1 / CC17IO	10	X2-45	I/O	Port P8.1 – direct connected
P8.2 / CC18IO	11	X2-46	I/O	Port P8.2 – direct connected
P8.3 / CC19IO	12	X2-47	I/O	Port P8.3 – direct connected
P8.4 / CC20IO	13	X2-48	I/O	Port P8.4 – direct connected
P8.5 / CC21IO	14	X2-49	I/O	Port P8.5 – direct connected
P8.6 / CC22IO	15	X2-50	I/O	Port P8.6 – direct connected
P8.7 / CC23IO	16	X2-51	I/O	Port P8.7 – direct connected
NMI#	142	X2-37	I	NMI# - direct connected / int. Connected through 4,7Kohm to VCC
RSTOUT#	141	X2-36	O	RSTOUT# - direct connected / internal Connected to an Inv. (RESET) RST - LED
RSTIN#	140	X2-35	I/O	RSTIN# - direct connected
ALE	98	X1-34	O	ALE - direct connected
EA#	99	X1-33	I	EA# - direct connected / int. Connected through 4,7Kohm to GND
READY#	97	X1-35	I	READY# - direct connected / int. Connected through 4,7Kohm to VCC
RD#	95	X1-37	O	RD# - direct connected
WRL#	96	X1-36	O	WRL# - direct connected
V_{PP}	84	X1-50	-	VPP- direct connected / int. Connected through 4,7Kohm to VCC
V_{AGND}		X2-118	-	Reference voltage for the A/D converter
V_{AREF}		X2-117		Reference ground for the A/D converter

[167CR] – only for SAB-C167CR

[167CS] – only for SAB-C167CS

= active low or inverted signal

6.2 Module Pins

Signal	Module-Pin	Type	Description
TxD0	X1-55	O	RS232 output of the internal serial interface ASCO Level adjustment by MAX202
RxD0	X1-56	I	RS232 input of the internal serial interface ASCO Level adjustment by MAX202
RSINS#	X1-52		Reset in (Bootstrap Loader)
BOOTSTR#	X1-53		Bootstrap loader input to activate the bootstrap loader mode via the serial interface. Positive voltage bootstrap mode active.
LOWL#	X1-54		Low-Line Comparator output
VBAT	X1-51	-	Backup Battery input
V_{CC} – 5V	X1-1	-	Digital voltage
V_{CC} – 5V	X1-39	-	Digital voltage
V_{CC} – 5V	X1-79	-	Digital voltage
V_{CC} – 5V	X2-1	-	Digital voltage
V_{CC} – 5V	X2-59	-	Digital voltage
V_{CC} – 5V	X2-119	-	Digital voltage
DGND	X1-2	-	Digital ground
DGND	X1-40	-	Digital ground
DGND	X1-80	-	Digital ground
DGND	X2-2	-	Digital ground
DGND	X2-60	-	Digital ground
DGND	X2-120	-	Digital ground

= active low or inverted signal

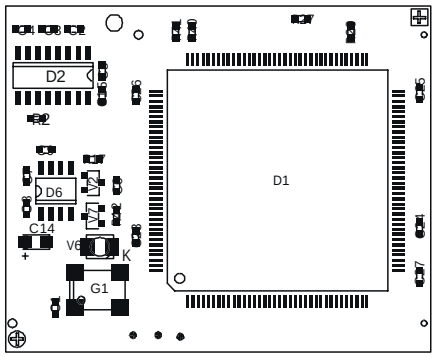
7. Mechanical Data

7.1 Connector

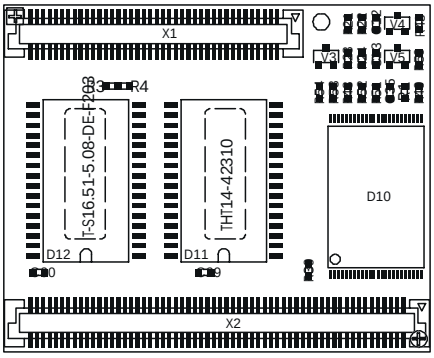
Board-to-Board Distance	Option	Modul			
		No. of Pin	**Qty**	**Supplier**	**Order No.**
5 mm	5	120	1	AMP Berg	177983-5 61082-121000
6 mm					
7 mm		80	1	AMP Berg	177983-3 61082-081000
8 mm					

Base Board Connector		
No. Of Pin	**Supplier**	**Order No.**
120	AMP	177984-5
	Berg	61083-121000
80	AMP	177984-3
	Berg	61083-081000
120	AMP	5-179029-5
	Berg	61083-122000
80	AMP	5-179029-3
	Berg	61083-082000
120	AMP	5-179030-5
	Berg	61083-123000
80	AMP	5-179030-3
	Berg	61083-083000
120	AMP	5-179031-5
	Berg	61083-124000
80	AMP	5-179031-3
	Berg	61083-084000

7.2 Connector Position



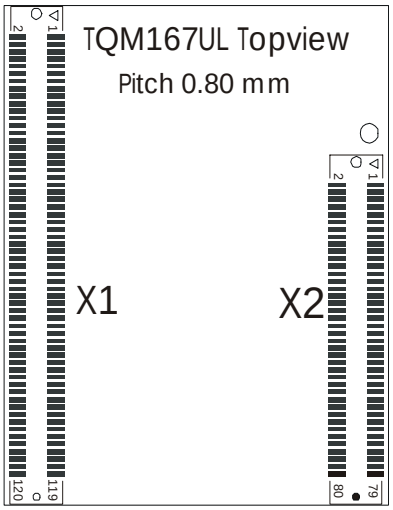
Top View: TQM167UL



Bottom View: TQM167UL

8. Pin Configuration

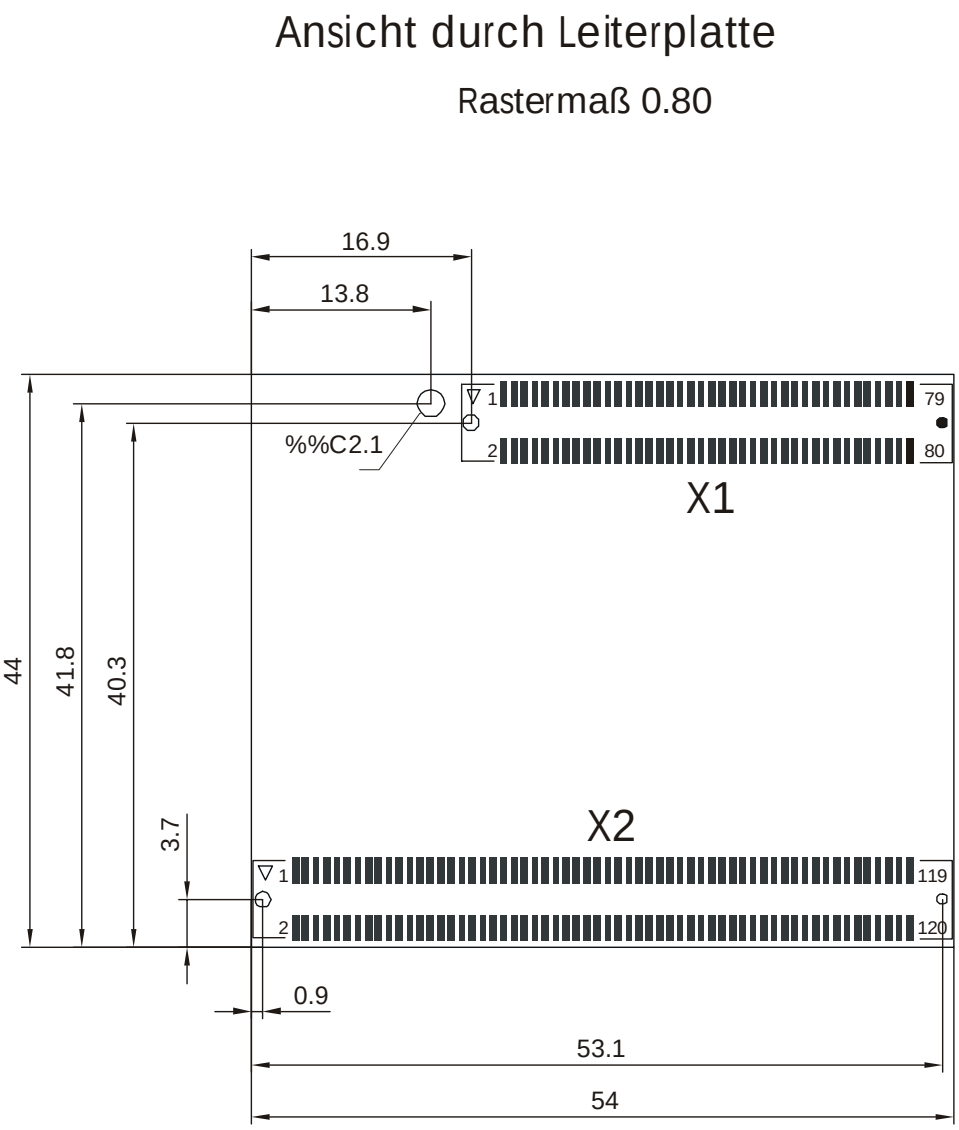
Pin No X2	Function	Pin No X2	Function
2	DGND	1	VCC5V
4	*NC – Spare*	3	NC – Spare
6	*NC – Spare*	5	*NC – Spare*
8	*NC – Spare*	7	*NC – Spare*
10	*NC – Spare*	9	*NC – Spare*
12	*NC – Spare*	11	*NC – Spare*
14	*NC – Spare*	13	*NC – Spare*
16	*NC - Spare*	15	*NC – Spare*
18	*NC - Spare*	17	*NC – Spare*
20	P1L1/A1	19	P1L0/A0
22	P1L3/A3	21	P1L2/A2
24	P1L5/A5	23	P1L4/A4
26	P1L7/A7	25	P1L6/A6
28	P1H1/A9	27	P1H0/A8
30	P1H3/A11	29	P1H2/A10
32	P1H5/A13	31	P1H4/A12
34	P1H7/A15	33	P1H6/A14
36	RSTOUT#	35	RSIN#
38	CS2#	37	NMI#
40	CS4#	39	CS3#
42	P6.6	41	P6.5
44	P8.0	43	P6.7
46	P8.2	45	P8.1
48	P8.4	47	P8.3
50	P8.6	49	P8.5
52	P7.0	51	P8.7
54	P7.2	53	P7.1
56	P7.4	55	P7.3
58	P7.6	57	P7.5
60	DGND	59	VCC5V
62	*NC - P9.0*	61	P7.7
64	*NC - P9.2*	63	*NC - P9.1*
66	*NC - P9.4*	65	*NC - P9.3*
68	*NC - P9.6*	67	*NC - P9.5*
70	*NC - USB*	69	*NC - P9.7*
72	P2.0	71	*NC - USB*
74	P2.2	73	P2.1
76	P2.4	75	P2.3
78	P2.6	77	P2.5
80	P2.8	79	P2.7
82	P2.10	81	P2.9
84	P2.12	83	P2.11
86	P2.14	85	P2.13
88	NC – IOM2	87	P2.15
90	*NC – IOM2*	89	*NC - IOM2*
92	*NC – IOM2*	91	*NC - IOM2*
94	NC – JTAG	93	*NC - JTAG*
96	*NC – JTAG*	95	*NC - JTAG*
98	*NC – JTAG*	97	*NC - JTAG*
100	*NC – JTAG*	99	*NC - JTAG*
102	P5.1	101	P5.0
104	P5.3	103	P5.2
106	P5.5	105	P5.4
108	P5.7	107	P5.6
110	P5.9	109	P5.8
112	P5.11	111	P5.10
114	P5.13	113	P5.12
116	P5.15	115	P5.14
118	AGND	117	VAREF
120	DGND	119	VCC5V



Pin No X1	Function	Pin No X1	Function
2	DGND	1	VCC5V
4	*NC*	3	*NC*
6	*NC*	5	*NC*
8	*NC*	7	*NC*
10	*NC*	9	*NC*
12	*NC - Uart_opt*	11	*NC*
14	*NC*	13	*NC*
16	*NC*	15	*NC*
18	AD14	17	AD15
20	AD12	19	AD13
22	AD10	21	AD11
24	AD8	23	AD9
26	AD6	25	AD7
28	AD4	27	AD5
30	AD2	29	AD3
32	AD0	31	AD1
34	ALE	33	EA#
36	WRLB#	35	READY#
38	P4.7	37	RD#
40	DGND	39	VCC5V
42	P4.5	41	P4.6
44	P4.3/A19	43	P4.4/A20
46	P4.1/A17	45	P4.2/A18
48	*NC – reserved*	47	P4.0/A16
50	VPP	49	*NC – Reserved*
52	RSINS#	51	VBAT
54	LOWL#	53	BOOTSTR#
56	RxD0	55	TxD0
58	*NC*	57	*NC*
60	*NC*	59	*NC*
62	*NC*	61	*NC*
64	*NC - P3.14*	63	P3.15
66	P3.12/WRHB#	65	P3.13
68	P3.10/TxD0#	67	P3.11/RxD0#
70	P3.8	69	P3.9
72	P3.6	71	P3.7
74	P3.4	73	P3.5
76	P3.2	75	P3.3
78	P3.0	77	P3.1
80	DGND	79	VCC5V

***NC – xxx* is not connected / for future use**

8.1 Mechanikal Drawing



9. Order Code:

Module	Order Code	Description
TQM167ULH7ACR	TQM167UL-AA	Module with • SAB-C167CR Processor • 20 MHz Processor speed • 256kByte Flash bottom boot, 70 ns • 256kByte SRAM, 70ns • with RS232 driver • temperature range 0°C...70°C
TQM167ULK7CCR-A	TQM167UL-AB	Module with • SAB-C167CR Processor • 24 MHz Processor speed • 1MByte Flash bottom boot, 70 ns • 1MByte SRAM, 55ns • with RS232 driver • temperature range 0°C...70°C

TQM *v_1* **UL** *w_1 w_2 x v_2 s z t*

t: Temperature Range

blank	=	0°C...+70°C
I	=	*-40°C...+85°C [1])*

z: Options

blank	=	Standard (RS232 Driver)
1	=	Without RS232 Driver

s: CPU Clock Speed

blank	=	20 MHz
A	=	24 MHz

v_2: Microcontroller Version

SR	=	*Infineon C167SR [1])*
CR	=	Infineon C167CR
CS	=	*Infineon C167C [1])*
F168	=	*ST Microelectronics ST10F168 [1])*

x: SRAM Memory

A	=	256 kByte (2* 128 kBit * 8 / 1 Mbit), 70 ns
C	=	1 MByte (2* 512 kBit * 8 / 4 Mbit), 70 ns
H		256 kByte (2* 128 kBit * 8 / 1 Mbit), 55 ns
K	=	1 MByte (2* 512 kBit * 8 / 4 Mbit), 55 ns
P		*256 kByte (2* 128 kBit * 8 / 1 Mbit), 50 ns [1])*
R	=	*1 MByte (2* 512 kBit * 8 / 4 Mbit), 50 ns [1])*

w: Flash Memory

W_2: Speed Option

9	=	90 ns
7	=	70 ns
5	=	*55 ns [1])*

w_1: Flash Memory Type

A	=	256 kByte (128 kBit * 16 / 2 Mbit), Top Boot
B	=	512 kByte (256 kBit * 16 / 4 Mbit), Top Boot
C	=	1 MByte (512 kBit * 16 / 8 Mbit), Top Boot
D	=	2 MByte (1 Mbit * 16 / 16 Mbit), Top Boot
H	=	256 kByte (128 kBit * 16 / 2 Mbit), Bottom Boot
I	=	512 kByte (256 kBit * 16 / 4 Mbit), Bottom Boot
K	=	1 MByte (512 kBit * 16 / 8 Mbit), Bottom Boot
L	=	2 MByte (1 Mbit * 16 / 16 Mbit), Bottom Boot

v1: Microcontroller Version

167	=	Infineon SAB-C167x
S10	=	*ST ST10x [1])*

10. References

SAB-C167CR / SAB-C167CS Microcontroller

http://www.infineon.com/products/index.htm
Microcontrollers
C167CR Users Manual / C167CS Users Manual

AM29F160DT Flash EPROM

http://www.amd.com/products/products.html
Non Volatile Memory
Flash – 5V only Flash Memory

MAX3233 RS232 Driver

http://www.maxim-ic.com
Products / Data Sheets
Data Sheet MAX3232

KM688100LT-7L / KM684000CLG-5L SRAM

http://www.usa.samsungsemi.com

Rev No.	Designed by:	Date	Approved by:	Date:	Changes:
100	ANW	14.03.02			Creation