User's Manual

MSC Q7-IMX6 Module
(Freescale® i.MX6™)

Rev. 2.4
June 3rd, 2014

Hardware Revision 4.0

Preface

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MSC products are developed and manufactured according to high quality standards. Our life-cycle-management assures long term availability through permanent product maintenance. Technically necessary changes and improvements are introduced if applicable. A product-change-notification and end-of-life management process assures early information of our customers.

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MSC engineers and technicians are committed to provide support to our customers whenever needed.
Before contacting Technical Support of MSC Vertriebs GmbH, please consult the respective pages on our web site at http://www.mscembedded.com/support-center.html for the latest documentation, drivers and software downloads.
If the information provided there does not solve your problem, please contact our Technical Support:

Email: support.boards@msc-ge.com
Phone: +49 8165 906-200

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1   General Information

1.1   Revision History

Rev.	Date	Pages	Description
1.0	06.03.2013	All	Initial Version Hardware Revision 2.0
2.0	23.09.2013	All	Initial Version Hardware Revision 4.0
2.1	08.11.2013	All	Revised and updated version
2.2	19.12.2013	12	Added GPIOs to the feature list
2.3	24.01.2014	11	Added UART on Debug connector in figure 2-1
2.4	03.06.2014	25	Exchanged PIN91 from USB_CC to USB_VBUS

1.2   Reference Documents

[1] Qseven Specification
Revision 2.0
Last update: July 2nd 2013
http://www.sget.org/standards/qseven.html

[2] Universal Bus Specification
usb_20.pdf
Last update: April 27th, 2000
http://www.usb.org

[3] IEEE Std. 802.3-2002
802.3-2002.pdf
http://www.ieee.org

[4] Serial ATA Specification
Serial ATA 1.0 gold.pdf
Last update: August 29th, 2002 Rev.1.0
http://www.sata-io.org/

1.3   Introduction

Qseven modules are compact, highly integrated Single Board Computers. Due to the standardized mechanics and interfaces the system can be scaled arbitrarily. Despite the modular concept the system design is very flat and compact.

Qseven modules require a carrier board to build a working system. For evaluation purposes MSC recommends the official Qseven Reference Platform MSC Q7-MB-RP2.

The MSC Q7-IMX6 is part of the MSC Qseven$^{®}$ family of Qseven$^{®}$ CPU modules. It is based on a Freescale$^{®}$ i.MX6™ System-on-a-Chip (SoC) which incorporates a low-power, high performance Single-, Dual or Quad-core ARM$^{®}$ Cortex TM -A9 Core processor.

All functionalities are listed in the Technical Description section. Depending on the assembly variant different subsets are available.

The module is fully compliant with the Qseven$^{®}$ Specification Revision 2.0.

2   Technical Description

2.1   Key Features

CPU

Single, Dual or Quad ARM$^®$ Cortex™-A9 Core processors, up to 1.2GHz

Each core includes:

- 32KB L1 instruction cache
- 32KB L1 data cache

The cores share:

- 1MB L2 unified cache (512KB for Single Core)

Memory

- Single core: 32-bit DDR3, 400MHz, max. 2GByte
- Dual/ Quad core: 64-bit DDR3, 532MHz, max. 4 GByte

Display Controller

- Single core: (2 independent displays)
- Dual/Quad core: 3 independent displays (HDMI + 2x LVDS) possible
- HDMI 1.4
- LVDS (one port up to 165 Mpixels/s or two ports up to 85 Mpixels/s)

GPU

GPU with OpenGL-ES 2.0, OpenGL-ES 1.1, OpenVG 1.1

Ethernet

Gigabit Ethernet Controller (10/100/1000 Mbps) + PHY

Audio

Audio Interface:

- AC'97 Controller or
- I2S Controller

USB

Eight USB 2.0 ports - 2 integrated in CPU (1x Host, 1x Host/Client), 7 implemented via USB Hub on module.

SATA

SATA II, 3.0 Gbps

PCI Express

PCI Express Gen 2.0 (x1 lane)

Serial, SPI, I^{2}C

- UART Controller
- SPI Controller (two slave selects) (60MHz max.)
- I^{2}C Controller (up to 400kbps)

Flash Memory

- eMMC Memory, minimum 32Gbit (8Bit data bus)
- SPI-Boot-Flash, up to 128Mbit (52MHz max.)

SDIO
SD/MMC Controllers (SD, MMC, HS-MMC, SDIO)

RTC
RTC with I^{2}C-Interface (typ. Power Consumption 800nA @ 3V)

GPIO
Support for 8 GPIOs (configurable as input / output)

Boot Sources

- SPI Flash (bootloader only)
- eMMC Flash (file system)
- SD-Card (file system)
- USB (recovery mode)

Power Supply

- 5V (4.75V – 5.25V)
- 5V (4.75V – 5.25V) optional standby voltage
- 3V (2.0V – 3.3V) optionally for RTC

2.2   Ordering Information

Ordering information can be obtained from the datasheet on the MSC website

http://www.mscembedded.com/products/qseven/msc-q7-imx6.html

There are different mounting options and combinations available. Therefore, not every feature is supported on every variant. The document refers to the maximum configuration.

2.3   Block Diagram
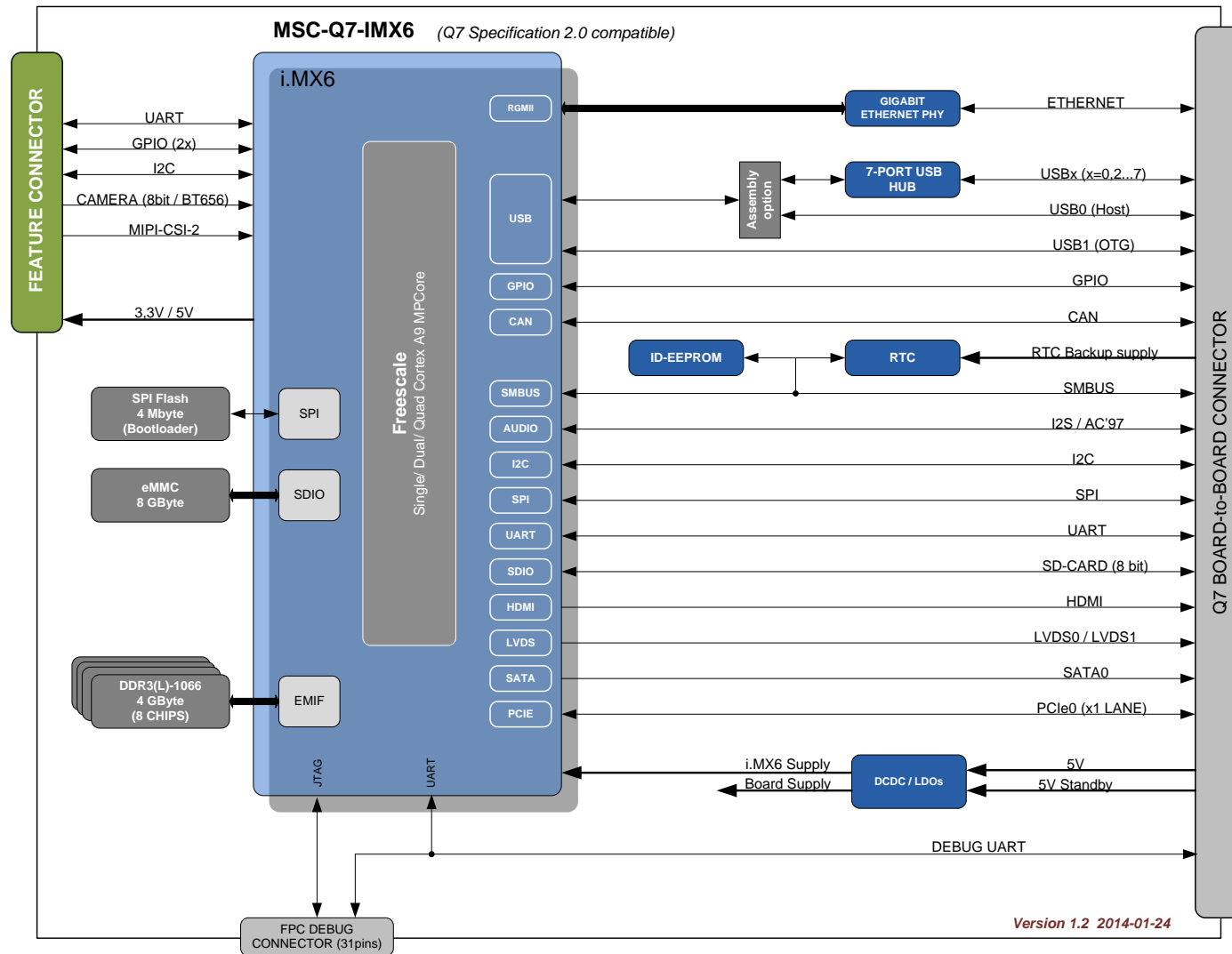
Figure 2-1: **Block diagram**

2.4   Qseven Implementation

Qseven® has mandatory and optional features. The following table shows the feature set of the Q7-IMX6 module compared to the minimum ARM/RISC based configuration.

System I/O Interface	ARM/RISC based minimum configuration	Q7-IMX6 configuration	ARM/RISC based maximum configuration
PCI Express lanes	0	1 (x1)	4
Serial ATA channels	0	1	2
USB 2.0 ports	3	2 minimum, up to 8	8
USB 3.0 ports	0	0	2
LVDS channels, embedded DisplayPort	0 / 0	Dual Channel LVDS / 0	Dual Channel 24 bits / 2
DisplayPort, TMDS	0	1 (HDMI)	1
High Definition Audio / AC'97 / I2S	0	1 (AC'97 or I2S)	1
Ethernet 10/100 Mbit/Gigabit	0	1 (Gigabit)	1 (Gigabit)
UART	0	1	1
Low Pin Count bus/ GPIOs	0	0 / 8x GPIO	1 or 8x GPIO
Secure Digital I/O 8-bit for SD/MMC cards	0	1	1
System Management Bus	0	1	1
I2C Bus	1	1	1
SPI Bus	0	1	1
CAN Bus	0	1	1
Watchdog Trigger	1	1	1
Power Button	1	1	1
Power Good	1	1	1
Reset Button	1	1	1
LID Button	0	1	1
Sleep Button	0	1	1
Suspend To RAM (S3 mode)	0	1	1
Wake	0	1	1
Battery low alarm	0	1	1
Thermal control	0	1	1
FAN control	0	1 (General Purpose PWM)	1
UART	Not specified	1 (on Feature connector)	Not specified
Parallel Camera (8 bit)	Not specified	1 (on Feature connector)	Not specified
MIPI-CSI2	Not specified	1 (on Feature connector)	Not specified

2.5   Power Supply

■ **+5V primary power supply input**

■ **+5V standby**:

Optional standby supply

⚠️ ***In case a standby supply is not present, connect the corresponding pins on the carrier board connector to the primary power supply.***

If not present as standby rail, suspend modes are not supported.

■ **RTC supply**:

Optional supply, not required for module operation

If not present, time and date information will be lost after removal of the standby supply rail.

2.6   Power Control

When +5V standby power is detected the Embedded Controller on the Q7-IMX6 module will enable the 5V primary power supply on the baseboard via the Qseven signal "Q7_SUS_S3#" (pin 18). No power button event is necessary.

As soon as the +5V primary supply is detected by the onboard supervisor and pin 26 ("Q7_PWGIN") of the Qseven connector shows a high level, the Embedded Controller will automatically start the power-up sequence of the i.MX6 and then start the bootloader.

⚠️ ***The board won't start with a low level on pin26 (Q7_PWGIN)!***

Pressing the power button (pin 20, "Q7_PWRBTN#") for more than 4s during running mode (S0) will switch off the system without notifying the software (power button override). The system will remain off until pressing (low edge) the power button again (in case a standby voltage is present).

A power failure during running mode causes the system to reset.

Onboard Supervisor	VCC = +5V (± 5%)	
	MIN	
V_{IH} @VCC_STBY = +5V (± 5%)	< 4.75V	
Q7_PWGIN	VCC = +5V (± 5%)	
	MIN	**MAX**
V_{IH}	0.7 x VCC	
V_{IL}		0.3 x VCC

2.7 Power Modes

The Q7-IMX6 module supports 4 different power modes:

- **G3 - Mechanical off:** optionally VCC_RTC can be present
- **S0 - Running:** The Q7-IMX6 module is running, all voltages are present
- **S3 - Suspend-to-RAM:**
  - Standby rail <u>must be</u> present (the Embedded Controller is running)
  - Baseboard is off except for interfaces powered by standby rail
  - CPU is partly on, some voltage may be switched off
  - Voltage scaling may be enabled

There may be some limitations or mutual dependencies regarding the use of interfaces related to Suspend-to-RAM.
Please check the processor vendor's webpage for chip errata and the MSC Q7-IMX6's software manuals for details.

- **S5 – Soft-Off:**
  - Standby rail <u>must be</u> present (the Embedded Controller is running)
  - CPU is off, Baseboard is off

2.8 Power Dissipation

Baseboard: MSC Q7-MB-EP4
MSC Q7-IMX6-143 (Freescale i.MX6 Quad) @ 792 MHz
RAM: 2 Gbyte, 64bit
Ethernet: connected
USB: disconnected
Graphics: DVI monitor

	Power Mode	Module Consumption @ Room temperature
Power supply disconnected, only RTC backup battery	G3	2.6V @ 880nA
System sent to S5 with "Power button override"	S5	0.08W
System sent to S3, Wake-on-lan enabled	S3	0.26W
Bootloader only; the bootloader is waiting at the command line, linux not started	S0	3.00W
Yocto Image started from sd-card, system idle, Ethernet link, DVI monitor is showing graphical user interface		2,50W
Yocto Image started from sd-card, memory test running, Ethernet link, DVI monitor shows ball demo		5.82W

Depending on the application running, the ambient temperature and the assembly variant chosen these values will differ. The numbers given in the table only serve as a rough guide.

2.9   Watchdog

The Q7-IMX6 module has a watchdog feature integrated in the IMX6. The watchdog can be enabled and disabled. Please see the software manual for details.

Any watchdog event creates a pulse on Q7_WDOUT (pin 72).

The watchdog can be serviced either by software or by hardware. The latter is done by pulling Q7_WDTRIG# (pin 70) low. The Q7_WDTRIG# signal has a pullup on the module so in case it is not used, it can be left floating.

3 Jumpers / Switches / LEDs

3.1 Jumpers

There are no jumpers.

3.2 Switches

There are no switches.

3.3 LEDs

There are five on-board LEDs. They are shown in the picture below:
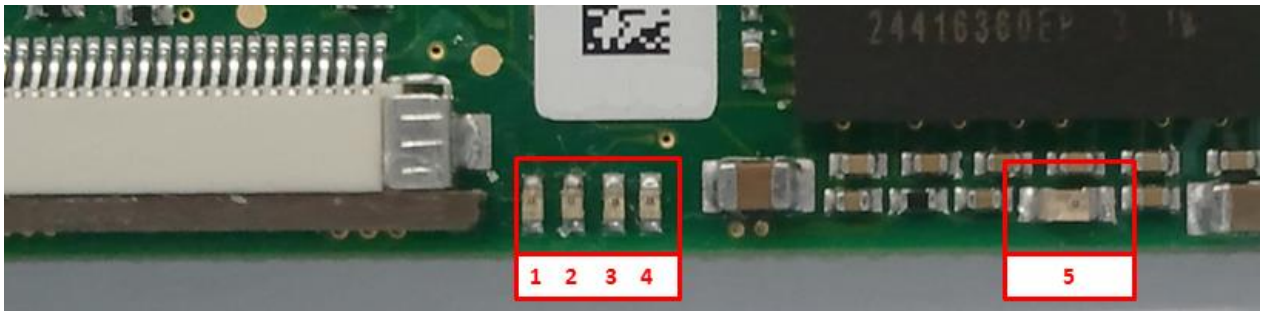
Figure 3-1: **LEDs**

	Type	Colour	Function	
1	Board Status LED1	Green	ON = BLINKING = OFF =	board is running in S0 and the power supply is ok board is running in S3 any other mode including power-up
2	Board Status LED2	Orange	ON = OFF =	Serial Downloader Mode / during wake-up from S3 Internal Boot from standard boot device
3	User LED2	Orange		General Purpose LED (IMX6 GPIO4.GPIO[15])
4	User LED1	Orange		General Purpose LED (IMX6 GPIO4.GPIO[8])
5	Reset	Red	ON = OFF =	Reset is active Reset is inactive

4   Thermal Specifications

4.1   Heat Spreader Concept

The cooling solution for a Qseven module is based on a heat spreader concept. The purpose of the heat spreader is to provide a standard thermal interface, it is not a heatsink.

A heat spreader is a metal plate (typically aluminium) mounted on top of the module. Its mechanical dimensions follow the module standard specification. The connection between the metal plate and the thermal active components on the module is typically made via thermal interface materials such as phase change foils, gap pads and metal blocks. A good thermal conductivity is required in order to transfer the heat from the hotspots to the heat spreader plate.

The heat spreader used for the Q7-IMX6 CPU module is thermally attached using phase change materials of different sizes (depending on the CPU type) and a small aluminium block that is part of the heat spreader plate.

4.2   MSC Q7-IMX6 HSP

The following drawings show the dimensions of the heat spreader. Depending on the CPU case gap pads with different thicknesses are used.

Also, there are additional holes for a heatsink:

Gap Pad

Gap Pad
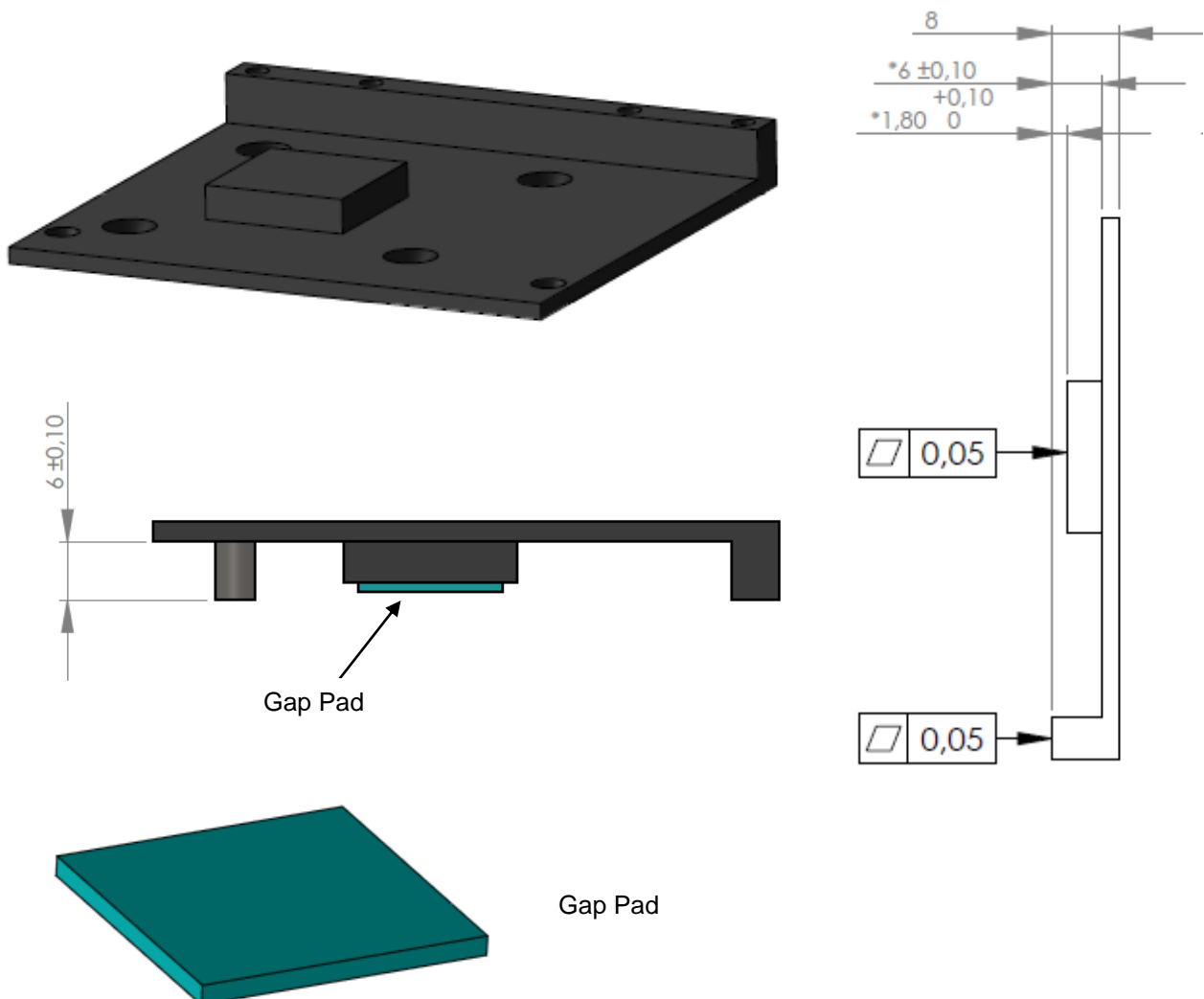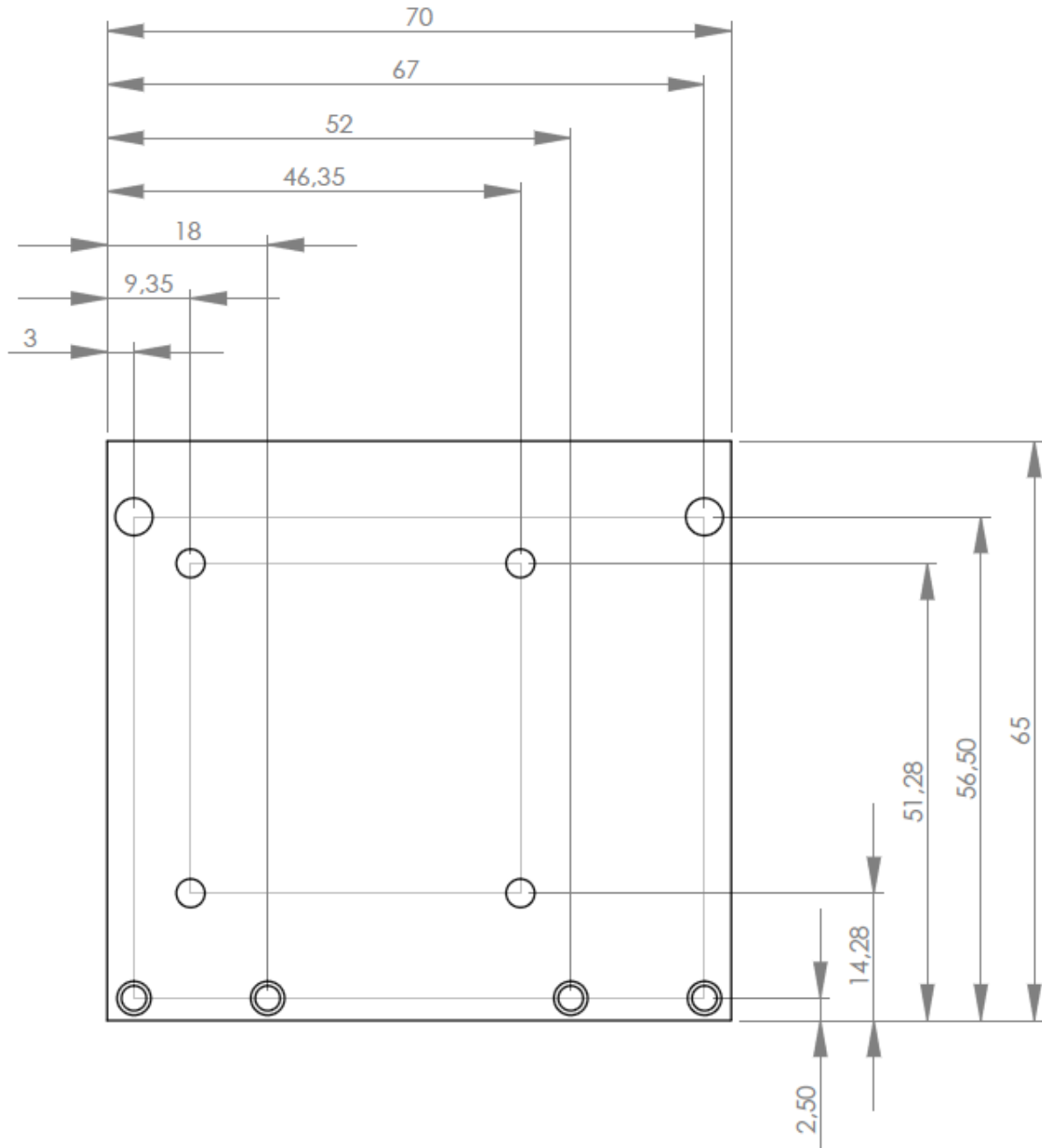
Figure 4-1: **Heat spreader – mechanical dimensions**

There might be circumstances that don't require any type of cooling solution and other cases that provide sufficient cooling just with the heat spreader. In any case it is the system designer's responsibility to make sure that each device in the system operates within its specified thermal limits. The cooling solution should ensure that the thermal specifications for each component are met over the full operating range of the system.

> ⚠️ *The heat spreader for the Q7-IMX6 modules may not be suited for extended temperature conditions as it has not been designed for that purpose.*

4.3   Identifying Critical Components

Thermal design is an important factor in creating a reliable system which is stable under all conditions. The thermally critical parts of the MSC Q7-IMX6 module are placed on the top side, so they can be easily connected to a heat spreader. For industrial temperature ranges also a heatsink will be necessary.

In order to identify the thermally active parts the following image will help:
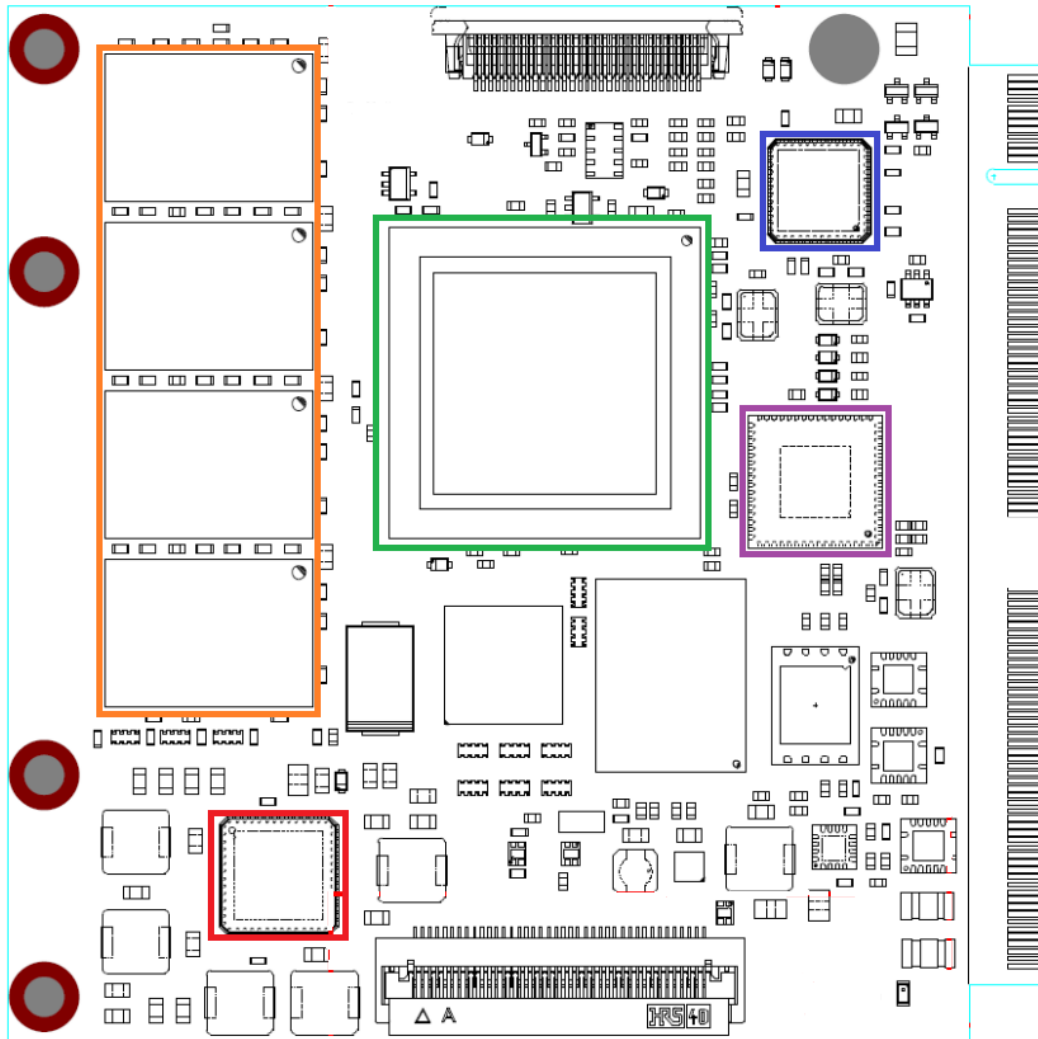
Figure 4-2: **Thermally active parts**

*Commercial grade parts (0/ +70°C) on variants that end in MSC Q7IMX6 -**0**xx:*

Colour	Component		Temperature Limit	Description
green	CPU	Dual / Quad Consumer	95°C	Junction Temperature
		Solo Consumer	95°C	Junction Temperature
orange	DDR3	NT5CC128M16FP-DII / NT5CC256M16CP-DII	95° C	Case Temperature
red	PMIC	MMPF0100	125°C	Junction Temperature
purple	USB-Hub	USB2517	125°C	Junction Temperature
blue	Ethernet Phy	KSZ9031RNX	125°C	Junction Temperature

*Industrial grade parts (-40/ +85°C) on variants that end in MSC Q7IMX6 -**1**xx:*

Colour	Component		Temperature Limit	Description
green	CPU	Dual / Quad Industrial	105°C	Junction Temperature
		Solo Industrial	105°C	Junction Temperature
orange	DDR3	NT5CC128M16FP-DI / NT5CC256M16CP-DI	95° C	Case Temperature
red	PMIC	MMPF0100	125°C	Junction Temperature
purple	USB-Hub	USB2517I	125°C	Junction Temperature
blue	Ethernet Phy	KSZ9031RNX	125°C	Junction Temperature

5　Mechanical Drawings
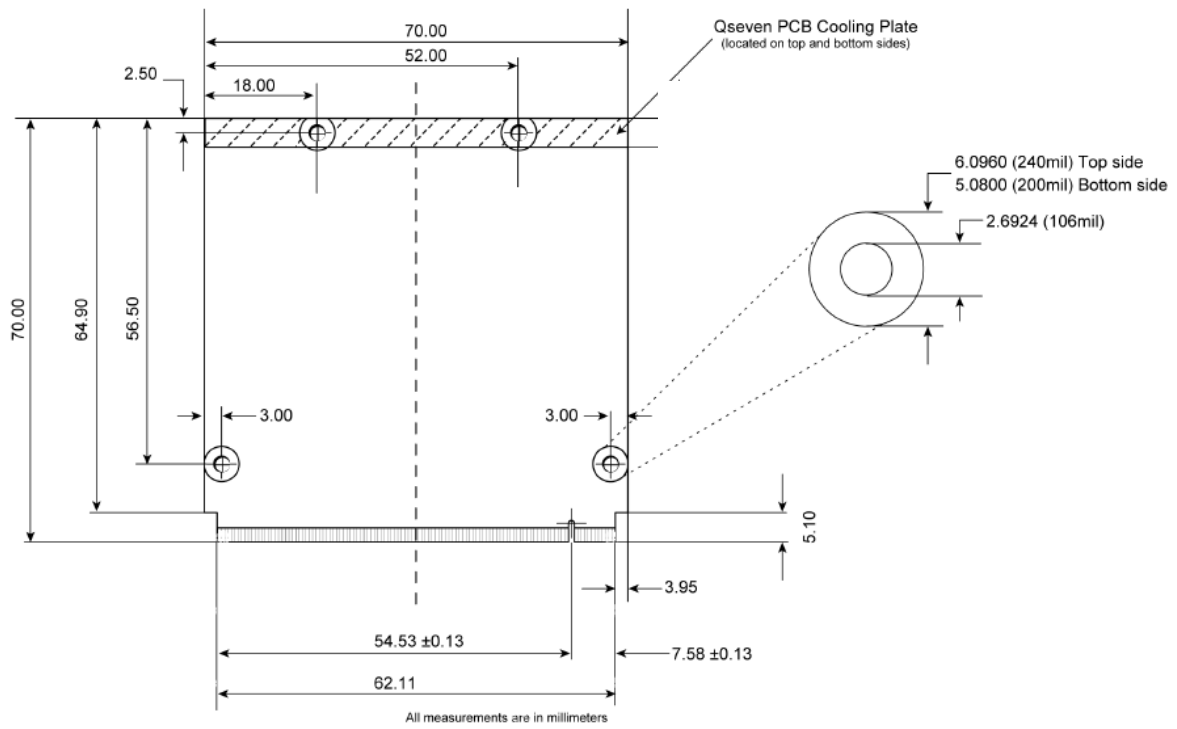
Figure 5-1: **Q7IMX6 module – mechanical dimensions**
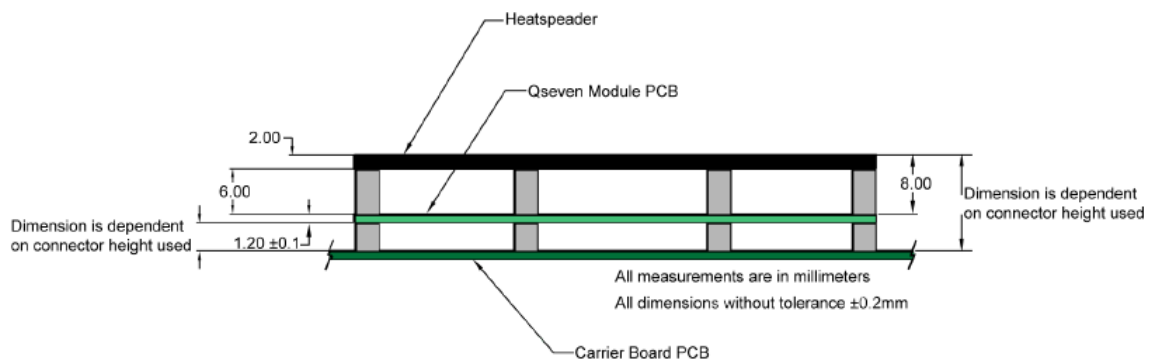
Figure 5-2: **Q7 system – mechanical dimensions**

The actual height depends on the Qseven connector used on the baseboard.

2x 2.5 x 12mm

2x 2.5 x 20mm

2x DIN7985 M2,5x6
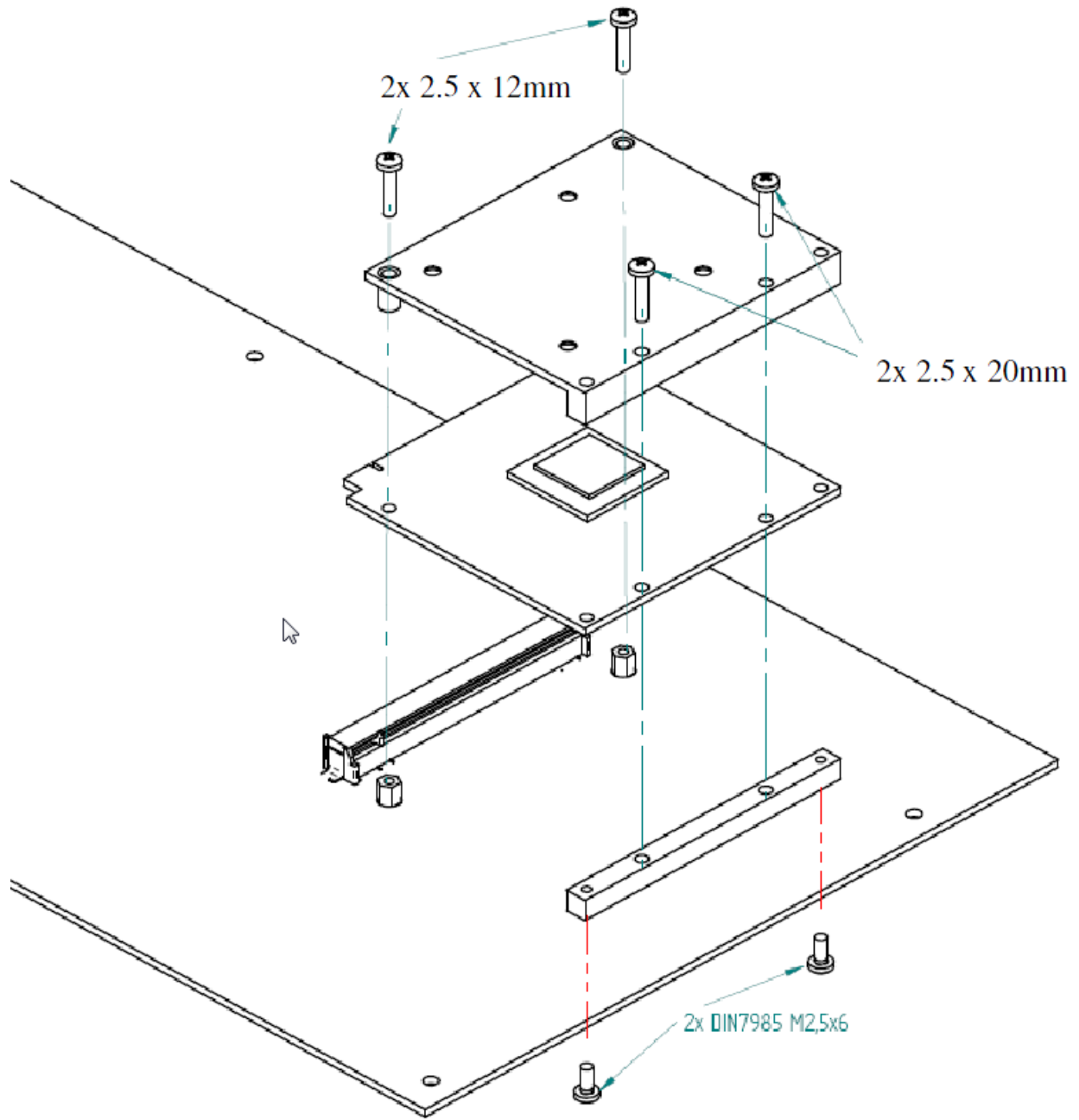
Figure 5-3: **Q7 – mounting the heatspreader**

6 Connectors

6.1 Overview
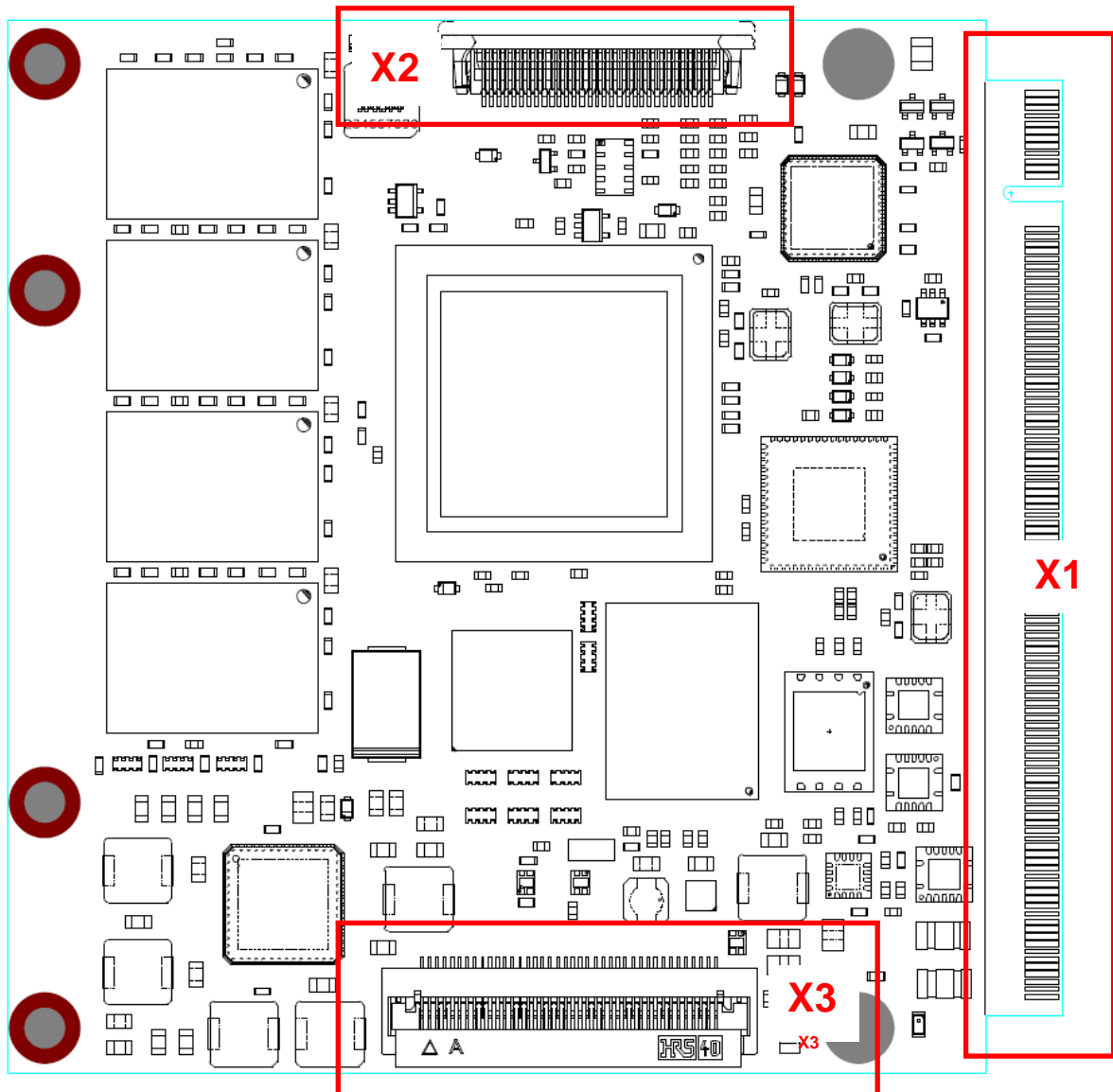
Figure 6-1: **Connector identification**

	Function	Description
X1	Qseven Finger – 230pins	Qseven edge contacts to connect to MXM connector (refer to Qseven specification)
X2	Debug Connector – 31 pins	Debug connector
X3	Qseven Feature Connector – 40pins	Optional Qseven I/O-Connector with additional features Type: *40 pin FPC connector, 0.5mm pitch, Hirose FH28-40S-0.5SH*

6.2 MXM Connector (X1)
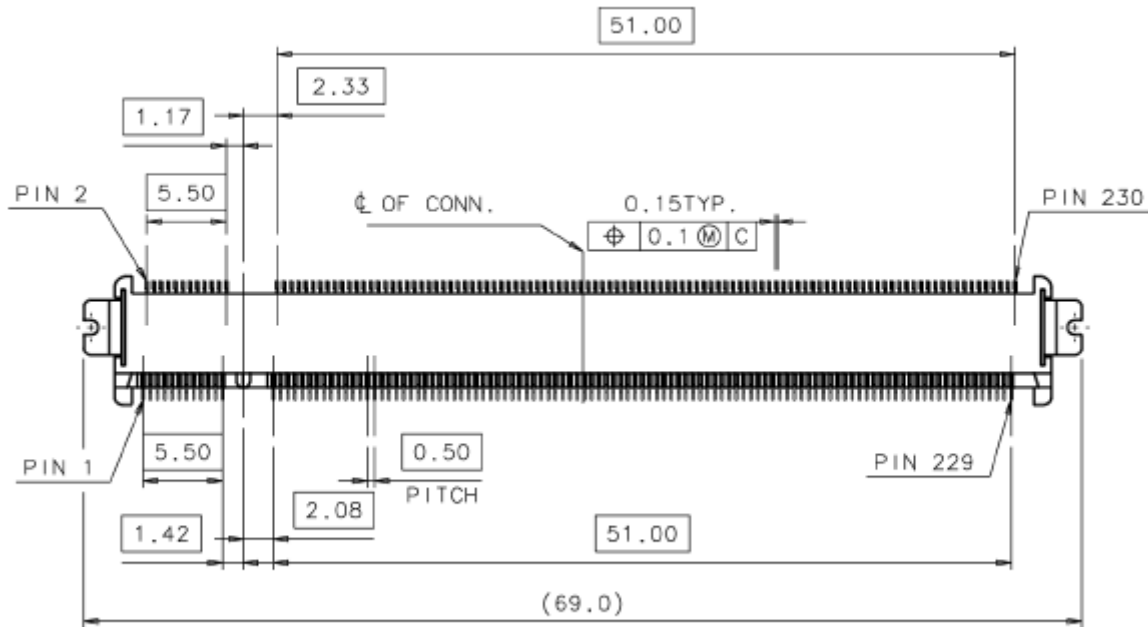
Figure 6-2: **MXM connector dimensions**

⚠️   *Signals in grey are not available on the MSC-Q7-IMX6 module*

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
KEY			
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE# / BOOT_ALT#	42	SDIO_CLK#
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP

47	SDIO_PWR#		48	SDIO_DAT1
49	SDIO_DAT0		50	SDIO_DAT3
51	SDIO_DAT2		52	SDIO_DAT5
53	SDIO_DAT4		54	SDIO_DAT7
55	SDIO_DAT6		56	RSVD
57	GND		58	GND
59	HDA_SYNC / AC97_SYNC / I2S_WS		60	SMB_CLK / GP1_I2C_CLK
61	HDA_RST# / AC97_RST# / I2S_RST#		62	SMB_DAT / GP1_I2C_DAT
63	HDA_BITCLK / AC97_BITCLK / I2S_CLK		64	SMB_ALERT#
65	HDA_SDI / AC97_SDI / I2S_SDI		66	I2C_CLK
67	HDA_SDO / AC97_SDO / I2S_SDO		68	I2C_DAT
69	THRM#		70	WDTRIG#
71	THRMTRIP#		72	WDOUT
73	GND		74	GND
75	USB_P7- / USB_SSTX0-		76	USB_P6- / USB_SSRX0-
77	USB_P7+ / USB_SSTX0+		78	USB_P6+ / USB_SSRX0+
79	USB_6_7_OC#		80	USB_4_5_OC#
81	USB_P5- / USB_SSTX1-		82	USB_P4- / USB_SSRX1-
83	USB_P5+ / USB_SSTX1+		84	USB_P4+ / USB_SSRX1+
85	USB_2_3_OC#		86	USB_0_1_OC#
87	USB_P3-		88	USB_P2-
89	USB_P3+		90	USB_P2+
91	USB_ VBUS		92	USB_ID
93	USB_P1-		94	USB_P0-
95	USB_P1+		96	USB_P0+
97	GND		98	GND
99	eDP0_TX0+ / LVDS_A0+		100	eDP1_TX0+ / LVDS_B0+
101	eDP0_TX0- / LVDS_A0-		102	eDP1_TX0- / LVDS_B0-
103	eDP0_TX1+ / LVDS_A1+		104	eDP1_TX1+ / LVDS_B1+
105	eDP0_TX1- / LVDS_A1-		106	eDP1_TX1- / LVDS_B1-
107	eDP0_TX2+ / LVDS_A2+		108	eDP1_TX2+ / LVDS_B2+
109	eDP0_TX2- / LVDS_A2-		110	eDP1_TX2- / LVDS_B2-
111	LVDS_PPEN		112	LVDS_BLEN
113	eDP0_TX3+ / LVDS_A3+		114	eDP1_TX3+ / LVDS_B3+
115	eDP0_TX3- / LVDS_A3-		116	eDP1_TX3- / LVDS_B3-
117	GND		118	GND
119	eDP0_AUX+ / LVDS_A_CLK+		120	eDP1_AUX+ / LVDS_B_CLK+
121	eDP0_AUX- / LVDS_A_CLK-		122	eDP1_AUX- / LVDS_B_CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0		124	GP_1-WIRE_BUS
125	LVDS_DID_DAT / GP_I2C_DAT		126	eDP0_HPD# / LVDS_BLC_DAT
127	LVDS_DID_CLK / GP_I2C_CLK		128	eDP1_HPD# / LVDS_BLC_CLK
129	CAN0_TX		130	CAN0_RX
131	DP_LANE3+ / HDMI_TMDS_CLK+		132	LVDS1_PPEN
133	DP_LANE3- / HDMI_TMDS_CLK-		134	LVDS1_BLEN
135	GND		136	GND
137	DP_LANE1+ / HDMI_TMDS_LINE1+		138	DP_AUX+
139	DP_LANE1- / HDMI_TMDS_LINE1-		140	DP_AUX-
141	GND		142	GND
143	DP_LANE2+ / HDMI_TMDS_LINE0+		144	RSVD
145	DP_LANE2- / HDMI_TMDS_LINE0-		146	RSVD

147	GND		**148**	GND
149	DP_LANE0+ / HDMI_TMDS_LINE2+		**150**	HDMI_CTRL_DAT
151	DP_LANE0- / HDMI_TMDS_LINE2-		**152**	HDMI_CTRL_CLK
153	HDMI_HPD#		**154**	RSVD
155	PCIE_CLK_REF+		**156**	PCIE_WAKE#
157	PCIE_CLK_REF-		**158**	PCIE_RST#
159	GND		**160**	GND
161	PCIE3_TX+		**162**	PCIE3_RX+
163	PCIE3_TX-		**164**	PCIE3_RX-
165	GND		**166**	GND
167	PCIE2_TX+		**168**	PCIE2_RX+
169	PCIE2_TX-		**170**	PCIE2_RX-
171	UART0_TX		**172**	UART0_RTS#
173	PCIE1_TX+		**174**	PCIE1_RX+
175	PCIE1_TX-		**176**	PCIE1_RX-
177	UART0_RX		**178**	UART0_CTS#
179	PCIE0_TX+		**180**	PCIE0_RX+
181	PCIE0_TX-		**182**	PCIE0_RX-
183	GND		**184**	GND
185	LPC_AD0 / GPIO0		**186**	LPC_AD1 / GPIO1
187	LPC_AD2 / GPIO2		**188**	LPC_AD3 / GPIO3
189	LPC_CLK / GPIO4		**190**	LPC_FRAME# / GPIO5
191	SERIRQ / GPIO6		**192**	LPC_LDRQ# / GPIO7
193	VCC_RTC		**194**	SPKR / GP_PWM_OUT2
195	FAN_TACHOIN / GP_TIMER_IN		**196**	FAN_PWMOUT / GP_PWM_OUT1
197	GND		**198**	GND
199	SPI_MOSI		**200**	SPI_CS0#
201	SPI_MISO		**202**	SPI_CS1#
203	SPI_SCK		**204**	MFG_NC4
205	VCC_5V_SB		**206**	VCC_5V_SB
207	MFG_NC0		**208**	MFG_NC2
209	MFG_NC1		**210**	MFG_NC3
211	VCC		**212**	VCC
213	VCC		**214**	VCC
215	VCC		**216**	VCC
217	VCC		**218**	VCC
219	VCC		**220**	VCC
221	VCC		**222**	VCC
223	VCC		**224**	VCC
225	VCC		**226**	VCC
227	VCC		**228**	VCC
229	VCC		**230**	VCC

6.3   Debug Connector (X2)

The MSC Q7-IMX6 module has a connector which enables connection to a debug adapter provided by MSC Vertriebs GmbH. That connector is not intended for customer's use and limited to debugging and programming purposes only.

6.4   Feature Connector (X3)

X3 is an optional connector with extra features. It's located on the top side of the module. The following features are supported:

■ Serial Port (LVTTL):
  A serial port with hardware handshaking (RTS, CTS) is also provided. An external transceiver is necessary for RS232, for example.

■ Camera Interface (BT656)
  8 bit parallel camera interface with pixel clock and I2C interface.

■ MIPI-CSI-2:
  Serial camera interface with 3 differential data pairs.

Type: 40 pin FPC connector, 0.5mm pitch, Hirose FH28-40S-0.5SH

Pin	Signal	Description	I/O
1	CAM_D0	Camera Data Bit 0 (*LSB)*	IN
2	CAM_D1	Camera Data Bit 1	IN
3	CAM_D2	Camera Data Bit 2	IN
4	CAM_D3	Camera Data Bit 3	IN
5	CAM_D4	Camera Data Bit 4	IN
6	CAM_D5	Camera Data Bit 5	IN
7	CAM_D6	Camera Data Bit 6	IN
8	CAM_D7	Camera Data Bit 7 (*MSB*)	IN
9	GND	Signal ground	-
10	CAM_SHFCLK	Camera pixel clock	IN
11	GND	Signal ground	-
12	CAM_I2C_SDA	Camera I2C Data (*I2C addresses shared with HDMI DDC Control Signals / LVDS DDC Control Signals*)	IN/ OUT
13	CAM_I2C_SCL	Camera I2C Clock (*I2C addresses shared with HDMI DDC Control Signals / LVDS DDC Control Signals*)	OUT
14	GND	Signal Ground	-
15	MIPI_CSI_CLK0+	MIPI-CSI-2: positive differential clock signal	IN
16	MIPI_CSI_CLK0-	MIPI-CSI-2: negative differential clock signal	IN
17	GND	Signal Ground	-
18	MIPI_CSI_D0+	MIPI-CSI-2: positive differential data signal – lane 0	IN
19	MIPI_CSI_D0-	MIPI-CSI-2: negative differential data signal – lane 0	IN

20	GND	Signal Ground	-
21	MIPI_CSI_D1+	MIPI-CSI-2: positive differential data signal – lane 1	IN
22	MIPI_CSI_D1-	MIPI-CSI-2: negative differential data signal – lane 1	IN
23	GND	Signal Ground	-
24	MIPI_CSI_D2+	MIPI-CSI-2: positive differential data signal – lane 2	IN
25	MIPI_CSI_D2-	MIPI-CSI-2: negative differential data signal – lane 2	IN
26	GND	Signal Ground	-
27	MIPI_CSI_D3+	MIPI-CSI-2: positive differential data signal – lane 3	IN
28	MIPI_CSI_D3-	MIPI-CSI-2: negative differential data signal – lane 3	IN
29	GND	Signal Ground	-
30	GP_PWM_OUT3	PWM signal	OUT
31	GND	Signal Ground	-
32	GPIO0	General purpose input / output	IN/ OUT
33	GPIO1	General purpose input / output	IN/ OUT
34	COM_TXD	Serial Port – Transmit Data *(LVTTL)*	OUT
35	COM_RXD	Serial Port – Receive Data *(LVTTL)*	IN
36	COM_CTS#	Serial Port – Clear to send *(LVTTL – low active)*	IN
37	COM_RTS#	Serial Port – Ready to send *(LVTTL – low active)*	OUT
38	GND	Signal Ground	-
39	VCC3V3_DEL	3,3V +/- 5% power supply (sequenced I/O voltage), maximum current 300mA (not fused)	-
40	VCC5V0_Q7	5V +/- 5% power supply, maximum current 500mA (not fused)	-

7   Signal Description

In the following tables signals are marked with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different.

An additional label, "Suspend", indicates that the pin is active during suspend states when available. If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

Signal Terminology

■   Signal direction: Signal directions are from the perspective of the module.
    For example: SATA0_TX+ (SATA, port0, transmit) is an output from the CPU module

■   The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is active at a high voltage level

■   Differential pairs are indicated by trailing "+" and "-" signs for the positive or negative signal, respectively

Abbreviation	Description
I	Input
O	Output
OD	Open Drain Output
I/OD	Bi-directional Input/ Open Drain Output Pin
I/O	Bi-directional Input/ Output
ePU	External pull-up resistor (on module)
ePD	External pull-down resistor (on module)
eSR	External series resistor (on module)
eSC	External AC-coupling capacitor (on module)
iPU	Integrated pull-up resistor (inside CPU or IC)
iPD	Integrated pull-down resistor (inside CPU or IC)
REF	Reference voltage

7.1   PCI Express

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
PCIE0_TX+ PCIE0_TX-	O	PCIe	CPU	AC coupled on module	eSC = 100nF	PCI Express Differential Transmit Pairs 0	CPU
PCIE0_RX+ PCIE0_RX-	I	PCIe	CPU	Requires AC coupling on baseboard		PCI Express Differential Receive Pairs 0	CPU
PCIE_CLK_REF+ PCIE_CLK_REF-	O	HCSL	CPU		Integrated Termination	Differential Reference Clock output for all PCI Express lanes.	Clock Buffer

7.2   Serial ATA

Signal	Pin Type	Signal Level	Power Rail	Remark	PU/PD/SR/SC	Description	Source / Target
SATA0_TX+ SATA0_TX-	O	SATA	CPU	AC coupled on module	eSC = 10nF	Serial ATA Channel 0: differential transmit pair.	CPU
SATA0_RX+ SATA0_RX-	I	SATA	CPU	AC coupled on module	eSC = 10nF	Serial ATA Channel 0: differential receive pair.	CPU

7.3   Ethernet

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD/SR/SC	Description	Source / Target
GBE_MDI[0:3]+ GBE_MDI[0:3]-	I/O	Analog	ETH			Gigabit Ethernet Controller: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. **1000BASE-T** *MDI configuration:* *MDI-X configuration:* MDI[0]+/- BI_DA+/- MDI[0]+/- BI_DB+/- MDI[1]+/- BI_DB+/- MDI[1]+/- BI_DA+/- MDI[2]+/- BI_DC+/- MDI[2]+/- BI_DD+/- MDI[3]+/- BI_DD+/- MDI[3]+/- BI_DC+/- **100BASE-TX/ 10BASE-T** *MDI configuration:* *MDI-X configuration:* MDI[0]+/- Transmit MDI[0]+/- Receive MDI[1]+/- Receive MDI[1]+/- Transmit MDI[2]+/- *unused* MDI[2]+/- *unused* MDI[3]+/- *unused* MDI[3]+/- *unused*	GBE PHY
GBE_ACT#	PP	CMOS	ETH	3.3V	ePU = 10k	Gigabit Ethernet Controller: activity indicator, active low.	GBE PHY
GBE_LINK#	PP	CMOS	ETH	3.3V	ePU = 10k	Gigabit Ethernet Controller: link indicator, active low.	GBE PHY
GBE_CTREF	REF					Center Tap Voltage: Connected to GND via 100nF	---

7.4   USB

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
USB_P0+ USB_P0-	I/O	USB	USB	3.3V		USB differential pair, channels 0	CPU or USB-Hub***
USB_P1+ USB_P1-	I/O	USB	USB	3.3V		USB differential pair, channels 1 This port may be optionally used as USB client port ***NOTE: This port has to be accessible on the carrier board for USB RECOVERY mode.***	CPU
USB[2:7]+ USB[2:7]-	I/O	USB	USB	3.3V		USB differential pairs, channels 2 to 7	USB-Hub***
USB_0_1_OC#	I	CMOS	3.3V		ePU = 10k	USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	CPU & USB-HUB***
USB_2_3_OC#	I	CMOS	3.3V		ePU = 10k	USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB-Hub***
USB_4_5_OC#	I	CMOS	3.3V		ePU = 10k	USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB-Hub***
USB_6_7_OC#	I	CMOS	3.3V		ePU = 10k	USB over-current sense, USB channels 6 and 7. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB-Hub***
USB_ID	I	ANALOG				USB ID pin	CPU
USB_DRIVE_VBUS	O	CMOS	3.3V		ePD = 10k	Enable VBUS on the Carrier Board for USB Port 1	CPU
USB_VBUS	Power		5V			USB VBUS pin	CPU

*** Depends on module version: Please check the datasheet for the different assembly variants (with and without USB-HUB)

7.5   SDIO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
SDIO_DAT[7:0]	I/O	CMOS	CPU	3.3V	iPU = 100k	SDIO Controller Data	CPU
SDIO_CD#	I	CMOS	CPU	3.3V	iPU = 22k	SDIO Controller Card Detect	CPU
SDIO_CMD	I/O	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	SDIO Controller Command	CPU
SDIO_CLK#	O	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	SDIO Controller Clock	CPU
SDIO_PWR#	O	CMOS	CPU	3.3V	iPD = 100k	SDIO Controller Power enable	CPU
SDIO_LED	O	CMOS	3.3V			SDIO Controller transfer activity LED	CPU
SDIO_WP	I	CMOS	CPU	3.3V	iPU = 100k	SDIO Controller Write Protect	CPU

7.6   Audio – AC97/ I2S

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
AC97_RST# / I2S_RST#	Output	CMOS	3.3V		iPU = 10k…110k	Reset output to CODEC, active low.	Embedded Controller
AC97_SYNC / I2S_WS	Output	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	Serial Bus Synchronisation Multiplexed with I2S Word Select.	CPU
AC97_BCLK I2S_CLK	Output	CMOS	CPU	3.3V	iPU = 100k	AC'97 Serial Bit Clock. Multiplexed with I2S Serial data Clock.	CPU
AC97_SDO I2S_SDO	Output	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	AC'97 Serial Data Output. Multiplexed with I2S Serial Data Output.	CPU
AC97_SDI I2S_SDI	Input	CMOS	CPU	3.3V	iPU = 100k	AC'97 Serial Data Input. Multiplexed with I2S Serial Data Input.	CPU

7.7   LVDS Flat Panel

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
LVDS_A[0:3]+ LVDS_A[0:3]-	O	LVDS	CPU			LVDS Channel A differential pairs – primary channel	CPU
LVDS_A_CLK+ LVDS_A_CLK-	O	LVDS	CPU			LVDS Channel A differential clock	CPU
LVDS_B[0:3]+ LVDS_B[0:3]-	O	LVDS	CPU			LVDS Channel B differential pairs – secondary channel	CPU
LVDS_B_CLK+ LVDS_B_CLK-	O	LVDS	CPU			LVDS Channel B differential clock	CPU
LVDS_PPEN	O	CMOS	CPU	3.3V	ePD = 1k	LVDS panel power enable	CPU
LVDS_BLEN	O	CMOS	CPU	3.3V	ePD = 1k	LVDS panel backlight enable	CPU
LVDS_BLT_CTRL	O	CMOS	CPU	3.3V	iPU = 100k	LVDS panel backlight brightness control	CPU
LVDS_DID_CLK	I/O OD	CMOS	3.3V		ePU = 2,7k	I2C clock output for LVDS display use (multiplexed bus)	CPU / Buffer
LVDS_DID_DAT	I/O OD	CMOS	3.3V		ePU = 2,7k	I2C data line for LVDS display use (multiplexed bus)	CPU / Buffer

7.8   HDMI

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
TMDS_LANE0+ TMDS_LANE0-	O	HDMI	CPU			TMDS differential pair lines lane 0	CPU
TMDS_LANE1+ TMDS_LANE1-	O	HDMI	CPU			TMDS differential pair lines lane 1	CPU
TMDS_LANE2+ TMDS_LANE2-	O	HDMI	CPU			TMDS differential pair lines lane 2	CPU
TMDS_CLK+ TMDS_CLK-	O	HDMI	CPU			TMDS differential pair clock lines	CPU
HDMI_HPD#	I	CMOS	3.3V		ePU = 10k	Hot plug detection signal that serves as an interrupt request.	CPU
HDMI_CTRL_CLK	I/O OD	CMOS	3.3V		ePU = 2,7k	DDC based control signal (clock) for HDMI device (multiplexed bus)	CPU / Buffer
HDMI_CTRL_DAT	I/O OD	CMOS	3.3V		ePU = 2,7k	DDC based control signal (data) for HDMI device(multiplexed bus)	CPU / Buffer

7.9   GPIO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
GPIO[0..3] (LPC_AD[0..3])	I/O	3.3V			iPD = 100k eSR = 33R	General purpose input/output [0..3]	CPU
GPIO4 (LPC_CLK)	I/O	3.3V			iPD = 100k eSR = 33R	General purpose input/output 4.	CPU
GPIO5 (LPC_FRAME#)	I/O	3.3V			iPD = 100k eSR = 33R	General purpose input/output 5.	CPU
GPIO6 (SERIRQ)	I/O	3.3V			iPD = 100k eSR = 33R	General purpose input/output 6.	CPU
GPIO7 (LPC_LDRQ#)	I/O	3.3V			iPD = 100k eSR = 33R	General purpose input/output 7.	CPU

7.10 CAN

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
CAN0_TX	O	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CPU
CAN0_RX	I	CMOS	CPU	3.3V	iPU = 100k	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CPU

7.11 SPI Interface

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
SPI_MOSI	O	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	Master serial output / Slave input signal – CPU is master	CPU
SPI_MISO	I	CMOS	CPU	3.3V	iPU = 100k	Master serial input / Slave output signal – CPU is master	CPU
SPI_SCK	O	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	SPI clock input	CPU
SPI_CS0#	O	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	SPI chip select 0 output, active low (chip select for primary device)	CPU
SPI_CS1#	O	CMOS	CPU	3.3V	iPU = 100k eSR = 33R	SPI chip select 1 output, active low (chip select for secondary device)	CPU

7.12 UART

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
UART0_TX	O	CMOS	CPU	3.3V	iPU = 100k	Serial Data Transmitter	CPU
UART0_RX	I	CMOS	CPU	3.3V	iPU = 100k	Serial Data Receiver	CPU
UART0_CTS#	I	CMOS	CPU	3.3V	iPU = 100k	Handshake signal, ready to send data	CPU
UART0_RTS#	O	CMOS	CPU	3.3V	iPU = 100k	Handshake signal, ready to receive data	CPU

7.13 Input Power Pins

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
VCC	Power		5V	(±5%)		Primary power input: +5V (±5%)	Voltage Regulators
VCC_5V0_SB	Power		5V	(±5%)		Standby power input: +5.0V (±5%) All available VCC5V0_STBY pins on the connector(s) shall be used. Used for embedded controller, standby and suspend functions. If no standby power is available connect to VCC.	Voltage Regulators
VCC_RTC	Power					Real-time clock circuit-power input : typ. +3.0V (+2.0V to +3.3V)	RTC
GND	Power					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

7.14 Manufacturing Signals

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
MFG_NC1	O	CMOS	3.3V	3.3V		COM_TXD: transmit signal for the serial debug port (UART)	Buffer / CPU
MFG_NC2	I	CMOS	3.3V	3.3V	ePU = 10k	COM_RXD: receive signal for the serial debug port (UART)	Buffer / CPU
MFG_NC3	I	CMOS	3.3V	3.3V	ePU = 10k	USB_RECOVERY#: 1: Internal Boot 0: USB Recovery (= Serial Downloader Mode)	Buffer / CPU
MFG_NC4	I	CMOS	3.3V	3.3V	ePD = 100k	Control Signal for multiplexer circuit: 1: RESERVED (choose this setting when the MFG Pins are not used) 0: UART & USB Recovery	Buffer / CPU

For more information on manufacturing pins and USB Recovery Mode see chapter 9.1.

7.15 Power And System Management

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
PWRBTN#	I	CMOS	Suspend	3.3V	iPU = 10k…110k	Power button to bring system into a power state, active low	Embedded Controller
RSTBTN#	I	CMOS	3.3V		iPU = 10k…110k	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.	Embedded Controller
LID_BTN#	I	CMOS	Suspend	3.3V	iPU = 10k…110k	LID button. Low active signal used to detect a LID switch and to bring system into sleep state or to wake it up again.	Embedded Controller
SLP_BTN#	I	CMOS	Suspend	3.3V	iPU = 10k…110k	Sleep button. Low active signal used to transition the system into sleep state or to wake it up again. This signal is triggered on the falling edge.	Embedded Controller
WAKE#	I	CMOS	Suspend	3.3V	iPU = 10k…110k	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	Embedded Controller
PCIE_WAKE#	I	CMOS	Suspend	3.3V	iPU = 10k…110k	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	Embedded Controller
BATLOW#	I	CMOS	Suspend	3.3V	iPU = 10k…110k	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	Embedded Controller
SUS_STAT#	O	CMOS	Suspend	3.3V	iPD = 10k…110k	Indicates low power suspend operation	Embedded Controller
SUS_S3#	O	CMOS	Suspend	3.3V	iPD = 10k…110k	Indicates that the system is in Suspend to RAM state. Active low output.	Embedded Controller
SUS_S5#	O	CMOS	Suspend	3.3V	iPD = 10k…110k	Indicates that the system is in Soft Off state. Active low output.	Embedded Controller
SMB_ALERT#	I	CMOS	Suspend	3.3V	iPU = 10k…110k	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	Embedded Controller
THRM#	I	CMOS	3.3V		iPU = 10k…110k	Input from off-module temp sensor indicating an over-temp situation.	Embedded Controller
THERMTRIP#	O	CMOS	3.3V		iPU = 100k	Active low output indicating that the CPU has entered thermal shutdown.	CPU
PWGIN	I	5V CMOS	5.0V	5V		Indicates that the external power supply is ready	Embedded Controller

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD/SR/SC	Description	Source / Target
WDOUT	O	CMOS	3.3V			Output indicating that a watchdog time-out event has occurred.	CPU
WDTRIG#	I	CMOS	3.3V		iPU = 10k…110k	Watchdog trigger input. This signal restarts the watchdog timer	Embedded Controller
GP_PWM_OUT1	O	CMOS	3.3V		iPU = 100k eSR = 33R	General purpose PWM output	CPU
GP_PWM_OUT2	O	CMOS	3.3V		iPU = 100k eSR = 33R	General purpose PWM output	CPU
SMB_CLK	I/O	CMOS	3.3V		ePU = 2,7k	System management clock line	CPU
SMB_DAT	I/O	CMOS	3.3V		ePU = 2,7k	System management data line	CPU
SMB_ALERT#	I/O	CMOS	3.3V		iPU = 10k…110k	System management bus alert input	CPU
I2C_CLK	I/O	CMOS	3.3V		ePU = 2,7k	General purpose I2C port clock output	CPU / Buffer
I2C_DAT	I/O	CMOS	3.3V		ePU = 2,7k	General purpose I2C port data I/O line	CPU / Buffer

8 System Resources

8.1 I2C Bus Address Map

There are no devices on the I^{2}C-Bus (GP0_I2C_CLK & GP0_I2C_DAT).
There are no blocked addresses.

8.2 SMBus Address Map

The devices listed in the following table can be found on the SMBus (SMB_CLK & SMB_DAT):

Device	A6	A5	A4	A3	A2	A1	A0	R/W	Address **	Address *
Power Management Chip	0	0	0	1	0	0	0	x	10_h / 11_h	08_h
CPLD	1	0	0	0	0	0	0	x	80_h / 81_h	40_h
	1	0	0	0	0	1	1	x	86_h / 87_h	43_h
PCIe Clock Buffer	1	1	0	1	0	1	1	x	$D6_h$ / $D7_h$	$6B_h$
ID-EEPROM	1	0	1	0	0	0	0	x	$A0_h$ / $A1_h$	50_h
Onboard RTC	1	0	1	0	1	1	0	x	AC_h / AD_h	56_h

 * 7 bit address (without R/W)

** 8 bit address (with R/W)

> ⚠️ ***Please take care when using additional SMBus devices on the Qseven carrier board to ensure that there are no address conflicts.***
> ***For example, the ATMEL AT24C16C has address conflicts with the ID-EEPROM and the onboard RTC of the module.***

8.3   PCI Express Lanes

The Q7-IMX6 module supports one (x1) lane

Signal / Slot	Source
PCIE0_TX+	i.MX6
PCIE0_TX-	i.MX6
PCIE0_RX+	i.MX6
PCIE0_RX-	i.MX6

The PCIe Clock is a 100 MHz differential clock generated by the i.MX6 and routed to a clock buffer with integrated termination.

The "PCIE_CLK_REF" signals on the Qseven connector (pins 155 / 157) have HCSL levels.

8.4   USB Ports

The Q7-IMX6 module supports two possible options:

- 8 USB Ports – with on-module USB Hub

- 2 USB Ports – without on-module USB Hub

> ⚠ *Please note that the minimum configuration with only 2 USB Ports is not compliant with the Qseven specification (see chapter 2.4). There are at least 3 USB Ports required. This low cost implementation may lead to compatibility issues on some baseboards due to a reduced function set.*

2 USB Ports:

Signal	Remark	Source / Target
USB_P0+ USB_P0-	USB1.1 / USB2.0	CPU
USB_P1+ USB_P1-	USB1.1 / USB2.0 with OTG support NOTE: This port is also used as USB-Recovery Port	CPU

8 USB Ports

Signal	Remark	Source / Target
USB_P0+ USB_P0-	USB1.1 / USB2.0	USB Hub
USB_P1+ USB_P1-	USB1.1 / USB2.0 with OTG support NOTE: This port is also used as USB-Recovery Port	CPU
USB_P2+ USB_P2-	USB1.1 / USB2.0	USB Hub
USB_P3+ USB_P3-	USB1.1 / USB2.0	USB Hub
USB_P4+ USB_P4-	USB1.1 / USB2.0	USB Hub
USB_P5+ USB_P5-	USB1.1 / USB2.0	USB Hub
USB_P6+ USB_P6-	USB1.1 / USB2.0	USB Hub
USB_P7+ USB_P7-	USB1.1 / USB2.0	USB Hub

8.5   Graphical Interfaces

The Q7-IMX6 module supports a total of three displays, i.e. a HDMI monitor and two LVDS panels can be used at the same time.

The HDMI monitor supports a hot plug detect signal (pin 153, "HDMI_HPD# ") and Full HD resolution (1920 x 1080).

The Q7-IMX6 module has two LVDS ports, A and B, which can either be used for one panel with up to 165 $^{Mpixel}/_s$ or as two separate ports up to 85 $^{Mpixel}/_s$. In either configuration, the Qseven specification only provides one set of backlight and panel power enable signals as well as one brightness control signal for both of them. For Display ID. data can be stored in an EEPROM on the baseboard with information on both panels having different offsets. The signals used for Display ID are LVDS_DID_DAT (pin 125) and LVDS_DID_CLK (pin 127).

 For more information please refer to the software manual.

8.5.1   One LVDS Panel / 1 Port

The simplest solution is to connect one display to port A. In that case, LVDS_B signals are not used. The panel can be enabled with the LVDS_PPEN signal (pin 111) and the backlight can be switched on with LVDS_BLEN (pin 112).
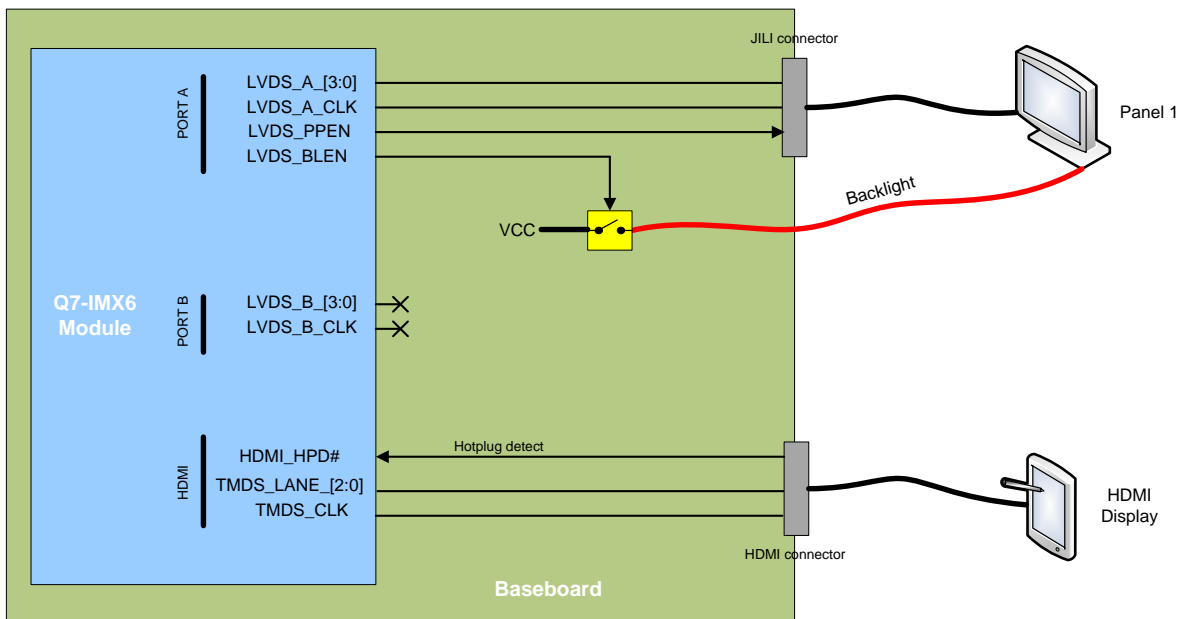

***Figure 8-1:* LVDS setup: one panel / one port**

8.5.2 One LVDS Panel / 2 Ports

Another option would be to connect one LVDS panel with a higher resolution. These panels frequently have more than one channel. In that case connect LVDS_A and LVDS_B signals to the same connector on the baseboard. The panel can be enabled with the LVDS_PPEN signal (pin 111) and the backlight can be switched on with LVDS_BLEN (pin 112).
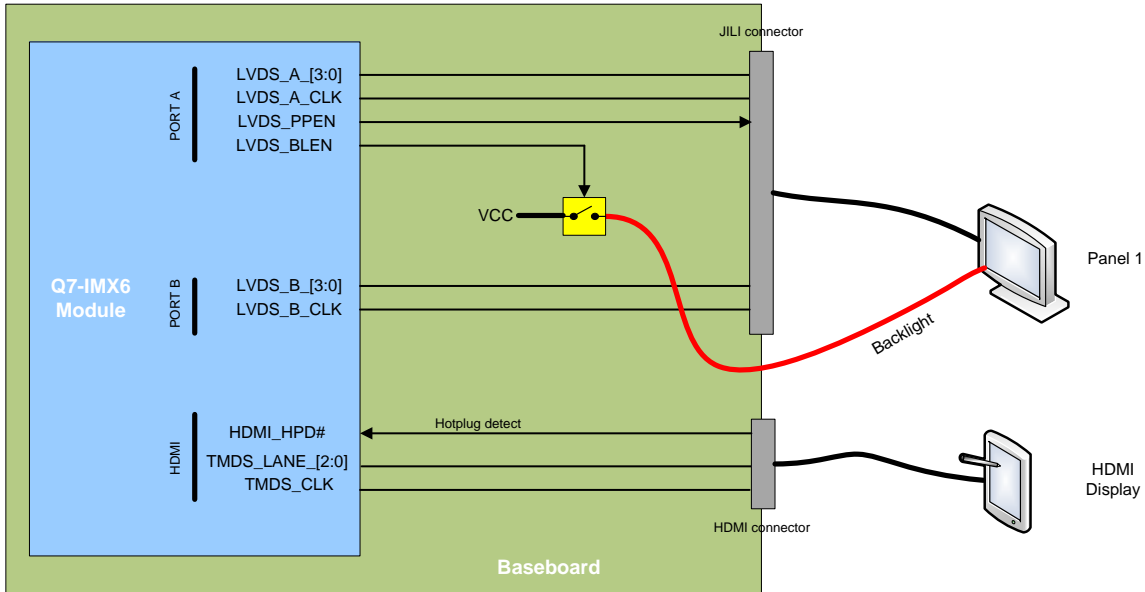

Figure 8-2: **LVDS setup: one panel / two ports**

8.5.3 Two LVDS Panel / 2 Ports – Alternative 1

The third option would be to connect two LVDS panels. Panel 1 – the primary one – is connected to port A with its corresponding panel power enable signal LVDS_PPEN (pin 111) and the associated backlight enable signal LVDS_BLEN (pin 112).

The second display has to be controlled through the baseboard!

> ⚠ ***Please note that the Qseven specification supports only one set of panel control signals. Therefore panel power sequencing cannot be guaranteed by software as the second display may have a different behaviour!***
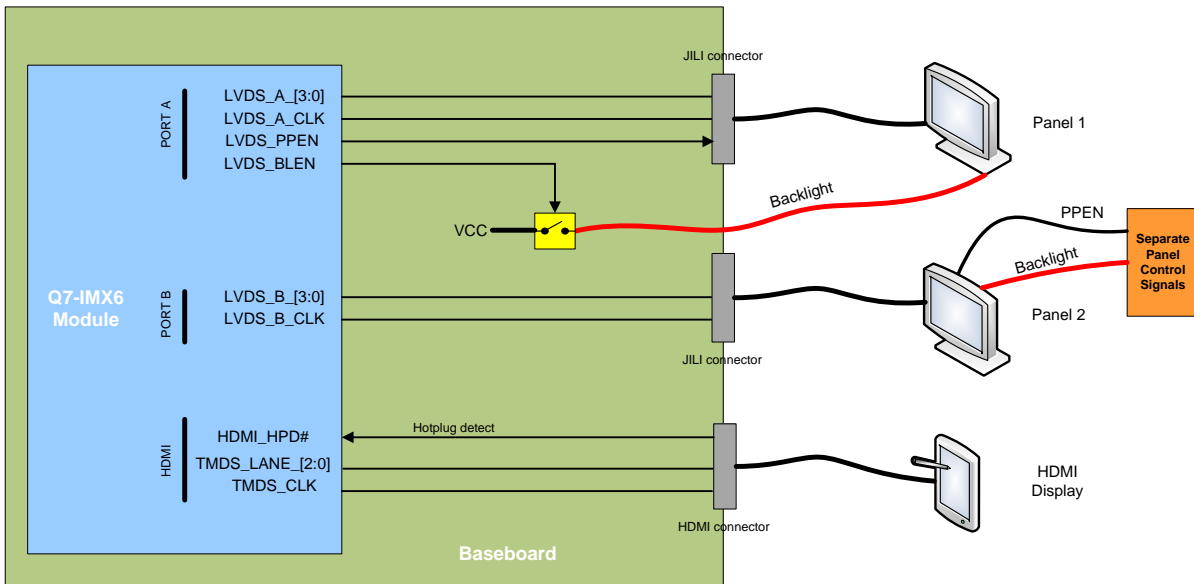

Figure 8-3: **LVDS setup: two panels / two ports / alternative 1**

8.5.4 Two LVDS Panel / 2 Ports – Alternative 2

Please note that this implementation is not compliant with the Qseven specification as it introduces a second pair of control signals that is not defined in the Qseven specification!
This may lead to incompatibilities with other module vendors' i.MX6 designs in terms of interchangeability.

The last option is unique for the Q7-IMX6 design as it introduces a second pair of panel control signals on currently unused Qseven pins. Nevertheless, it is the only solution that offers the possibility to do proper panel power sequencing and control using the i.MX6 controller and the Qseven connector. The setup is displayed in the following diagram:
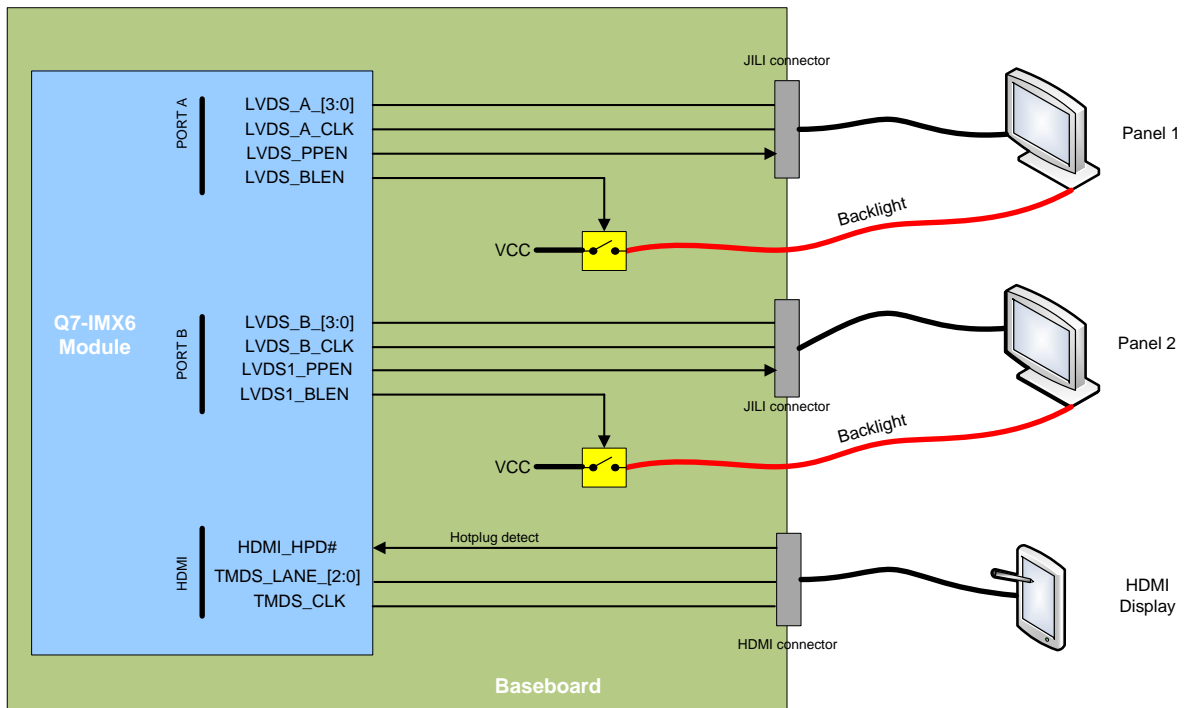

Figure 8-4: **LVDS setup: two panels / two ports / alternative 2**

Panel 1 is connected to port A and controlled with LVDS_PPEN (pin 111) and the associated backlight enable signal LVDS_BLEN (pin 112).

Panel 2 is connected to port B and controlled with LVDS1_PPEN (pin 132) and the associated backlight enable signal LVDS1_BLEN (pin 134).

Both panels use the same I2C Bus for Display ID.

9 USB Recovery Mode / Debug Port

The Freescale i.MX6 has a special mode for bootloader update called USB recovery mode.

This mode is necessary in case the pre-flashed bootloader (and the update function integrated therein) has been corrupted or became non-functional.

9.1 Manufacturing Pins

The Qseven specification defines manufacturing pins which are dual function pins. The basic idea is to have JTAG pins on the one hand and special chip dependent mode pins in combination with a COM debug port on the other hand. The "MFG_NC4" signal switches between those two modes.
Please refer to chapter 7.14 for a detailed pin description of the Q7-IMX6 manufacturing pins.

> ⚠ ***The JTAG interface of the Qseven connector is not supported on the Q7-IMX6 module. It can only be accessed via the debug connector.***

On the MSC Q7-IMX6 Module only UART/USB Recovery Mode is supported, but it is also possible to leave the pins unused.

Therefore, two different configurations are possible on the baseboard:

	UART/RECOVERY mode		Manufacturing Interface unused
	Function	**How to connect**	
MFG_NC0	Not available on Q7-IMX6 module	Don't care	Don't care
MFG_NC1	"UART_TXD" (module output)	Connect to transceiver on baseboard	Floating
MFG_NC2	"UART_RXD" (module input)	Connect to transceiver on baseboard	Floating
MFG_NC3	USB_RECOVERY#: 1: Internal Boot 0: USB Recovery (= Serial Downloader Mode)	Connect to jumper or switch: 1: leave floating 0: pull to ground	Floating
MFG_NC4	UART/RECOVERY signal	Pull to ground	- Pull high: Disable buffers on Q7-IMX6 module - … or leave floating: **In that case do not drive the MFG_NC3 pin**!

In Recovery Mode the COM debug port is accessible on *"MFG_NC1" and "MFG_NC2"* signals, whereas *"MFG_NC3"* is the recovery pin which selects the boot source, i.e. booting from the standard boot device or from USB-Recovery Mode.

The bootloader data is downloaded using USB data lines on Qseven port 1 (refer to Qseven specification) when the MSC Q7-IMX6 Module is an USB client.

9.2 How to access the USB Recovery Mode

With Qseven specification 1.20 the standard was expanded to include ARM based modules. Those modules require a bootloader instead of BIOS. The initial bootloader is pre-installed during production run but in case this bootloader is deleted or non-functional the USB Recovery mode still provides access to the i.MX6 CPU via USB. Therefore, compatible carrier boards have to provide the MFG_NC3 and MFG_NC4 signals as well as the USB Port1 in client mode.

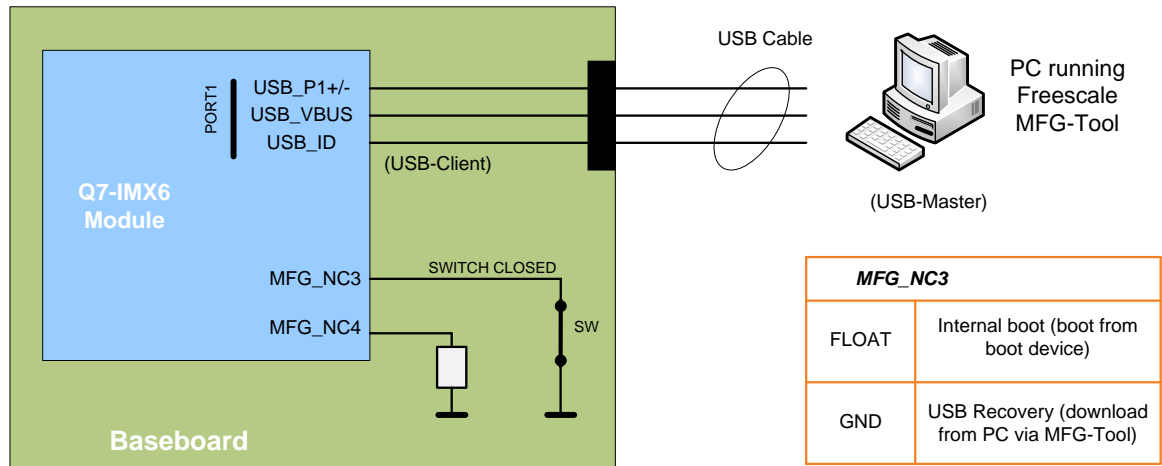The basic setup for USB recovery is shown in the following figure:

Figure 9-1: **USB Recovery Mode on Q7IMX6**

⚠️ *Do not connect MFG_NC3 permanently to GND (=close switch) as this will prevent the board from booting!*

9.3   How to access the COM Debug port

The COM Debug port is available on the *"MFG_NC1" and "MFG_NC2"* pins of the Qseven connector when *"MFG_NC4"* is connected to GND. In this case the carrier board has to provide the transceiver chip for the RS232 levels and the corresponding connector as implemented on the MSC Q7-EP4 baseboard, for example.
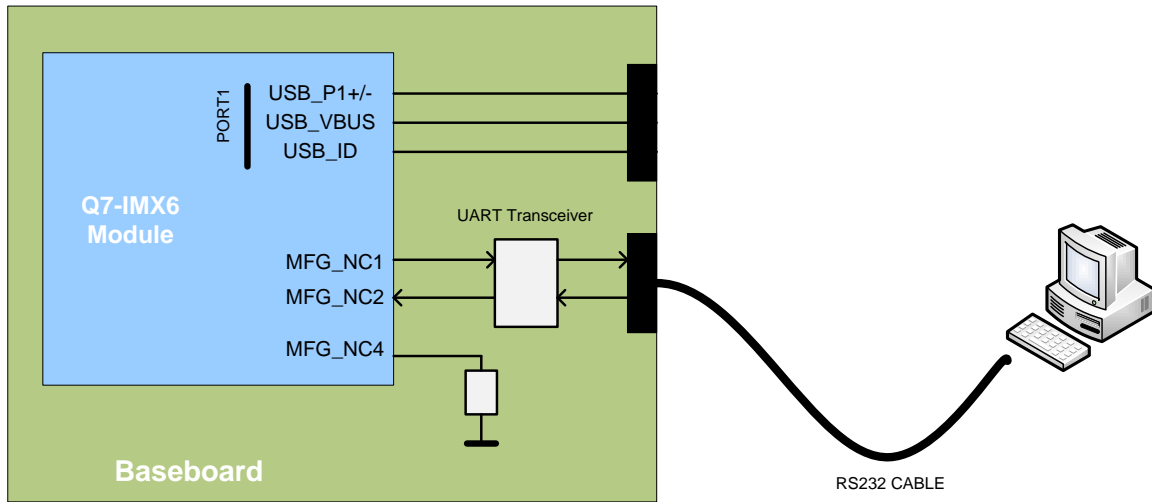

Figure 9-2: **Debug Port on Q7IMX6 – connection through carrier board**

Another way to access the debug port is by using an additional hardware adapter like the "EXM-Debugadapter" which can be directly connected to the debug connector "X2" (refer to chapter 6.1 onwards) of the MSC Q7-IMX6 module. In that case the *MFG_NCx"* pins should be left open (see chapter 9.1).
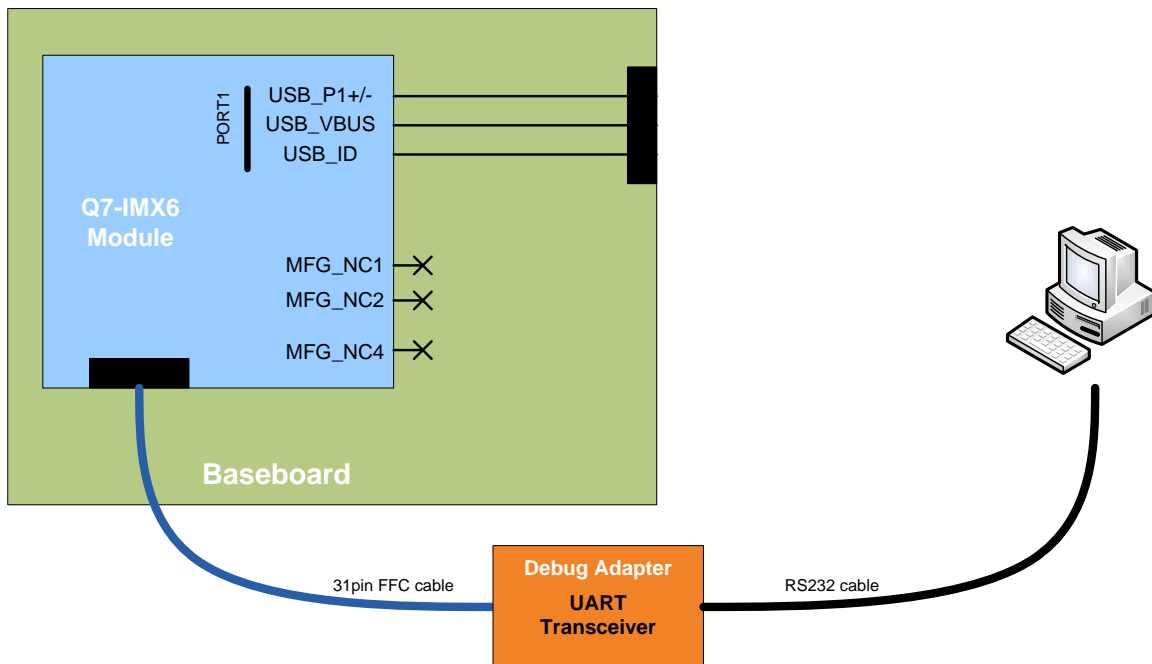

Figure 9-3: **Debug Port on Q7IMX6 – connection through EXM Debugadapter**

9.4   EXM Debugadapter

The "EXM Debugadapter" can be used in combination with the MSC Q7-IMX6 module and baseboards that do not implement the requirements for a Debug Port, for example the MSC Q7-MB-EP2-003.

On such a baseboard the "EXM Debugadapter" provides the serial port required for the linux remote console.

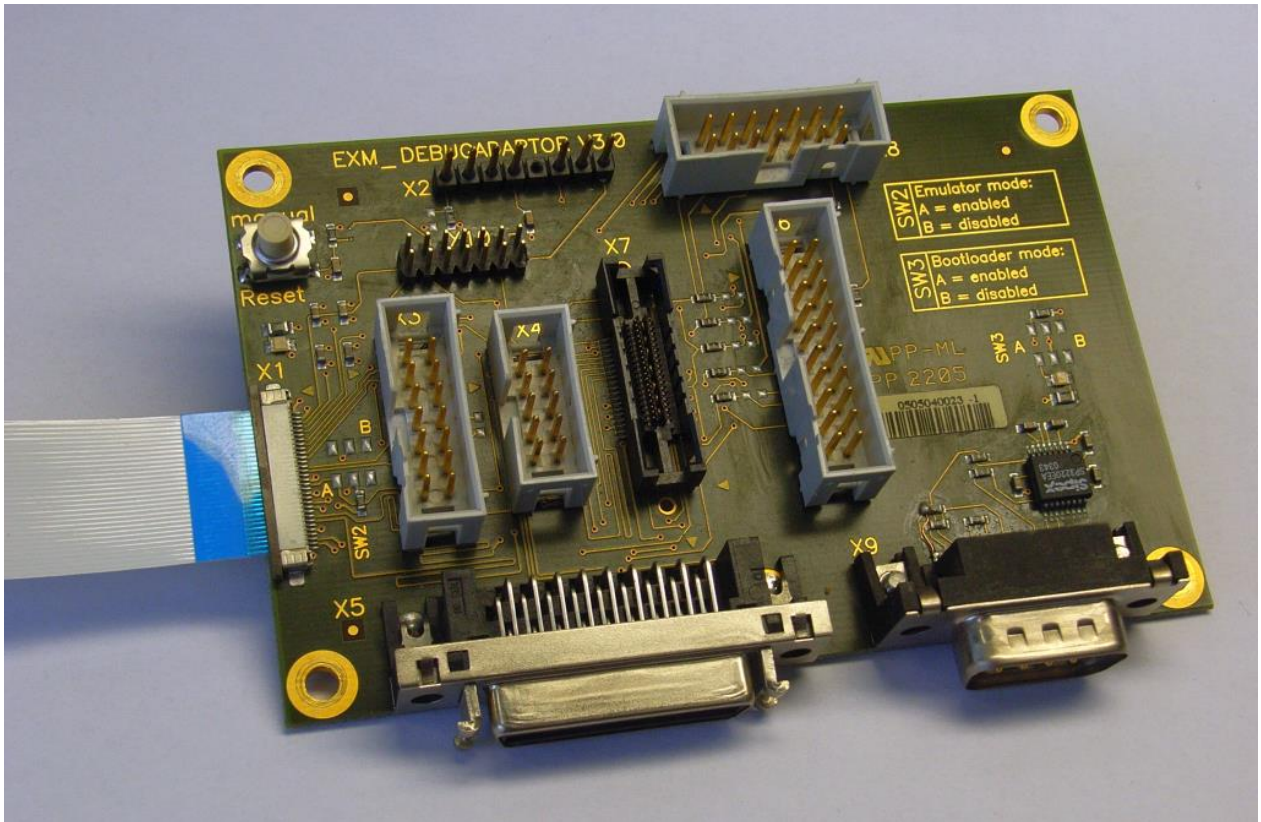Additionally, a push button is implemented so a module reset can be triggered manually.

Figure 9-4: **EXM Debugadapter**

⚠️ *The EXM-Debugadapter has many connectors that have no functionality when used with the Q7-IMX6 module as it was designed for the EXM32 COM family. Please do not connect any cable to the pin headers not explicitly mentioned in this description.*

9.4.1 Connector Overview

When using the "EXM Debugadapter" with the Q7-IMX6 module only the following connectors are relevant:

- **X1:** Connect a 31 pin FFC cable to connector "X2 of the MSC Q7-IMX6 module
- **X6:** Connect a 20 pin cable for debuggers, for example Lauterbach TRACE32
- **X9:** Connect a "Null-Modem" RS232 cable between the EXM Debugadapter and your computer

9.4.2　Connector Description

X1:

Debug connector with confidential pinout not intended for customer's use. Use a 31 pin FFC cable (0.5mm pitch, top – bottom contact) to establish a connection between EXM Debugadapter and the Q7-IMX6 module.

X6:

Connector for standard 20 pin ARM Multi-ICE interface:

20 pin, RM2.54 pin header

Pin	Signal	Pin	Signal
1	VTREF	2	VSUPPLY
3	TRST#	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	RTCK	12	GND
13	TDO	14	GND
15	SRST#	16	GND
17	DBGRQ	18	GND
19	DGBACK	20	GND

Only the following pins are supported with the MSC Q7-IMX6 module:

Pin	Signal	Pin	Signal
1	VCC3V3_STBY	2	VCC3V3_DEL
3	n.c.	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	n.c.	12	GND
13	TDO	14	GND
15	SRST#	16	GND
17	n.c.	18	GND
19	n.c.	20	GND

X9:

9 pin DSUB connector to establish a RS232 connection between the EXM Debugadapter and your computer. The serial interface features RX / TX <u>without</u> hardware handshake signals.

Pin	Signal	Description
1	DCD	Not used – shorted with DSR and DTR
2	RX	Receive data (adapter input)
3	TX	Transmit data (adapter output)
4	DTR	Not used – shorted with DSR and DTR
5	GND	Ground
6	DSR	Not used – shorted with DCD and DTR
7	RTS	Not used – shorted with CTS
8	CTS	Not used – shorted with RTS
9	RI	Not connected