Am79C971
PCnet™-*FAST*
Hardware User's Manual

AMD

CHAPTER

1 INTRODUCTION

1.1 INTRODUCTION

The PCnet™-*FAST* board is an advanced PC network interface adapter card targeted for the Ethernet-PCI adapter card market. It is based on the Am79C971 PCnet-*FAST* device, a single-chip 32-bit full-duplex, 10/100-Mbps highly integrated Ethernet system solution. Designed to address high performance system applications, the flexible bus master architecture provides high data throughput in the system and low CPU and system bus utilization. The PCnet-*FAST* board supports the PCI Specification (Rev. 2.1), jumperless bus and media configuration, and driver software compatible with the existing PCnet family of drivers.

This manual provides a complete description of the PCnet-*FAST* board, with sections covering the functional description of each building block, the setup and installation of the board, and the hardware specification.

It is assumed that the user of this manual has access to the information listed below, since references to these documents are made throughout this manual:

- *AMD Ethernet/IEEE 802.3 Family, 1994 World Network Data Book/Handbook (PID# 14287).*
- *Am79C971 PCnet-FAST Single-Chip Full-Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus Preliminary Data Sheet (PID# 20550B)*
- *PCnet Family Network Family Driver Installation Guide (PID# 18233D)*
- *PCI Specification, Revision 2.1*

CHAPTER

2 FUNCTIONAL DESCRIPTION

2.1 BOARD DESCRIPTION

The PCnet-*FAST* board is a 10/100-Mbps PCI network interface card. The Ethernet connection is implemented through the single RJ-45 jack which is connected to an external 10/100 TX transceiver. The transceiver is connected to the PCnet-*FAST* controller through the integrated Media Independent Interface (MII). Due to the high integration of the PCnet-*FAST* device, very few external parts are needed. The PCnet-*FAST* evaluation board provides the remote boot capability via an EPROM on the FLASH device. In addition, SRAMs may be added to optimize performance. In most applications, two 15-ns 32x8 SRAMs are sufficient to satisfy the buffer requirement.

The following diagram illustrates the implementation of the PCnet-*FAST* board.

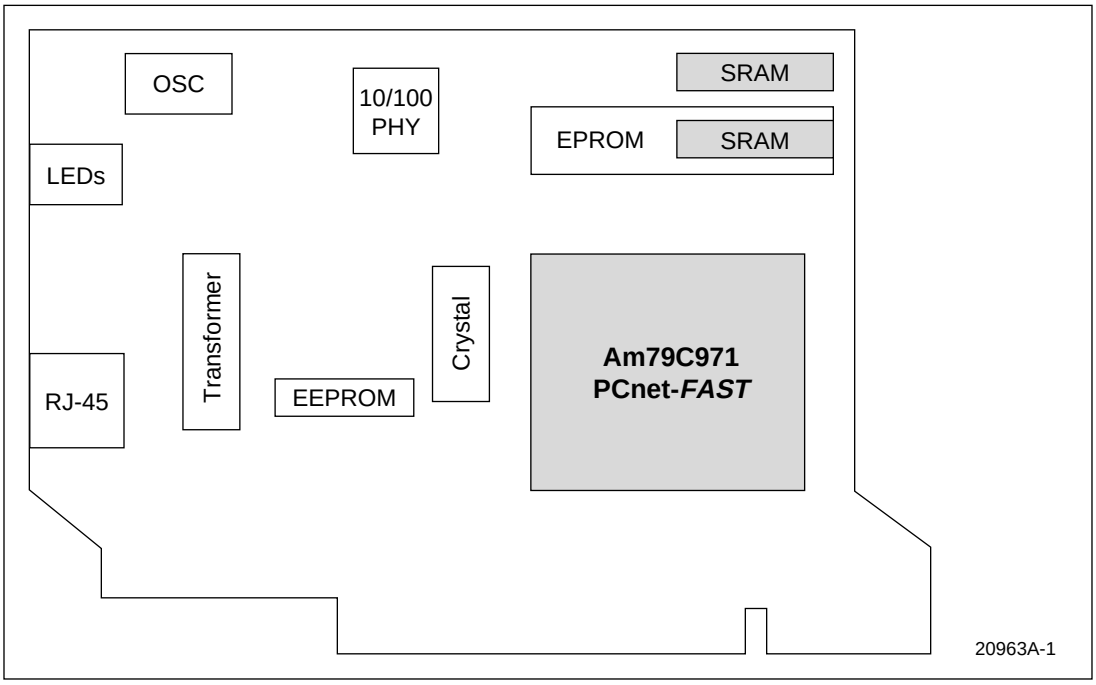

Figure 2-1 Board Diagram

2.2 ETHERNET NODE CONTROLLER

The single-chip Am79C971 PCnet-*FAST* Ethernet solution is a highly integrated solution that contains a Bus Interface Unit (BIU), a DMA buffer management unit, an ISO/IEC 8802-3 and ANSI/IEEE 802.3-compliant Media Access Control (MAC) function, a flexible buffer architecture with an SRAM-based FIFO extension for support up to 128 Kbytes of external frame buffering, optional remote boot PROM/FLASH, integrated 10BASE-T and 10BASE-2/5 (AUI) physical layer interface, and an ANSI/IEEE 802.3-compliant Media Independent Interface (MII).

2.3 LOCAL BUS INTERFACE

The PCnet-*FAST* board implements the local bus interface to the Peripheral Components Interconnect (PCI) revision 2.1 specification through the Am79C971 chip. The BIU in the chip is designed to operate as a PCI bus master during normal operations, and some slave I/O accesses to the controller are required in normal operation as well. Initialization of the Ethernet controller is achieved through a combination of PCI Configuration Space accesses, bus slave accesses, bus master accesses, and an optional read of a serial EEPROM that is performed by the controller.

2.4 ETHERNET INTERFACE

The Ethernet interface for the PCnet-*FAST* board is achieved through the single RJ-45 jack. The RJ-45 jack is connected to an external 10/100-Mbps transceiver connected to the PCnet-*FAST* controller through the integrated MII.

2.5 EXPANSION BOOT ROM/FLASH

The PCnet-*FAST* board can accommodate up to 256K bits of Boot ROM Code. An external latch is used to allow Boot ROM Address and Data Latching when $\overline{\text{AS\_EBOE}}$ is asserted. The PCnet-*FAST* board supports EPROM or Flash as an Expansion boot ROM device. Both are configured using the same methods and operate the same way.

2.6 SRAM INTERFACE

When using the controller in a 100-Mbps environment, additional frame buffering capability is provided by a 16-bit wide SRAM interface which provides high performance and high latency tolerance on the system bus and network. The controller can use up to 128 Kbytes of SRAM as an extension of its dual transmit and receive FIFOs. When no SRAM is used, the Am79C971 controller's FIFOs are programmed to bypass the SRAM interface.

2.7 SERIAL EEPROM INTERFACE

The PCnet-*FAST* board stores the unique IEEE physical address and bus configuration of each node in the serial EEPROM. Once powered up, the Am79C971 chip automatically detects the presence of the EEPROM and reads the 32 words stored in it through the MicroWire interface protocol. For details of the MicroWire interface, refer to the Am79C971 data sheet. The interface also supports the WRITE operation to the EEPROM.

2.8 AUTO-NEGOTIATION CONTROL

The PCnet-*FAST* board implements the Auto-Negotiation standard per the IEEE 802.3 specification for the 10BASE-T Media Attachment Unit (MAU) and the MII port. Auto-Negotiation automatically configures the link between two link partners through the Fast Link Pulse. The Fast Link Pulse is made up of a train of 17 clocks alternating with the 16 data fields for a total of 33 pulses. The two link partners send information in the 16 data positions between themselves. Both sides look to see what is possible and then connect at the greatest speed and capability (without any software support) as shown in the table below. The Auto-Negotiation capabilities for the PCnet-*FAST* board are as follows:

Table 2-1 Auto-Negotiation Capabilities

Network Speed	Physical Network Type
200 Mbps	100BASE-TX, Full Duplex
100 Mbps	100BASE-TX, Half Duplex
20 Mbps	10BASE-T, Full Duplex
10 Mbps	10BASE-T, Half Duplex

CHAPTER

3 SETUP AND INSTALLATION

3.1 BOARD CONFIGURATION

Configuration of the I/O base address and the interrupt channel is automatic upon power up, without any hardware jumpers. The system BIOS routine is responsible for assigning the I/O base address and binding the appropriate interrupt channels to the PCnet-*FAST* board. One may find out what the I/O base assignment and the interrupt channel binding through the AMD installation software and configuration utility. For more detailed information on this utility, refer to the *PCnet Family Network Driver Installation Guide*.

3.2 10/100BASE-T PHYSICAL CONNECTIONS

A Data Terminal Equipment (DTE) system with the installed PCnet-*FAST* board can connect to an Ethernet network using the on-board RJ-45 jack for either 10BASE-T or 100BASE-TX connection. Figure 3-1 illustrates a typical network configuration for the network using the PCnet-*FAST* board.

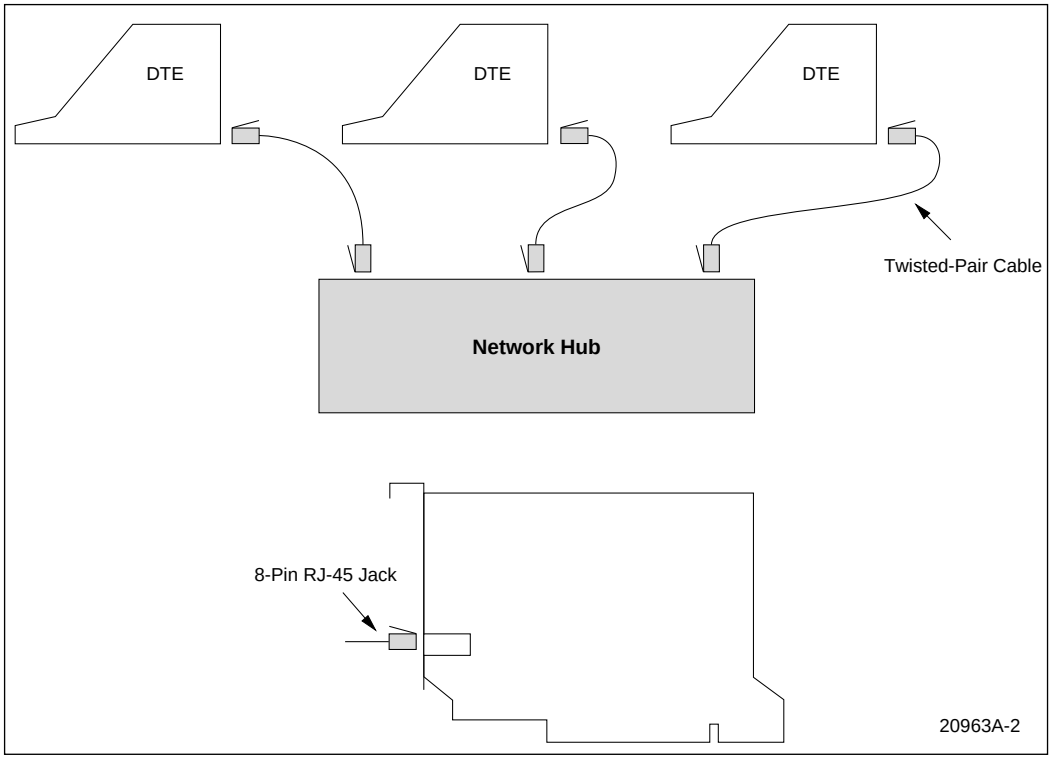

Figure 3-1 PCnet-*FAST* 10/100BASE-T Physical Connections

The Auto-Poll™ feature of the PCnet-*FAST* controller determines that the MII port is used for the network connection. Since an external 10/100-Mbps transceiver is used in the PCnet-*FAST* board, the Auto-Negotiation feature of the PCnet-*FAST* controller configures

whether the capability of the network is 10 Mbps or 100 Mbps, and whether it is full or half-duplex.

3.3 NETWORK STATUS

Four LEDs on the bracket provide the network status as shown in the following table:

LED	LED 0	LED 1	LED 2	LED 3
Color	**Green**	**Green**	**Amber**	**Green**
Function	LNKST	ACT	10/100*	COL
Meaning	On = Link Pass Off = Link Fail	For XMT: On = Transmit Off = No Trans. For ACT: On = Busy Off = No Activity	On = 100 Mbps Off = 10 Mbps	On = Collision Off = No Collision

**Valid only when LED 0 is On.*

The placement of the LEDs are shown in Figure 3-2.

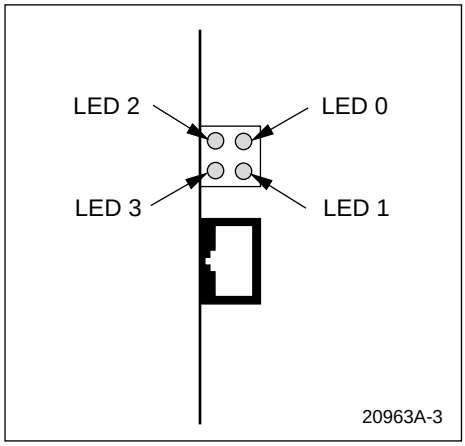

Figure 3-2 LED Placement

CHAPTER

4 HARDWARE SPECIFICATIONS

4.1 PCI INTERFACE

The Am79C971 chip on the PCnet-*FAST* board contains the interface logic to the PCI bus. Connections to the PCI bus are straightforward in that there is no external glue logic on the PCnet-*FAST* board, thus making the PCnet-*FAST* board fully compliant to the PCI loading and trace length specifications.

The types of PCI cycles supported on the PCnet-*FAST* board are as follows:

- Master Memory Read
- Master Memory Write
- Master Memory Read Line
- Slave Configuration Read
- Slave Configuration Write
- Slave I/O Read
- Slave I/O Write

The first three types are the Master cycles that the Am79C971 chip uses to transfer data across the PCI bus. The Am79C971 chip owns and controls the address/data bus after its request is acknowledged by the system arbiter. If there are two or less double words to read, the Am79C971 chip uses the Memory Read cycle; if there are more than two double words to read, the Am79C971 chip uses the Memory Read Line cycle. All Master cycles also support the four types of slave termination schemes specified in the PCI Revision 2.1 specification.

The last four types are the Slave cycles that the host CPU uses to access configuration and register information in the Am79C971 chip.

4.2 I/O BASE ADDRESS AND INTERRUPT

In a PCI system, the I/O base address and the interrupt channel that the PCnet-*FAST* board uses are assigned by the POST routine. Software drivers determine the I/O base address and the interrupt channel assigned to the PCnet-*FAST* board by reading the PCI configuration space of the device.

Table 4-1 I/O Port Address

I/O Resource	Access Code
APROM	I/O Base address + 0h
RDP	I/O Base address + 10h
RAP	I/O Base address + 12h for word I/O mode (in Am1500 driver compatible mode)
	I/O Base address + 14h for double word mode
Reset Register	I/O Base address + 14h for word I/O mode (in Am1500 driver compatible mode)
	I/O Base address + 1Ch for double word I/O mode
BDP	I/O Base adddres + 16h for word I/O mode (in Am1500 driver compatible mode)
	I/O Base address +1Ch for double word I/O mode

4.3 RJ-45 INTERFACE

The PCnet-*FAST* board is equipped with a RJ-45 type, eight-pin modular interface. The pin configuration and definition for the RJ-45 connection are as follows:

Table 4-2 RJ-45 Pinout

Pin Number	Color Code	Function
Pin 1	white/orange band	TX+
Pin 2	orange/white band	TX-
Pin 3	white/green band	RX+
Pin 6	green/white band	RX-
Pin 4	blue/white band	Not Used
Pin 5	white/blue band	Not Used
Pin 7	solid orange	Not Used
Pin 8	solid gray	Not Used

The color code may vary from one cable manufacturer to another. Make sure that the TX+ and the TX- wires are twisted as a pair and the RX+ and the RX- wires are twisted as another pair. For 100-Mbps operation, category 5 wire must be used for proper 100BASE-TX operation.

Note: *Do not use the telephone-type cable commonly known as "silver satin" (flat, with silver vinyl jacket) to connect the stations as none of the wires are twisted.*

4.4 SERIAL EEPROM

The serial EEPROM contains the IEEE physical address unique to each node, the bus configuration, and the MAU configuration information. The format of the EEPROM contents is the following, beginning with the byte that resides at the lowest EEPROM address:

Table 4-3 EEPROM Address Format

Word Address	Byte Addr	Most Significant Byte (MSB)	Byte Addr	Least Significant Byte (LSB)
00h	01h	2nd byte of the ISO 8802-3 (IEEE/ANSI 802.3) station physical address for this node	00h	1st byte of the ISO 8802-3 (IEEE/ANSI 802.3) station physical address for this node
01h	03h	4th byte of node address	02h	3rd byte of node address
02h	05h	6th byte of node address	04h	5th byte of node address
03h	07h	Reserved location; must be 00h	06h	Reserved location; must be 00h
04h	09h	Hardware ID: must be 11h if compatibility to AMD drivers is desired	08h	Reserved location; must be 00h
05h	0Bh	User programmable space	0Ah	User programmable space
06h	0Dh	MSB of two-byte checksum, which is the sum of bytes 00h-0Bh and bytes 0Eh and 0Fh	0Ch	LSB of two byte checksum, which is the sum of bytes 00h-0Bh and bytes 0Eh and 0Fh
07h	0Fh	Must be ASCII “W” (57h) if compatibility to AMD driver software is desired	0Eh	Must be ASCII “W” (57h) if compatibility to AMD driver software is desired
08h	11h	BCR2[15:8] (Miscellaneous Configuration)	10h	BCR2[7:0] (Miscellaneous Configuration)
09h	13h	BCR4[15:8] (Link Status LED)	12h	BCR4[7:0] (Link Status LED)
0Ah	15h	BCR5[15:8] (LED1 Status)	14h	BCR5[7:0] (LED1 Status)
0Bh	17h	BCR6[15:8] (LED2 Status)	16h	BCR6[7:0] (LED2 Status)
0Ch	19h	BCR7[15:8] (LED3 Status)	18h	BCR7[7:0] (LED3 Status)
0Dh	1Bh	BCR9[15:8] (Full-Duplex Control)	1Ah	BCR9[7:0] (Full-Duplex Control)
0Eh	1Dh	BCR18[15:8] (Burst & Bus Control)	1Ch	BCR18[7:0] (Burst & Bus Control)
0Fh	1Fh	BCR22[15:8] (PCI Latency)	1Eh	BCR22[7:0] (PCI Latency
10h	21h	BCR23[15:8] (PCI Subsystem Vendor ID)	20h	BCR23[7:0] (PCI Subsystem Vendor ID)
11h	23h	BCR24[15:8] (PCI Subsystem ID)	22h	BCR24[7:0] (PCI Subsystem ID)
12h	25h	BCR25[15:8] (SRAM Size)	24h	BCR25[7:0] (SRAM Size)
13h	27h	BCR26[15:8] (SRAM Boundary)	26h	BCR26[7:0] (SRAM Bounder)
14h	29h	BCR27[15:8] (SRAM Interface Control)	28h	BCR27[7:0] (SRAM Interface Control)
15h	2Bh	BCR32[15:8] (MII Control & Status)	2Ah	BCR32[7:0] (MII Control & Status)
16h	2Dh	BCR33[15:8] (MII Address)	2Ch	BCR33[7:0] (MII Address)
17h	2Fh	BCR35[15:8] (PCI Vendor ID)	2Eh	BCR35[7:0] (PCI Vendor ID)
18h	31h	Reserved location; must be 00h	30h	Reserved location; must be 00h
19h	33h	Reserved location; must be 00h	32h	Reserved location; must be 00h

1Ah	35h	Reserved location; must be 00h	34h	Reserved location; must be 00h
1Bh	37h	Reserved location; must be 00h	36h	Reserved location; must be 00h
1Ch	39h	Reserved location; must be 00h	38h	Reserved location; must be 00h
1Dh	3Bh	Reserved location; must be 00h	3Ah	Reserved location; must be 00h
1Eh	3Dh	Reserved location; must be 00h	3Ch	Reserved location; must be 00h
1Fh	3Fh	Checksum adjust byte for the 64 bytes of the EEPROM contents, checksum of the 64 bytes of the EEPROM should total to Ffh	3Eh	Reserved location; must be 00h

The IEEE physical address is unique to each node and manufacturer. Each manufacturer of the PCnet-*FAST* board must only use the address block assigned to the company. AMD uses *00 00 1A 18 XX XX address block.* To apply for an IEEE block address, the board manufacturer must contact:

IEEE Standard Department
445 Hoer Lane
Piscataway, NJ 08855-1331
c/o OUI Registrar
Tel: (908) 562-3809

The EEPROM contents could either be pre-programmed on an off-line EEPROM programmer, or be programmed on the PCnet-*FAST* board via the MicroWire protocol. The actual programming procedure on the off-line is left to the user.

Note: *The last four digits of the IEEE address can be found on a label attached to the EEPROM of the PCnet-FAST board.*

4.5 PHYSICAL DIMENSIONS

Without the bracket mounted to the board, the physical dimensions of the board are as follows:

- Width: 4.7 inches
- Height: 3.6 inches

4.6 POWER REQUIREMENTS

The power requirements are as follows:

- 3.25 W maximum, 5 V DC, at 25°C (with NSC 10/100 PHY)
- 1.90 W maximum, 5 V DC, at 25°C (with ICS 10/100 PHY)

To properly reflect the power consumption of the board in the PCI environment, the PRSNT#1 and PRSNT#2 signals on the boards are shorted to Ground according to the PCI rev 2.1 Specification.