cPCI-7249R

3U, 48 Parallel

Digital I/O Card

User Guide

Recycled Paper

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Table of Contents

How to Use This Guide

This manual is designed to help you use the cPCI-7249R. It describes how to modify and control various functions on the cPCI-7249R card to meet your requirements. It is divided into three chapters:

- **Chapter 1,** "Introduction," gives an overview of the product features. applications, and specifications.
- **Chapter 2,** "Installation," describes how to install the cPCI-7249R. The layout of cPCI-7249R are shown, the jumper settings, the connectors specifications, and the notes for installation are described.
- **Chapter 3,** "Operation Theorem" describes more details about the versatile functions, including DIO, timer / counter, and interrupt systems.
- **Chapter 4,** "Software Library" specifies the software library of C language under DOS environment that makes you can operate the functions on this card easily.

1

Introduction

The cPCI-7249R are multi-functions digital I/O board used for industrial PC with PCI bus. The PCI cards are plug and play therefore it is not necessary to set any jumper for matching the PC environment. cPCI-7249R is a 48-bit Parallel DIO card and it supports external edge trigger

signal for latch 48-bit digital input data .

The cPCI-7249R emulates two industry standard mode zero configuration of 8255 Programmable Peripheral Interface (PPI) chips.

Every PPI connector offers 3 ports: PA, PB, and PC. The PC can also be subdivided into 2 nibble-wide (4-bit) ports - PC Upper and PC Lower.

The cPCI-7249R is programmed using the ADLink's software library. The programming of these cPCI cards is as easy as AT bus add-on cards.

1.1 Features

The cPCI-7249R Multi-functions Digital I/O Boards provide the following advanced features:

1.1.1 Digital I/O Ports

- 48 TTL/DTL compatible digital I/O lines
- Use SCSI-100 connector
- Emulates two industry standard mode 0 of 8255 PPI
- Buffered circuits for higher driving capability
- Output status readback
- Support external edge trigger signal for latch 48 channel digital data

1.1.2 Timer / Counter and Interrupt System

- A 32 bits timer to generate watchdog timer interrupt
- A 16 bits event counter to generate event interrupt
- Programmable interrupt source
- Dual interrupt system

1.1.3 Miscllenous

- Provide 12V and 5V power supply on SCSI-100 connector
- On board resettable fuses to protect power supply for external devices

1.1.4 Accessory

- R7249 daughter board for rear I/O

1.2 Applications

- Programmable mixed digital input & output
- Industrial monitoring and control
- Digital I/O control
- Contact closure, switch / keyboard monitoring
- Connects with OPTO-22 compatible modules
- Useful with A/D and D/A to implement a data acquisition & control system

1.3 Specifications

I/O channels	48-bit for cPCI-7249R
Input Signal	Logic High Voltage :2.0 V to 5.25V Logic Low Voltage : 0.0 V to 0.80V Logic High Current : 20.0 uA Logic Low Current : -0.2 mA
Output Signal	Logic High Voltage : Minimum 2.4 V Logic Low Voltage : Maximum 0.5V Logic High Current : -15.0 mA Logic Low Current : 24.0 mA
Operating Temperature	0° ~ 60° C
Storage Temperature	-20° ~ 80° C
Humidity	5% ~ 95% non-condensing
I/O Connectors	100-pin SCSI II Connector
Bus	cPCI bus
IRQ Level	Set by Plug and Play BIOS
I/O port address	Set by Plug and Play BIOS
Power Consumption (without external devices)	cPCI-7249R : 700mA @5VDC (Typical)
Transfer Rate	500 K bytes/sec (Typical)
Size	cPCI-7249R : Standard 3U Compact PCI form factor

2

Installation

This chapter describes how to install the cPCI-7249R. At first, the contents in the package and unpacking information that you should be careful are described.

2.1 What You Have

In addition to this *User's Manual*, the package includes the following items:

- cPCI-7249R 48-bits Parallel Digital I/O Card
- All-In-One Compact Disc

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2 Unpacking

Your cPCI-7249R card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be done on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handing damages on the module before processing.

After opening the card module carton, exact the system module and place it only on a grounded anti-static surface component side up.

Note : DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

You are now ready to install your cPCI-7249R.

2.3 Device Installation for Windows 95

While you first plug cPCI-7249R card and enter Windows 95, the system will detect this device automatically and show a dialog box that prompts you to select the device information source.

Place ADLINK's All-in-one CD into the appropriate CD drive. Type "X:\Win95inf\7249" (these directory includes cPCI-7249R device information files "7249.inf") in the Location input field (**X indicates the CD ROM driver**) or click Browse button to find thes directory, and then click OK. The system will start the installation of cPCI-7249R. Please refer to PCISetup.doc or PCISetup.pdf in ADLink's All-in-one CD for the detailed procedure descriptim.

2.4 cPCI-7249R Layout

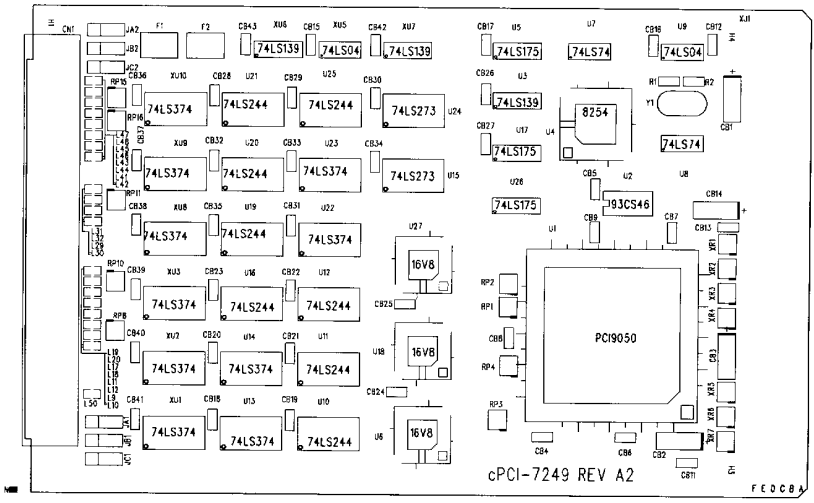
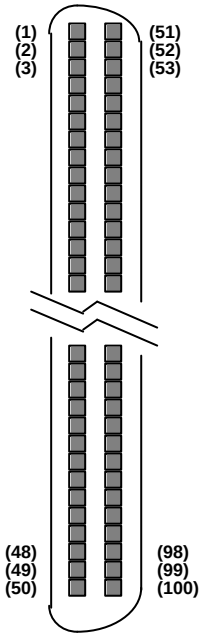


Figure 2.1 cPCI-7249R Layout

2.5 Connector Pin Assignment

The I/O ports of cPCI-7249R emulate the mode 0 configuration of the 8255 general purpose programmable peripheral interface. This card comes equipped with SCSI -100 Pin connector. And the cPCI-7249R supports R7249 daughter board for rear I/O, it includes two OPTO-22 connectors and one SCSI -100 connector.



(1) P1A0	(26) P2A0	(51) EVENT	(76) GND
(2) P1A1	(27) P2A1	(52) GND	(77) GND
(3) P1A2	(28) P2A2	(53) GND	(78) GND
(4) P1A3	(29) P2A3	(54) GND	(79) GND
(5) P1A4	(30) P2A4	(55) GND	(80) GND
(6) P1A5	(31) P2A5	(56) GND	(81) GND
(7) P1A6	(32) P2A6	(57) GND	(82) GND
(8) P1A7	(33) P2A7	(58) GND	(83) GND
(9) P1B0	(34) P2B0	(59) GND	(84) GND
(10) P1B1	(35) P2B1	(60) GND	(85) GND
(11)P1B2	(36) P2B2	(61) GND	(86) GND
(12) P1B3	(37) P2B3	(62) GND	(87) GND
(13) P1B4	(38) P2B4	(63) GND	(88) GND
(14) P1B5	(39) P2B5	(64) GND	(89) GND
(15) P1B6	(40) P2B6	(65) GND	(90) GND
(16) P1B7	(41) P2B7	(66) GND	(91) GND
(17) P1C0	(42) P2C0	(67) GND	(92) GND
(18) P1C1	(43) P2C1	(68) GND	(93) GND
(19) P1C2	(44) P2C2	(69) GND	(94) GND
(20) P1C3	(45) P2C3	(70) GND	(95) GND
(21) P1C4	(46) P2C4	(71) GND	(96) GND
(22) P1C5	(47) P2C5	(72) GND	(97) GND
(23) P1C6	(48) P2C6	(73) GND	(98) GND
(24) P1C7	(49) P2C7	(74) GND	(99) EXTCLK
(25) V5V	(50) +12V	(75) V5V	(100) +12V

The DIO pin names are specified as PnXb, where
n : means the connector reference number n=1~2.
X : means the port name, X= 'A' , 'B' or 'C'
b : means the bit number of a port, b=0~7

For example, P1C4 means bit 4 of port C on connector CN1.

EXTCLK **:** External edge trigger signal for latch digital input data.
EVENT **:** External clock source for counter 0.
V5V **:** Onboard un-regulated 5V power supply output.
+12V **:** Onboard un-regulated +12V power supply output.

Figure 2.2 Connectors Pin Assignment of cPCI-7249R & R7249 (daughter Board) XCN1 SCSI 100 pin Assignment

2.6 R7249 OPTO-22 Connector Pin Assignment

The R7249 eguipped with two 50 pin male IDC connectors XCN2, XCN3, that interface with OPTO-22

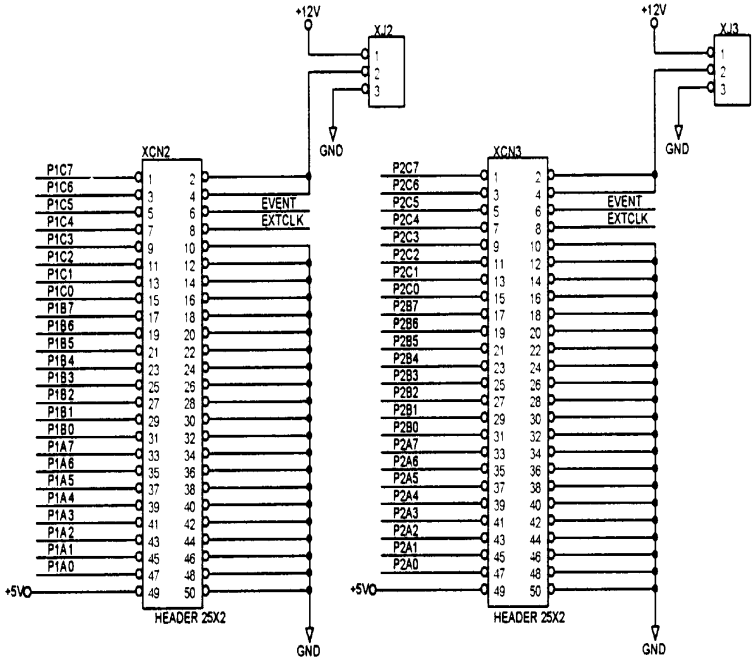


Figure 2.3 R7249 OPTO-22 Connectors Pin Assignment

Note : The power supply pins are protected by resetable fuses. Refer to section 3.7 for details of the power supply.

2.7 Jumper Description

The cPCI-7249R. DIO cards are 'plug and play' cards using cPCI bus. It is not necessary to setup the card configurations to fit the computer system's hardware configurations. However, to fit users' versitile operation environment, there are still a few jumpers to set the power on state of ports and the usage of the +12V output pins.

2.7.1 Power on State of Ports

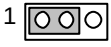
For every port on the cPCI-7249R cards, the power on state is set as input, therefore, the voltage could be pulled high, pulled low, or floating. It is dependent on the jumpers setting. Table 2.6 lists the reference number of the jumpers and the corresponding port names.

Jumper	Port Name
JA1	P1A (Port A of CN1)
JB1	P1B (Port B of CN1)
JC1	P1C (Port C of CN1)
JA2	P2A (Port A of CN2)
JB2	P2B (Port B of CN2)
JC2	P2C (Port C of CN2)

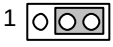
Table 2.6 Jumpers and Port names list

The physical meaning of all the jumpers are identical. The power on state of each port can be set independently. The defalut is to pull all signals high. The following diagram use JA1 as an example to show the possible configurations.And the JA1, JB1, JC1, JA2, JB2, JC2, default setting are pulled 'H'.

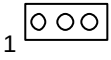
1. Port A of CN1 are power on pulled 'H'.



2. Port A of CN1 are power on pulled 'L'.



3. Port A of CN1 are power on floating. (The jumper is removed).



2.8 cPCI-7249R Installation Outline

2.8.1 Hardware configuration:

cPCI-7249R has plug and play component, the card can requests an interrupt via a system call. The system BIOS responds with an interrupt assignment based on the cPCI-7249R's configuration registers and on known system parameters(which are set by system BIOS). Interrupts assigned are a function of the system, the system BIOS, the installed driver and the installed cPCI boards.

Memory usage (I/O port locations) of the cPCI-7249R is also assigned by system BIOS. The address assignment is done on a board-by-board basis for all cPCI-7249Rs in the system.

2.8.2 cPCI slot selection

The cPCI-7249R only for ADLink 3U compact PCI system.

2.8.3 Installation Procedures

1. Turn off your computer.

2. Turn off all accessories (printer, modem, monitor, etc.) connected to computer.

3. Before handling the cPCI-7249R, discharge any static buildup on your body by touching the metal case of the computer. Hold the edge and do not touch the components.

4. Position the board into the Compact PCI slot you selected.

2.8.4 Running the 7249UTIL.EXE

A testing program is included in this utility, you can check if your cPCI-7249R can work properly. Refer Section 5.2 for further detailed information.

3

Registers and Operation Theorem

In this chapter, a register format and primitive digital I/O operations of 7249 series products will be specified. The operation theorem of the digital I/O, timer, and interrupt are introduced. Before programming or applying the cPCI-7249R cards to your applications, please go through this chapter to understand the features of the functions.

3.1 I/O Port Base Address

The cPCI-7249R products function as a 32-bit cPCI target device to any master on the cPCI bus. There are three types of registers on the cPCI-7249R: PCI Configuration Registers (PCR), Local Configuration Registers (LCR) and cPCI-7249R registers.

The PCR which conforms the cPCI-bus specifications is initialized and controlled by the system plug & play cPCI BIOS. Please refer to the cPCI BIOS specification to understand how to get information from the PCRs.

The LCR is specified by the PCI bus controller PLX-9050. It is not necessary for users to understand the details of the LCR if you use the software library. The base address of the LCR is assigned by the PCI p&p BIOS. The assigned address is located at offset 14h of PCR. Please refer to the PCI-9050's data sheet for the detail operation of the LCR and also the register format of the PCR.

The registers of 7249R series are shown in the Table 3.1. The base address of these registers is also assigned by the cPCI p&p BIOS. The assigned base address is stored at offset 18h of PCR. Therefore, users can read the PCR to know the base address by using the BIOS function call.

Note that the cPCI-7249R registers are all 8 bits. The users can access these registers by 8 bits I/O instructions only.

3.2 Registers Map

Table 3.1.1 shows the registers' description and offset address relative to the base address. Please refer to the following sections for more detail of every registers.

Offset	Write	Read
0x00	P1A	P1A
0x01	P1B	P1B
0x02	P1C	P1C
0x03	P1Ctrl	No used
0x04	P2A	P2A
0x05	P2B	P2B
0x06	P2C	P2C
0x07	P2Ctrl	No used
0x08	No used	P1AE
0x09	No used	P1BE
0x0A	No used	P1CE
0x0C	No used	P2AE
0x0D	No used	P2BE
0x0E	No used	P2CE
0x10	Timer/Counter #0	Timer/Counter #0
0x11	Timer/Counter #1	Timer/Counter #1
0x12	Timer/Counter #2	Timer/Counter #2
0x13	Timer/Counter Mode Control	Timer/Counter Mode Status
0x20	ISC: Interrupt Source Control	No used
0x30	Clear Interrupt	No used

Table 3.1.1 Register Description

3.3 Digital I/O Ports

3.3.1 Introduction

The 7249 products can emulate one/ two mode 0 configuration of 8255 programmable peripheral interface (PPI) chips.

3.3.2 8255 Mode 0

The basic functions of 8255 mode 0 are :

- Two 8-bit I/O ports - port A (PA) and port B (PB)
- Two nibble-wide (4-bit) ports C - PC upper and PC lower
- Any port can be used as either input or output
- Outputs are latched whereas inputs are buffered
- 16 different input / output configurations are available

3.3.3 Special Funtion of the DIO Signals

Two I/O signals (PC0 and PC3) of CN1 and CN2 can be used to generate hardware interrupt. Refer to the 'interrupt system' section for details about the interrupt control. In addition, the event signals(for SCSI-100 Pin 50) can be used as input signal of event counter.

3.3.4 Digital I/O Port Programming

Users can write the digital output value to or read back the digital signal level from the PPI ports by using the software library. Here we define the port name in Table 3.1.1. These port names are used both in software library and all through this manual. Althought there are two 8255 PPIs in cPCI-7249R.

There are four ports on every 8255 PPI, including port A,B,C and the control prot. PA,PB and PC could be wrote or read but the control port is write only.The cPCI-7249R suppose P1AE, P1BE, P1CE, P2AE,P2BE, P2CE for read only.Refer to section 4.3 for details about programming of DIO ports.

3.3.5 Control Word

The *control word* written in the control port is used to setup PA, PB and PC as input or output port. Fig 3.1 shows the format of the control word. Table 3.1.2 shows the 16 possible control word and the respective I/O configurations .

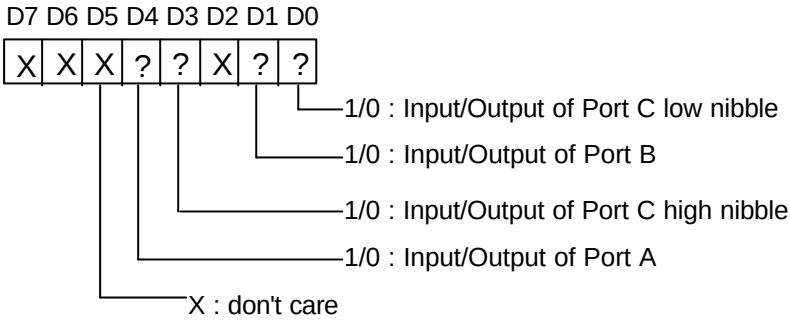


Figure 3.1 Control Word Format

Control Word	D 4	D 3	D 1	D 0	PORT A	PORT C UPPER	PORT B	PORT C LOWER
00H	0	0	0	0	O/P	O/P	O/P	O/P
01H	0	0	0	1	O/P	O/P	O/P	I/P
02H	0	0	1	0	O/P	O/P	I/P	O/P
03H	0	0	1	1	O/P	O/P	I/P	I/P
08H	0	1	0	0	O/P	I/P	O/P	O/P
09H	0	1	0	1	O/P	I/P	O/P	I/P
0AH	0	1	1	0	O/P	I/P	I/P	O/P
0BH	0	1	1	1	O/P	I/P	I/P	I/P
10H	1	0	0	0	I/P	O/P	O/P	O/P
11H	1	0	0	1	I/P	O/P	O/P	I/P
12H	1	0	1	0	I/P	O/P	I/P	O/P
13H	1	0	1	1	I/P	O/P	I/P	I/P
18H	1	1	0	0	I/P	I/P	O/P	O/P
19H	1	1	0	1	I/P	I/P	O/P	I/P
1AH	1	1	1	0	I/P	I/P	I/P	O/P
1BH*	1	1	1	1	I/P	I/P	I/P	I/P

Table 3.1.2 Summary of control word (D0 - D4).

(* power on defalut configuration)

3.3.6 Power On Configuration

The defalut configuration after *power on*, *hardware reset* or *software reset* is to set all ports as input ports, therefore the users won't worry about damaging the external devices when system is power on. In addition, the default signal level can be pulled high or pulled low by setting the jumpers. Refer to section 2.6 for setting the power on state of the DIO ports.

3.3.7 Note for Output Data

Be careful about the initial condition of dgital output signals. If user set the control word as output port after power on, the previous uncertain output value will be put on the output pins immediately. Therefore, **BE SURING TO SET A SAFE OUTPUT VALUE BEFORE SETTING ANY PORT AS OUT PORT.**

3.4 8254 Timer / Counter Operation

3.4.1 Introduction

One 8254 programmable timer/counter chip is installed in cPCI-7249R. There are three counters in one 8254 chip and 6 possible operation modes for each counter. The block diagram of the timer /counter system is shown in Figure 3.2.

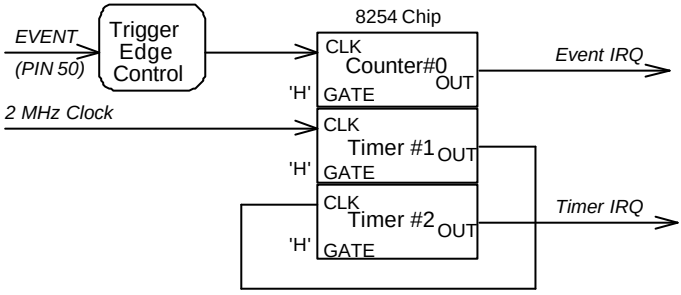


Figure 3.2 Timer / counter system of cPCI-7249R.

The timer #1 and timer #2 of the 8254 chip are cascaded as a 32-bits programmable timer. In software library, the timer #1 and #2 are always set as mode 2 (rate generater).

In software library, the counter #0 is used as an event counter, that is, interrupt on terminal count of 8254 mode 0 . Please refer to section 4.4 for programming the timer / counter functions.

3.4.2 Cascaded 32 bits Timer

The input clock frequency of the cascaded timers is 2M Hz. The output of the timer is sent to the interrupt circuit (refer to section 3.3). Therefore, the maximum and minimum watchdog timer interrupt frequency is (2M Hz)/(2*2)=(500K Hz) and (2M Hz)/(65535*65535) respectively.

3.4.3 Event Counter and Edge Control

The counter #0 of the 8254 chip can be used as event counter. The input of counter #0 is SCSI-100 Pin-50 “EVENT”. The counter clock trigger direction (H to L or L to H) is programmable. The gate control is always enabled. The output is send to interrupt system which named as event IRQ. If counter #0 is set as 8254 mode 0, the event counter IRQ will generate when the counter value is counting down to zero.

3.5 Interrupt Circuit

3.5.1 System Architecture

The cPCI-7249R's interrupt circuit is a powerful and flexable system which is suitable for many applications. The system is a ***Dual Interrupt System***. The dual interrupt means the hardware can generate two interrupt request signals in the same time and the software can service these two request signals by ISR. Note that the dual interrupt do not mean the card occupy two IRQ levels.

The two interrupt request signals (INT1 and INT2) are comes from digital input signals or the timer / counter output. An interrupt sources multiplexer (MUX) is used to select the IRQ sources. Fig 3.3.1 shows the interrupt system.

3.5.2 IRQ Level Setting

There is only one IRQ level is used by this card, althought it is a dual interrupt system. This card uses INT #A interrupt request siganl to PCI bus. The mother board circuits will transfer INT #A to one of the AT bus IRQ levels. The IRQ level is set by the PCI plug and play BIOS and saved in the PCI controller. It is not necessary for users to set the IRQ level. Users can get the IRQ level setting by software library. Refer the section 4.11.

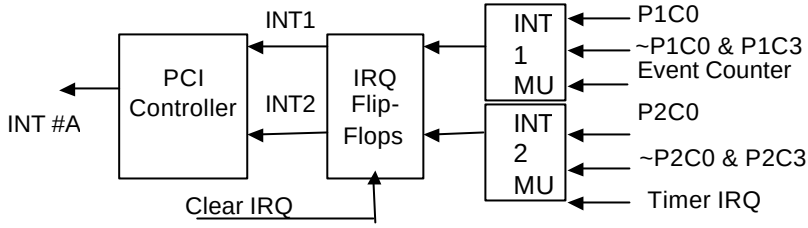


Figure 3.3.1 Dual Interrupt System of cPCI-7249R

3.5.3 Dual Interrupt System

The cPCI controller of cPCI-7249R can receive two hardware IRQ sources. However, a PCI controller can generate only one IRQ to cPCI bus, the two IRQ sources must be distinguished by ISR of the application software if the two IRQ are all used.

The two IRQs are named as INT1 and INT2. INT1 comes from P1C0, P1C3 or the event counter interrupt. INT2 comes from P2C0, P2C3 or the timer interrupt. The sources of INT1 and INT2 is selectable by the Interrupt Source Control (ISC) Register.

3.5.4 Interrupt Source Contorl

There are four bits to control the IRQ sources of INT1 and INT2. The Table 3.3.1 shows the selection of the IRQ sources and the interrupt trigger conditions.

If the application need only one IRQ, you can disable one of the IRQ sources by software. If your application do not need any IRQ source, you can disable all the two interrupts. However, the cPCI BIOS still assign a IRQ level to the cPCI card and occupy the PC resource, if you only disable the IRQ sources without change the initial condition of the

cPCI controller.

It is not suggested to re-design the initial condition of the cPCI card by users' own application software.

The table 3.3.4 shows the register format of the ISC (address offset ox20). This register is read only. The 4 LSBs are used to control the source of INT1 and INT2.

INT1	D3	D2	D1	D0	IRQ Sources	IRQ Trigger Condition
Disable	X	X	0	0	INT1 disable	--
Mode 1	X	X	0	1	~P1C0	falling edge of P1C0
Mode 2	X	X	1	0	P1C0 OR ~P1C3	(see following)
Mode 3	X	X	1	1	Event Counter	Counter count down to 0

INT2	D3	D2	D1	D0	IRQ Sources	IRQ Trigger Condition
Disable	0	0	X	X	INT2 disable	--
Mode 1	0	1	X	X	~P2C0	falling edge of P2C0
Mode 2	1	0	X	X	P2C0 OR ~P2C3	(see following)
Mode 3	1	1	X	X	Timer Output	Timer count down to 0

Table 3.3.1 ISC register format

When the IRQ sources is set as “P1C0 OR ~P1C3”, the IRQ trigger conditions are summarized in table 3.3.2,

P1/2C0	P1/2C3	IRQ Trigger Condition
High	X	PC0=‘H’ disable all IRQ
X	Low	PC3=‘L’ disable all IRQ
Low	1->0	PC3 falling edge trigger when PC0=L
0->1	High	PC0 rising edge trigger when PC3=H

Table 3.3.2 IRQ Trigger conditions

Because the P1/P2C0 and P1/P2C3 are external signals, the applications can utilize the combination of the four signals to generate a proper IRQ.

3.6 External Trigger Register

The cPCI-7249R supposes independent register to latch data. User can usr pin99 EXTCLK to latch Digital Input Data.

3.7 12V and 5V Power Supply

The SCSI-100 connectors provide external devices the +12 volts and +5 volts power supply. To aviod short or overload of the power supply, the ***resetable fuses*** are added on all the power supply pins. Refer to Figure 2.2. The power supply of the rear daughter boand refers to Figure 2.3.

The maximun current for 5 volts on every connector is 0.5 A. If the load current is larger than 0.5 A, the resistance of fuse will increase because of the temperature rising. The rising resistance will cause the power supply drop and reduce current. If the overload or short condition is removed, the fuse will get to normal condition. It is not nessary to repair or re-install the fuse.

The maximum current of 12 volts for all the fuse connectors is also 0.5 A. The action of the fuse is the same as which used for +5V power. The limitation is more resitrict than 5V power supply because the cPCI bus can not provide large current.

4

C/C++ Software Libraries

In this chapter, the cPCI-7249R software libraries for DOS and Windows 95 are described.

4.1 Installation

4.1.1 Installation

The cPCI-7249R's Software Library supplied with cPCI-7249R includes a utility software, C-language library and some demonstration programs which can help you reduce programming work.

- **MS-DOS Software Installation**

1. Turn your PC's power switch on.
2. Put the ADLINK's "All-in-one" CD into the appropriate CD driver.
3. Type the commands(X indicates the CD ROM driver) under DOS environment:

   For cPCI-7249R:

   X:\> **CD NuIPC\7249\DOS**

   X:\ NuIPC\7249\DOS> **SETUP**

4. An installation completed message will be shown on the screen.

After installation, all the files *of cPCI-7249R Library & Utility for DOS* are stored in C:\ADLINK\7249\DOS directory.

- **Windows 95 Software Installation**

1. Turn your PC's power switch on and enter Windows 95.

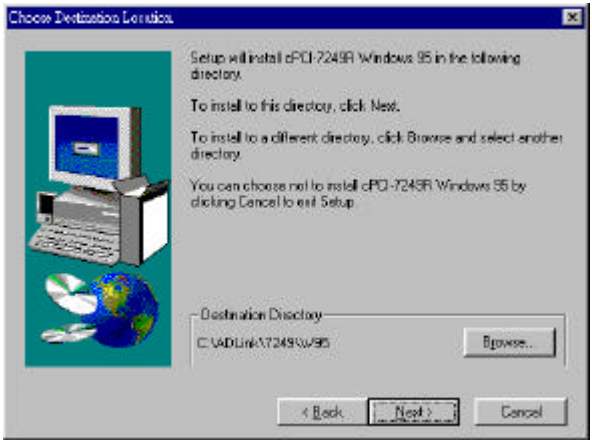
2. Put the ADLink's "All-in-one" CD into the appropriate CD drive.

3. If autorun setup program is not invoked automatically,please execute X:\Setup.exe (X indicates the CD-ROM drive).

4. Select NuIPC→Drivers→Win95/98→cPCI-7249R to setup cPCI-7249R Windows95 DLL driver.

Setup first displays a Welcome dialog box. Please click Next button to go on installation.

After a welcome dialog box, Setup prompts the following dialog box for you to specify the destination directory. The default path is C:\ADLink\7249\w95. If you want to install c*PCI-7249R DLL for Windows 95* in another directory, please click Browse button to change the destination directory.



Then you can click Next to begin installing c*PCI-7249R DLL for Windows 95*.

After you complete the installation of cPCI-7249R Software, PCI-7249R's DLL is copied to Windows System directory (default is C:\WINDOWS\SYSTEM for Win-95) and the driver files (W95_7249.VXD and PCIW95.VXD) are also copied to the appropriate directory.

4.2 Running Testing Utility (7249UTIL.EXE)

After finishing the DOS installation, you can execute the utility by typing as follows :

C> cd \7249\DOS\UTIL

C> 7249UTIL

4.3 Software Driver Naming Convention

The functions of cPCI-7249R's software drivers are using full-names to represent the functions' real meaning. The naming convention rules are :

In DOS Environment :

_{hardware_model}_{action_name}. e.g. _7249_Initial().

In order to recognize the difference between DOS library and Windows 95 library, A capital "W" is put on the head of each function name of the Windows 95 DLL driver. e.g. W_7249_Initial().

There are 5 functions provided by cPCI-7249R software drivers. The detail descriptions of each function are specified in the following sections. The functions prototype and some useful constants are defined in Acl_pci.h.

4.4 _7249_Initial

@ Description

The cPCI-7249R cards are initialized by this function. The software library could be used to control multiple cPCI-7249R cards. Because cPCI-7249R is in cPCI bus architecture and meets the plug and play specifications, the ***IRQ*** and ***I/O address*** are assigned by system BIOS directly.

@ Syntax

cPCI-7249R:

C/C++ (DOS, Windows 95)

U16 W_7249_Initial (U16 *existCards, PCI_INFO *pciInfo)

Visual Basic (Windows 95)

W_7249_Initial (existCards As Integer, pciInfo As PCI_INFO) As Integer

@ Argument

existCards : The numbers of installed cPCI-7249R cards. The returned value shows how many cPCI-7249R cards are installed in your system.

pciinfo: It is a structure to memorize the cPCI bus plug and play initiallization information which is decided by p&p BIOS. The cPCI_INFO structure is defined in ACL.PCI.H The base I/O address and the interrupt channel number is stored in pciinfo which is for reference.

@ Return Code

ERR_NoError
ERR_PCIBiosNotExist

4.5 _7249_DI

@ Description

This function is used to read 8-bit digital inputs data from digital input port. You can get the 8 bits data from _7249_DI by using this function.

The written data and read in data is 8 bits data. Each data is mapped to a signal as the table below.

D7	D6	D5	D4	D3	D2	D1	D0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

D7	D6	D5	D4	D3	D2	D1	D0
PA7E	PA6E	PA5E	PA4E	PA3E	PA2E	PA1E	PA0E
PB7E	PB6E	PB5E	PB4E	PB3E	PB2E	PB1E	PB0E
PC7E	PC6E	PC5E	PC4E	PC3E	PC2E	PC1E	PC0E

External trigger Register

@ Syntax

cPCI-7249R:

C/C++ (DOS)

U16 _7249_DI (U16 cardNo, U16 channelPort, U16 *diData)

C/C++ (Windows 95)

U16 W_7249_DI (U16 cardNo, U16 channelPort, U16 *diData)

Visual Basic (Windows 95)

W_7249_DI (ByVal cardNo As Integer, ByVal channelPort As Integer, diData As Integer) As Integer

- **@ Argument**

cardNo : card number to select borad

channelPort : port of each channel

PCI_CH0_PA : CH1's Port A
PCI_CH0_PB : CH1's Port B
PCI_CH0_PC : CH1's Port C
PCI_CH0_PCU : CH1's Port C Upper Nibble
PCI_CH0_PCL : CH1's Port C Low Nibble
PCI_CH1_PA : CH2's Port A
PCI_CH1_PB : CH2's Port B
PCI_CH1_PC : CH2's Port C
PCI_CH1_PCU : CH2's Port C Upper Nibble
PCI_CH1_PCL : CH2's Port C Low Nibble
PCI_CH0_PAE : CH1s Port A uses External Trigger
PCI_CH0_PBE : CH1s Port B uses External Trigger
PCI_CH0_PCE : CH1's Port C uses External Trigger

PCI_CH1_PAE : CH2's Port A uses External Trigger
PCI_CH1_PBE : CH2's Port B uses External Trigger
PCI_CH1_PCE : CH2's Port C uses External Trigger

diData : return 8-bit value from digital port.

@ **Return Code**

ERR_NoError

4.6 _7249_DO

@ **Description**

This function is used to write data to digital output port. There are 6 digital output ports (P1A, P1B, P1C, P2A, P2B, P2C) could be configured as digital output channel on the cPCI-7249R,

@ **Syntax**

cPCI-7249R:

C/C++ (DOS)

U16 _7249_DO (U16 cardNo, U16 channelPort, U16 doData)

C/C++ (Windows 95)

U16 W_7249_DO (U16 cardNo, U16 channelPort, U16 doData)

Visual Basic (Windows 95)

W_7249_DO (ByVal cardNo As Integer, ByVal channelPort As Integer, ByVal doData As Integer) As Integer

@ **Argument**

cardNo : card number to select borad channelPort :

channelPort : port of each channel

PCI_CH0_PA : CH1's Port A
PCI_CH0_PB : CH1's Port B
PCI_CH0_PC : CH1's Port C
PCI_CH0_PCU : CH1's Port C Upper Nibble
PCI_CH0_PCL : CH1's Port C Low Nibble
PCI_CH1_PA : CH2's Port A
PCI_CH1_PB : CH2's Port B
PCI_CH1_PC : CH2's Port C
PCI_CH1_PCU : CH2's Port C Upper Nibble
PCI_CH1_PCL : CH2's Port C Low Nibble

doData : value will be written to digital output port

@ **Return Code**

ERR_NoError

4.7 _7249_Config_Port

@Description

This function is used to configure the Input or Ouput of each Port. Each I/O Port of cPCI-7249R is either input or output, so it has to configure as input or output before I/O operations are applied.

@Syntax

cPCI-7249R:

C/C++ (DOS, Windows 95)

U16 W_7249_Config_Port (U16 cardNo, U16 channelPort, U16 direction)

Visual Basic (Windows 95)

W_7249_Config_Port (ByVal cardNo As Integer, ByVal channelPort As Integer, ByVal direction As Integer) As Integer

@Argument

cardNo : card number to select borad channelPort :

channelPort : port of each channel

PCI_CH0_PA : CH1's Port A
PCI_CH0_PB : CH1's Port B
PCI_CH0_PC : CH1's Port C
PCI_CH0_PCU : CH1's Port C Upper Nibble
PCI_CH0_PCL : CH1's Port C Low Nibble
PCI_CH1_PA : CH2's Port A
PCI_CH1_PB : CH2's Port B
PCI_CH1_PC : CH2's Port C
PCI_CH1_PCU : CH2's Port C Upper Nibble
PCI_CH1_PCL : CH2's Port C Low Nibble

direction : port I/O direction

INPUT_PORT : the port is configure as INPUT
OUTPUT_PORT : the port is configure as OUTUT

@ Return Code

ERR_NoError

4.8 _7249_Software_Reset

@ Description

This function is used to reset the I/O port configuration. After reset cPCI-7249R, all the ports will be set as input ports. Note that this function can not re-start the cPCI bus and all the hardware setting won't be change either.

@ Syntax

cPCI-7249R:

C/C++ (DOS, Windows 95)

U16 W_7249_Software_Reset (U16 cardNo)

Visual Basic (Windows 95)

W_7249_Software_Reset (ByVal cardNo As Integer) As Integer

@ Argument

cardNo : card number which the DIO will be reset.

@Return Code

ERR_NoError

4.9 _7249_INT_Start

@ Description

This function is only available in Windows 95 driver. This function is used to initialize and start up the interrupt control. Please refer to section 3.3 for detailed description of interrupt system. After calling this function, every time an interrupt request signal generated, a software event is signaled. So that in your program, you can use wait operation to wait for the event. When the event is signaled, it means an interrupt is generated. Please refer to the sample program 7249int.c .

@ Syntax

cPCI-7249R:

C/C++ (DOS, Windows 95)

void W_7249_INT_Start (U16 cardNo, U16 c1, U16 c2, U16 ctrlValue, HANDLE *hIntEvent)

Visual Basic (Windows 95)

W_7249_INT_Start (ByVal cardNo As Integer, ByVal c1 As Integer, ByVal c2 As Integer, ByVal ctrlValue As Integer, hIntEvent As Long)

@ Argument

cardNo : card number which the DIO will be reset.

c1 : If the interrupt source is set as internal timer source, this value is the frequency divider of Timer#1.

c2 : If the interrupt source is set as internal timer source, this value is the frequency divider of Timer#2.

ctrlValue: the value for INT mode setting. The value can be set for INT1 is INT1_OFF, INT1_P1C0, INT1_P1C3C0, or INT1_EVENT_IRQ. The value can be set for INT2 is INT2_OFF, INT2_P2C0, INT2_P2C3C0, or INT2_TIMER_IRQ. Please refer to section 3.3.4 for detailed description.

hIntEvent : the handle of the event for interrupt signals.

@ **Return Code**

ERR_NoError

4.10 _7249_INT_Stop

@ **Description**

This function is only available in Windows 95 driver. This function is used to disable the interrupt signal generation.

@ **Syntax**

cPCI-7249R:

C/C++ (DOS, Windows 95)

void W_7249_INT_Stop (U16 cardNo)

Visual Basic (Windows 95)

W_7249_INT_Stop (ByVal cardNo As Integer)

@ **Argument**

cardNo : card number which the DIO will be reset.

@ **Return Code**

ERR_NoError

4.11 _7249_INT_Source_Control

@ **Desctiption**

The cPCI-7249 has dual interrupts system, two interrupt sources can be generated and be checked by the software. This function is used to select and control cPCI-7249 interrupt sources by writing data to interrupt control register. Please refer to section 3.5 for detailed description of interrupt system.

@ **Syntax**

C/C++ (DOS)

void _7249_INT_Source_Control (U16 cardNo, U16 Int1Ctrl , U16 Int2Ctrl)

C/C++ (Windows 95)

void W_7249_INT_Source_Control (U16 cardNo, U16 Int1Ctrl , U16 Int2Ctrl)

Visual Basic (Windows 95)

W_7249_INT_Source_Control (ByVal cardNo As Integer, ByVal Int1Ctrl As Integer , ByVal Int2Ctrl As Integer)

@ **Argument**

cardNo: the card number of cPCI-7249 card initialized.

Int1Ctrl the value to control INT1, the value can be set and the corresponding definition is the following:

0: INT1_OFF

1: INT1_P1C0

2: INT1_P1C3C0

3: INT1_EVENT_IRQ

int2Ctrl: the value to control INT2, the value can be set and the corresponding definition is the following:

int2Ctrl0: INT2 _OFF

1 : NT2 _P2C0

2: NT2 _P2C3C0

3: INT2_TIMER_IRQ

@ **Retutn Code**

None

4.12 7249_CLR_IRQ

@ **Description**

This function is used to clear interrupt request which is requested by cPCI-7249.

@ **Syntax**

C/C++ (DOS)

void _7249_CLR_IRQ (U16 cardNo)

C/C++ (Windows 95)

void W_7249_CLR_IRQ (U16 cardNo)

Visual Basic(Windows 95)

W_7249_CLR_IRQ (ByVal cardNo As Integer)

@ **Argument**

None

@ **Return Code**

None

Product Warranty/Service

ADLINK warrants that equipment furnished will be free from defects in material and workmanship for a period of one year from the date of shipment. During the warranty period, we shall, at our option, either repair or replace any product that proves to be defective under normal operation.

This warranty shall not apply to equipment that has been previously repaired or altered outside our plant in any way as to, in the judgment of the manufacturer, affect its reliability. Nor will it apply if the equipment has been used in a manner exceeding its specifications or if the serial number has been removed.

ADLINK does not assume any liability for consequential damages as a result from our product uses, and in any event our liability shall not exceed the original selling price of the equipment. The remedies provided herein are the customer's sole and exclusive remedies. In no event shall ADLINK be liable for direct, indirect, special or consequential damages whether based on contract of any other legal theory.

The equipment must be returned postage-prepaid. Package it securely and insure it. You will be charged for parts and labor if the warranty period is expired or the product is proves to be misuse, abuse or unauthorized repair or modification.