NEC

Preliminary User's Manual

ET-0170

μPD720133 (USB2.0 to IDE Bridge) Evaluation Board

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[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

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INTRODUCTION

Readers

This manual is intended for engineers who will test USB2.0 to IDE bridge system by using the ET-0170.

Purpose

This manual explains the functions of the ET-0170 in the following arrangements.

Arrangement

This manual includes the following chapters.

- Overview
- Usage of the ET-0170
- Parts information
- Reference for connection
- The ET-0170 board information

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, USB specification, USB mass storage class specification, and AT Attachment with Packet Interface-6 (ATA/ATAPI-6) specification.

Conventions

Data significance:	Higher significant digits on the left and lower significant digits on the right
Active low representation:	xxxB (B suffixed to pin name or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric notation:	Binary … xxxx or xxxxB Decimal … xxxx Hexadecimal … xxxxH

Related Documents

The related documents indicated in this document may include preliminary versions.

- μPD720133 Data Sheet: To be released soon
- μPD720133 User's Manual: To be released soon
- μPD720133 Application Note Serial ROM Utility: To be released soon

- Universal Serial Bus Specification 2.0
- Universal Serial Bus Mass Storage Class Specification Overview (Including documents listed in the Overview)
- AT Attachment with Packet Interface-6 (ATA/ATAPI-6) specification

Be sure to read the latest version of the above documents when using the ET-0170.

Version History

No.	Version	Description
1	ET-0170 (FB-2471A)	1st Version

Details in difference are described in this manual.

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CHAPTER 1 OVERVIEW

This document describes the functions of the μPD720133 evaluation board ET-0170.

The μPD720133 and a serial ROM are implemented on the ET-0170. This board allows quick test of different serial ROM's data setting against the μPD720133 during prototyping.

1.1 Features

This section explains the main features of the ET-0170.

(1) Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 12/480 Mbps)
This board has the μPD720133 which is the bus/self-powered high-speed capable device and works at 12 Mbps data rate (FS: full speed) or 480 Mbps date rate (HS: high speed).

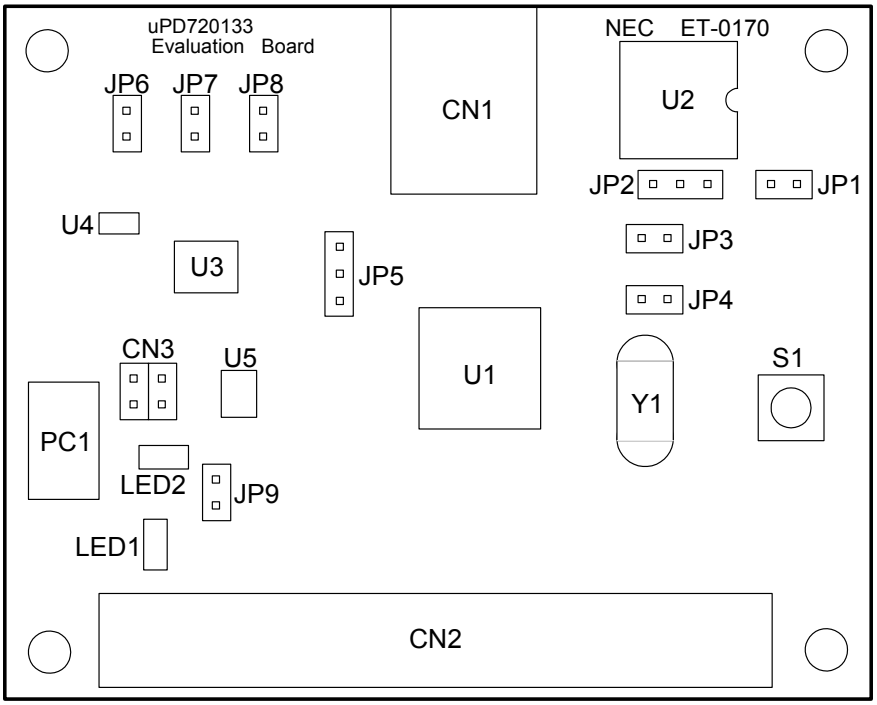
(2) Compliant with AT Attachment with Packet Interface-6 (ATA/ATAPI-6). The IDE controller in the μPD720133 supports PIO Mode 0-4, Multi Word DMA Mode 0-2, Ultra DMA Mode 0-4, and LBA48. The evaluation kit comes with Ultra DMA Mode 4 IDE cable. The IDE bridge system will be ready for test once IDE target device is attached.

(3) Bus-powered USB2.0 to IDE bridge system
The device supports bus-powered operation if the power consumption for whole USB2.0 to IDE bridge system is less than the specification for bus-powered device. The μPD720133 has some features such as power supply control signaling for IDE device. The power supply circuitry on the board uses either VBUS or external power supply for the power line connector connecting to the IDE target device. The power line connector has DPC, GND and V_{DD} line, and it is readily for bus-powered application using the power supply circuit on board.

(4) Extension for function
The function of the μPD720133 is controlled by data in serial ROM. Also, It is possible to realize firmware extension by using the serial ROM. This board has a serial ROM socket for quick serial ROM replacement.

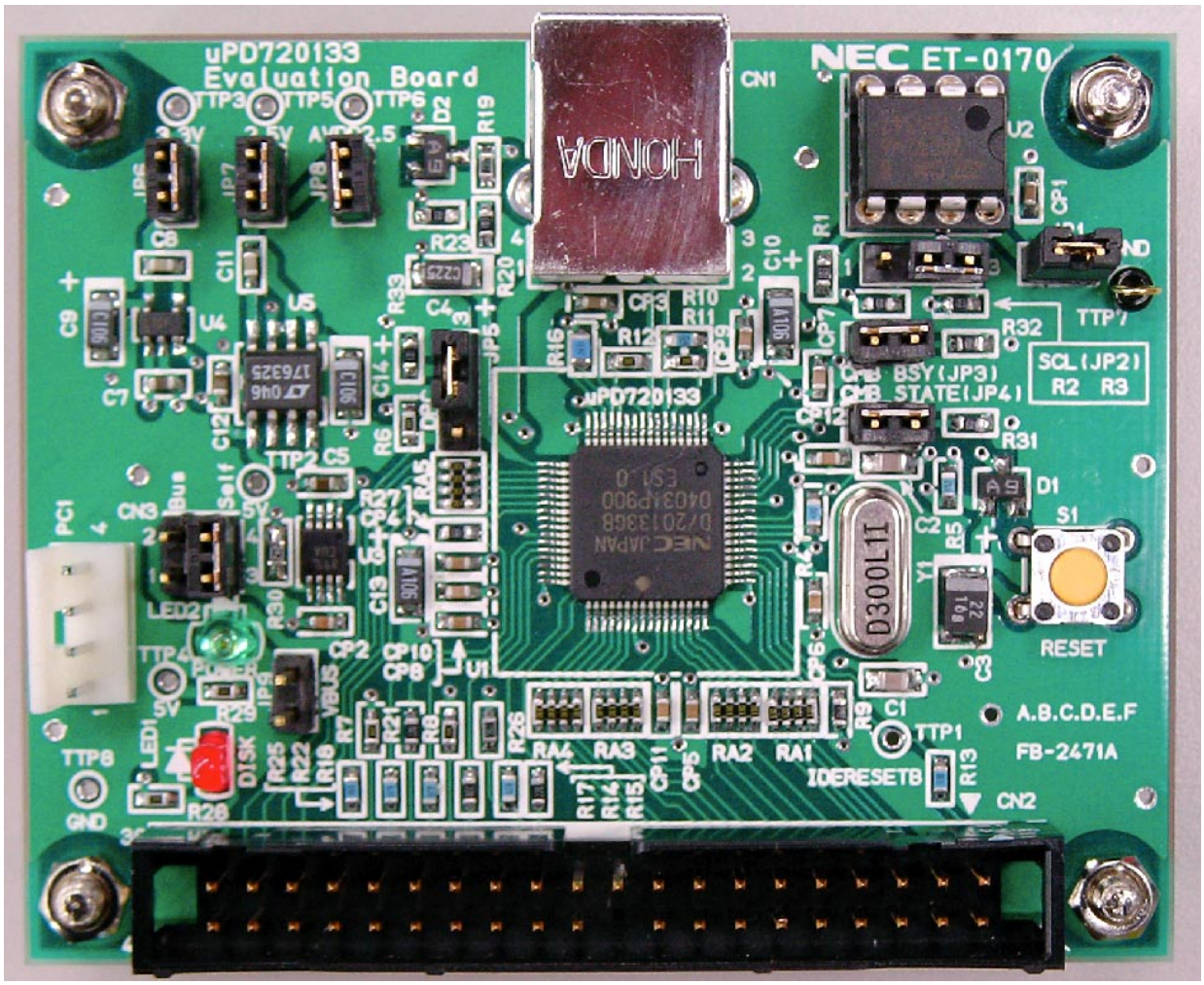
1.2 Board Diagram

Figure 1-1. Board Diagram



PC1 : Power line connector
CN1 : USB connector
CN2 : IDE connector
CN3 : Power line selection connector
U1 : USB to IDE bridge chip (*μ*PD720133)
U2 : Socket (Serial ROM)
U3 : Regulator
U4 : Regulator
U5 : Power switch
LED1 : Access lamp
LED2 : Power LED
Y1 : X'tal
S1 : Reset switch
JP(9:1) : Jumper

1.3 Picture of the ET-0170



CHAPTER 2 USAGE OF THE ET-0170

2.1 Required Items to Test IDE Bridge System with the μPD720133

This section explains the required items to test IDE bridge system with the ET-0170.

2.1.1 Power supply

The ET-0170 requires 5 V power supply. Typical ATX power supply or any other 5 V power supply is applicable. The PC1 connector on this board uses the power connector of 3.5” floppy drive (FDD).

2.1.2 USB cable

A USB cable is required certifying by USB Implementers Forum as high-speed capable. If the uncertified cable is used for this system, the transaction error on USB bus may be occurred. And if any transaction error occurs on USB bus, the performance of the ET-0170 will be degraded.

2.1.3 PC

It is required that PC should have a USB 2.0 Host controller on the mother board or on the PCI card plugged into PCI slot. If the IDE bridge system operates in high-speed transactions at 480 Mbps, EHCI driver should be installed on Windows® 2000 or Windows XP system. USB Mass Storage Class Driver is also required for test of the IDE bridge system. A standard USB Mass Storage Class Driver is bundled in Windows Me, Windows 2000 and Windows XP.

2.1.4 IDE device

It is required that an IDE device compliant with ATA/ATAPI-5 (Also ATA/ATAPI-6) be connected to the ET-0170.

2.2 How to Setup IDE Bridge System

This section explains how to set up the IDE bridge system with the ET-0170 before evaluation.

2.2.1 Check jumper and connector setting

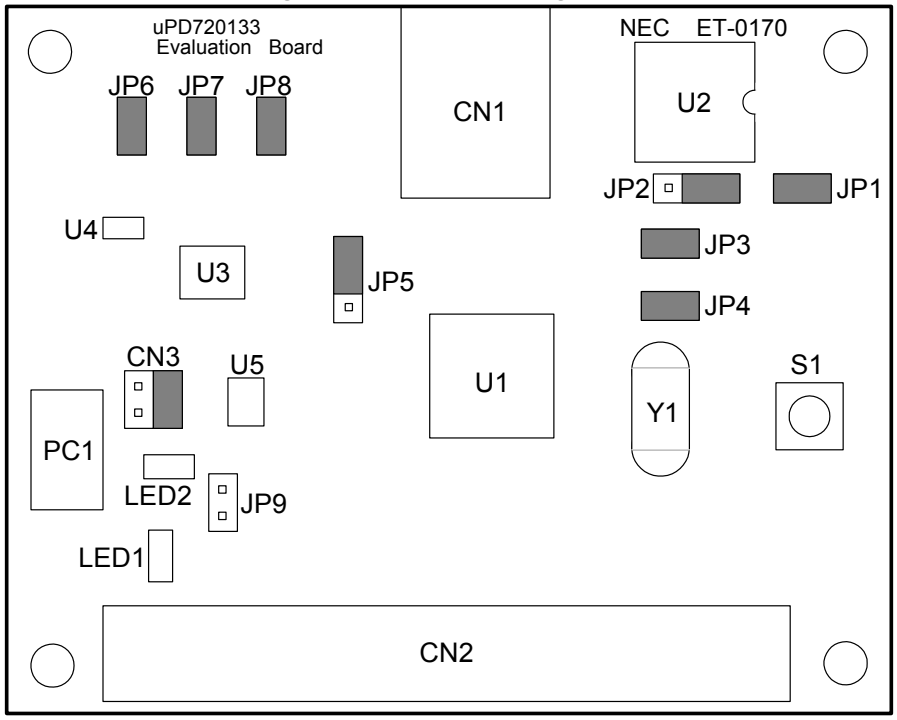
Be sure to check Jumper setting as follows.

Table 2-1. Jumper Setting

Symbol	Jumper	Setting		Description
		1 - 2	2 - 3	
JP1		Short	-	Power supply to an serial ROM (U2)
JP2	SCL	Open	Short	SCL pin (μPD720133)
JP3	CMB_BSY	Short	-	CMB_BSY pin (μPD720133)
JP4	CMB_STATE	Short	-	CMB_STATE pin (μPD720133)
JP5	DPC	Open	Short	DPC pin (μPD720133)
JP6		Short	-	Current measurement point for V_{DD33}
JP7		Short	-	Current measurement point for V_{DD25}
JP8		Short	-	Current measurement point for AV_{DD}
JP9	VBUS	Short	-	Power supply from the VBUS line

Symbol	Setting		Description
CN3	1 - 2	Open	Power line from a power switch (U3)
	3 - 4	Short	Power line from PC1

Figure 2-1. Jumper Setting



2.2.2 Board checking

Check a serial ROM has been inserted into a socket (U2) properly (The ET-0170 is shipped with one serial ROM). Check the board is damaged from shipment.

2.2.3 Connects IDE device to the ET-0170

Connect both ends of IDE cable to IDE device and the ET-0170. An IDE cable must support Ultra DMA/66 for test of an Ultra DMA/66 IDE device.

2.2.4 Connects power supply to IDE device and the ET-0170

This section assumes that the power supply is ATX type. Before a connector for FDD of an ATX power supply is connected to the ET-0170, the ATX power supply must be turned OFF. Choose the appropriate power supplying to the IDE device.

2.3 How to Test IDE Bridge System

2.3.1 Power ON

When the output from an ATX power supply is activated, the LED2 (green) is turned on. At this time, if the LED2 is not turned on, the ATX power supply should be turned off immediately. And be sure to recheck jumper settings, board, IDE device, and connection of power supply. Next, check LED1 (red) is flashed on and off. (Operations of LED1 depend on IDE devices)

At this point, the initialization of the μPD720133 is done and the μPD720133 is communicating to IDE device.

2.3.2 Connect to USB port

Connect the ET-0170 to a USB2.0 host with a USB cable. Once the μPD720133 detects the valid voltage level at the VBUS pin from USB connection, the μPD720133 enables a Pull-up resistor on D+ line. And then, the host controller detects the ET-0170.

After the enumeration has been completed, the IDE device is shown in the Device Manager and Explorer window. And IDE device is ready for use.

2.3.3 Disconnect from USB port

When the ET-0170 is disconnected from the USB2.0 host, the application software accessing a device should be stopped at first. And it is preferred to use the unplug tool found in Windows' system tray to avoid instability in OS before the removable device is disconnected from USB bus. There is no damage to the ET-0170 without using the unplug tool.

CHAPTER 3 PARTS INFORMATION

3.1 Parts Information

This section describes main components on the ET-0170.

3.1.1 μPD720133

The μPD720133 implements USB2.0 transceiver, endpoint controller, firmware and etc to realize USB2.0 to IDE bridge system.

Detailed function descriptions are provided in the following user's manual.

μPD720133 Preliminary User's Manual: To be released soon

Figure 3-1. Pin Configuration (Top View)

- 64-pin plastic TQFP (Fine pitch) (10 × 10)
  μPD720133GB-YEU

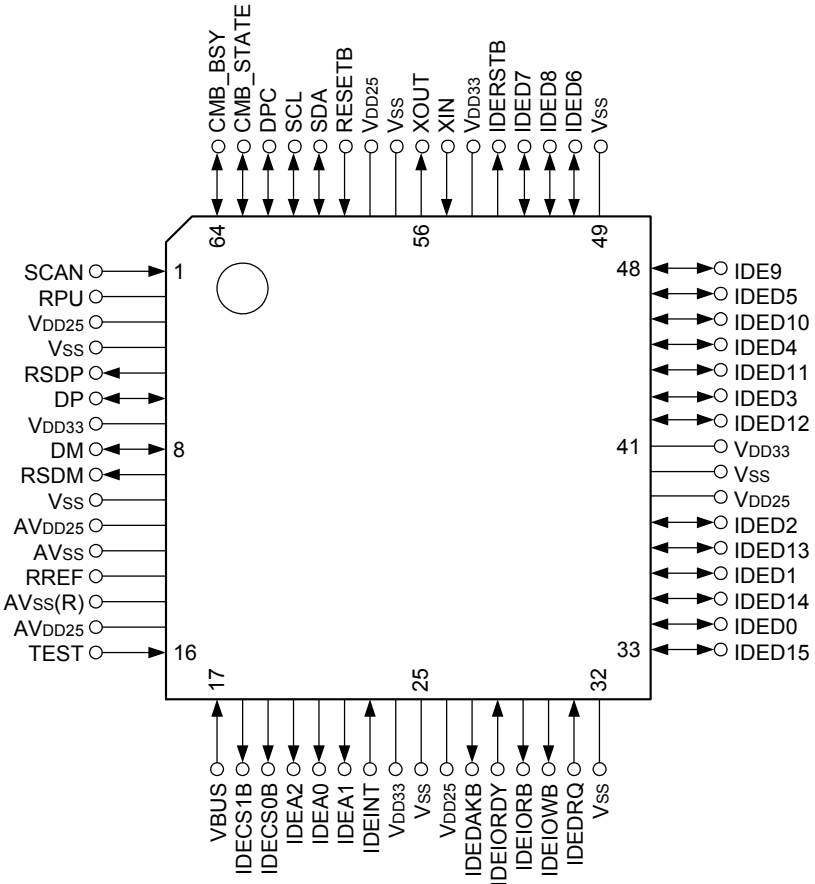


Table 3-1. Pin Information

Pin Name	I/O	Buffer Type	Active Level	Function
XIN	I	2.5 V Input		System clock input or oscillator In
XOUT	O	2.5 V Output		Oscillator out
RESETB	I	3.3 V Schmitt Input	Low	Asynchronous reset signaling
IDECS(1:0)B	O (I/O)	5 V tolerant Output	Low	IDE host chip select
IDEA(2:0)	O (I/O)	5 V tolerant Output		IDE address bus
IDEINT	I	5 V tolerant Input	High	IDE interrupt request from device to host
IDEDAKB	O (I/O)	5 V tolerant Output	Low	IDE DMA acknowledge
IDEIORDY	I	5 V tolerant Input	High	IDE IO channel ready
IDEIORB	O (I/O)	5 V tolerant Output	Low	IDE IO read strobe
IDEIOWB	O (I/O)	5 V tolerant Output	Low	IDE IO write strobe
IDEDRQ	I	5 V tolerant Input	High	IDE DMA request from device to host
IDED(15:0)	I/O	5 V tolerant I/O		IDE data bus
IDERSTB	O (I/O)	5 V tolerant Output	Low	IDE reset from host to device
CMB_BSY (GPIO7)	I/O	3.3 V I/O		Combo IDE bus busy
CMB_STATE (GPIO6)	I/O	3.3 V I/O		Combo IDE bus state
DPC (GPIO5)	I/O	3.3 V I/O		Power control signaling for IDE device
SDA (PIO0)	I/O	3.3 V I/O		Serial ROM data signaling
SCL (PIO1)	I/O	3.3 V I/O		Serial ROM clock signaling
VBUS	I	5 V Schmitt Input [Note]		VBUS monitoring
DP	I/O	USB high speed D+ I/O		USB's high speed D+ signal
DM	I/O	USB high speed D– I/O		USB's high speed D– signal
RSDP	O	USB full speed D+ Output		USB's full speed D+ signal
RSDM	O	USB full speed D– Output		USB's full speed D– signal
RPU	A	USB Pull-up control		USB's 1.5 kΩ pull-up resistor control
RREF	A	Analog		Reference resistor
SCAN	I	3.3 V Input		Scan mode control
TEST	I	3.3 V Input		Test mode setting
AV_{DD25}				2.5 V V_{DD} for Analog circuit
V_{DD25}				2.5 V V_{DD}
V_{DD33}				3.3 V V_{DD}
AV_{SS}				V_{SS} for Analog circuit
V_{SS}				V_{SS}

Remarks 1. "5 V tolerant" means that the buffer is 3.3 V buffer with 5 V tolerant circuit.

2. The signal marked as "(I/O)" in the above table operates only as I/O signals during testing.

3.1.2 Serial ROM Socket (U2)

(1) Data in serial ROM

The μPD720133 loads data such as Vendor ID, Product ID and some additional USB related information from a serial ROM when the μPD720133 is initialized. Example of data in serial ROM is as follows. NEC Electronics releases tool to generate serial ROM data. Tool should be used to calculate the checksum needed in the serial ROM.

Detailed function descriptions are provided in the following user's manual and detailed information of tools is provided in following application note.

μPD720133 Preliminary User's Manual: To be released soon

μPD720133 Preliminary Application Note Serial ROM Utility: To be released soon

Table 3-2. Serial ROM Data

Offset (H)	Data Size	Symbol	Description
+00	1 Word	idMark	Validation Mark of 55AAH
+02	1 Word	CheckSum	Check sum of serial ROM
+04	1 Word	Flags	Control for descriptor overwrite
+06	1 Byte	ModeReset	PWR, CLC, DCC, DV[1:0], DPC Reset bit map field
+07	1 Byte	ModeSet	PWR, CLC, DCC, DV[1:0], DPC Set bit map field
+08	1 Word	idVendor	idVendor field in Device descriptor
+0A	1 Word	idProduct	idProduct field in Device descriptor
+0C	1 Word	bcdDevice	bcdDevice field in Device descriptor
+0E	1 Word	Reserved	Reserved for future use.
+10	1 Byte	MaxPower Bus	bMaxPower field in Configuration descriptor for Bus powered mode
+11	1 Byte	MaxPower Self	bMaxPower field in Configuration descriptor for Self powered mode
+12	1 Byte	bInterfaceClass	bInterfaceClass field in Interface descriptor
+13	1 Byte	bInterfaceSubClass	bInterfaceSubClass field in Interface descriptor
+14	1 Byte	bInterfaceProtocol	bInterfaceProtocol field in Interface descriptor
+15	1 Byte	Reserved	Reserved for future use.
+16	1Word	TxModeReset	IDE transmission type such as Ultra DMA 66 Reset bit map field
+18	1Word	TxModeSet	IDE transmission type such as Ultra DMA 66 Set bit map field
+1A	1Word	RompatchSW	ROM Patch information (Patch On or Off) of External Function
+1C	4 Bytes	Reserved	Reserved for future use.
+20	32 Bytes	ManufactureString	String descriptor for Manufacturer
+40	32 Bytes	ProductString	String descriptor for Product
+60	32 Bytes	SerialString	String descriptor for Device serial number
+80	128 × n Bytes	FW Patch	Firmware patch module for self-powered/bus-powered mode

(2) Control Bit in Serial ROM

The following tables show IDE status and control bit in serial ROM.

Table 3-3. DV1/DV0, CLC, PWR Setting

No.	Device Power	Internal Clock	ATA/ATAPI	PWR	CLC	DV1	DV0
0	Bus Powered	7.5 MHz	No device connected	1	1	1	1
1			ATA	1	1	1	0
2			ATAPI	1	1	0	1
3			Reserved	1	1	0	0
4		60 MHz	No device connected	1	0	1	1
5			ATA	1	0	1	0
6			ATAPI	1	0	0	1
7			Reserved	1	0	0	0
8	Self Powered	60 MHz	No device connected	0	1	1	1
9			Combo (ATA)	0	1	1	0
10			Combo (ATAPI)	0	1	0	1
11			Combo auto device detect	0	1	0	0
12			No device connected	0	0	1	1
13			ATA	0	0	1	0
14			ATAPI	0	0	0	1
15			Auto device detect	0	0	0	0

Remarks 1. Setting of no. 0, 3, 4, 7, 8, and 12 are not allowed.

2. For bus powered setting, some critical considerations such as power consumption for the total system should be observed.

3. The slave device function cannot use Auto device detect.

Table 3-4. DV1/DV0, DCC Setting

Condition				DCC setting in Serial ROM	Description
DV1	DV0	Mode	Target Device		
1	0	ATA	ATA	Reset	Ultra, Multi Word DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.
0	1	ATAPI	ATAPI	Reset	Ultra DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.
0	0	Auto device detect	ATA	Reset	Ultra, Multi Word DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.
			ATAPI	Reset	Ultra DMA are disabled.
				Set	Ultra, Multi Word DMA are enabled.

Remark PIO mode 0-4 are always enabled.

3.1.3 Power switch (U3)

In bus-powered system, in order to control the power supply to an IDE device with the DPC pin of the μPD720133, the ET-0170 has the power switch (U5).

3.1.4 Regulator (U4, U5)

The μPD720133 uses dual power rails. The ET-0170 uses two regulators. One is 2.5 V regulator (U4), another is 3.3 V regulator (U3).

3.1.5 Oscillator (Y1)

The ET-0170 uses the AT-49 30 MHz.

3.1.6 Power supply and reset information

Table 3-5. Power Supply and Reset Information

Symbol	Name	Description
PC1	Power line connector	Power line connector
S1	Reset SW	μPD720133's hardware reset switch During pressing this switch, a reset signal is activated.

3.1.7 Jumper information

Jumper information is as follows.

Table 3-6. Jumper Information

Symbol	Jumper	Setting		Description
		1 - 2	2 - 3	
JP1		Short	-	Power supply to serial ROM
JP2	SCL	Open (Short)	Short (Open)	SCL pin (μPD720133) setting (If the size of Serial ROM ≤ 2 Kbytes, settings in parentheses are available.) JP2 (Pin 1): 3.3 V JP2 (Pin 3): GND
JP3	CMB_BSY	Short	-	CMB_BSY pin (μPD720133) setting If not using the CMB_BSY pin, the JP3 is needed to be short.
JP4	CMB_STATE	Short	-	CMB_STATE pin (μPD720133) setting If not using the CMB_STATE pin, the JP4 is needed to be short.
JP5	DPC	Open	Short	DPC pin (μPD720133) setting JP5 (Pin 1): connected to the power switch (U3) JP5 (Pin 3): GND
JP6		Short	-	Current measurement point for V_{DD33}
JP7		Short	-	Current measurement point for V_{DD25}
JP8		Short	-	Current measurement point for AV_{DD}
JP9	VBUS	Open	-	Power supply from the VBUS line Short: Enable Open: Disable

3.1.8 Connector information

Connector information is as follows.

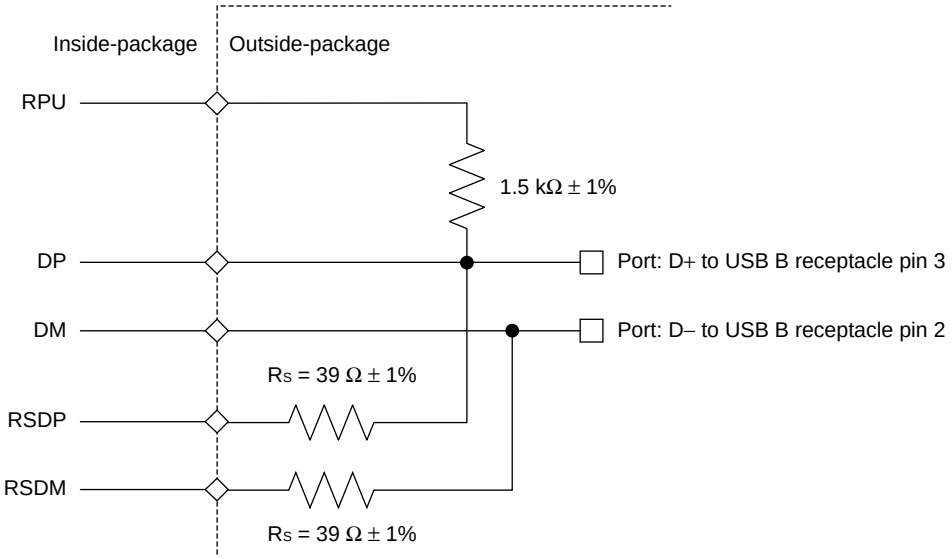
Table 3-7. Connector Information

Symbol	Connector	Setting		Description
CN1	USB connector	ALL	-	USB Connector
CN2	IDE connector	ALL	-	IDE connector Pin 20 : Open Pin 28 (CSEL) : Open Pin 34 (PDIAG) : Connected to JP1 Pin 39 (DASPB) : Connected to LED1 Disk Access Lamp Pin 32 (IOCS16B) : 5 V pull up through 1 kΩ Any other pins : Refer IDE specification.
CN3	Power line selection connector	1 - 2	Open	Power line from the power switch (U3) (In bus-powered system, these pins are needed to be short if controlling the power supply to an IDE device with the DPC pin.)
		3 - 4	Short	Power line from the PC1 connector (In bus-powered system, these pins are needed to be open if controlling the power supply to an IDE device with the DPC pin.)

CHAPTER 4 REFERENCE FOR CONNECTION

4.1 USB Circuit

Figure 4-1. USB Data Signaling



$R_S + R_{on}$ (Resistance for driver which is active) = 45 Ω ± 10%

Figure 4-2. USB Reference Resistor

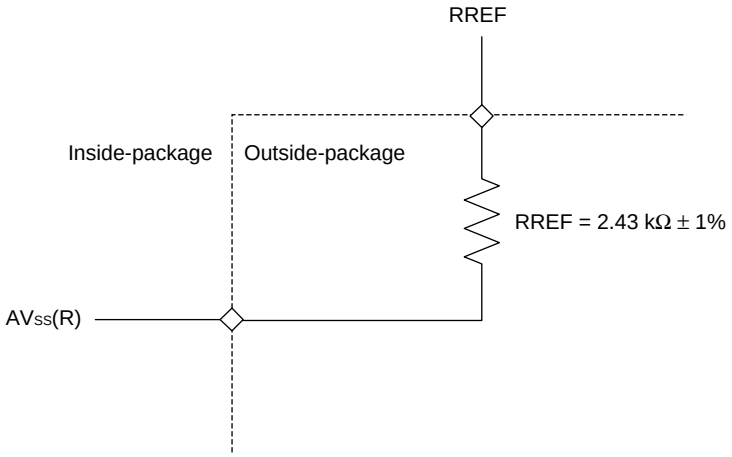
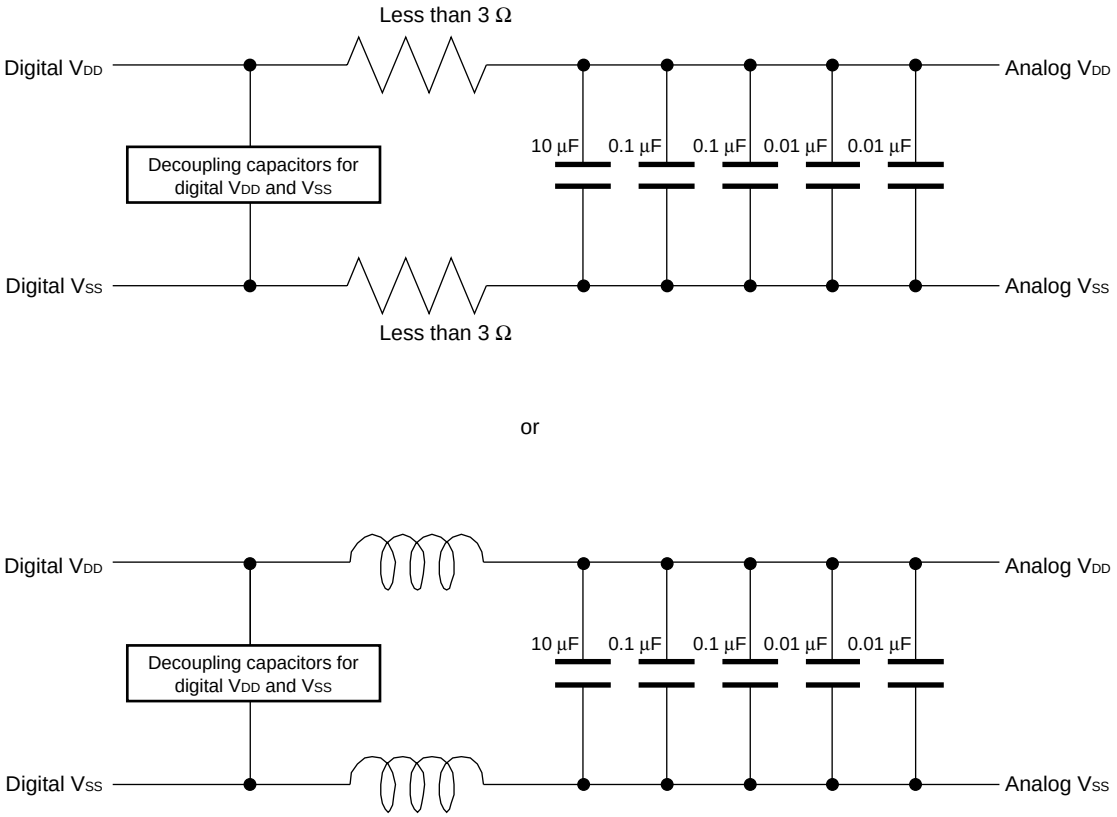
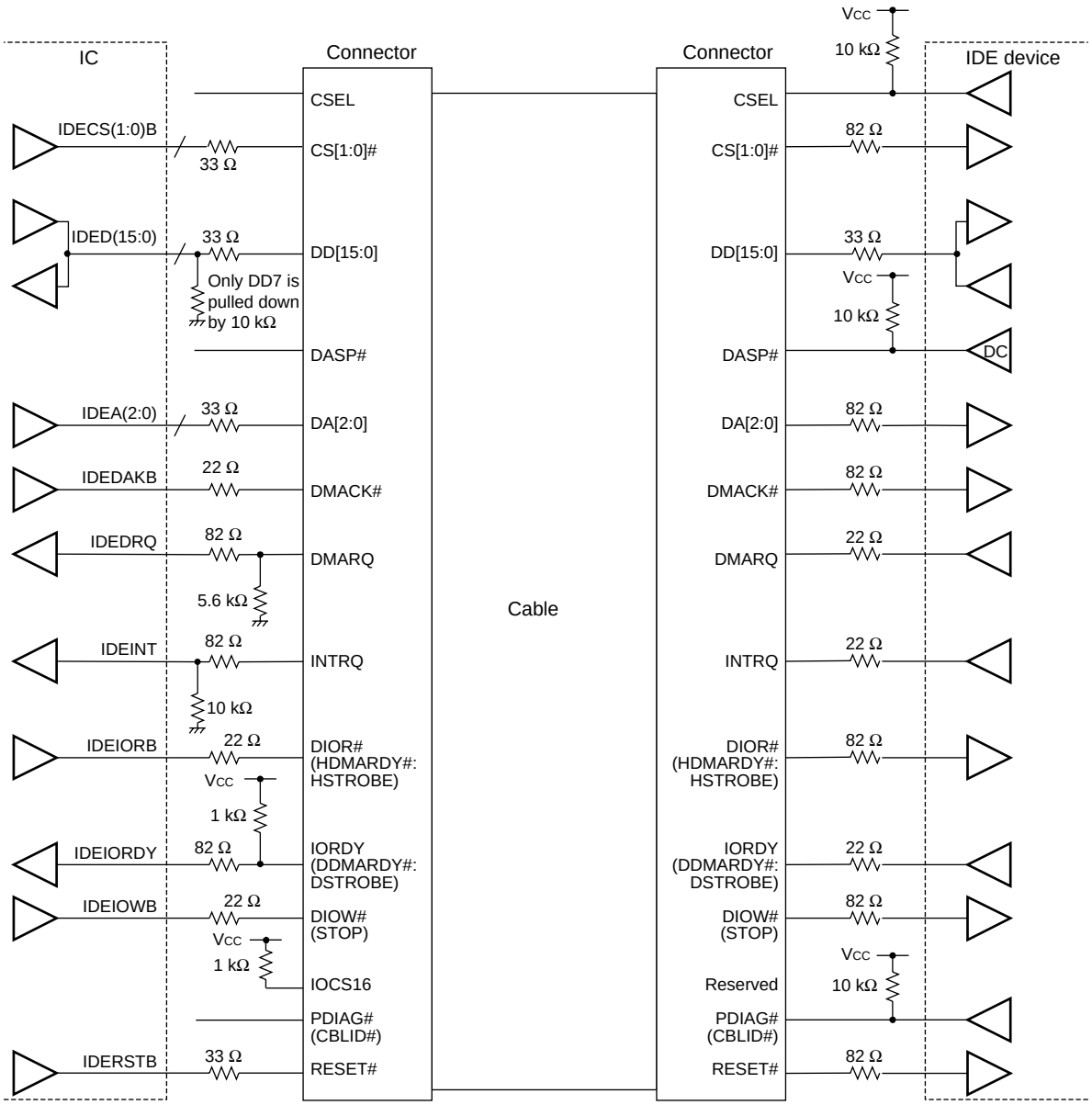


Figure 4-3. Decoupling Capacitor



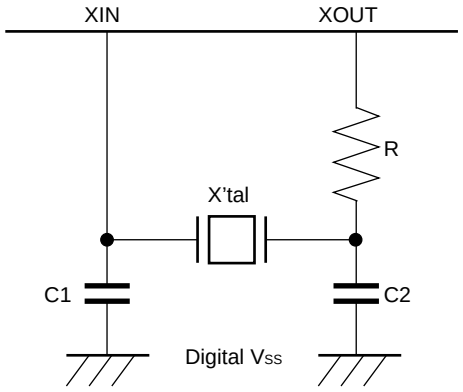
4.2 IDE Circuit

Figure 4-4. IDE Connection



4.3 Oscillator

Figure 4-5. Oscillator Circuit



The AT-49 30-MHz X'tal is used on the current ET-0170 board. The following table shows the external parameters for the AT-49 30. NEC Electronics is scheduled to evaluate the oscillator circuit.

Vendor	Name	R	C1	C2
KDS	AT-49 (30.000 MHz)	47 Ω	12 pF	12 pF

If AT-49 30 MHz is used on the board, contact to Daishinku Corp. (KDS) for getting the best external parameters depending on the board configuration.

KDS's home page : http://www.kdsj.co.jp
AT-49 catalogue No. : 1AI300002CA

Also, NEC Electronics is scheduled to evaluate NDK's X'tal. The following table shows the external parameters for the AT-41.

Vendor	Name	R	C1	C2
NDK	AT-41 (30.000 MHz)	47 Ω	10 pF	10 pF

If NDK's X'tal is used on the board, contact to NIHON DEMPA KOGYO CO.,LTD. (NDK) for getting the best external parameters depending on the board configuration.

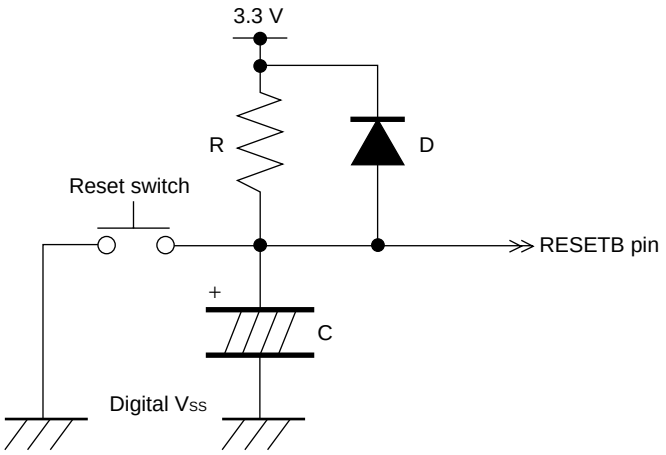
NDK's home page : http://www.ndk.com
X'tal catalogue No. : 02092X

Caution When an oscillator circuit is used, the following guidelines should be observed.

- **Keep the signal length as short as possible.**
- **Do not cross the signal with the other signal lines.**
- **Do not route the signal near a signal line with high current flows**
- **Always keep the V_{SS} point of the oscillator to the same potential as V_{SS} of the μPD720133.**
- **Do not ground the capacitor to a V_{SS} of high current flow.**

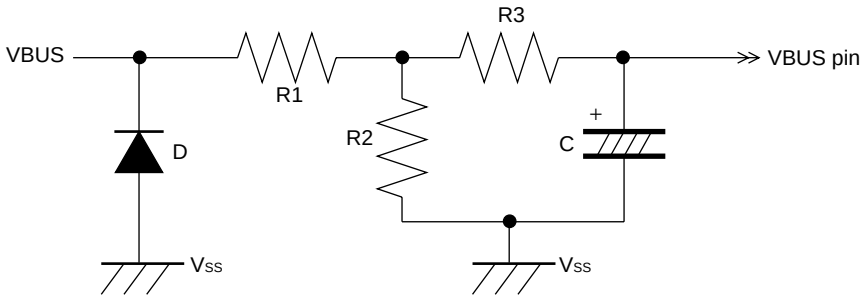
4.4 Reset Circuit

Figure 4-6. Reset Reference Circuit



4.5 VBUS Monitoring Circuit

Figure 4-7. VBUS Monitoring Circuit



Remarks 1. VBUS pin may be used to monitor for VBUS line even if V_{DD33}, V_{DD25}, and AV_{DD25} are shut off. System must ensure that the input voltage level for VBUS pin is less than 3.0 V in avoid exceeding the absolute maximum rating.

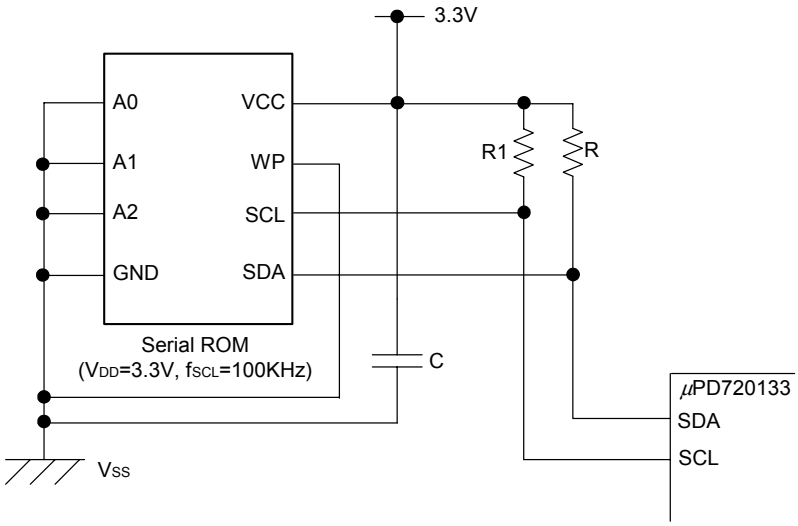
2. The unit of R1, R2, and R3 is kΩ order.

3. This circuit is not applicable in bus-powered system.

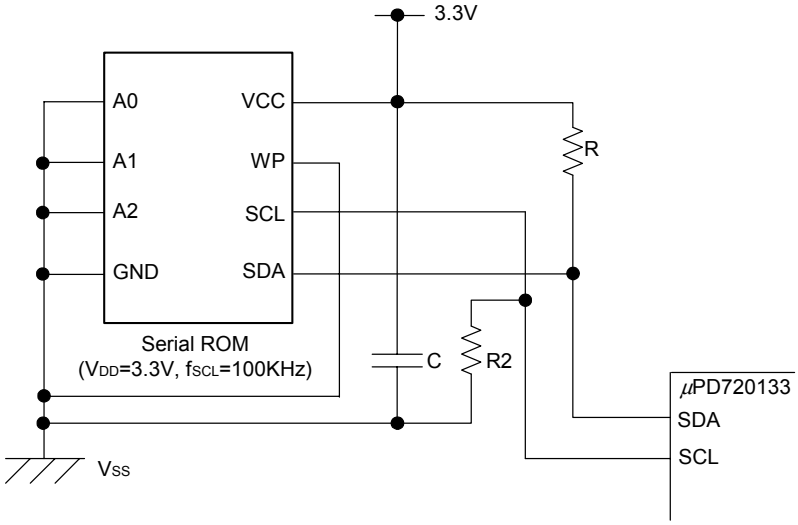
4.6 Serial ROM Connection

Figure 4-8. Serial ROM Connection

(a) Serial ROM Size ≤ 2 Kbytes

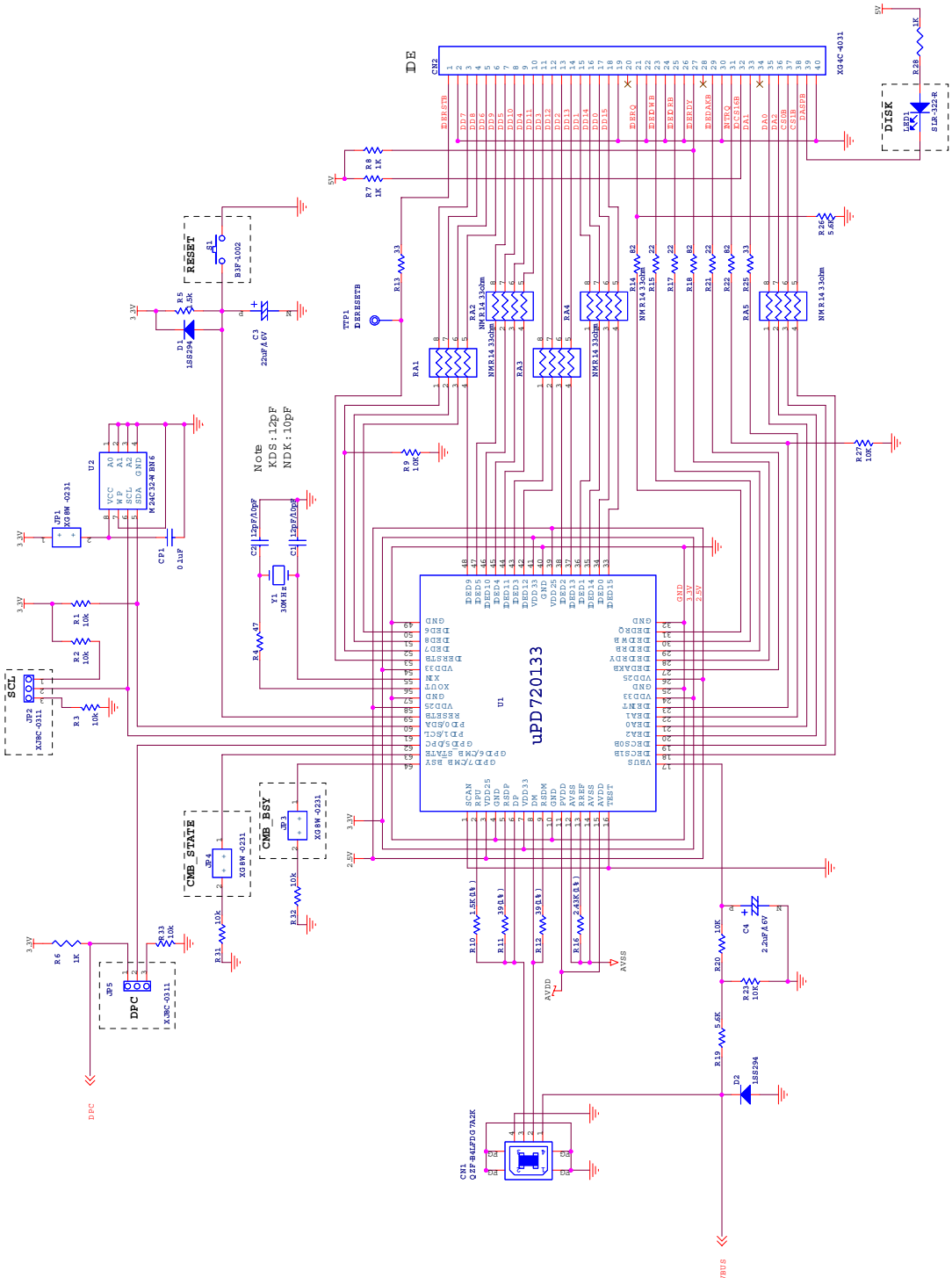


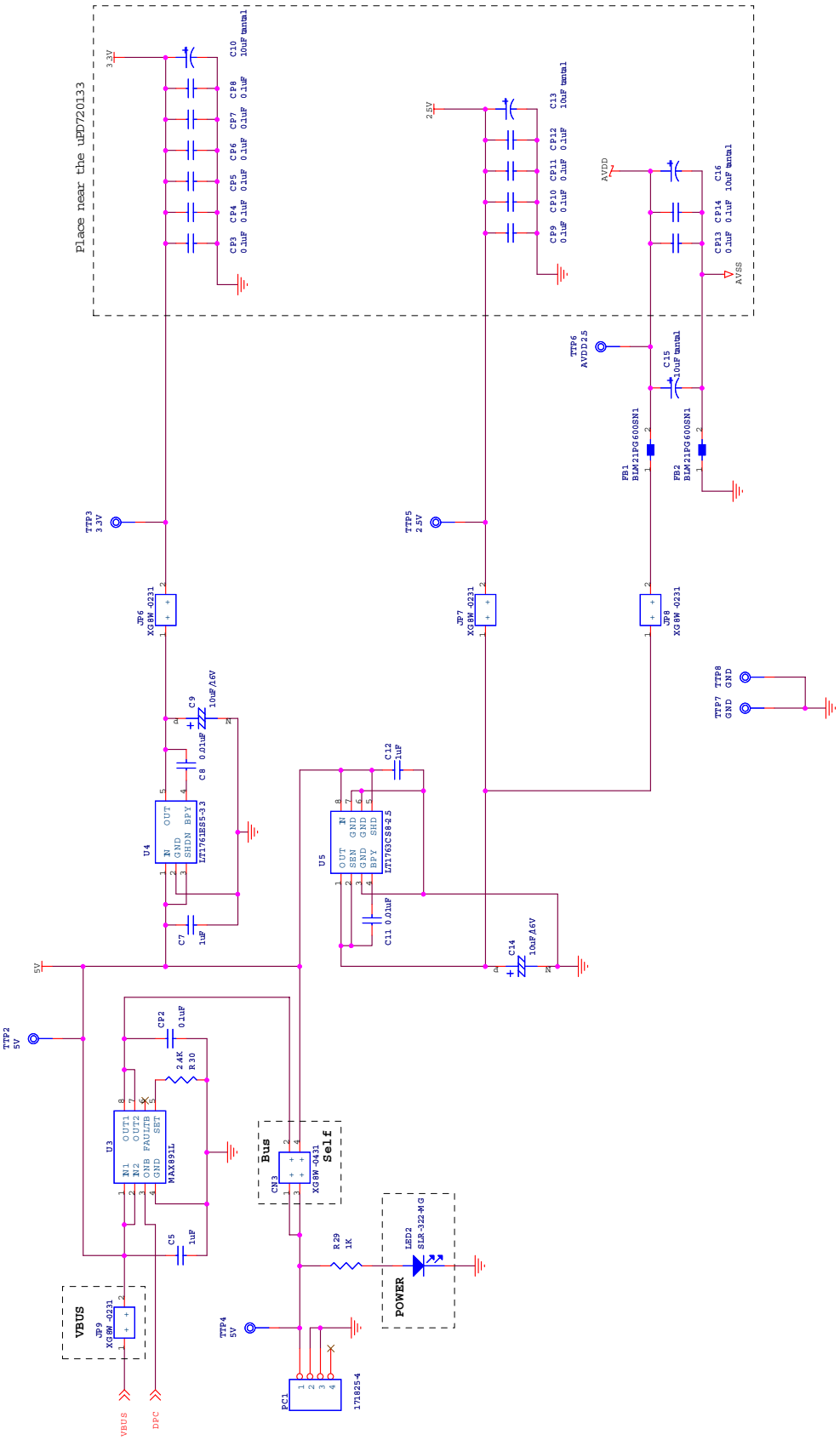
(b) Serial ROM Size > 2 Kbytes



5.1 Schematic for ET-0170 (FB-2471A)

Different components may be used depending on the availability of the component at the time of production of the ET-0170.




Place near the uPD720133
3.3V
2.5V
AVDD
AVSS
C10 10uF tantal
CP8 0.1uF
CP7 0.1uF
CP6 0.1uF
CP5 0.1uF
CP4 0.1uF
CP3 0.1uF
C13 10uF tantal
CP12 0.1uF
CP11 0.1uF
CP10 0.1uF
CP9 0.1uF
C16 10uF tantal
CP14 0.1uF
CP13 0.1uF
TTP6 AVDD2.5
C15 10uF tantal
FB1 BLM21PG600SN1
FB2 BLM21PG600SN1
TTP3 3.3V
TTP5 2.5V
JP6 XG8W-0231
JP7 XG8W-0231
JP8 XG8W-0231
TTP7 GND
TTP8 GND
C9 10uF/6V
C8 0.01uF
U4 LT1761ES5-3.3
C7 1uF
C12 1uF
U5 LT1763CS8-2.5
C11 0.01uF
C14 10uF/6V
5V
TTP2 5V
CP2 0.1uF
2.4K R30
U3 MAX891L
C5 1uF
Bus
Self
CN3 XG8W-0431
R29 1K
LED2 SLR-322-MG
POWER
VBUS
JP9 XG8W-0231
TTP4 5V
PC1 1718254
VBUS
DPC

5.2 Parts List for ET-0170 (FB-2471A)

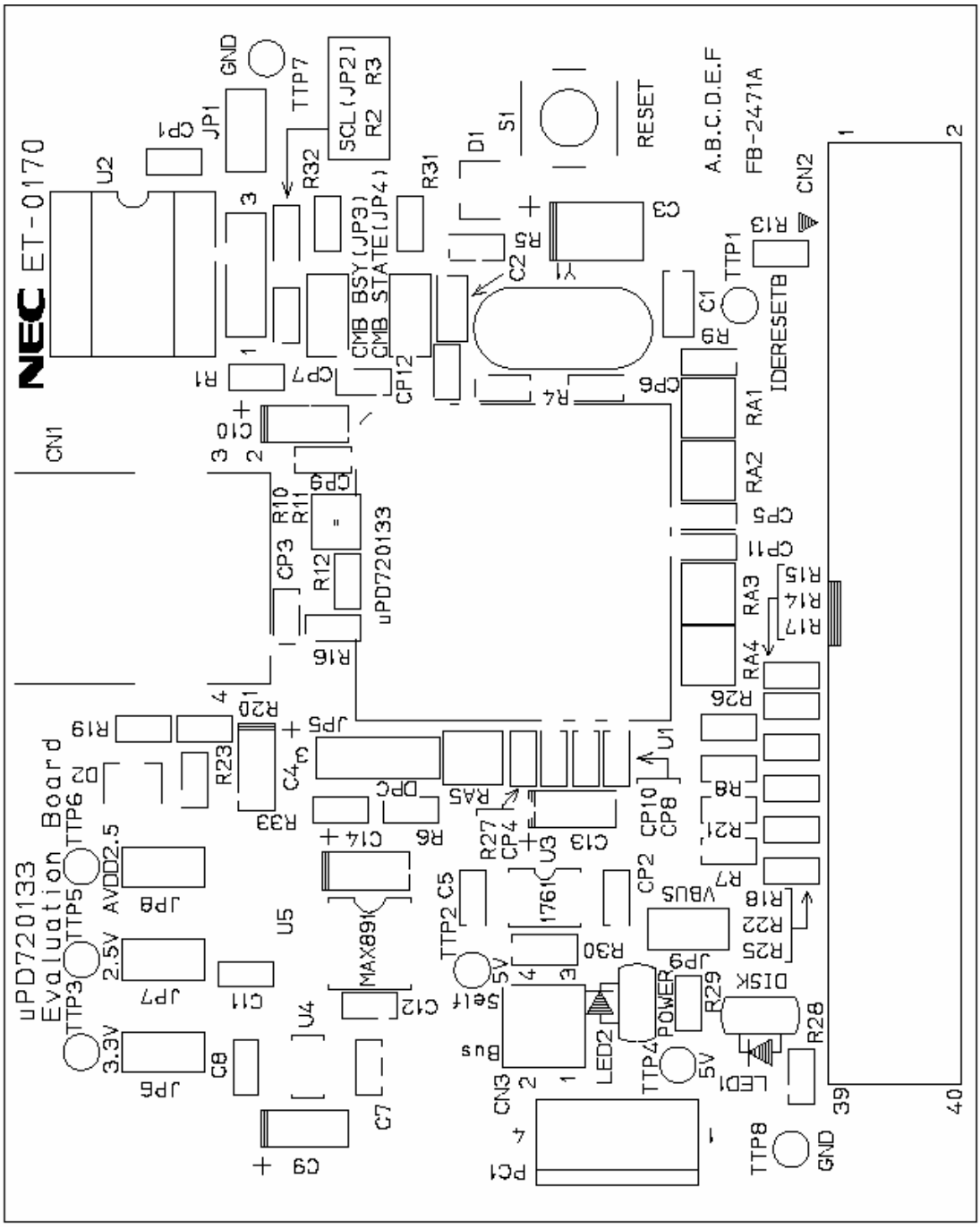
(1/2)

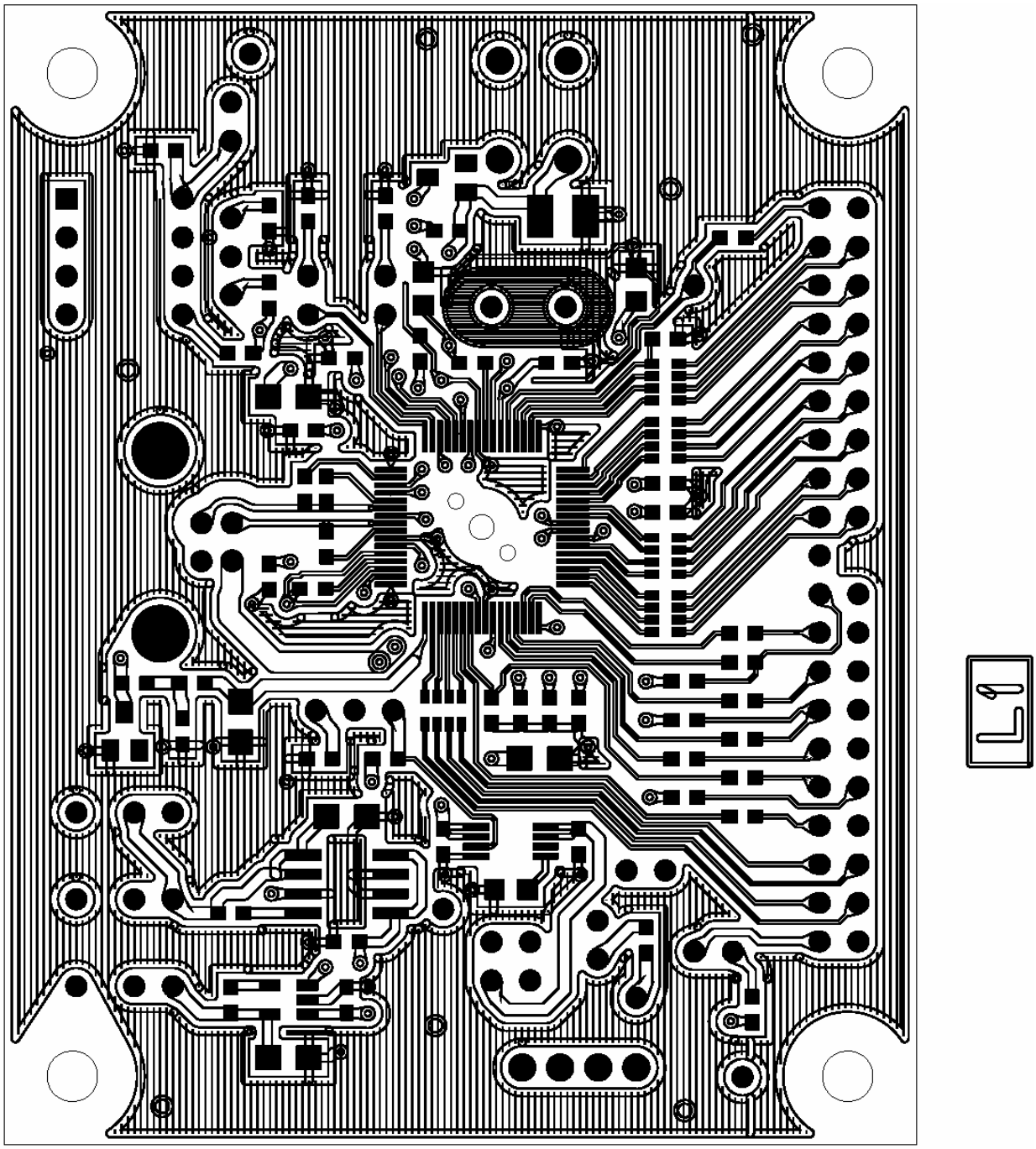
No.	Name	Type	Products	Product No.	Vendor	Count	Comment
1	U1	LSI	USB2.0 – IDE Bridge	μPD720133	NEC Electronics	1	
2	U2	Socket	8-pin DIP	-	-	1	A socket for serial ROM
3	U3	IC	3.3 V regulator	LT1761ES5-3.3	Linear	1	
4	U4	IC	2.5 V regulator	LT1763CS8-2.5	Linear	1	
5	U5	IC	Power switch	MAX891L	MAXIM	1	
6	RA1, RA2, RA3, RA4, RA5	R	Chip resistor networks (0603) 33 Ω	MNR14E0ABJ33	ROHM	5	
7	R1, R2, R3, R9, R20, R23, R27, R31, R32, R33	R	Chip resistor (0603) 10 kΩ	MCR03EZHJ	ROHM	10	
8	R6, R7, R8, R28, R29	R	Chip resistor (1608) 1 kΩ	MCR03EZHJ	ROHM	5	
9	R13	R	Chip resistor (2125) 33 Ω	MCR03EZHJ	ROHM	1	
10	R25	R	Chip resistor (1608) 33 Ω	MCR03EZHJ	ROHM	1	
11	R14, R18, R22	R	Chip resistor (1608) 82 Ω	MCR03EZHJ	ROHM	3	
12	R15, R17, R21	R	Chip resistor (1608) 22 Ω	MCR03EZHJ	ROHM	3	
13	R10	R	Chip resistor (1608) 1.5 kΩ (1%)	MCR03EZHF	ROHM	1	
14	R11, R12	R	Chip resistor (2125) 39 Ω (1%)	MCR03EZHF	ROHM	2	
15	R16	R	Chip resistor (2125) 2.43 kΩ (1%)	MCR03EZHF	ROHM	1	
16	R4	R	Chip resistor (1608) 47 Ω	MCR03EZHJ	ROHM	1	
17	R19, R26	R	Chip resistor (1608) 5.6 kΩ	MCR03EZHJ	ROHM	2	
18	R5	R	Chip resistor (1608) 1.5 kΩ	MCR03EZHJ	ROHM	1	
19	R30	R	Chip resistor (1608) 2.4 kΩ	MCR10EZHJ	ROHM	1	
20	CP1, CP2, CP3, CP4, CP5, CP6, CP7, CP8, CP9, CP10, CP11, CP12, CP13, CP14	C	Chip capacitor (2125) 0.1 μF	GRM188F11E104 ZA01	Murata	14	
21	C1, C2	C	Chip capacitor (2125) 12 or 10 pF Note	GRM40CH120J50	Murata	2	
22	C9, C14	C	Tantalum Electrolytic cap. 10 μF 16 V	16MCE106MATER	NIPPON CHEMI-CON	2	

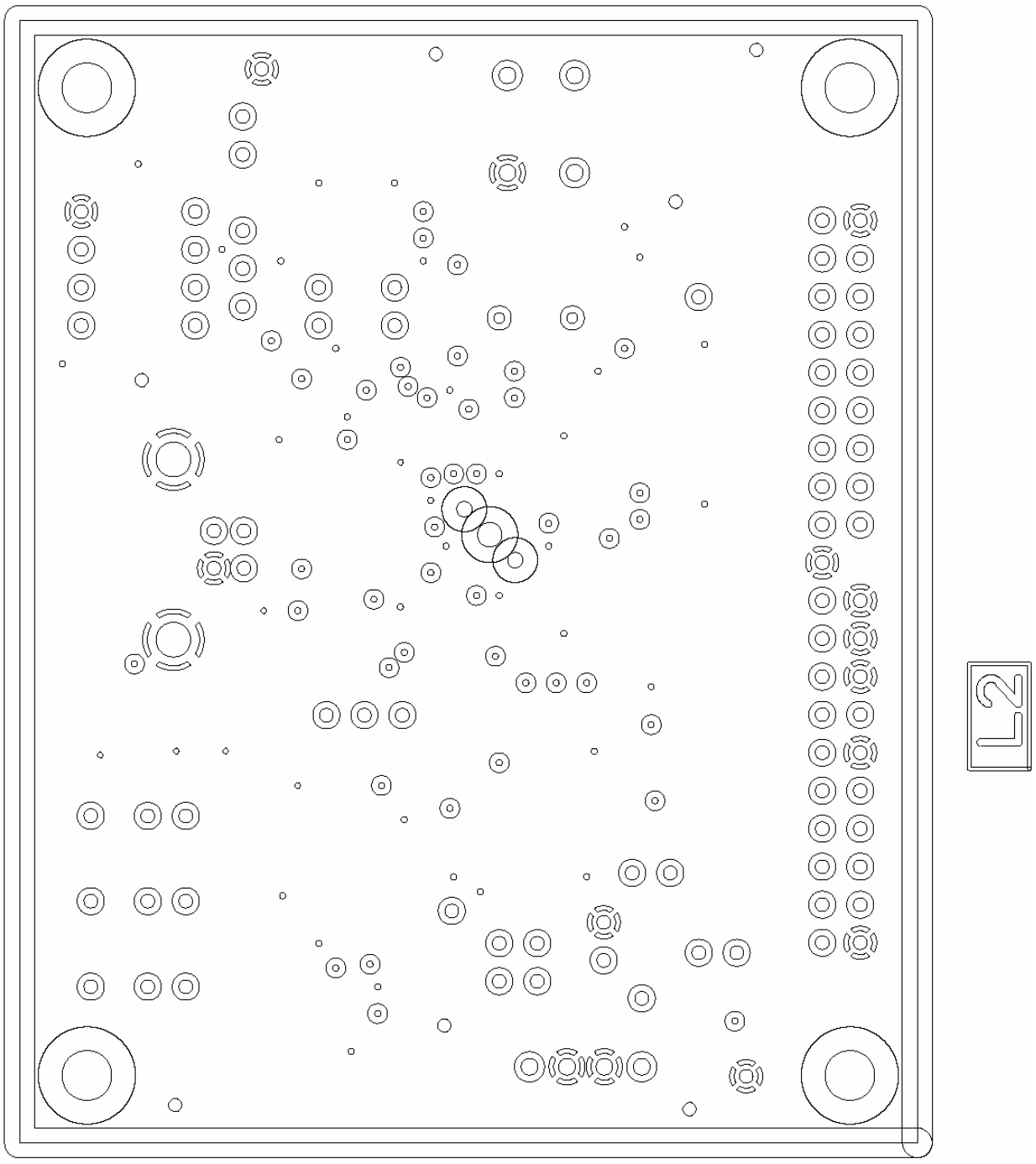
(2/2)

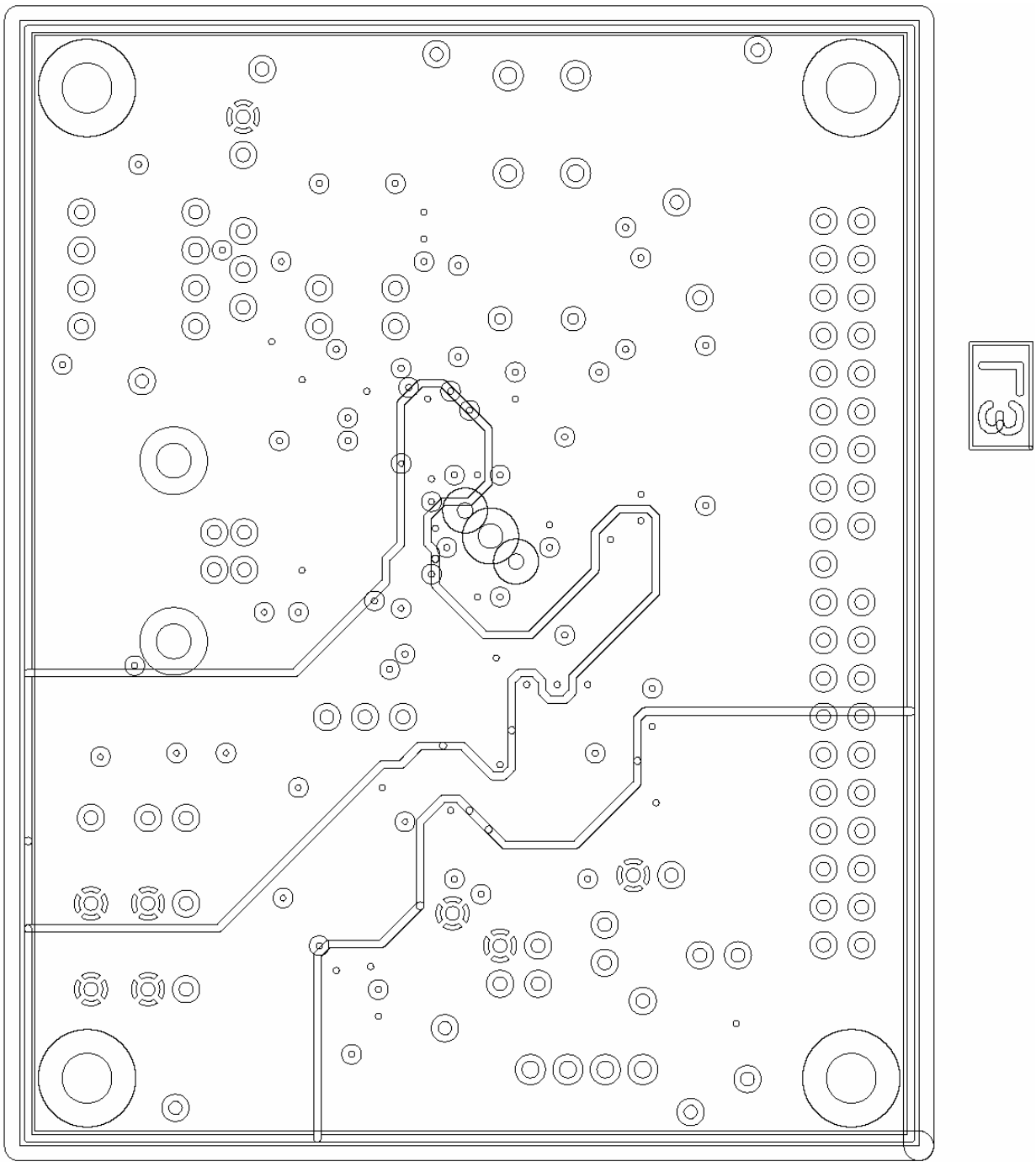
No.	Name	Type	Products	Product No.	Vendor	Count	Comment
23	C4	C	Tantalum Electrolytic cap. 2.2 μF 16 V	16MCE225MA2TER	NIPPON CHEMI-CON	1	
24	C3	C	Tantalum Electrolytic cap. 22 μF 16 V	16MCE226MB2TER	NIPPON CHEMI-CON	1	
25	C10, C13, C16	C	Tantalum capacitor 10 μF	10MCM106MA	NIPPON CHEMI-CON	3	
26	C5, C7, C12	C	Chip capacitor (1608) 1 μF	GRM188F11C105ZA01	Murata	3	
27	C8, C11	C	Chip capacitor (1608) 0.01 μF	GRM1882C1H100JA01	Murata	2	
28	D1, D2	Di	Chip diode	1SS294	Toshiba	2	
29	CN1	CN	Connector	QZF-B4LFDG7A2K	Honda	1	USB B-type connector
30	CN2	CN	Connector	XG4C-4031	OMRON	1	
31	CN3	CN	Connector	XG8W-0431	OMRON	1	
32	JP2, JP5	JP	Jumper	XJ8C-0311	OMRON	2	
33	JP1, JP3, JP4, JP6, JP7, JP8, JP9	JP	Jumper	XG8W-0231	OMRON	7	
34	LED1	LED	LED (Red)	SLR-322-VR3F	ROHM	1	
35	LED2	LED	LED (Green)	SLR-322-MG3F	ROHM	1	
36	Y1	X'tal	X'tal 30 MHz	AT-49 or AT-41 (30 MHz)	KDS or NDK	1	
37	PC1	CN	Power Connector	171825-4	AMP	1	
38	S1	SW	Switch	B3F-1002	OMRON	1	
39	FB1, FB2	FB	Ferrite beads	BLM21PG600SN1	Murata	2	
40	TTP(9:1)	TP	Test pin	-	-		Not used
41	-	-	Serial ROM	M24C32	STMicro electronics	1	
42	-	-	IDE cable	-	-	1	
43	-	-	Board	FB-2471A	-	-	

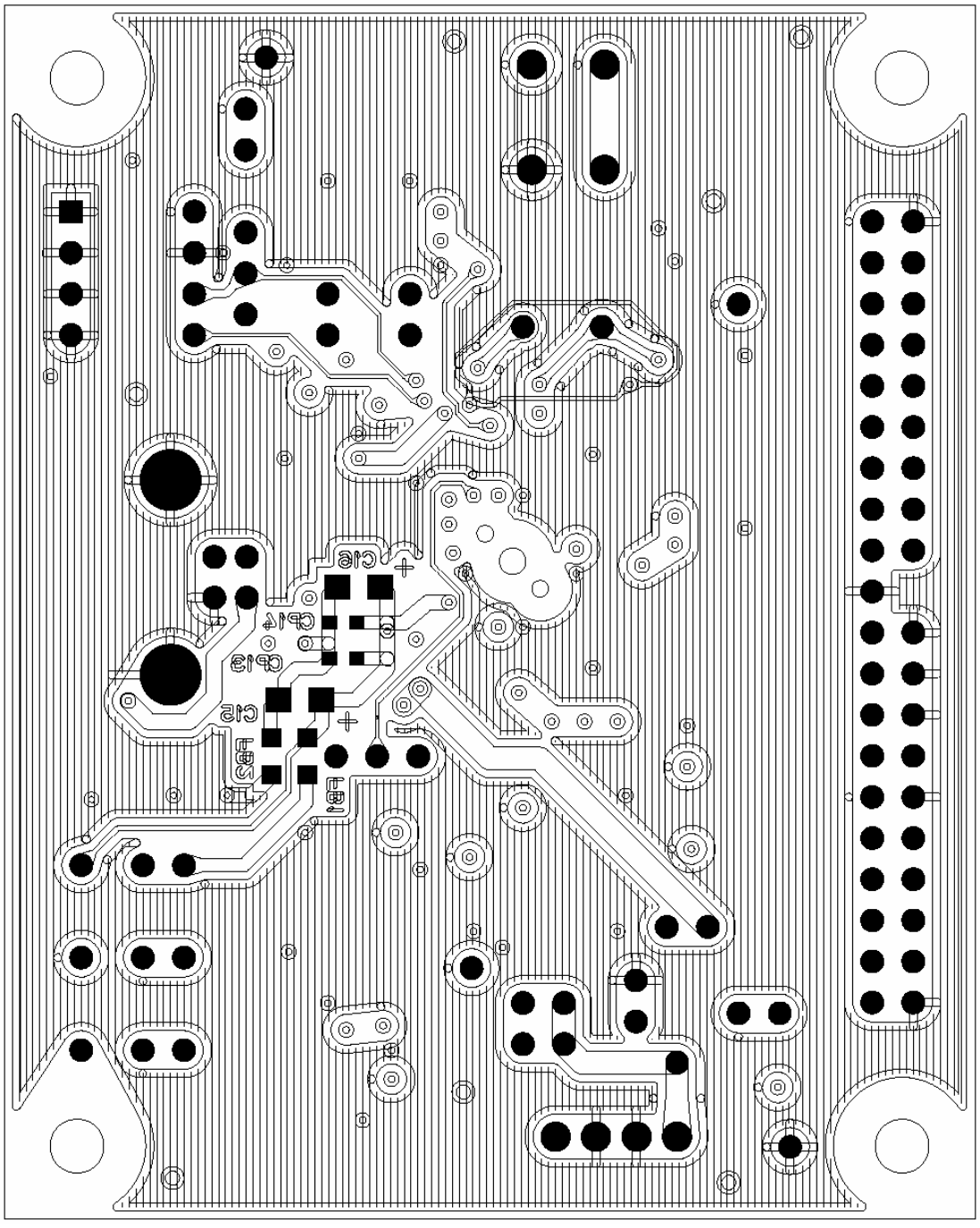
5.3 Board Pattern for ET-0170 (FB-2471A)




L1


L2




C16
CP14
CP13
C15
CP12
CP11

[MEMO]