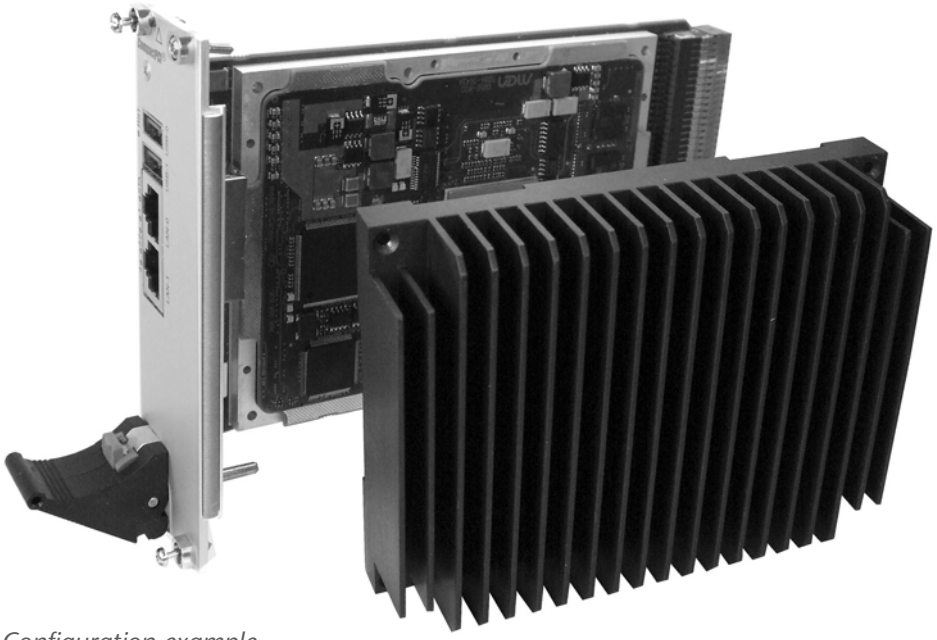
Embedded Solutions

# F50P – 3U CompactPCI® PlusIO MPC8548 SBC



*Configuration example*
*(8 HP, with heat sink unmounted)*

## *User Manual*

mikro elektronik
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# F50P – 3U CompactPCI® PlusIO MPC8548 SBC

The F50P is a versatile, rugged PowerPC® based single-board computer for embedded applications. It is controlled by an MPC8548, or optionally an MPC8543 PowerPC® processor (alternatively with encryption unit) with clock frequencies between 800 MHz and 1.5 GHz. The SBC is equipped with ECC-controlled, soldered-on DDR2 RAM for data storage, with up to 16 GB of solid-state Flash disk for program storage as well as industrial FRAM and SRAM.

The board provides up to three Gigabit Ethernet channels, six USB ports, up to two SATA interfaces and up to 64 user-definable I/O lines controlled by an optional onboard FPGA. These interfaces can be combined in many variations and are available at the front or at the rear using the board's J2 connector. The J2 pin assignment and connector type are in compliance with the PICMG 2.30 CompactPCI PlusIO standard – the migration path towards CompactPCI Plus. Two USB and two RJ45 Ethernet connectors are already provided at the front panel, and space is left for an optional VGA connector.

The large FPGA on the F50P allows to add additional user-defined functions such as graphics, touch, serial interfaces, fieldbus controllers, binary I/O etc. for the needs of the individual application in an extremely flexible way. Before boot-up of the system, the FPGA is loaded from boot Flash. Updates of the FPGA contents can be made inside the boot Flash during operation. If the FPGA is assembled, the card needs an extra 4 HP in front panel space.

Equipped with a PCI-bridge chip, the F50P offers a full CompactPCI® interface (system slot functionality) for reliable system expansion. Apart from that, the F50P can also be used as a busless, stand-alone board, with power supply from the backplane.

Being designed for operation in a conduction or convection cooled environment, the F50P provides flexibility also in its cooling concept. Its firmly plugged-on CPU module is embedded in a covered frame. This ensures EMC protection and allows efficient conductive cooling for the F50C model, which is also available by standard. For air cooling, the F50P version comes with a tailor-made heat sink on top of the cover, requiring an 8-HP front panel, for an extended temperature range of -40 to +70°C. The soldered components on the F50P withstand shock and vibration, and the board design is optimized for conformal coating.

The F50P comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.

# Technical Data

### CPU

- PowerPC® PowerQUICC™ III MPC8548, MPC8548E, MPC8543 or MPC8543E
  - 800MHz up to 1.5GHz
  - Please see Configuration Options for available standard versions.
  - e500 PowerPC® core with MMU and double-precision embedded scalar and vector floating-point APU
  - Integrated Northbridge and Southbridge

### Memory

- 2x32KB L1 data and instruction cache, 512KB/256KB L2 cache integrated in MPC8548/MPC8543
- Up to 2GB SDRAM system memory
  - Soldered
  - DDR2 with or without ECC
  - Up to 300 MHz memory bus frequency, depending on CPU
- Up to 16GB soldered Flash disk (SSD solid state disk)
- Up to 32MB additional DDR2 SDRAM, FPGA-controlled, e.g. for video data
- 16MB boot Flash
- 2MB non-volatile SRAM
  - With GoldCap backup
- 128KB non-volatile FRAM
- Serial EEPROM 4kbits for factory settings

### Mass Storage

- Parallel IDE (PATA)
  - Up to 16GB soldered ATA Flash disk (SSD solid state disk)
- Serial ATA (SATA)
  - Up to two ports via rear I/O J2
  - Transfer rates up to 150MB/s (1.5 Gbits/s)
  - Via PCI-to-SATA bridge
  - See Interface Configuration Matrix showing possible I/O combinations

### Graphics

- FPGA-controlled (optional)
- VGA connector prepared at front panel

### I/O

- USB (host)
  - Five USB 2.0 host ports
  - One series A connector at front panel
  - Four ports via rear I/O J2
  - OHCI and EHCI implementation
  - Data rates up to 480Mbits/s

- USB (client)
  - One USB client port on series A connector at front panel
  - Via UART-to-USB converter
  - Data rates up to 115.2kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: none
- Ethernet
  - Up to three 10/100/1000Base-T Ethernet channels with MPC8548/E (two channels with MPC8543/E)
  - Two RJ45 connectors at front panel
  - Two front-panel LEDs for channels  for LAN link, activity status and connection speed
  - All three possible also via rear I/O J2 (Note: requires additional Ethernet transformers on rear I/O board or backplane.)
  - See Interface Configuration Matrix showing possible I/O combinations
- User-defined I/O
  - FPGA-controlled (optional)
  - Up to 64 I/O lines
  - Connection via rear I/O J2
  - See Interface Configuration Matrix showing possible I/O combinations

### *Front Connections (Standard)*

- One USB 2.0 host (Series A)
- One USB client (Series A)
- Two Ethernet (RJ45)

### *Rear I/O*

- Four USB 2.0
- Up to three 1000Base-T Ethernet
- Up to two SATA
- Up to 64 I/O lines with optional FPGA
  - Reduces Ethernet/SATA interfaces
  - See Interface Configuration Matrix showing possible I/O combinations
- Standard version compatible with PICMG 2.30 CompactPCI PlusIO
  - Four USB 2.0
  - Two SATA

### *FPGA*

- The FPGA offers the possibility to add customized I/O functionality. See Configuration Options
- Standard: FPGA not assembled

### *Miscellaneous*

- Real-time clock with GoldCap backup
- Temperature sensor, power supervision and watchdog
- Status LED at the front
- Reset button

### CompactPCI® Bus

- Compliance with CompactPCI® Core Specification PICMG 2.0 R3.0
- System slot
- 32-bit/32-MHz PCIe®-to-PCI bridge
- V(I/O): +3.3V (+5V tolerant)

### Busless Operation

- Board can be supplied with +5V, +3.3V and +12V from backplane, all other voltages are generated on the board
- Backplane J1 connector used only for power supply

### Electrical Specifications

- Supply voltage/power consumption:
  - +5V (-3%/+5%), 800mA approx.
  - +3.3V (-3%/+5%), 350mA approx.
  - ±12V (-5%/+5%), 1A approx.

### Mechanical Specifications

- Dimensions: conforming to CompactPCI® specification for 3U boards
- Front panel:
  - 8HP without FPGA
  - 12HP with FPGA
  - See also Figure 1, Map of the board – front panel view, on page 17
- Weight: 626g

### Environmental Specifications

- Temperature range (operation):
  - -40..+70°C (screened)
  - Airflow: min. 1.0m/s
  - Conduction cooled variety F50C also available
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 1g/10..150Hz
- Conformal coating on request

### MTBF

- 162,822h @ 40°C according to IEC/TR 62380 (RDF 2000)

### Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

### EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

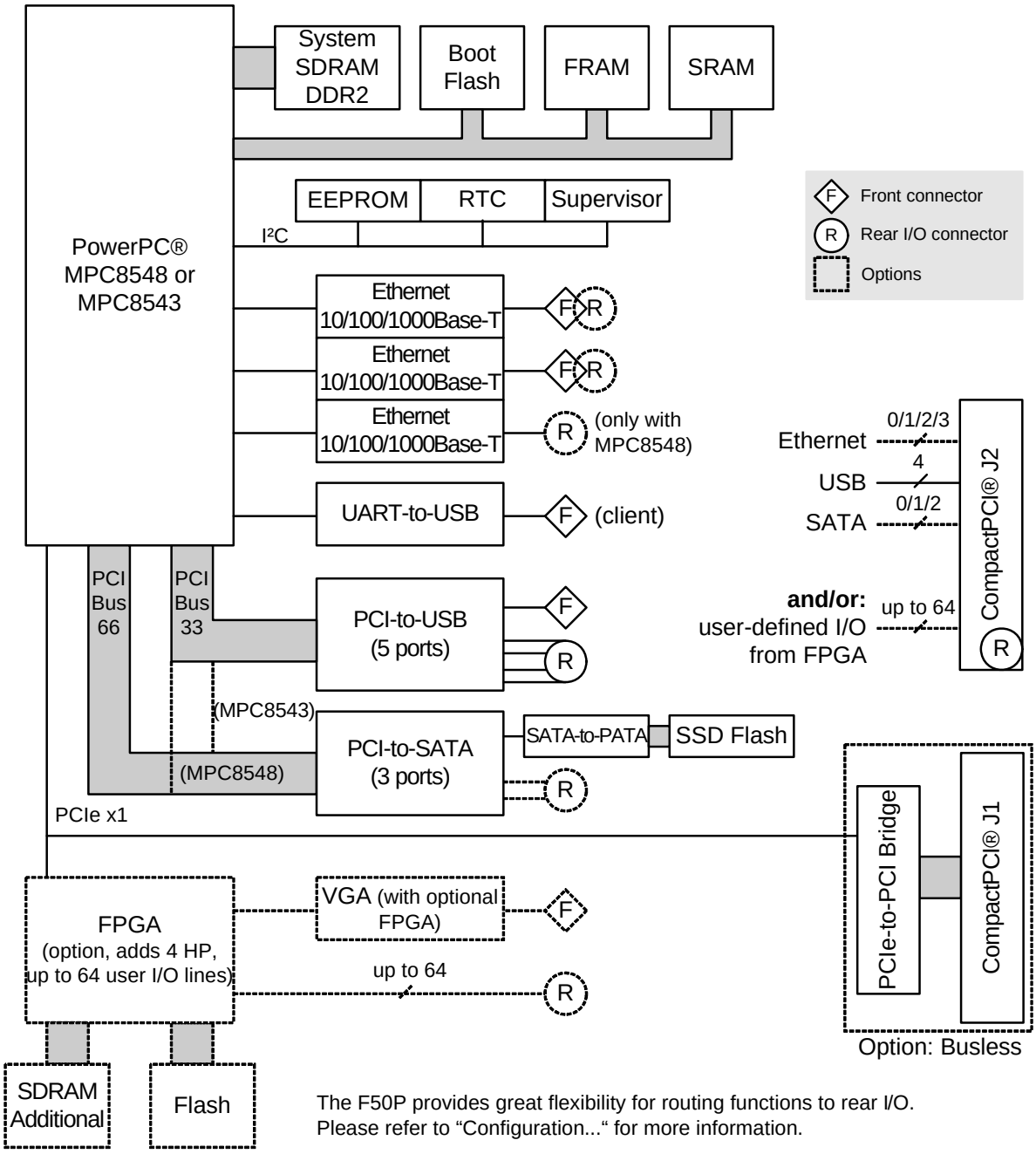
### BIOS

- MENMON™

### Software Support

- Linux
- VxWorks®
- QNX® (on request; support of the FPU is currently not provided by QNX®)
- INTEGRITY® (Green Hills® Software)
- OS-9® (on request)
- For more information on supported operating system versions and drivers see online data sheet.

# Block Diagram




The F50P provides great flexibility for routing functions to rear I/O.
Please refer to “Configuration...“ for more information.

# Configuration Options

### CPU

- Several PowerQUICC™ III types with different clock frequencies
- MPC8548 or MPC8548E
  - 1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz
- MPC8543 or MPC8543E
  - 800 MHz or 1 GHz

### Memory

- System RAM
  - 512 MB, 1 GB or 2 GB
  - With or without ECC
- Flash Disk
  - 2 GB, 4 GB, 6 GB, 8 GB, 12 GB or 16 GB
- FRAM
  - 0 KB or 128 KB
- Additional SDRAM
  - 0 MB or 32 MB
  - With optional FPGA

### I/O

- See Interface Configuration Matrix showing possible I/O combinations
- VGA at front (with optional FPGA)
- Ethernet
  - Up to two channels at front
  - Up to three channels at rear
  - Only two channels total with MPC8543
- SATA
  - Up to two channels at rear
- Up to 64 user-defined I/O lines
  - With optional FPGA, see below
  - Reduces number of Ethernet/SATA channels

### FPGA

- The optional onboard FPGA offers the possibility to implement customized I/O functionality.
- FPGA Altera® Arria® GX AGX35C
  - 33,520 logic elements
  - 1,348,416 total memory bits
  - Connected to CPU via PCI Express® x1 link
- Connection
  - Available pin count: 64 pins
  - Functions available via rear I/O J2 connector
- Please note that the FPGA expands the board's width by 4 HP, to 12 HP!
  - See also Figure 1, Map of the board – front panel view, on page 17
- You can find more information on our web page "User I/O in FPGA"

### Cooling concept

- -40..+70°C on 8 HP with heat sink (without FPGA) for convection cooling
- Conduction cooled variety F50C also available, for -40..+85°C

**Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.**

### Interface Configuration Matrix

| FPGA I/O pins | (No FPGA) | | | | 29 | 38 | 47 | 56 | 33 | 42 | 51 | 60 | 37 | 46 | 55 | 64 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Front I/O | No VGA | | | | VGA (routed to FPGA) | | | | | | | | | | | |
| | 2 USB | 2 USB | | | 2 USB | | | | | | | | | | | |
| | 2 ETH | 2 ETH | 1 ETH | - | - | 1 ETH | 2 ETH | - | - | 1 ETH | 2 ETH | - | - | 1 ETH | 2 ETH | - |
| Rear I/O | - | 1 ETH | 2 ETH | 3 ETH | 3 ETH | 2 ETH | 1 ETH | - | 3 ETH | 2 ETH | 1 ETH | - | 3 ETH | 2 ETH | 1 ETH | - |
| | 2 SATA | 2 SATA | 2 SATA | 2 SATA | 2 SATA | 2 SATA | 2 SATA | 2 SATA | 1 SATA | 1 SATA | 1 SATA | 1 SATA | - | - | - | - |
| | 4 USB | 4 USB | | | 4 USB | | | | | | | | | | | |
| Form factor | 8/12 HP | 8/12 HP | | | 12 HP | | | | | | | | | | | |

The standard configuration is compatible with the PICMG 2.30 CompactPCI PlusIO specification.

The standard configuration is highlighted in **bold blue** in the table.

**For available standard configurations see online data sheet.**

# Product Safety

## Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

# About this Document

This user manual describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

## History

| Issue | Comments | Date |
|---|---|---|
| E1 | First issue | 2009-11-20 |

## Conventions

This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

*italics* Folder, file and function names are printed in *italics*.

**bold** **Bold** type is used for emphasis.

`monospace` A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

hyperlink Hyperlinks are printed in blue color.

The globe will show you where hyperlinks lead directly to the Internet, so you can look for the latest information online.

IRQ# /IRQ Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".

Vertical lines on the outer margin signal technical changes to the previous issue of the document.

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# Contents

## Figures

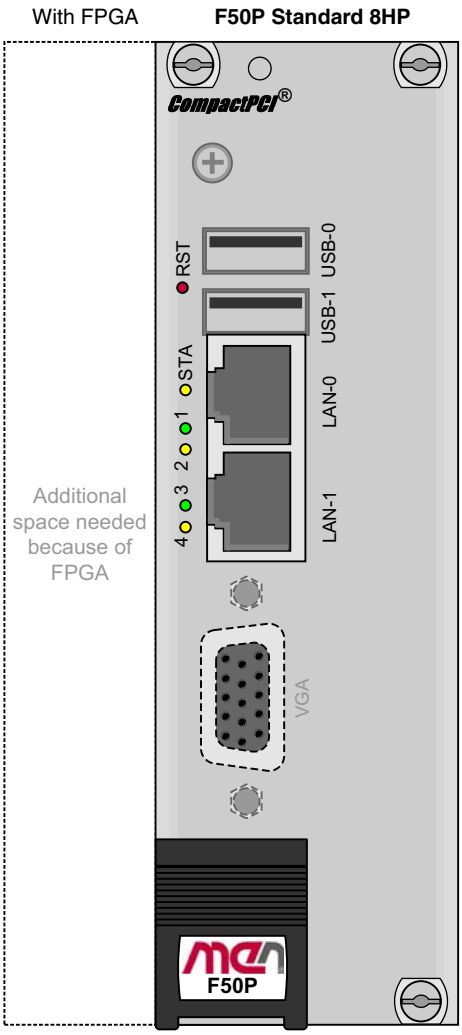
## Tables

# 1 Getting Started

This chapter gives an overview of the board and some hints for first installation in a system.

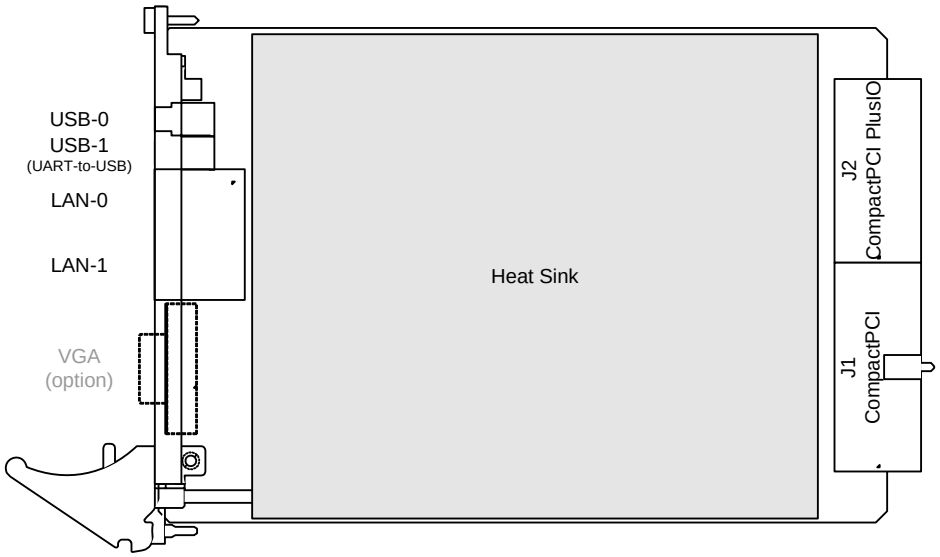
## 1.1 Maps of the Board

***Figure 1.*** *Map of the board – front panel view*




Note: VGA can be implemented as an option with an onboard FPGA.

***Figure 2.*** *Map of the board – top view*



## 1.2 Integrating the Board into a System

If you need electrical isolation between shield (rack or enclosure) and (digital) ground, you need to use guide rails without a shield strip in your CompactPCI rack for the slot where the F50P is inserted.

You can use the following check list when installing the board in a system for the first time and with minimum configuration.

- ☑ Power-down the system.
- ☑ Remove all boards from the CompactPCI system.
- ☑ Insert the F50P into the system slot of your CompactPCI system, making sure that the CompactPCI connectors are properly aligned.

  Note: The system slot of every CompactPCI system is marked by a △ triangle on the backplane and/or at the front panel. It also has red guide rails.

You should generally use a host computer for first operation, typically under Linux or Windows.

- ☑ Install a USB-to-UART driver on your host computer.
  You can use a Windows driver provided by MEN (article number 13T005-70, third-party) or go to the FTDI web site (www.ftdichip.com/FTDrivers.htm) and download a driver there.
- ☑ Connect your host computer to the front panel USB-1 port of the F50P (UART-to-USB interface). To do this, you need a suitable USB cable (type A to A).
- ☑ Power-up the system.
- ☑ Start up a terminal program on your host computer, e.g. HyperTerm under Windows, and open a terminal connection.
- ☑ Set your terminal connection to the following protocol:
  - 9600 baud data transmission rate
  - 8 data bits
  - 1 stop bit
  - No parity

☑ When the terminal connection is made, press Enter. Now you can use the MENMON BIOS/firmware (see detailed description in Chapter 3 MENMON on page 37).
If you enter command "LOGO" on the MENMON prompt, the terminal displays a message similar to the following:

```
 _________ Secondary MENMON for MEN MPC8548 Family (XM50) 1.7 ____________________
|                                                                                 |
|          (c) 2007 - 2008 MEN Mikro Elektronik GmbH Nuremberg                    |
|         MENMON 2nd Edition, Created  Jun 12 2008     10:45:08                   |
|_________________________________________________________________________________|
|    CPU Board: XM50-03                |           CPU: MPC8548                   |
|Serial Number: 4                      |   CPU/MEM Clk:   1386 / 198 MHz          |
|  HW Revision: 00.00.00               |   CCB/LBC Clk:    396 /  50 MHz          |
|                                      |                                          |
|    PCI1/PCI2: 32Bit 66MHz/32Bit 33MHz|          PCIe:   x4                      |
|   DDR2 SDRAM: 512 MB ECC on 3.0/3/8  |     FRAM/SRAM:    128 /2048 kB           |
|     Produced:                        |         FLASH:   16 MB                   |
|  Last repair:                        |   Reset Cause: Power On                  |
|_________________________________________________________________________________|
|  Carrier Board: F503-00, Rev 00.01.00, Serial 3                                 |
 \_______________________________________________________________________________/
```

Note: Don’t power off the F50P now, otherwise the USB-to-UART interface on the host computer will be disconnected.

☑ Observe the installation instructions for the respective software.

## 1.3 Installing Operating System Software

The board supports Linux, VxWorks, and INTEGRITY.

By default, no operating system is installed on the board. Please refer to the respective manufacturer's documentation on how to install operating system software!

You can find any software available on MEN’s website.

## 1.4 Installing Driver Software

For a detailed description on how to install driver software please refer to the respective documentation.

You can find any driver software available for download on MEN’s website.

# 2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPU. They can be obtained from the data sheets or data books of the semiconductor manufacturer concerned (Chapter 5.1 Literature and Web Resources on page 61).

## 2.1 Power Supply

The board is supplied via CompactPCI connector J1 with +5 V, +3.3 V and ±12 V. All other required voltages are generated on the board.

The F50P may also be operated as a stand-alone card, without the CompactPCI bus. In this case, power is also supplied via the J1 connector. Three voltages are needed: +5 V, +3.3 V and +12 V.

## 2.2 Board Supervision

The board features a temperature sensor and voltage monitor.

A voltage monitor supervises all used voltages and holds the CPU in reset condition until all supply voltages are within their nominal values.

In addition the board contains a PLD watchdog that must be triggered. After configuration the CPU serves the PLD watchdog. The watchdog timeout is automatically set to 1.12 s after the first trigger pulse by the CPU.

The watchdog can be enabled or disabled through MENMON and can be triggered by a software application. This function is normally supported by the board support package (see BSP documentation).

## 2.3 Real-Time Clock

The board includes an RA8581 real-time clock. Interrupt generation of the RTC is not supported. For data retention during power off the RTC is supplied by a GoldCap.

A control flag indicates a back-up power fail condition. In this case the contents of the RTC cannot be expected to be valid. A message will be displayed on the MENMON console in this case.

## 2.4 Processor Core

The board is equipped with the MPC8548 or MPC8543 processor, which includes a 32-bit PowerPC e500 core, the integrated host-to-PCI bridge, Ethernet controllers and UARTs.

### 2.4.1 General

The MPC8548/3 family of processors integrates an e500v2 processor core built on Power Architecture technology with system logic required for networking, telecommunications, and wireless infrastructure applications. The MPC8548/3 is a member of the PowerQUICC III family of devices that combine system-level support for industry-standard interfaces with processors that implement the embedded category of the Power Architecture technology.

The MPC8548/3 offers a double-precision floating-point auxiliary processing unit (APU), up to 512 KB of level-2 cache, up to four integrated 10/100/1Gbits/s enhanced three-speed Ethernet controllers with TCP/IP acceleration and classification capabilities, a DDR/DDR2 SDRAM memory controller, a programmable interrupt controller, two I²C controllers, a four-channel DMA controller, a general-purpose I/O port, and dual universal asynchronous receiver/transmitters (DUART).

The MPC8548/3 is available with (MPC8548/3E) or without an integrated security engine with XOR acceleration.

***Table 1.*** *Processor core options on F50P*

| Processor Type | Core Frequency | L2 Cache | Encryption Unit | Ethernet Ports |
|---|---|---|---|---|
| MPC8548 | 1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz | 512 KB | No | 3 |
| MPC8548E | 1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz | 512 KB | Yes | 3 |
| MPC8543 | 800 MHz or 1 GHz | 256 KB | No | 2 |
| MPC8543E | 800 MHz or 1 GHz | 256 KB | Yes | 2 |

### 2.4.2 Thermal Considerations

The F50P generates around 17 W of power dissipation when operated at 1.33 GHz.

A suitable heat sink is provided to meet thermal requirements.

Please note that if you use any other heat sink than that supplied by MEN, or no heat sink at all, warranty on functionality and reliability of the F50P may cease. If you have any questions or problems regarding thermal behavior, please contact MEN.

## 2.5 Bus Structure

### 2.5.1 Host-to-PCI Bridge

The integrated host-to-PCI bridge is used as host bridge and memory controller for the PowerPC processor. All transactions of the PowerPC to the PCI bus are controlled by the host bridge. The FRAM, SRAM and boot Flash are connected to the local memory bus of the integrated host-to-PCI bridge.

The PCI interface is PCI bus Rev. 2.2 compliant and supports all bus commands and transactions. Master and target operations are possible. Only big-endian operation is supported.

### 2.5.2 Local PCI Buses

Two local PCI buses are controlled by the integrated host-to-PCI bridge. One is connected to the PCI-to-USB bridge and runs at 33 MHz. The other connects the PCI-to-SATA bridge and operates at 66 MHz. Board versions with the MPC8543 processor only have one local PCI bus operating at 33 MHz.

The I/O voltage is fixed to 3.3V. The data width is 32 bits.

### 2.5.3 Local PCI Express Connections

A PCI Express x1 link connects the PowerPC processor with the CompactPCI bus (via a PCIe-to-PCI bridge) and with the optional FPGA.

## 2.6 Memory

### 2.6.1 DRAM System Memory

The board provides up to 2 GB onboard, soldered DDR2 (double data rate) SDRAM on nine memory components (incl. ECC). The memory bus is 72 bits wide and operates at up to 300 MHz (physical), depending on the processor type.

Depending on the board version the SDRAM may have ECC (error-correcting code). ECC memory provides greater data accuracy and system uptime by protecting against soft errors in computer memory.

### 2.6.2 FRAM

The board has up to 128 KB non-volatile FRAM memory connected to the local bus of the CPU.

The FRAM does not need a back-up voltage for data retention.

### 2.6.3 SRAM

The board has up to 2 MB non-volatile SRAM memory connected to the local bus of the CPU. For data retention during power off the SRAM is supplied with a back-up voltage by a GoldCap.

### 2.6.4 Boot Flash

The board has 16 MB of onboard Flash. It is controlled by the CPU.

Flash memory contains the boot software for the MENMON/operating system bootstrapper and application software. The MENMON sectors are software-protected against illegal write transactions through a password in the serial download function of MENMON (cf. Chapter 3.4.1 Update via the Serial Console using SERDL on page 41).

### 2.6.5 Solid State Flash Disk

The board includes up to 16 GB soldered NAND Flash disk.

A solid state disk (SSD) is a data storage device that uses solid-state memory to store persistent data. An SSD behaves like a conventional hard disk drive. On F50P it has a PATA interface connected to a SATA-to-PATA bridge and controlled by one SATA channel. (See also Chapter 2.7 Mass Storage: Serial ATA (SATA) / SSD on page 25.)

With no moving parts, a solid state disk is more robust, effectively eliminating the risk of mechanical failure, and usually enjoys reduced seek time and latency by removing mechanical delays associated with a conventional hard disk drive.

## 2.7 Mass Storage: Serial ATA (SATA) / SSD

The F50P provides three serial ATA channels through a PCI-to-SATA converter that is connected to the PowerPC processor via a dedicated 66-MHz PCI bus. (On board versions with the MPC8543 processor PCI-to-SATA shares one 33-MHz PCI bus with PCI-to-USB.)

The SATA interfaces support 1.5 Gbits/s.

One SATA channel is used for the SSD solid state Flash disk. (See also Chapter 2.6.5 Solid State Flash Disk on page 24.) The other two SATA channels are led to the rear I/O J2 connector. The pin assignment is in compliance with the PICMG 2.30 CompactPCI PlusIO standard.

See Chapter 2.11 Rear I/O (CompactPCI PlusIO) on page 30 for J2 rear I/O pin assignments.

## 2.8 USB Interfaces

The F50P provides five USB 2.0 host ports with OHCI/EHCI implementation and one USB client port. One host port (USB-0) and the client port (UART-to-USB, USB-1) are led to the front panel. Up to four host ports are available via rear I/O on connector J2.

The host ports are controlled via PCI-to-USB bridges from the PowerPC processor, while the client port is driven by a UART-to-USB converter.

The UART-to-USB interface supports data rates up to 115.2 kbits/s. It has no handshake lines. In connection with USB-to-UART driver software it can be used as a COM interface and is supported by MENMON as a console device.

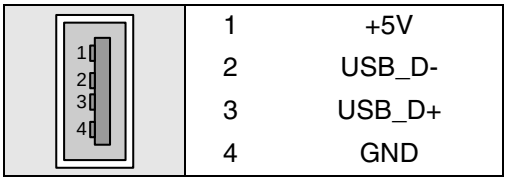
### 2.8.1 Front-Panel Connection

One host port (USB-0) and the client port (UART-to-USB, USB-1) are accessible at the front panel.

Connector types:

- 4-pin USB Series A receptacle according to Universal Serial Bus Specification Revision 1.0
- Mating connector:
  4-pin USB Series A plug according to Universal Serial Bus Specification Revision 1.0

***Table 2.*** *Pin assignment of USB front-panel connectors*




| | |
|---|---|
| 1 | +5V |
| 2 | USB_D- |
| 3 | USB_D+ |
| 4 | GND |

***Table 3.*** *Signal mnemonics of USB front-panel connectors*

| Signal | Direction | Function |
|---|---|---|
| +5V | USB-0: out<br>USB-1: in | +5 V power supply<br>Output for host port USB-0<br>Input for client port USB-1 |
| GND | - | Digital ground |
| USB_D+, USB_D- | in/out | USB lines, differential pair |

### 2.8.2 Rear I/O Connection (CompactPCI PlusIO)

Up to four USB interfaces are accessible via rear I/O in compliance with the PICMG 2.30 CompactPCI PlusIO standard.

See Chapter 2.11 Rear I/O (CompactPCI PlusIO) on page 30 for J2 rear I/O pin assignments.

## 2.9 Ethernet Interfaces

The F50P has up to three Ethernet interfaces controlled by the CPU. All channels support up to 1000 Mbits/s and full-duplex operation.

LAN-0 and LAN-1 are accessible at the front panel, while LAN-2 is available as an option at the J2 rear I/O connector. As an option, even all three Ethernet channels can be made available via J2 rear I/O. The rear Ethernet interfaces are **not** compliant with PICMG 2.30 CompactPCI PlusIO.

Please note that LAN-2 is **not available** on board versions with the MPC8543 processor.

The unique MAC address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable. The MAC addresses on F50P are:

- LAN-0: `0x 00 C0 3A 87 xx xx`
- LAN-1: `0x 00 C0 3A 88 xx xx`
- LAN-2: `0x 00 C0 3A 89 xx xx`

where "00 C0 3A" is the MEN vendor code, "87", "88" and "89" are the MEN product codes, and "xx xx" is the hexadecimal serial number of the product, which depends on your board, e. g. "... `00 2A`" for serial number "000042".

### 2.9.1 Front-Panel Connection

Two standard RJ45 connectors for ports LAN-0 and LAN-1 are available at the front panel. There are also two status LEDs for each channel at the front panel.

The pin assignment corresponds to the Ethernet specification IEEE802.3.

Connector types:

- Modular 8/8-pin mounting jack according to FCC68
- Mating connector:
  Modular 8/8-pin plug according to FCC68

***Table 4.*** *Pin assignment and status LEDs of Ethernet front-panel connectors*

| | | | | 1000Base-T | 10/100Base-T |
|---|---|---|---|---|---|
| Blinks whenever there is transmit or receive activity | 1/3 ● | 4 ○ 3 ● 2 ○ 1 ○ | 1 | BI_DA+ | TX+ |
| | | | 2 | BI_DA- | TX- |
| | | | 3 | BI_DB+ | RX+ |
| | | | 4 | BI_DC+ | - |
| | | | 5 | BI_DC- | - |
| On: 1000Base-T link<br>Off: 10/100Base-T link | 2/4 ○ | | 6 | BI_DB- | RX- |
| | | | 7 | BI_DD+ | - |
| | | | 8 | BI_DD- | - |

***Table 5.*** *Signal mnemonics of Ethernet front-panel connectors*

| Signal | Direction | Function |
|---|---|---|
| BI_Dx+/- | in/out | Differential pairs of data lines for 1000Base-T |
| RX+/- | in | Differential pair of receive data lines for 10/100Base-T |
| TX+/- | out | Differential pair of transmit data lines for 10/100Base-T |

### 2.9.2 Rear I/O Connection

All of the three Ethernet channels can alternatively be routed to the J2 rear I/O connector. By default, no Ethernet is led to connector J2.

See Chapter 2.11 Rear I/O (CompactPCI PlusIO) on page 30 for more information and possible J2 rear I/O pin assignments.

### 2.9.3 General

Ethernet is a local-area network (LAN) protocol that uses a bus or star topology and supports data transfer rates of 100 Mbits/s and more. The Ethernet specification served as the basis for the IEEE 802.3 standard, which specifies the physical and lower software layers. Ethernet is one of the most widely implemented LAN standards.

Ethernet networks provide high-speed data exchange in areas that require economical connection to a local communication medium carrying bursty traffic at high-peak data rates.

A classic Ethernet system consists of a backbone cable and connecting hardware (e.g. transceivers), which links the controllers of the individual stations via transceiver (transmitter-receiver) cables to this backbone cable and thus permits communication between the stations.

### 2.9.4 10Base-T

10Base-T is one of several adaptations of the Ethernet (IEEE 802.3) standard for Local Area Networks (LANs). The 10Base-T standard (also called Twisted Pair Ethernet) uses a twisted-pair cable with maximum lengths of 100 meters. The cable is thinner and more flexible than the coaxial cable used for the 10Base-2 or 10Base-5 standards. Since it is also cheaper, it is the preferable solution for cost-sensitive applications.

Cables in the 10Base-T system connect with RJ45 connectors. A star topology is common with 12 or more computers connected directly to a hub or concentrator.

The 10Base-T system operates at 10 Mbits/s and uses baseband transmission methods.

### 2.9.5 100Base-T

The 100Base-T networking standard supports data transfer rates up to 100 Mbits/s. 100Base-T is actually based on the older Ethernet standard. Because it is 10 times faster than Ethernet, it is often referred to as Fast Ethernet. Officially, the 100Base-T standard is IEEE 802.3u.

There are several different cabling schemes that can be used with 100Base-T, e.g. 100Base-TX, with two pairs of high-quality twisted-pair wires.

### 2.9.6 1000Base-T

1000Base-T is a specification for Gigabit Ethernet over copper wire (IEEE 802.3ab). The standard defines 1 Gbit/s data transfer over distances of up to 100 meters using four pairs of CAT-5 balanced copper cabling and a 5-level coding scheme.

Because many companies already use CAT-5 cabling, 1000Base-T can be easily implemented.

Other 1000Base-T benefits include compatibility with existing network protocols (i.e. IP, IPX, AppleTalk), existing applications, Network Operating Systems, network management platforms and applications.

## 2.10 CompactPCI Interface

The F50P is a 3U CompactPCI system slot board. It implements a 32-bit PCI interface to the CompactPCI backplane which uses a +3.3 V signaling voltage. It also tolerates +5 V.

The CompactPCI bus connects to the MPC8548/MPC8543 processor via a PCI Express x1 link and a PCIe-to-PCI bridge.

The pin assignment of connector J1 as defined in the CompactPCI specification will not be repeated here.

## 2.11 Rear I/O (CompactPCI PlusIO)

The F50P provides great flexibility for routing functions to rear I/O. An optional onboard FPGA allows to implement customized functions on rear I/O connector J2 of the board, with a total available pin count of 64 pins. Different combinations of interfaces controlled by the CPU and the FPGA are possible. The standard version of the F50P is compliant to the PICMG 2.30 CompactPCI PlusIO standard. It supports the pin assignment defined by PICMG 2.30 with 2 SATA and 4 USB interfaces at the J2 connector.

The four USB ports are **always** routed to the J2 connector.

**Please note that the rear I/O Ethernet interfaces of the F50P are not compliant to the CompactPCI PlusIO standard! The Ethernet transformers for the rear Ethernet ports are not located on the F50P but must be placed on a rear I/O board or on the backplane.** This means that it is possible to route up to three Ethernet channels to rear I/O, but additional transformers need to be implemented then, and the pinout will not be compliant with PICMG 2.30 CompactPCI PlusIO.

MEN offers a rear I/O transition module on which the two SATA and four USB interfaces from the J2 connector can be accessed, the CT12. Please note that because of the fixed PICMG 2.30 J2 pin assignment of CT12, only PICMG 2.30 compliant versions of F50P should be used with the CT12. Otherwise signals that have a different function on the F50P may interfere with the CT12 signals.

The Interface Configuration Matrix shows an overview of all varieties that are possible.

Chapter 2.11.2 Standard and Possible Pin Assignments on page 32 gives the standard pin assignment along with possible signal routings.

For further information on the CT12 rear I/O transition module see MEN's website.

In any case please contact our sales team for specially configured board versions. This chapter only summarizes the board's options.

### 2.11.1 User-Defined I/O from Onboard FPGA

The F50P provides the option to include an onboard FPGA. The component is a powerful Altera Arria GX AGX35C device, and is connected to the CPU via a fast, serial PCI Express x1 link. It permits to configure the board's rear I/O according to your needs without any hardware modifications.

Please note that a J2 pin assignment compliant with the PICMG 2.30 CompactPCI PlusIO standard is not possible when customized functions are implemented through the FPGA.

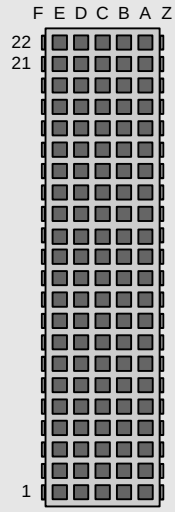
With regard to the FPGA resources such as available logic elements or pins it is not possible to grant all possible combinations of FPGA IP cores.

You can find an overview and descriptions of all available FPGA IP cores on MEN's website.

Table 8, Pin assignment of rear I/O connector J2 – I/O options: maximum FPGA control on page 34 gives the I/O pins available for custom FPGA functions (64 pins).

### 2.11.2 Standard and Possible Pin Assignments

***Table 6.*** *Pin assignment of rear I/O connector J2 – standard board version (PICMG 2.30 CompactPCI PlusIO compatible)*



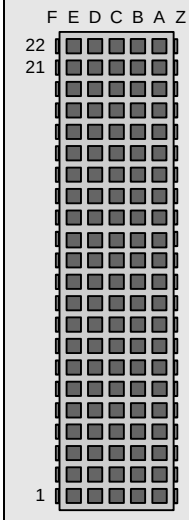

| | F | E | D | C | B | A | Z |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA0 | GA1 | GA2 | GA3 | GA4 | GND |
| 21 | GND | - | - | - | GND | CLK6 | GND |
| 20 | GND | - | - | - | GND | CLK5 | GND |
| 19 | GND | - | - | - | GND | GND | GND |
| 18 | GND | - | - | - | - | - | GND |
| 17 | GND | GNT6# | REQ6# | - | - | - | GND |
| 16 | GND | - | GND | - | - | - | GND |
| 15 | GND | GNT5# | REQ5# | - | - | - | GND |
| 14 | GND | - | - | - | - | - | GND |
| 13 | GND | - | - | - | - | - | GND |
| 12 | GND | - | - | - | - | - | GND |
| 11 | GND | - | - | USB6+ | - | - | GND |
| 10 | GND | - | - | USB6- | - | - | GND |
| 9 | GND | - | - | USB5+ | - | - | GND |
| 8 | GND | SATA2_RX+ | - | USB5- | - | - | GND |
| 7 | GND | SATA2_RX- | SATA2_TX+ | USB4+ | - | - | GND |
| 6 | GND | SATA1_RX+ | SATA2_TX- | USB4- | - | - | GND |
| 5 | GND | SATA1_RX- | SATA1_TX+ | USB3+ | - | - | GND |
| 4 | GND | - | SATA1_TX- | USB3- | - | VIO | GND |
| 3 | GND | GNT4# | REQ4# | GNT3# | GND | CLK4 | GND |
| 2 | GND | REQ3# | GNT2# | SYSEN# | CLK3 | CLK2 | GND |
| 1 | GND | REQ2# | GNT1# | REQ1# | GND | CLK1 | GND |

Note: The F50P's J2 connector type complies with the PICMG 2.30 CompactPCI PlusIO standard.

Note: The signal mnemonics in the above table correspond to the PICMG 2.30 CompactPCI PlusIO standard and therefore do not show the F50P-internal interface numbering. Please see Chapter Table 7. Pin assignment of rear I/O connector J2 – I/O options: Ethernet, USB, SATA on page 33 for the board-internal numbering.

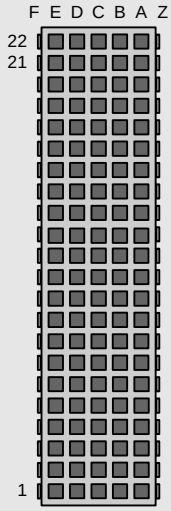
The following table shows **all options for non-FPGA-controlled interfaces**. For this reason, only those pins are marked for FPGA I/O that cannot be used for other functions. See Table 8, Pin assignment of rear I/O connector J2 – I/O options: maximum FPGA control on page 34 for the assignment of the maximum number of FPGA-controlled pins.

***Table 7.*** *Pin assignment of rear I/O connector J2 – I/O options: Ethernet, USB, SATA*




| | F | E | D | C | B | A | Z |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA0 | GA1 | GA2 | GA3 | GA4 | GND |
| 21 | GND | ETH0_1+ | ETH0_3+ | ETH1_1+ | GND | CLK6 | GND |
| 20 | GND | ETH0_1- | ETH0_3- | ETH1_1- | GND | CLK5 | GND |
| 19 | GND | ETH0_0+ | ETH0_2+ | ETH1_0+ | GND | GND | GND |
| 18 | GND | ETH0_0- | ETH0_2- | ETH1_0- | ETH1_2+ | ETH1_3+ | GND |
| 17 | GND | GNT6# | REQ6# | - | ETH1_2- | ETH1_3- | GND |
| 16 | GND | ETH0_VCC | GND | - | ETH1_ACT# | ETH1_VCC | GND |
| 15 | GND | GNT5# | REQ5# | - | ETH2_0+ | ETH1_LNK# | GND |
| 14 | GND | ETH0_ACT# | ETH0_LNK# | IO[63] | ETH2_0- | ETH2_1+ | GND |
| 13 | GND | IO[29] | IO[28] | - | ETH2_2+ | ETH2_1- | GND |
| 12 | GND | IO[27] | IO[26] | IO[64] | ETH2_2- | ETH2_3+ | GND |
| 11 | GND | IO[25] | IO[24] | USB6+ | ETH2_ACT# | ETH2_3- | GND |
| 10 | GND | IO[23] | IO[22] | USB6- | +3.3V | ETH2_VCC | GND |
| 9 | GND | IO[21] | IO[20] | USB5+ | ETH2_LNK# | +3.3V | GND |
| 8 | GND | SATA2_RX+ | IO[18] | USB5- | +5V | +5V | GND |
| 7 | GND | SATA2_RX- | SATA2_TX+ | USB4+ | IO[6] | IO[5] | GND |
| 6 | GND | SATA1_RX+ | SATA2_TX- | USB4- | IO[8] | IO[7] | GND |
| 5 | GND | SATA1_RX- | SATA1_TX+ | USB3+ | USB_OC5/6# | IO[9] | GND |
| 4 | GND | IO[11] | SATA1_TX- | USB3- | USB_OC3/4# | VIO | GND |
| 3 | GND | GNT4# | REQ4# | GNT3# | GND | CLK4 | GND |
| 2 | GND | REQ3# | GNT2# | SYSEN# | CLK3 | CLK2 | GND |
| 1 | GND | REQ2# | GNT1# | REQ1# | GND | CLK1 | GND |

***Table 8.*** *Pin assignment of rear I/O connector J2 – I/O options: maximum FPGA control*




| | F | E | D | C | B | A | Z |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA0 | GA1 | GA2 | GA3 | GA4 | GND |
| 21 | GND | IO[36] | IO[40] | IO[44] | GND | CLK6 | GND |
| 20 | GND | IO[35] | IO[39] | IO[43] | GND | CLK5 | GND |
| 19 | GND | IO[34] | IO[38] | IO[42] | GND | GND | GND |
| 18 | GND | IO[33] | IO[37] | IO[41] | IO[45] | IO[46] | GND |
| 17 | GND | GNT6# | REQ6# | - | IO[47] | IO[48] | GND |
| 16 | GND | IO[32] | GND | - | IO[49] | IO[50] | GND |
| 15 | GND | GNT5# | REQ5# | - | IO[51] | IO[52] | GND |
| 14 | GND | IO[31] | IO[30] | IO[63] | IO[53] | IO[54] | GND |
| 13 | GND | IO[29] | IO[28] | - | IO[55] | IO[56] | GND |
| 12 | GND | IO[27] | IO[26] | IO[64] | IO[57] | IO[58] | GND |
| 11 | GND | IO[25] | IO[24] | USB6+ | IO[59] | IO[60] | GND |
| 10 | GND | IO[23] | IO[22] | USB6- | IO[61] | IO[62] | GND |
| 9 | GND | IO[21] | IO[20] | USB5+ | IO[2] | IO[1] | GND |
| 8 | GND | IO[19] | IO[18] | USB5- | IO[4] | IO[3] | GND |
| 7 | GND | IO[17] | IO[16] | USB4+ | IO[6] | IO[5] | GND |
| 6 | GND | IO[15] | IO[14] | USB4- | IO[8] | IO[7] | GND |
| 5 | GND | IO[13] | IO[12] | USB3+ | USB_OC5/6# | IO[9] | GND |
| 4 | GND | IO[11] | IO[10] | USB3- | USB_OC3/4# | VIO | GND |
| 3 | GND | GNT4# | REQ4# | GNT3# | GND | CLK4 | GND |
| 2 | GND | REQ3# | GNT2# | SYSEN# | CLK3 | CLK2 | GND |
| 1 | GND | REQ2# | GNT1# | REQ1# | GND | CLK1 | GND |

***Table 9.*** *Signal mnemonics of rear I/O connector J2*

| | Signal | Direction | Function |
|---|---|---|---|
| **Power** | GND | - | Ground |
| | VIO | in | 3.3 V V(I/O) supply voltage |
| | +3.3V | in | +3.3V supply voltage, optional |
| | +5V | in | +5V supply voltage, optional |
| **CompactPCI** | CLK[6:1] | out | Clocks 1 to 6 |
| | GA[4:0] | in | Geographic addressing signals 0 to 4 |
| | GNT#[6:1] | out | Grant 1 to 6 |
| | REQ#[6:1] | in | Request 1 to 6 |
| | SYSEN# | in | System slot identification |
| **Ethernet** | ETH0_[3:0]+, ETH0_[3:0]- | in/out | Differential data pairs 0 to 3, port 0 |
| | ETH1_[3:0]+, ETH1_[3:0]- | in/out | Differential data pairs 0 to 3, port 1 |
| | ETH2_[3:0]+, ETH2_[3:0]- | in/out | Differential data pairs 0 to 3, port 2 |
| | ETH0_ACT#, ETH1_ACT#, ETH2_ACT# | out | Signal for activity status LED, ports 0 to 2, optional |
| | ETH0_LNK#, ETH1_LNK#, ETH2_LNK# | out | Signal for link status LED, ports 0 to 2, optional |
| | ETH0_VCC, ETH1_VCC, ETH2_VCC | out | Reference voltage, ports 0 to 2 |
| **SATA** | SATA1_RX+, SATA1_RX-<br>(PICMG 2.30: 1_SATA_Rx+, 1_SATA_Rx-) | in | Differential SATA receive lines, port 1 |
| | SATA1_TX+, SATA1_TX-<br>(PICMG 2.30: 1_SATA_Tx+, 1_SATA_Tx-) | out | Differential SATA transmit lines, port 1 |
| | SATA2_RX+, SATA2_RX-<br>(PICMG 2.30: 2_SATA_Rx+, 2_SATA_Rx-) | in | Differential SATA receive lines, port 2 |
| | SATA2_TX+, SATA2_TX-<br>(PICMG 2.30: 2_SATA_Tx+, 2_SATA_Tx-) | out | Differential SATA transmit lines, port 2 |
| **USB** | USB3+, USB3-<br>(PICMG 2.30: 1_USB2+, 1_USB2-) | in/out | Differential USB 2.0 lines, port 3 |
| | USB4+, USB4-<br>(PICMG 2.30: 2_USB2+, 2_USB2-) | in/out | Differential USB 2.0 lines, port 4 |
| | USB5+, USB5-<br>(PICMG 2.30: 3_USB2+, 3_USB2-) | in/out | Differential USB 2.0 lines, port 5 |
| | USB6+, USB6-<br>(PICMG 2.30: 4_USB2+, 4_USB2-) | in/out | Differential USB 2.0 lines, port 6 |
| | USB_OC3/4#, USB_OC5/6# | in | USB overcurrent, ports 3 and 4,and ports 5 and 6, optional |
| **FPGA I/O** | IO[64:1] | in/out | FPGA I/O pins, 64 lines |

## 2.12 Reset Button and Status LED

The F50P has a reset button and one status LED at the front panel. The reset button is recessed within the front panel and requires a tool, e.g. paper clip to be pressed, preventing the button from being inadvertently activated.

The yellow status LED shows board status messages. If the onboard FPGA is implemented, the LED lights up as soon as the FPGA was initialized. If no FPGA is implemented on the board, the LED has no function.

# 3 MENMON

## 3.1 General

MENMON is the CPU board firmware that is invoked when the system is powered on.

The basic tasks of MENMON are:

- Initialize the CPU and its peripherals.
- PCI/PCIe auto configuration.
- Perform self-test.
- Provide debug/diagnostic features on MENMON command line.
- Interaction with the user via touch panel/TFT display (if supported through FPGA).
- Boot operating system.
- Update firmware or operating system.

The following description only includes board-specific features. For a general description and in-depth details on MENMON, please refer to the MENMON 2nd Edition User Manual.

### 3.1.1 State Diagram

***Figure 3.*** *MENMON – State diagram, Degraded Mode/Full Mode*

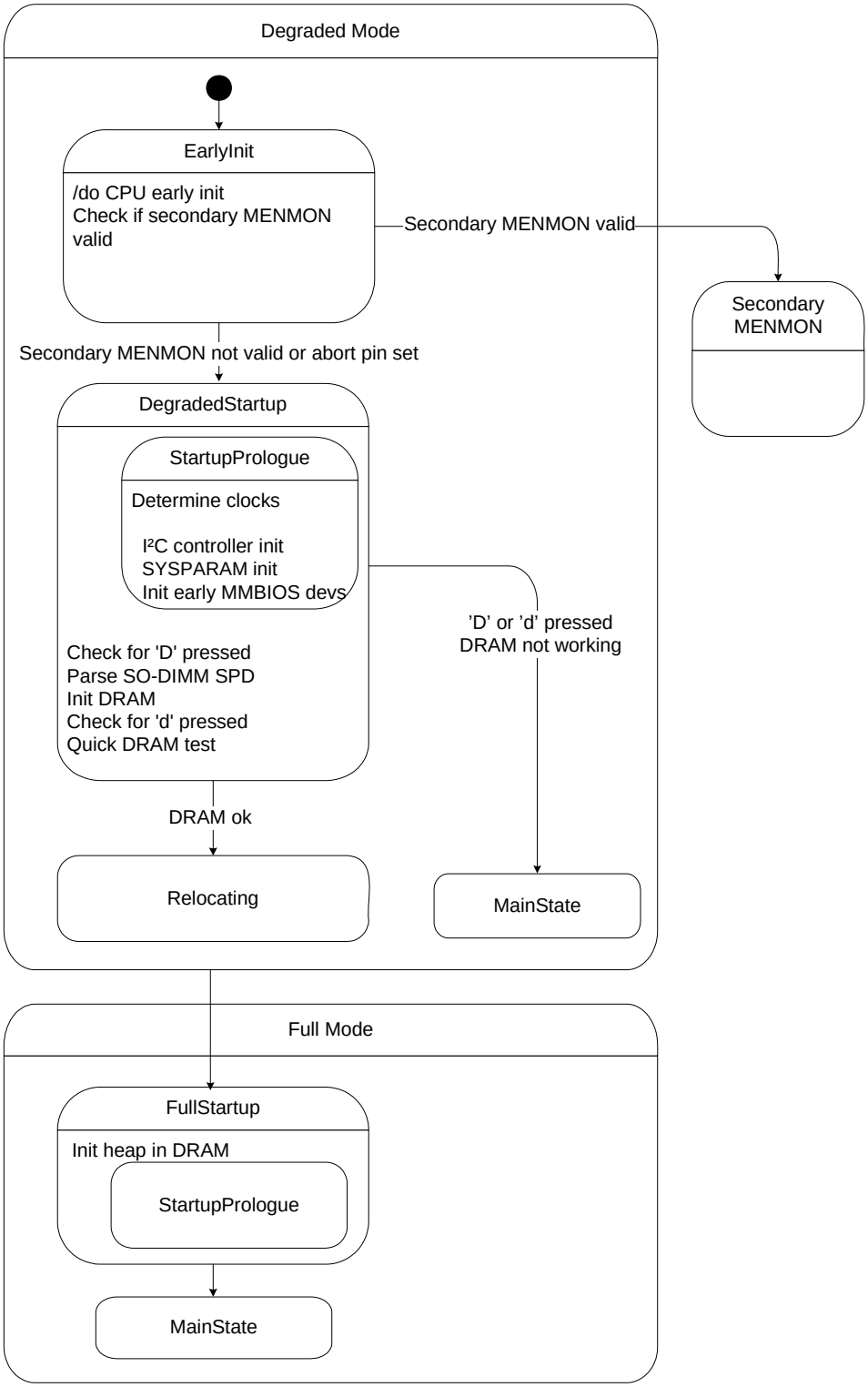
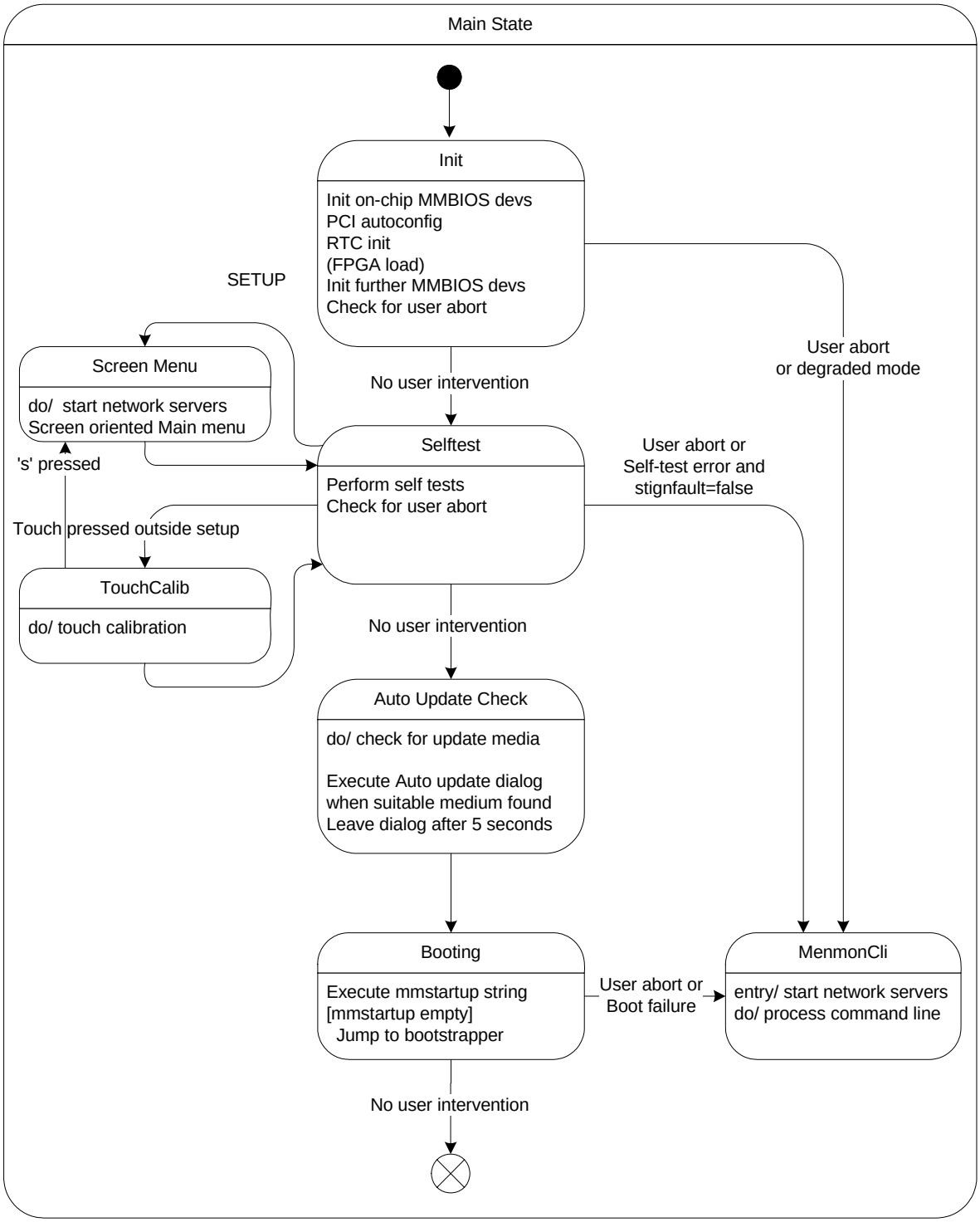


***Figure 4.*** *MENMON – State diagram, main state*



## 3.2 Interacting with MENMON

To interact with MENMON, you can use the following consoles:

- UART-to-USB COM (via UART-to-USB interface)
- Touch panel / TFT interface (if present)
- Telnet via network connection
- HTTP */monpage* via network connection

The default setting of the COM ports is 9600 baud, 8 data bits, no parity, and one stop bit.

### 3.2.1 Entering the Setup Menu/Command Line

During normal boot, you can abort the booting process in different ways during the self-test, depending on your console:

- With a touch panel press the "Setup" button to enter the Setup Menu.
- With a text console press the "s" key to enter the Setup Menu.
- With a text console press "ESC" to enter the command line.

By default, the self-test is not left until 3 seconds have elapsed (measured from the beginning of the self-test), even if the actual test has finished earlier, to give the user a chance to abort booting and enter the Setup Menu.

You can modify the self-test wait time through MENMON system parameter *stwait* (see *stwait*).

## 3.3 Configuring MENMON for Automatic Boot

You can configure how MENMON boots the operating system either through the Setup Menu or through the command line.

In the Basic Setup Menu you can select the boot sequence for the bootable devices on the F50P. The selected sequence is stored in system parameter *mmstartup* as a string of MENMON commands. For example, if the user selects: "Int. CF, Ether, (None)", the *mmstartup* string will be set to "DBOOT 0; NBOOT TFTP".

You can view and modify this string directly, using the Expert Setup Menu, option *Startup string*, or through the command-line command *EE-MMSTARTUP*.

(See also MENMON 2nd Edition User Manual for further details.)

## 3.4 Updating Boot Flash

### 3.4.1 Update via the Serial Console using *SERDL*

You can use command *SERDL* to update program data using the serial console.

The following table shows the F50P locations:

***Table 10.*** *MENMON – Program update files and locations*

| File Name Extension | Typical File Name | Password for *SERDL* | Location |
|---|---|---|---|
| *.SMM* | *14XM50-00_01_02.SMM* | MENMON | Secondary MENMON |
| *.Fxxx* | *MYFILE.F000* | - | Starting at sector *xxx* in boot Flash |
| *.Exx* | *MYFILE.E00* | - | Starting at byte *xx* in EEPROM |

### 3.4.2 Update from Network using *NDL*

You can use the network download command *NDL* to download the update files from a TFTP server in network. The file name extensions, locations and passwords are the same as for the *SERDL* command.

### 3.4.3 Update via Program Update Menu

MENMON scans an external medium connected to the first USB port (USB0) for files named *14XM50*.SMM*. The Program Update Menu will then give a list of all files on this medium conforming with this name pattern for selection.

### 3.4.4 Automatic Update Check

MENMON's automatic update check looks for some special files on an external medium connected to the first USB port (USB0). However, the F50P implementation does not support program update here but can boot from the external medium.

The file that is searched for has a name stored in system parameter *bf* or *bootfile*, or – if this is empty – *BOOTFILE*. If this file is found, it is assumed that the external medium is supposed to be booted from.

To allow MENMON to locate this file, it must be in the root directory of a DOS FS. This works on unpartitioned media or on drives with one partition.

MENMON does not automatically start the boot but presents the following menu to the user:

```
Detected an update capable external medium

  >Ignore, continue boot

   Boot from external medium
```

If there is no user input for 5 seconds after the menu appears, booting continues.

### 3.4.5 Updating MENMON Code

Updates of MENMON are available for download from MEN's website. MENMON's integrated Flash update functions allow you to do updates yourself. However, you need to take care and follow the instructions given here. Otherwise, you may make your board inoperable!

**In any case, read the following instructions carefully!**

**Please be aware that you do MENMON updates at your own risk. After an incorrect update your CPU board may not be able to boot.**

Do the following to update MENMON:

- ☑ Unzip the downloaded file, e.g. *14xm50-00_01_02.zip*, into a temporary directory.
- ☑ Power on your F50P.
- ☑ Connect a terminal emulation program with the UART-to-USB port of your F50P and set the terminal emulation program to 9600 baud, 8 data bits, 1 stop bit, no parity, no handshaking (if you haven't changed the target baud rate on your own).[1]
- ☑ Reset the F50P by pressing the reset button, or through software (e.g. reboot command under VxWorks).
- ☑ Press "ESC" immediately after resetting the F50P.
- ☑ In your terminal emulation program, you should see the "MenMon>" prompt.
- ☑ Enter "SERDL MENMON" to update the secondary MENMON. You should now see a "C" character appear every 3 seconds.
- ☑ In your terminal emulation program, start a "YModem" download of file *14xm50-00_01_02.smm* (for example, with Windows Hyperterm, select *Transfer > Send File* with protocol "YModem").
- ☑ When the download is completed, reset the F50P.

[1] You can change the baud rate at runtime using command *cons-baud*. See Table 27, MENMON – Command reference (page 56). If you want to accelerate file transfer you can select a higher baud rate in MENMON and then set the terminal emulation program accordingly.

## 3.5 Diagnostic Tests

### 3.5.1 Ethernet

***Table 11.*** *MENMON – Diagnostic tests: Ethernet*

| Test Name | Description | Availability |
|---|---|---|
| *ETHER0*<br>*ETHER1*<br>*ETHER2* | Ethernet 0/1/2 (LAN-0/1/2) internal loopback test<br>Groups: POST AUTO | Always<br>(except ETHER2 with an MPC8543 processor) |
| *ETHER0_X*<br>*ETHER1_X*<br>*ETHER2_X* | Ethernet 0/1/2 (LAN-0/1/2) external loopback test<br>Groups: NONAUTO ENDLESS | Always<br>(except ETHER2 with an MPC8543 processor) |

#### 3.5.1.1 Ethernet Internal Loopback Test

The test

- configures the network interface for loopback mode (on PHY)
- verifies that the interface's ROM has a good checksum
- verifies that the MAC address is valid (not `0xFFFFFF`...)
- sends 10 frames with `0x400` bytes payload each
- verifies that frames are correctly received on the same interface.

If the network interface to test is the currently activated interface for the MENMON network stack, the interface is detached from the network stack during test and reactivated after test.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY

Does not check:

- Connection between PHY and physical connector
- Interrupt line
- All LAN speeds

#### 3.5.1.2 Ethernet External Loopback Test

This test is the same as the Ethernet Internal Loopback Test, but requires an external loopback connector. Before sending frames, the link state is monitored. If it is not ok within 2 seconds, the test fails.

Note: A loopback connector makes a connection between the following pins of the 8-pin Ethernet connector: 1-3, 2-6, 4-7, 5-8.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY
- Connection between PHY and physical connector

Does not check:

- Interrupt line
- All LAN speeds

### 3.5.2 SDRAM, SRAM and FRAM

***Table 12.*** *MENMON – Diagnostic tests: SDRAM, SRAM and FRAM*

| Test Name | Description | Availability |
|---|---|---|
| *SDRAM* | Quick SDRAM connection test<br>Groups: POST AUTO | Always |
| *SDRAM_X* | Full SDRAM test<br>Groups: NONAUTO ENDLESS | Always |
| *SRAM* | Quick SRAM test<br>Groups: POST AUTO | F50P is known to have SRAM |
| *SRAM_X* | Full SRAM test<br>Groups: NONAUTO ENDLESS | |
| *FRAM* | Quick FRAM test<br>Groups: POST AUTO | F50P is known to have FRAM |
| *FRAM_X* | Full FRAM test<br>Groups: NONAUTO ENDLESS | |

#### 3.5.2.1 Quick RAM Test

This quick test checks most of the connections to the RAM chips but does not test all RAM cells. It executes very quickly (within milliseconds).

This test is non-destructive (saves/restores original RAM content).

Checks:

- All address lines
- All data lines
- Byte enable signals
- Indirectly, checks clock and other control signals

Does not check:

- SDRAM cells
- Burst mode

#### 3.5.2.2 Extended RAM Test

This full-featured memory test allows to test all RAM cells. Depending on the size of the SDRAM, this test can take up to one minute.

It tests 8-, 16- or 32-bit access, each with random pattern, and single and burst access.

On each pass, this test first fills the entire memory (starting with the lowest address) with the selected pattern, using the selected access mode, and then verifies the entire block.

This test is destructive.

Checks:

- All address lines
- All data lines
- All control signals
- All SDRAM cells

### 3.5.3 EEPROM

***Table 13.*** *MENMON – Diagnostic tests: EEPROM*

| Test Name | Description | Availability |
|---|---|---|
| *EEPROM* | I²C access/Magic nibble check<br>Groups: POST AUTO ENDLESS | Always |

This test reads the first EEPROM cell over SMB and checks if bits 3..0 of this cell contain the magic nibble `0xE`.

### 3.5.4 USB

***Table 14.*** *MENMON – Diagnostic tests: USB*

| Test Name | Description | Availability |
|---|---|---|
| *USB0..USB5* | USB device access / sector 0 access<br>Groups: NONAUTO ENDLESS | Always |

The test performs a sector 0 read from the Flash disk without verifying the content of the sector.

Checks:

- USB control lines (Data- / Data+)
- Basic USB transfer

Does not check:

- IRQ signals
- Partition table or file system on disk

### 3.5.5 Hardware Monitor Test

***Table 15.*** *MENMON – Diagnostic tests: hardware monitor*

| Test Name | Description | Availability |
|---|---|---|
| *LM81* | LM81 basic access test<br>Groups: POST AUTO | Always |

### 3.5.6 RTC

***Table 16.*** *MENMON – Diagnostic tests: RTC*

| Test Name | Description | Availability |
|---|---|---|
| *RTC* | Quick presence test of RTC<br>Groups: POST AUTO | Always |
| *RTC_X* | Extended test of RTC<br>Groups: NONAUTO ENDLESS | Always |

#### 3.5.6.1 RTC Test

This is a quick presence test of the real-time clock (RTC) and is executed on POST.

Checks:

- Presence of RTC (I²C access)

Does not check:

- If RTC is running
- RTC backup voltage

#### 3.5.6.2 Extended RTC Test

Checks:

- Presence (e.g. I²C access)
- RTC is running

Does not check:

- RTC backup voltage

## 3.6 MENMON Configuration and Organization

### 3.6.1 Consoles

You can select the active consoles by means of system parameters *con0..con3* and configure the console through parameters *ecl*, *gcon*, *hdp* and *tdp*. MENMON commands *CONS(-xxx)* also give access to the console settings (see Chapter 3.7 MENMON Commands (page 56)).

***Table 17.*** *MENMON – System parameters for console selection and configuration*

| Parameter (alias) | Description | Default | User Access |
|---|---|---|---|
| *cbr (baud)* | Baud rate of all UART consoles (decimal) (default: 9600 baud, 8n1) | 9600 | Read/write |
| *con0..con3* | CLUN of console 0..3<br>CLUN=0x00: disable<br>CLUN=0xFF: Autoselect next available console<br>*con0* is implicitly the debug console | *con0*: 08 (UART-to-USB COM)<br>*con1*: 00 (none)<br>*con2*: 00 (none)<br>*con3*: 00 (none) | Read/write |
| *ecl* | CLUN of attached network interface (hex)<br>CLUN=0x00: none<br>CLUN=0xFF: first available Ethernet | 0xFF | Read/write |
| *gcon* | CLUN of graphics device to display boot logo<br>CLUN=0x00: disable<br>CLUN=0xFF: Autoselect first available graphics console | 0xFF (AUTO) | Read/write |
| *hdp* | HTTP server TCP port (decimal)<br>0: don't start telnet server<br>-1: use default port 23<br>else: TCP port for telnet server | -1 | Read/write |
| *tdp* | Telnet server TCP port (decimal)<br>0: don't start HTTP server<br>-1: use default port 80<br>else: TCP port for HTTP server | -1 | Read/write |

### 3.6.2 MENMON Memory Map

#### 3.6.2.1 MENMON Memory Address Mapping

***Table 18.*** *MENMON – Address map (full-featured mode)*

| Address Space | Size | Description |
|---|---|---|
| 0x 0000 0000 .. 0000 1400 | 5 KB | Exception vectors |
| 0x 0000 3000 .. 0000 3FFF | 4 KB | MENMON parameter string |
| 0x 0000 4200 .. 0000 42FF | 256 bytes | VxWorks bootline |
| 0x 0000 4300 .. 00FF FFFF | Nearly 16 MB | Free |
| 0x 01D0 0000 .. 01DF FFFF | 2 MB | Heap2 |
| 0x 01E0 0000 .. 01EF FFFF | 1 MB | Text + Reloc |
| 0x 01F0 0000 .. 01F1 FFFF | 128 KB | Stack |
| 0x 01F2 0000 .. 01F4 FFFF | 128 KB | Stack for user programs and operating system boot |
| 0x 01F5 0000 .. 01FE FFFF | 640 KB | Heap |
| 0x 01FF 0000 .. 01FF FFFF | 64 KB | Not touched for OS post mortem buffer i.e. VxWorks WindView or MDIS debugs (requires ECC to be turned off!) |
| 0x 0200 0000 .. End of RAM | | Free or download area |

#### 3.6.2.2 Boot Flash Memory Map

***Table 19.*** *MENMON – Boot Flash memory map*

| Flash Offset | CPU Address | Size | Description |
|---|---|---|---|
| 0x 00 0000 | 0x FF00 0000 | 14 MB (- 128 KB) | Available to user |
| 0x DE 0000 | 0x FFDE 0000 | 128 KB | System parameter section in boot Flash (if *useflpar* system parameter is set to 1) |
| 0x E0 0000 | 0x FFE0 0000 | 1 MB | Secondary MENMON |
| 0x F0 0000 | 0x FFF0 0000 | 1 MB | Primary MENMON |

### 3.6.3 MENMON BIOS Logical Units

The following table shows fixed assigned CLUNs. All other CLUNs are used dynamically.

***Table 20.*** *MENMON – Controller Logical Units (CLUNs)*

| CLUN | MENMON BIOS Name | Description |
|---|---|---|
| 0x02 | ETHER0 | Ethernet #0 (LAN-0) |
| 0x03 | ETHER1 | Ethernet #1 (LAN-1) |
| 0x04 | ETHER2 | Ethernet #2 (LAN-2) |
| 0x06 | USB | USB controller |
| 0x08 | UART-to-USB COM | MPC854X DUART channel #0 |
| 0x0A | TOUCH | Reserved for touch console |
| 0x10 | SATA0 | SATA port 0 (routed to SSD Flash) |
| 0x11 | SATA1 | SATA port 1 |
| 0x12 | SATA2 | SATA port 2 |
| 0x2x | | All other devices dynamically detected on PCI or FPGA devices |
| 0x40 | | Telnet console |
| 0x41 | | HTTP monitor console |

***Table 21.*** *MENMON – Device Logical Units (DLUNs)*

| CLUN/DLUN | MENMON BIOS Name | Description |
|---|---|---|
| 0x06/0x00 | USB | USB controller[1] |
| 0x10/0x00 | SATA0 | Disk at SATA port 0 (onboard SSD Flash) |
| 0x11/0x00 | SATA1 | Disk at SATA port 1 |
| 0x12/0x00 | SATA2 | Disk at SATA port 2 |

[1] The actual disks can be selected through command USBDP, see also page 57.

### 3.6.4 System Parameters

System parameters are parameters stored in EEPROM. Some parameters are automatically detected by MENMON (such as CPU type and frequency). The parameters can be modified through the *EE-xxx* command via the command line.

#### 3.6.4.1 Physical Storage of Parameters

Most parameters are stored in the 1024-byte serial EEPROM on the F50P.

If required, you can configure MENMON to store some strings in boot Flash rather than in EEPROM.

#### 3.6.4.2 Start-up with Faulty EEPROM

If a faulty EEPROM is detected (i.e. the checksum of the EEPROM section is wrong), the system parameters will use defaults. The behavior is the same if the EEPROM is blank. The default baud rate is 9600.

#### 3.6.4.3 F50P System Parameters

Note: Parameters marked by "Yes" in section "Parameter String" are part of the MENMON parameter string.

***Table 22.*** *MENMON – F50P system parameters – Autodetected parameters*

| Parameter (alias) | Description | Standard Default | Parameter String | User Access |
|---|---|---|---|---|
| *ccbclkhz* | CCB clock frequency (decimal, Hz) | | Yes | Read-only |
| *clun* | MENMON controller unit number that MENMON used as the boot device (hexadecimal) | | Yes | Read-only |
| *cons* | Selected console. Set to name of first selected console | | Yes | Read-only |
| *cpu* | CPU type as ASCII string (e.g. "MPC8548E") | | Yes | Read-only |
| *cpuclkhz* | CPU core clock frequency (decimal, Hz) | | Yes | Read-only |
| *dlun* | MENMON device unit number that MENMON used as the boot device (hexadecimal) | | Yes | Read-only |
| *flash0* | Flash size (decimal, kilobytes) | | Yes | Read-only |
| *fram0* | FRAM size (decimal, kilobytes) | | Yes | Read-only |
| *immr* | Physical address of CCSR register block | | Yes | Read-only |
| *mem0* | RAM size (decimal, kilobytes) | | Yes | Read-only |
| *mem1* | Size of SRAM[1] (decimal, kilobytes) | | Yes | Read-only |
| *memclkhz* | Memory clock frequency (decimal, Hz) | | Yes | Read-only |

| Parameter (alias) | Description | Standard Default | Parameter String | User Access |
|---|---|---|---|---|
| *mm* | Info whether primary or secondary MENMON has been used for booting, either "smm" or "pmm" | | Yes | Read-only |
| *mmst* | Status of diagnostic tests, as a string | | Yes | Read-only |
| *nmac0/1/2* | MAC address of Ethernet interface x (0..n). Format e.g. "00112233445566".<br>Set automatically according to serial number of the board | | Yes | Read-only |
| *pciclkhz* | PCI bus clock frequency = system input clock (decimal, Hz) | | Yes | Read-only |
| *rststat* | Reset status code as a string, see Chapter 3.6.4.4 Reset Cause – Parameter rststat on page 55 | | Yes | Read-only |
| *usbdp* | USB boot device path in format “bus>1st_port_no>…>last_port_no”<br>(e.g. “00>02>01” for USB bus = 0, port no. 1 = 2, port no. 2 = 1) | | Yes | Read-only |

[1] If implemented.

***Table 23.*** *MENMON – F50P system parameters – Production data*

| Parameter (alias) | Description | Standard Default | Parameter String | User Access |
|---|---|---|---|---|
| *brd* | Board name | - | Yes | Read-only |
| *brdmod* | Board model "mm" | - | Yes | Read-only |
| *brdrev* | Board revision "xx.yy.zz" | - | Yes | Read-only |
| *prodat* | Board production date MM/DD/YYYY | - | Yes | Read-only |
| *repdat* | Board last repair date MM/DD/YYYY | - | Yes | Read-only |
| *sernbr* | Board serial number | - | Yes | Read-only |

***Table 24.*** *MENMON – F50P system parameters – MENMON persistent parameters*

| Parameter (alias) | Description | Standard Default | Parameter String | User Access |
|---|---|---|---|---|
| *bsadr (bs)* | Bootstrapper address. Used when BO command was called without arguments. (hexadecimal, 32 bits) | 0 | No | Read/write |
| *cbr (baud)* | Baudrate of all UART consoles (dec) | 9600 | Yes | Read/write |
| *con0..con3* | CLUN of console 0..3. (hex) (see Chapter 3.6.1 Consoles on page 48) | 0xFF = auto | No | Read/write |
| *eccsth* | ECC single-bit error threshold | 32 | No | Read/write |
| *ecl* | CLUN of attached network interface (hex) | 0xFF | No | Read/write |
| *gcon* | CLUN of graphics screen (hex) (see Chapter 3.6.1 Consoles on page 48) | 0xFF = auto | No | Read/write |
| *hdp* | HTTP server TCP port (decimal) | -1 | No | Read/write |
| *kerpar* | Linux Kernel Parameters (399 chars max). Part of VxWorks bootline if *useflpar*=0. (400 chars max if *useflpar*=1) | Empty string | No | Read/write |
| *ldlogodis* | Disable load of boot logo (bool) | 0 | No | Read/write |
| *mmstartup (startup)* | Start-up string<br>256 chars max if *useflpar*=0<br>512 chars max if *useflpar*=1 | Empty string | No | Read/write |
| *nobanner* | Disable ASCII banner on start-up | 0 | No | Read/write |
| *noecc* | Do not use ECC even if board supports it (bool) | 0 | No | Read/write |
| *nspeed0/1/3* | Speed setting for Ethernet interface 0..3.<br>Possible values: *AUTO*, *10HD*, *10FD*, *100HD*, *100FD*, *1000* | AUTO | Yes | Read/write |
| *stdis* | Disable POST (bool) | 0 | No | Read/write |
| *stdis_XXX* | Disable POST test with name XXX (bool)<br>*stdis_ether* – Internal ETHER0/1/2 loopback<br>*stdis_fram* – FRAM test[1]<br>*stdis_sram* – SRAM test[2]<br>*stdis_touch* – Touch controller test | 0 | No | Read/write |
| *stignfault* | Ignore POST failure, continue boot (bool) | 1 | No | Read/write |
| *stwait* | Time in 1/10 seconds to stay at least in SELFTEST state (decimal)<br>0 = Continue as soon as POST has finished | 30 | No | Read/write |

| Parameter (alias) | Description | Standard Default | Parameter String | User Access |
|---|---|---|---|---|
| *tdp* | Telnet server TCP port (decimal) | -1 | No | Read/write |
| *tries* | Number of network tries | 20 | No | Read/write |
| *tto* | Minimum timeout between network retries (decimal, in seconds) | 0 | No | Read/write |
| *u00..u15* | User parameters (hex, 16 bits) | 0x0000 | No | Read/write |
| *updcdis* | Disable auto update check (bool) | 0 | No | Read/write |
| *useflpar* | Store *kerpar* and *mmstartup* parameters in boot Flash rather than in EEPROM (bool) | 0 | No | Read/write |
| *vmode* | Vesa Video Mode for graphics console (hex) | 0x0101 | No | Read/write |
| *wdt* | Time after which watchdog timer shall reset the system after MENMON has passed control to operating system (decimal, in 1/10 s)<br>If 0, MENMON disables the watchdog timer before starting the operating system.<br>Note: The F50P watchdog supports only the following values:<br>0: Disable watchdog timer<br>11: Short time-out (1.12 seconds)<br>260: Long time-out (26.0 seconds) | 0 (disabled) | No | Read/write |

[1] If FRAM is implemented.
[2] If SRAM is implemented.

***Table 25.*** *MENMON – F50P system parameters – VxWorks bootline parameters*

| Parameter (alias) | Description | Standard Default | Parameter String | User Access |
|---|---|---|---|---|
| *bf (bootfile)* | Boot file name (127 chars max) | Empty string | No | Read/write |
| *bootdev* | VxWorks boot device name | Empty string | No | Read/write |
| *e (netip)* | IP address, subnet mask, e.g. 192.1.1.28:ffffff00 | Empty string | No | Read/write |
| *g (netgw)* | IP address of default gateway | Empty string | No | Read/write |
| *h (nethost)* | Host IP address (used when booting over *NBOOT TFTP*) | Empty string | No | Read/write |
| *hostname* | VxWorks name of boot host | Empty string | No | Read/write |
| *netaddr* | Access the IP address part of *netip* parameter | | No | Read/write |
| *netsm* | Access the subnet mask part of *netip* parameter | | No | Read/write |
| *procnum* | VxWorks processor number (decimal) | 0 | No | Read/write |
| *s* | VxWorks start-up script | Empty string | No | Read/write |
| *tn (netname)* | Host name of this machine | Empty string | No | Read/write |
| *unitnum* | VxWorks boot device unit number (decimal) | 0 | No | Read/write |

#### 3.6.4.4 Reset Cause – Parameter *rststat*

The following *rststat* values are possible:

When MENMON starts up, it determines the reset cause and sets system parameter *rststat* accordingly:

***Table 26.*** *MENMON – Reset causes through system parameter* rststat

| ***rststat* Value** | **Description** |
|---|---|
| *cbrst* | Board was reset using the reset button |
| *pwon* | Power On |
| *swrst* | Board was reset by software (by means of the board's reset controller). |
| *wdog* | Board was reset by watchdog timer unit |

## 3.7 MENMON Commands

The following table gives all MENMON commands that can be entered on the F50P MENMON prompt. You can call this list also using the *H* command.

***Table 27.*** *MENMON – Command reference*

| Command | Description |
|---|---|
| .[<reg>] [<val>] | Display/modify registers in debugger model |
| ACT [<addr>] [<size>] | Execute a HWACT script |
| ARP | Dump network stack ARP table |
| B[DC<no>] [<addr>] | Set/display/clear breakpoints |
| BIOS_DBG <mask> [net] \| cons <clun> | Set MENMON BIOS or network debug level, set debug console |
| BO [<addr>] [<opts>] | Call OS bootstrapper |
| BOOTP [<opts>] | Obtain IP config via BOOTP |
| C[BWLLNAX#] <addr> [<val> ...] | Change memory |
| CHAM [<clun>] | Dump FPGA Chameleon table |
| CONS | Show active consoles |
| CONS-ACT <clun1> [<clun2>] ... | Test console configuration |
| CONS-BAUD <baud> | Change baud rate instantly without storing |
| CONS-GX <clun> | Test graphics console |
| D [<addr>] [<cnt>] | Dump memory |
| DBOOT [<clun>] [<dlun>] [<opts>] | Boot from disk |
| DCACHE OFF \| ON | Enable/disable data cache |
| DIAG [<which>] [VTF] | Run diagnostic tests |
| DSKRD <args> | Read blocks from RAW disk |
| DSKWR <args> | Write blocks to RAW disk |
| EE[-xxx] [<arg>] | Persistent system parameter commands |
| EER[-xxx] [<arg>] | Raw serial EEPROM commands |
| ERASE <D> [<O>] [<S>] | Erase Flash sectors |
| FI <from> <to> <val> | Fill memory (byte) |
| GO [<addr>] | Jump to user program |
| H<br>HELP | Print help |
| I [<D>] | List board information |
| ICACHE OFF \| ON | Enable/disable instruction cache |
| IOI | Scan for BIOS devices |
| LM81 | Show current voltage and temperature values |
| LOGO | Display MENMON start-up text screen |
| LS <clun> <dlun> [<opts>] | List files/partitions on device |

| Command | Description |
|---|---|
| MC <addr1> <addr2> <cnt> | Compare memory |
| MII <clun> [<reg>] [<val>] | Ethernet MII register command |
| MO <from> <to> <cnt> | Move (copy) memory |
| MS <from> <to> <val> | Search pattern in memory |
| MT [<opts>] <start> <end> [<runs>] | Memory test |
| NBOOT [<opts>] | Boot from network |
| NDL [<opts>] | Update Flash from network |
| NETSTAT | Show current state of networking parameters |
| PCI | PCI probe |
| PCIC <dev> <addr> [<bus>] [<func>] [<val>] | PCI config register change |
| PCID[+] <dev> [<bus>] [<func>] | PCI config register dump |
| PCIR | List PCI resources |
| PCI-VPD[-] <devNo> [<busNo>] [<capId>] | PCI Vital Product Data dump |
| PFLASH <D> <O> <S> [<A>] | Program Flash |
| PGM-XXX <args> | Media copy tool |
| PING <host> [<opts>] | Network connectivity test |
| RELOC | Relocate MM to RAM |
| RST | Cause an instant system reset |
| RTC[-xxx] [<arg>] | Real time clock commands |
| S [<addr>] | Single step user program |
| SERDL [<passwd>] | Update Flash using YModem protocol |
| SETUP | Open interactive Setup menu |
| UNZIP src size [<opt>] [<dest>] [<size>] | Unzip memory zipped by *gzip* |
| USB [<bus>] | Init USB controller and devices on a USB bus |
| USBT [<bus> <p1>..<p5>] | Shows the USB device tree |
| USBDP [<bus p1..p5>] [-d<x>] | Display/modify USB device path |

# 4 Organization of the Board

To install software on the board or to develop low-level software it is essential to be familiar with the board's address and interrupt organization.

## 4.1 Memory Mappings

***Table 28.*** *Memory map – processor view*

| CPU Address Range | Size | Description |
|---|---|---|
| 0x 0000 0000..End of RAM | 512/1024/ 2048 MB | SDRAM |
| 0x 8000 0000..DFFF FFFF | 1536 MB | PCIe Memory Space |
| 0x E000 0000..E7FF FFFF | 128 MB | PCI1 Memory Space |
| 0x E800 0000..EFFF FFFF | 128 MB | PCI2 Memory Space |
| 0x F000 0000..F00F 0000 | 128 MB | CCSR |
| 0x F200 0000..F200 3FFF | | Config PLD |
| 0x F300 0000..F301 FFFF | | FRAM (opt.) |
| 0x F400 0000..F41F FFFF | | SRAM (opt.) |
| 0x FB00 0000..FBFF FFFF | 16 MB | PCIe I/O / ISA Space |
| 0x FC00 0000..FC00 7FFF | 32 KB | PCI1 I/O Space |
| 0x FF00 0000..FFFF FFFF | 16 MB | Flash |

***Table 29.*** *Address mapping for PCI*

| CPU Address Range | Interface | Mapped to PCI Space | Description |
|---|---|---|---|
| 0x 8000 0000..9FFF FFFF | PCIe | 0x 8000 0000..9FFF FFFF (MEM) | PCIe memory space (prefetchable BARs) |
| 0x A000 0000..DFFF FFFF | PCIe | 0x A000 0000..DFFF FFFF (MEM) | PCIe memory space (non-prefetchable BARs) |
| 0x E000 0000..E7FF FFFF | PCI1 | 0x E000 0000..E7FF FFFF (MEM) | PCI1 memory space |
| 0x E700 0000..EFFF FFFF | PCI2[1] | 0x E700 0000..EFFF FFFF (MEM) | PCI2 memory space |
| 0x FB00 0000..FBFE FFFF | PCIe | 0x 0000 0000..00FE FFFF (ISA) | PCIe ISA memory |
| 0x FBFF 8000..FBFF FFFF | PCIe | 0x 0000..7FFF (I/O) | PCIe I/O space |
| 0x FC00 0000..FC00 7FFF | PCI1 | 0x 8000..FFFF (I/O) | PCI1 I/O space |

[1] PCI2 not available for MPC8543.

## 4.2 Interrupt Handling

Interrupt handling is done via the 12 external interrupt lines of the CPU (IRQ[11:0]). While the IRQ lines 8 to 10 are used as PCI interrupt lines (see Table 31, Interrupt numbering assigned by MENMON, on page 59), the Ethernet function unit interrupt is routed to a dedicated interrupt line. The mapping is as follows:

***Table 30.*** *Dedicated interrupt line assignment*

| MPC854X IRQ Input | Function |
|---|---|
| IRQ0 | Ethernet |

***Table 31.*** *Interrupt numbering assigned by MENMON*

| MPC854X IRQ Input | PCI Interrupt Line | Function | Assigned Number (MENMON) |
|---|---|---|---|
| IRQ0 | PCIe_INTA | - | 0xF0 |
| IRQ1 | PCIe_INTB | FPGA | 0xF1 |
| IRQ2 | PCIe_INTC | - | 0xF2 |
| IRQ3 | PCIe_INTD | - | 0xF3 |
| IRQ8 | PCI_INTA | SATA | 0x8 |
| IRQ9 | PCI_INTB | 1st USB Controller (USB0/2) | 0x9 |
| IRQ10 | PCI_INTC | 2nd USB Controller (USB3/4/5) | 0xA |

## 4.3 SMB Devices

***Table 32.*** *SMB devices*

| I²C Bus | Address | Function |
|---|---|---|
| 0x0 | 0x5E | LM81 hardware monitor |
| | 0xA2 | Real-time clock |
| | 0xA8 | CPU EEPROM |
| | 0xD2 | Clock generator |
| 0x1 | 0xAC | ID EEPROM |

## 4.4 Onboard PCI Devices

***Table 33.*** *Onboard PCI devices*

| Interface | Bus | Device | Vendor ID | Device ID | Function | Interrupt |
|---|---|---|---|---|---|---|
| PCI1 | 0x00 | 0x00 | 0x1057 | 0x0013 | PCI host bridge in MPC854X | - |
| | | 0x10 | 0x1095 | 0x3114 | SATA | PCI_INTA (IRQ8) |
| PCI2 | 0x01 | 0x00 | 0x1057 | 0x0013 | PCI host bridge in MPC854X | - |
| | | 0x11 | 0x1033 | 0x0035/ 0x00E0 | 1st USB Controller (USB0/2) | PCI_INTB (IRQ9) |
| | | 0x12 | | | 2nd USB Controller (USB3/4/5) | PCI_INTC (IRQ10) |
| PCIe | 0x02 | 0x00 | 0x1957 | 0x0013 | PCIe bridge in MPC854X | - |
| | 0x03 | 0x00 | 0x12D8 | 0x0404 | PCIe switch for CompactPCI bus | - |
| | 0x04 | 0x01 | 0x12D8 | 0x0404 | | |
| | | 0x02 | | | | |
| | | 0x03 | | | | |
| | 0x05 | 0x00 | 0x1A88 | 0x4D45 | FPGA (if implemented) | PCIe_INTB (IRQ 1) |
| | 0x06 | 0x00 | 0x12D8 | 0xE110 | PCIe bridge (CompactPCI bus) | - |

# 5 Appendix

## 5.1 Literature and Web Resources

- F50P data sheet with up-to-date information and documentation:
  www.men.de/products/02F050P.html

### 5.1.1 PowerPC

- MPC8548:
  MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual
  MPC8548ERM; 2007; Freescale Semiconductor, Inc.
  www.freescale.com

### 5.1.2 SATA

- Serial ATA International Organization (SATA-IO)
  www.serialata.org

### 5.1.3 USB

- USB:
  Universal Serial Bus Specification Revision 1.0; 1996; Compaq, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC, Northern Telecom
  www.usb.org

### 5.1.4 Ethernet

- ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE
  www.ieee.org
- Charles Spurgeon's Ethernet Web Site
  Extensive information about Ethernet (IEEE 802.3) local area network (LAN) technology.
  www.ethermanage.com/ethernet/
- InterOperability Laboratory, University of New Hampshire
  This page covers general Ethernet technology.
  www.iol.unh.edu/services/testing/ethernet/training/

### 5.1.5 CompactPCI

- CompactPCI Specification PICMG 2.0 R3.0:
  1999; PCI Industrial Computers Manufacturers Group (PICMG)
  www.picmg.org
- PCI Local Bus Specification Revision 2.2:
  1995; PCI Special Interest Group
  P.O. Box 14070
  Portland, OR 97214, USA
  www.pcisig.com

### 5.1.6 CompactPCI PlusIO

- CompactPCI PlusIO Specification PICMG 2.30 R1.0: 2009; PCI Industrial Computers Manufacturers Group (PICMG) www.picmg.org
- Introduction to CompactPCI PlusIO on Wikipedia: en.wikipedia.org/wiki/CompactPCI_PlusIO

## 5.2 Finding out the Board's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or hardware revisions of the F50P. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

***Figure 5.*** *Label giving the board's article number, revision and serial number*