# Tutorial for Altera DE1 and Quartus II

#### Qin-Zhong Ye

#### December, 2013

This tutorial teaches you the basic steps to use Quartus II version 13.0 to program Altera's FPGA, Cyclone II EP2C20 on the Development & Education Board DE1. One can also use it as a simplified user manual.

Some screen prints are taken from Quartus II version 9 and therefore may be slightly different from that of Quartus II version 13.0.

#### Contents

1.	Create a new project	2
2.	Copy VHDL files and the assignment file for DE1	9
3.	Create a new schematic file	9
4.	Open an existing VHDL file and add it to a project	. 13
5.	Create a symbol for a VHDL file	. 16
6.	Importing symbols to the schematic file	. 18
7.	Importing assignments	. 21
8.	Importing input and output symbols	. 23
9.	Connect symbols in a schematic	. 26
10.	Connect individual signals to a bus	. 27
11.	Specify the unused pins setting	. 30
12.	Compilation	. 33
13.	Programming FPGA Chip	. 34
14.	Viewing implementation logic	. 36
15.	Checking the problem with pin assignment	. 37
16.	How to update a symbol after making changes to signal names	. 39
17.	What to do after add/remove input/output signals in a VHDL file	. 41
18.	How to create a VHDL file for the schematic file	. 42
19.	How to copy a project	. 43
20.	How to change top-level entity	. 44
21.	How to change revision name	. 45
22.	How to use In-System Sources and Probes Editor	. 48
23.	How to install USB driver	. 54

#### 1. Create a new project

(Notice that you should create a working directory in the local disk (e.g., D:\) of the PC before creating a new project.)



Click "Create a New Project".

New Project Wizard: Introduction
The New Project Wizard helps you create a new project and preliminary project settings, including the following:
<ul> <li>Project name and directory</li> <li>Name of the top-level design entity</li> <li>Project files and libraries</li> <li>Target device family and device</li> <li>EDA tool settings</li> </ul>
You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.
C Don't show me this introduction again
< Back Next > Finish Avbryt

Click "Next".

New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5]	×
What is the working directory for this project?	
C:\altera\91sp2\quartus\bin	
What is the name of this project?	
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	
Use Existing Project Settings	
Dise Existing Project Settings	
< Back Next > Finish Avbryt	

Change the working directory name to your own working directory name. A working directory in the local drive (e.g., D:\) of the PC is preferred.

New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5]	-
Author in the condition discovery for this provide 12	
What is the working directory for this project? D:\TNGE15_lab1	
What is the name of this project?	
Counter_example	
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	
Counter_example	
Use Existing Project Settings	
	_
< Back Next > Finish Cancel	

Fill in the name of your project. Click "Next".

Quartus	: 11
♪	Directory "E:/Arbets/teaching/Altera/Sche_VHDL_projects/Tutorial_counter" does not exist. Do you want to create it?
	Ja Nej

Click "Ja".

New Project	Wizard: Add Files	[page 2 of 5	]				×
Select the d project direc	esign files you want to in tory to the project. Note:	iclude in the proj you can always	ect. Click A add desigr	dd All to add al n files to the pro	l design fil ject later.	es in the	
File name:						Add	
File name		Туре	Library	Design entry/s	y	Add All	
						Remove	
						Properties	
						Up	
						Down	
<					>		
Specify the	path names of any non-c	lefault libraries.	Use	er Libraries			
							_
		< Back	Next	> Fini:	sh	Avbryt	

If there is no design file (e.g. schematic or VHDL files) to add, click "Next".

Device family     Show in 'Available device' list       Family:     Cyclone II   Package: Any													
Family: Ucione II	Package:	Ar	у У	•									
Devices: All	Pin count:	Ar	у.	•									
Target device Speed grade: Any													
C Auto device selecte	d by the Fitter			Show a	idvance:	devices							
<ul> <li>Specific device sele</li> </ul>	cted in 'Availa	able devices	' list	HardCo	py comp	atible only							
Available devices:		L.F.	[111]		<b>F</b> ach and		- 10						
Name EP2C20AF484A7	Core v 1.2V	LEs 18752	User I/. 315	<u>Memor</u> 239616	Embed 52	I PLL 4							
EP2C20AF48418	1.2V	18752	315	239616	52	4							
EP2C20F256C6	1.2V	18752	152	239616	52	4							
EP2C20F256C7	1.2V	18752	152	239616	52	4							
EP2C20F256C8	1.2V	18752	152	239616	52	4							
EP2C20F256I8	1.2V	18752	152	239616	52	4							
EP2C20F484C6	1.2V	18752	315	239616	52	4							
EP2C20F484C7	1.2V	18752	315	239616	52 52	4	•						
<	1 /11		216	, , , , , , , , , , , , , , , , , , ,	)	4	>						
- Companion device													
							_						
HardCopy:													
HardCopy:		✓ Limit DSP & RAM to HardCopy device resources											

If the selected device is EP2C20F484C7, click "Next".

Tool name:	//Synthesis	<b>•</b>
Format:		
	I tool automatically to synthesize the current design	
Simulation – Tool name:	(None)	•
Format:		
	<ul> <li>e-level simulation automatically after compilation</li> </ul>	_
Tinin And		
Timing Analy Tool name:		•
Format:		-
	tool automatically after compilation	

Click "Next".

New Project Wizard: Summary [page 5 of 5]										
When you click Finish, the projec	at will be created with the following settings:									
Project directory:										
E:/Arbets/teaching/Altera/So	che_VHDL_projects/Tutorial_counter/									
Project name:	Counter_example									
Top-level design entity:	Counter_example									
Number of files added:	0									
Number of user libraries added:	0									
Device assignments:										
Family name:	Cyclone II									
Device:	EP2C20F484C7									
EDA tools:										
Design entry/synthesis:	<none></none>									
Simulation:	<none></none>									
Timing analysis:	<none></none>									
Operating conditions:										
Core voltage:	1.2V									
Junction temperature range:	0-85 °C									
		_								
	<back next=""> Finish Avbryt</back>									

Click "Finish".

#### 2. Copy VHDL files and the assignment file for DE1

Use Windows Explorer to copy all files in the directory

"S:\TN\E\094\_Digitalteknik\_och\_konstruktion\VHDL\_and\_assignment\_files" to your project directory.

#### 3. Create a new schematic file

🐇 Quartus II - E:/Arbets/teaching/Altera/Sche_VHDL_projects/Tutorial_counter/Counter_example - Counter_example 📃 🖃	×
File Edit View Project Assignments Processing Tools Window Help	
🗋 🗅 😂 🖬 🕼 🖉 🔗 🗠 🔽 Counter_example 💽 💢 🖉 🏈 🚳 🕨 🕨 🧐 🏷 😓 🕹 🔞	
Project Navigator	
Entity Enterna	
Cyclone II: EP2C20F48      Quartus II Software      New Tool!	
Purchase Quartus® IL Compare Altera®	
Download Software Get a Nios® II Devices	
Free 30-day Trial Limited Time Offer	
+ Buy Now	
QUARTUS <sup>®</sup> II	
Version 9.1	
VC131011 3.1	
View Quartus II	
Information	
Documentation	
× Type Message	
	_
🖇 System Λ Processing λ Extra Info λ Info λ Warning λ Critical Warning λ Error λ Suppressed λ Flag /	
System & Processing & Extra Info & Info & Warning & Critical Warning & Error & Suppressed & Flag /         Wessage:         Image:         Image:	
For Help, press F1	

Select "File > New ..."



Select "BlockDiagram/Schematic File" and click "OK".



Select "File > Save as …" to change the file name to a new name. This file name of the schematic will be used as the "top-level design entity" name of your whole design. You should choose the same name as the name of "top-level design entity". However, please notice that the file name for the schematic **cannot** be the same as any entity name in the VHDL codes.

Save As						
Spara i:	Count Tutorial_count	er	•	🕂 🔁 I		
à	🛅 db					
Senast använda dokument						
B						
Skrivbord						
6						
Mina dokument						
<b>I</b>						
Den här datorn						
<b></b>						
Mina nätverksplatser	Filnamn:	Counter_example			•	Spara
	Filformat:	Block Diagram/Schematic	File (*.bdf)		•	Avbryt
		Add file to current project	x			

Click "Spara". Notice that the file name "Counter\_example" should be the same as the "top-level design entity" name.

#### 😍 Quartus II - E:/Arbets/teaching/Altera/Sche\_VHDL\_projects/Tutorial\_counter/Counter\_example - Counter\_example - [Counter\_example.bdf] 🔀 File Edit View Project Assignments Processing Tools Window Help **- - X** 🗅 😅 🖬 🎒 👗 🖻 💼 🗠 👓 Counter\_example 🔄 💥 🖉 🎯 🕸 🕨 🕨 🕫 🏷 🐚 😓 🕘 👱 🙆 - **x** Project Navigator 🕆 Counter\_example.bdf Entity Cyclone II: EP2C20F48... **.** 💷 🔹 Counter\_... 🌆 4 Đ Öppna Leta i: C Tutorial\_counter 💌 🔶 🖻 + <u>ب</u> 🗀 db 📸 Counter\_example Ò Senast använda dokument Æ Skrivbord $\bigotimes$ Mina dokument Den här datorn • 🛆 🖻 🗗 Mina nätverksplatser Öppna > • Filnamn Type Message Filformat: Device Design Files (\*.tdf;\*.vhd;\*.vhd);\*.v;\*.vlg;\* Avbryt Add file to current project Open as: Auto -System / Processing / Extra Info / Info / Warning / Critical Warning / Error / Suppressed / Flag / Message: Locate For Help, press F1 Idle 🛃 Start 🔰 🔒 2 Client... 🔻 👽 2 Client... 🔻 🔯 2 Micro... 🔹 🕎 Tutorial\_... 😻 Quartus ... DE1\_tuto.. 🖄 Adobe A. 🥔 Seagate SV 🔇 11:04

#### 4. Open an existing VHDL file and add it to a project

Select "File > Open...". Find the VHDL file and click "Öppna".

Notice that you should have already copied all files in the directory

"S:\TN\E\094\_Digitalteknik\_och\_konstruktion\VHDL\_and\_assignment\_files" to your project directory.

😵 Quartus II - E:/Arbets/teachir				_counter/	Counte	r_exam	ple - C	ounte	er_exa	mple	- [Count	er_exa	ample.I	odf]		- 7 🛛
🚰 File Edit View Project Assignm					• 0	niðe 📣				l ber	-Tu   🛌	A	100	• 6		_ @ ×
Project Navigator ×		Counter_example		• 🗙	2 🧐	• 🧇 🍪	•		V 10	0°	⊕   <del>"</del> .	٩	۹ 🍜	<u>-</u> 0		
Entity	📸 Coun	ter_example.bdf														
Ensy → Cyclone II: EP2C20F48 → Counter 200																
		<														>
× Type Message																
System (Processing) Extra In	fo λ Info λ		Warning 入 E	rror λ Sup	pressed	λ Flag ,	1								~	Locate
For Help, press F1									111, 1:	15	\begin{bmm} b = 1 \end{bmm} bm			Idle		
🛃 Start 🛛 🔒 2 Client	2 Clier	t 👻 🙆 2 Micro	• 🗐 1	utorial		Quartus .	. 0	👌 Tuto	orial	~	Adobe A		🙆 Sea		SV	11:29
		1.								- <u>)</u>		1	11			

Select "Project > Add/Remove Files in Project ..." in the main toolbar.

Settings - Counter_example			×
Category:			
General Files Libraries Device	Files Select the design files you want to project directory to the project.	include in the project. Click Add All to	add all design files in the
Operating Settings and Conditions     Compilation Process Settings     EDA Tool Settings	File name:		Add
Analysis & Synthesis Settings	File name		gnientry/ Add All
<ul> <li>Fitter Settings</li> <li>Timing Analysis Settings</li> <li>Assembler</li> </ul>	Counter_example.bdf	Block Diagra <non< td=""><td>Remove</td></non<>	Remove
- Design Assistant - SignalTap II Logic Analyzer			Up
Logic Analyzer Interface			Down
Simulator Settings     Simulation Verification			Properties
Simulation Output Files PowerPlay Power Analyzer Settings SSN Analyzer			>
			OK Cancel

Click "Add All". (Notice that you should have already copied all files in the directory "S:\TN\E\094\_Digitalteknik\_och\_konstruktion\VHDL\_and\_assignment\_files" to your project

directory.) (Alternatively, you can also click "..." and navigate to your project directory and find the VHDL files.)

General	Files			
Files				
Libraries	Select the design files you want project directory to the project.	to include in the project. Click Ad	d All to add all desi	gn files in the
Device	project directory to the project.			
Operating Settings and Conditions				
⊩ Compilation Process Settings ⊩EDA Tool Settings	File name:			Add
- Analysis & Synthesis Settings	1			
- Fitter Settings	File name Counter27bit.vhd	Type Library VHDL File	Design entry/ <none></none>	Add All
Timing Analysis Settings	Seven_seg.vhd	VHDL File	<none></none>	Remove
- Assembler	Counter_example.bdf	Block Diagra	<none></none>	Homevo
- Design Assistant				Up
- SignalTap II Logic Analyzer				
- Logic Analyzer Interface				Down
- Simulator Settings				Properties
<ul> <li>Simulation Verification</li> </ul>				Fiopenies
Simulation Output Files				
PowerPlay Power Analyzer Settings				
SSN Analyzer				
	<		>	

The list shows that two VHDL files are added to your project. Click "OK".



## 5. Create a symbol for a VHDL file

Click the file symbol at the bottom of the Project Navigator. Double-click "Counter27bit.vhd" to open it.

(Alternatively, if you don't want to open the VHDL file, you can right-click on the file name "Counter27bit.vhd" in the file list and choose "Create Symbol files for Current file" in the pop-up menu.)

🍕 Quartus II - E:/Arbets/teaching	g/Altera/S	che_VHDL	_projects/T	utorial_cour	iter/Cou	nter_exam	ple - C	ounter	_exan	iple - [C	Counte	27bit.	vhd]		
🎨 File Edit View Project Assignme	nts Proces	sing Tools	Window Hel	þ											_ 8 ×
D 🛎 🛛 🦪 🖊 🕹 🛝 🖻 🖻	IC CI	Counter_	example	•	💢 🦉	🥝 🦁 🍪		► R	₹ ►⊗	<b>`</b> @ <b>@</b>	5	۵ 😔	D   👱	0	
Project Navigator 🛁 👻 🗙	😭 Cour	iter_example	.bdf		🌵 Co	ounter27bit.v	hd			1					
Files 	-	1 2	■Filna En 27	mn: Counte bitars ré	iknare	som kan									^
Counter_example.bdf	<b>서</b> 않 장	3 4 5	Nedde library	<pre>lning av : IEEE;</pre>	frekver	nsen från	osci	llato	rn me	d frei	kvens:	en 50	MHz		
	₩ ₩ ₩	6 7 8	use IEE	E.std_log: E.std_log: E.std_log:	ic_arit	h.all;									
	**	9 10 11	<pre>entity</pre>	Counter278 t(Clk: in	- Dit is										
		11 12 13 14	- ···		it23, d	clkbit24,	clkb	it25,	clkk	oit26:	out :	std_lo	ogic);		
	267 268 ab/ │	15 16	sub	cture beta type state	etype	is intege	r ran	ige O	to 13	42177	27;				
	<u> </u>	17 18 19	sig	nal state. nal Count					wnto	0);					
		20 21 22	beg												
		23 24 25			0 to :	134217726 7727 => n				(= stai	te +	1;			~
🛆 🗈 🗗		<													>
× Type Message															
System A Processing A Extra Inf	o λ Info λ	Warning )	∖ Critical Warni	ing λ Error λ	Suppress	sed ) Flag ;									
Message:	Locat	ion:												-	Locate
For Help, press F1								[	Ln 1, Co	ol 1	<u>_</u> •	>∭ [	ld	le	
🛃 Start 🛛 🕹 2 Client 🕞	🕜 2 Clie	nt 🔻 🚺	🧿 2 Micro	- 🖭 Tutoria	L	🐇 Quartus .	. (	🗿 Tutor	ial	🔁 Ad	dobe A	é	) Seagati	e	SV 🔇 11:50

Select "Processing > Analyze Current File".

Quartus	II 🔀
(į)	Flow Analyze Current File E:\Arbets\teaching\Altera\Sche_VHDL_projects\Tutorial_counter\Counter27bit.vhd was successful
	ОК

Click "OK".

Click "File > Create/Update > Create Symbol Files for Current File".

Quartus	II 🔀
(į)	Create Symbol File was successful
	ОК

Click "OK".

Perform the same operations (i.e., open file, analyze file, create symbol files) as above for the VHDL file "Seven\_seg.vhd".

#### 6. Importing symbols to the schematic file

Click "Counter\_example.bdf" to view the schematic file.

Double-click on the blank space of the Graphic Editor window or click on the AND-gate icon in the toolbar.

🔇 Quartus II - E:/Arbets/teaching/	Altera/Sche_VHDL_projects/Tutori	al_counter/Counter_examp	le - Counter_example - [Counter_	_example.bdf*] 💦 🖪 🛛
📸 File Edit View Project Assignmen	ts Processing Tools Window Help			
D 🛎 🖬 🕼   🎒   🅉 🖻 🏨	🖍 😋 Counter_example	💽 💥 🖉 🏈 🗞	🎯 🕨 🦻 🗠 🏷 🕒 💺	🖻 🐌 👱 🙆
Project Navigator X	📳 Counter_example.bdf*	Compilation Report	🕸 Counter27bit.vhd	😳 Seven_seg.vhd
Tiles  Tiles  Seven_seg.vhd  Tile  Counter_example.bdf	Symbol			
	Libraries:			
	MegaWizard Plug-In Manager			
				nter_examplegenerate_symbol=
System (16) Processing (4) (	- ()	tul. O errors, O warnings IWarning λ Error λ Suppresse		<u>«</u>
S Message: 0 of 10	Location:			Locate
For Help, press F1				
Start 8 2 Client to	🗸 🕜 2 Client to 👻 🙆 2 Microsof	🕞 🖳 Tutorial_cou 🛛 💘	Quartus II 🏼 🔄 Tutorial_cou	😕 Adobe Acro SV 🔇 13:59

Click the "+" sign to expand "Project" in the Libraries box.

Symbol	
Libraries: Project D bod7seg D counter27bit C c:/altera/91sp2/quartus/libraries	
Name:	
Repeat-insert mode	
Insert symbol as block	
Launch MegaWizard Plug-In	
MegaWizard Plug-In Manager	
OK Cancel	









The symbol for "Counter27bit" will appear in the Graphic Editor window. Move the symbol to a proper location and click the left mouse button. If the symbol continues to follow the mouse movement, click on the "Esc" button on your keyboard or click the right button of the mouse and select "Cancel".

Perform the same operations as above for the symbol "bcd7seg". Notice that the symbol name "bcd7seg" is the same as the entity name in the VHDL file "seven\_seg.vhd".



## 7. Importing assignments

You should use the assignment file "DE1\_pin\_assignments.csv" for your project. In this assignment file, input and output signal names are assigned to the pins of FPGA. These pins of FPGA are connected to various components on the printed circuit board. Click "Assignments > Import Assignments …" in the main toolbar.

Import Assign	ments	×
Specify the sour	ce and categories of assignments to import.	
File name:		Categories
🔽 Copy existing	g assignments into Counter_example.qsf.bak before impor	Advanced
	OK	Cancel

Click "..." to find the assignment file.

Select File					X
Leta i: Senast använda dokument Ekrivbord Mina dokument Den här datorn Mina nätverksplatser	Tutorial_count db Counter_examp DE1_pin_assign	ole.qsf			
	Filnamn: Filformat:	DE1_pin_assignments Import Files (*.qsf;*.esf;*.acf;	*.csv;*.txt;*.so	tc)	Öppna Avbryt

Click "Öppna".

Import Assign	nments		X
Specify the sou	rce and categories of assignments to impo	rt.	
File name:	E:/Arbets/teaching/Altera/Sche_VHDL_	projects/	Categories
🔽 Copy existin	ng assignments into Counter_example.qsf.b	ak before impor	Advanced
		ок	Cancel

Click "OK".



Click "Assignments > Pin Planner" in the main toolbar.

The content of the assignment file is shown in the lower part of the window. If you want to connect the output signals of the 7-segment decoder to the input signals of a 7-segment display on DE1, you should use the pre-defined output signal names in the Node Name column of the assignment editor. For example, HEX0[0], HEX0[1], ... HEX0[6] are the 7 output signals of the right-most 7-segment display on DE1. The input pins of the display are connected to 7 output pins of the FPGA chip. For each pre-defined signal name, you can find the corresponding pin of the FPGA chip in the column "Location". The 50 MHz oscillator on DE1 has a pre-defined input signal name CLOCK\_50 and it is connected to the pin "PIN\_L1" of the FPGA chip.

#### 8. Importing input and output symbols

Double-click on the blank space of the Graphic Editor window or click on the AND-gate icon in the toolbar.



Click the "+" sign to expand "c:/altera/13.0/quartus/libraries" in the Libraries box. You can expand the hierarchy as show in the follow window to find input and output symbols.

(Notice that you can also find the instructions for importing input and output symbols as in the tutorial "tut\_quartus\_intro\_schem.pdf".)



Click "OK".

The symbol will appear in the schematic. You can move the symbol by using the mouse. When the symbol is at the correct position, left-click to place the symbol. If the "repeat insert mode" is chosen, you can place several symbols. You can stop the repeated symbol placement by clicking "Esc" key on the keyboard.

Double-click on the symbol in the schematic, the following window is shown.

<b>Pin Properties</b>		×
General Format	1	
To create multi "name[30]"),	ple pins, enter a name in AHDL bus notation (for example, or enter a comma-separated list of names.	
Pin name(s):	HEX0[06]	
	OK Avbryt	

You should use these pre-defined names (e.g., HEX0[0], CLOCK\_50, etc.) as the pin names for input and output symbols. Since the output of the 7-segment decoder is a bus. The output symbol should also be a bus. Use the notation HEX0[0..6] as the pin name. Click "OK".



## 9. Connect symbols in a schematic

Click "Orthogonal Node Tool" (for a single signal) in the toolbar. Use the tool to connect the input CLOCK\_50 to the Clk input of Counter27bit.

Click "Orthogonal Bus Tool" (for a bus) in the toolbar. Use the tool to connect the output of the decoder to the output symbol.

#### 10. Connect individual signals to a bus

Connect the counter and the 7-segment decoder as shown in the following window.



#### Assign a name to a bus

Click the selection tool (Arrow) in the toolbar. Select the bus connected to the input of the 7-segment decoder. Right-click on the bus and select "Properties". The following window will appear.



Fill in a bus name (any name you like). Click "OK". Assign a name to a node (signal) line

Click the selection tool (Arrow) in the toolbar. Select the node (signal) line connected to the output of the counter. Right-click on the line and select "Properties". The following window will appear.

Node Properties	s	×
General Font	Format	
Name:	[b[3]	
🔲 Hide name i	in block design file	
	OK Avbryt	

Fill in a node (signal) line name which is connected to a single bit of the connected bus. For the output signal "clkbit26", the node line name is b[3]. Click "OK".

Assign node line names to the other 3 lines. The result is shown in the following window. Save the file.



## **11.** Specify the unused pins setting

Click "Assignments > Device ..." in the main toolbar, the "Device" window is shown.

Device family				Show in 'Availa	ble devices' li	st	
Eamily: Cyclo	ne II		• I	Pac <u>k</u> age:	Any		•
Devices: Al			-	Pin <u>c</u> ount:	Any		•
Target device				Sp <u>e</u> ed grade: Name filter:	Any		•
_	e selected by the Fi vice selected in 'Av		s' list	✓ S <u>h</u> ow adva	nced devices	HardCopy compatible only	۵
Other: n/a	1						
Available devices	:		De	evice and Pin (	ptions		
A <u>v</u> ailable devices Name	: Core Voltage	e LEs	User I		mory Bits	Embedded multiplier 9-bit	e *
-		e LEs 18752			mory Bits	Embedded multiplier 9-bit	€ ^
Name	Core Voltage		User I	/Os Me	mory Bits	-	€ ▲
Name EP2C20F256C8	Core Voltage	18752	<b>User I</b> , 152	/ <b>Os Me</b> 23961	mory Bits	52	¢ ^
Name EP2C20F256C8 EP2C20F256I8	Core Voltage	18752 18752	<b>User I</b> 152 152	/ <b>Os Me</b> 23961 23961	mory Bits 6 6	52 52	¢ ^
Name EP2C20F256C8 EP2C20F256I8 EP2C20F484C6	Core Voltage 1.2V 1.2V 1.2V 1.2V 1.2V	18752 18752 18752	User I, 152 152 315	/ <b>Os Me</b> 23961 23961 23961	<b>mory Bits</b> 6 6 6 6	52 52 52	•
Name EP2C20F256C8 EP2C20F256I8 EP2C20F484C6 EP2C20F484C7	Core Voltage 1.2V 1.2V 1.2V 1.2V 1.2V	18752 18752 18752 18752 18752	User I 152 152 315 315	23961 23961 23961 23961 23961	<b>mory Bits</b> 6 6 6 6	52 52 52 52 52	
Name EP2C20F256C8 EP2C20F256I8 EP2C20F484C6 EP2C20F484C7 EP2C20F484C8	Core Voltage 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V	18752 18752 18752 18752 18752 18752	User I, 152 152 315 315 315	23961 23961 23961 23961 23961	<b>mory Bits</b> 6 6 6 6	52 52 52 52 52	
Name EP2C20F256C8 EP2C20F256I8 EP2C20F484C6 EP2C20F484C7 EP2C20F484C8 ◀	Core Voltage 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V	18752 18752 18752 18752 18752 18752	User I, 152 152 315 315 315	23961 23961 23961 23961 23961	<b>mory Bits</b> 6 6 6 6	52 52 52 52 52	

Click "Device and Pin Option..." icon.

💱 Device and Pin Options - lab1_t2								
Category:								
General	General							
Configuration Programming Files	Specify general device options. These options are not dependent on the configuration scheme.							
Unused Pins Dual-Purpose Pins	Options:							
Capacitive Loading	Auto-restart configuration after error							
Board Trace Model I/O Timing	Release clears before tri-states							
Voltage	Enable user-supplied start-up clock (CLKUSR) Enable device-wide reset (DEV_CLRn)							
Pin Placement Error Detection CRC	Enable device-wide output enable (DEV_OE)							
CvP Settings Partial Reconfiguration	Enable INIT_DONE output							
	Auto <u>u</u> sercode							
	JTAG user code (32-bit hexadecimal): FFFFFFFF							
	In-system programming clamp state:							
	Delay entry to user mode:							
	Device initialization clock source:							
	Description:							
	Directs the device to restart the configuration process automatically if a data error is encountered. If this option is turned off, you must externally direct the device to restart the configuration process if an error occurs.							
	Reset							
	OK Cancel Help							

Select "Unused Pins" in "Category"



In the pull-down menu, select "As input tri-stated". Click "OK".

Click "OK" in the "Device" window.

#### 12. Compilation

Click "Processing > Start Compilation".

If the compilation is successful, the following window is displayed.

Quartus	II 🔀
٩	Full Compilation was successful (435 warnings)
	ОК

The large number of warnings is due to the unused node names in the assignment file.

Click "Assignments > Pins" in the main menu. Observe that the used pins are moved to the top of the list as shown in the following window.

*	Quartu	s    -	E:/Arbets/teaching/	Altera/Sche_VHDL_	projects/Tutorial_co	ounter/Counter_exa	mple - Counter	
File	Edit 1	View I	Processing Tools Wind	wob				
		Q	Groups				fop View - Wire Bond Ione II - EP2C20F484C7	
	_			<b>_</b>		•	report a report of an er si si si in in in	
	. et 🖻	• ₽2	2°20	Node Name	Direction	1950 V		
:23	1 III III		<u>₽</u>	HEX0[06]	Output Group	000000	000000000000000000000000000000000000000	
				< <new node="">&gt;</new>				
器	, 🔛 🏨	5 16	🔓 🎮 🛛			00000		
3	- - - - 					COSO YO	X ALL ALL ALL ALL ALL ALL ALL ALL ALL AL	
$\sim$		2					ACTION OF ACTION	
						000000X		
			<		>	22000	00000000000000000000000000000000000000	
						J	Capacity Capacity	
×	Named:	*	👻 «» Edit				Filter: Pins: all	•
Ť.		-	Node Name	Direction	Location	I/O Bank	VREF Group	I
	1		CLOCK_50	Input	PIN_L1	2	B2_N1	3.3-V -
	2	•	HEX0[0]	Output	PIN_J2	2	B2_N1	3.3-V
	3	ð	HEX0[1]	Output	PIN_J1	2	B2_N1	3.3-V
	4	0	HEX0[2]	Output	PIN_H2	2	B2_N1	3.3-V
	5	•	HEX0[3]	Output	PIN_H1	2	B2_N1	3.3-V
	6	•	HEX0[4]	Output	PIN_F2	2	B2_N1	3.3-V
	7	•	HEX0[5]	Output	PIN_F1	2	B2_N1	3.3-V
	8		HEX0[6]	Output	PIN_E2	2	B2_N1	3.3-V
ins	9		GPIO_0[0]	Unknown	PIN_A13	4	B4_N1	3.3-V 🐱
All Pins	<							>
_	Help, pre	= 1						

## **13. Programming FPGA Chip**

Check whether the AC/DC adapter and the USB cable are connected. Turn on the power of DE1 by pushing the red button on DE1.

Pile Edit Process	:/Arbets/teaching/Al	tera/Sche_VHDL_p	projects/Tutori	al_counter/Co	ounter_exan	nple - C	ounter		
🔔 Hardware Setu	p USB-Blaster (USB-0)		Mode: JTA	à	✓ Prog	ress:	(	0%	
	ISP to allow background p	rogramming (for MAX II	devices)			,			
🏓 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	S
📲 Stop	Counter_example.sof	EP2C20F484	001A9795	FFFFFFF					-
\mu Auto Detect	j								
🗙 Delete	1								
📛 Add File	1								
🎬 Change File	1								
💾 Save File	1								
😂 Add Device	1								
📲 Up	1								
📣 Down									
For Help, press F1	<								>

Click "Tools > Programmer" in the main toolbar.

Make sure the Mode is "JTAG". Click "Start". If "Start" is not clickable, as shown in the following window, click "Hardware Setup...".

🖺 Quartus II - [Cha	ain1.cdf]											X
	ssing Tools Window											
🔔 Hardware Setup	No Hardware				Mode:	JTAG		•	Progress:		0%	
Enable real-time I	SP to allow background prog	amming (for MAX II devi	ces)									
🟴 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
📲 Stop												
Auto Detect												
X Delete												
Add File												
🞬 Change File												
Save File												
Add Device												
1 Up												
🔑 Down												
For Help, press F1	J										NUM	

#### Click "Hardware Setup..." at the upper-left corner of the window.

dware Setup Hardware Settings JTAG Settin Select a programming hardware	setup to use whe		vices. This programming
hardware setup applies only to t Currently selected hardware: Available hardware items:	No Hardware No Hardware USB-Blaster [U		<b>-</b>
Hardware USB-Blaster	Server Local	Port USB-0	Add Hardware
	Local	0.000	Remove Hardware
			Close

In the pull-down menu for "Currently selected hardware", select "USB-Blaster[USB-0]". Click "Close". Now "Start" should be clickable. (Notice that USB driver for DE1 should have been installed. If it is not installed, follow the instructions in chapter 22, How to install USB driver.)

## 14. Viewing implementation logic



Click "Tools > Netlist Viewers > RTL Viewer". Quartus II - C/wort/Teaching/TNE094/Lab\_test/Lab1/Lab1\_t1 - Iab1\_t1 - [RTL Viewer]

Double click the symbols to expand "counter27bit" and "bcd7seg" to view details.
## Chapters 15 – 23 are not tutorial steps and may be used as a simple user manual.

## 15. Checking the problem with pin assignment

Note that this chapter is not a tutorial step. When you are looking for the reasons why you circuit does not work, you may need to read this chapter and check whether you have a problem with pin assignment.

One problem with the pin assignment in Quartus II version 13.0 is the setting for "Block Design Naming". After compilation of your schematic and VHDL codes with the schematic as the top-level design entity, you should find the names of the input and output signals which you have used in the schematic at the top of the node name list in Pin Planner. If you find that there are other signal names which are added into the node name list, it is an indication that the setting for "Block Design Naming" is causing a problem for the compilation. The synthesized circuit may not work properly. The in-system sources and probes may also be affected by this problem.

You can correct the setting for "Block Design Naming" as follows.

Click on "Assignment > Settings..." in the main toolbar, the following window is shown.

Category: Device	✓ Settings - lab_t3	
	Category:	Device
General       Files         Ubraries       Operating Settings and Conditors         Voltage       Specify options for analysis & synthesis. These options control Quartus II Integrated Synthesis and do not affect VQM or         Differentiate       Completion Process Settings         Early Timing Estimate       Specify options for analysis & synthesis. These options control Quartus II Integrated Synthesis and do not affect VQM or         Provemental Completion       Physical Synthesis Optimizations         EDA Tool Settings       Design Entry/Synthesis         Design Entry/Synthesis       Specify optione Optimization         PowerAlp Don't Care       Specify optive resynthesis         Design Entry/Synthesis Settings       PowerAlp Don't Care         Perform WYSIW/G primitive resynthesis       PowerAlp Don't Care         Design Assistant       Specify optive optimization:         Signal Tap I Logic Analyzer       Description:         Source Analyzer Interface       Description:         Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.         When Eight Performance with minimal logic usage.       Were Buy Software	Libraries Operating Settings and Conditions Voltage Temperature Compilation Process Settings Early Timing Estimate Incremental Compilation Physical Synthesis Optimizations EDA Tool Settings Design Entry/Synthesis Simulation Formal Verification Board-Level Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Fitter Settings TimeQuest Timing Analyzer Assembler Design Assistant SignalTap II Logic Analyzer Logic Analyzer Settings	EDIF netlists unless WYŚIWYG primitive resynthesis is enabled.  Optimization Technique Speed Balanced Area Iming-Driven Synthesis Power-Up Don't Care Perform WYSIWYG primitive resynthesis BowerPlay power optimization: Normal compilation More Settings  Description: Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

Click on "Analysis & Synthesis Settings" and the click on "More settings..." button. The following window is shown.

Setting:	
	•

Double-click on "Auto" of the setting "Block Design Naming". The pull-down menu will show 3 alternatives. Select "Quartus II" and click "OK" to close the window.

Compile your project again and check whether the synthesized circuit works. Note that the added names in the node name list might still be there in "Pin Planner". But they are not causing the problem. (If you notice any problems or errors with this part of text, please let me know.)

# 16. How to update a symbol after making changes to signal names

If you change the names of any input/output signals in a VHDL file, you should do the following steps:

Click "Processing > Analyze Current File" to check the modified VHDL code. View the schematic in Graphic Editor. Right-click on the symbol.



Select "Edit Selected Symbol" from the pull-down menu.

## Change the names of the signals

	🗠 😝 Counter_example	💌 💥 :	/ 🥝 🦁 🚸		r 🦻 👦	00	5	۲	20	
avigator 🔤 👻 🧃	Counter27bit.vhd	🚼 Co	unter_example.bo	lf		[	🗗 Cou	nter27bit	bsf	
slone II: EP2C20F484C7 Counter_example 2 Counter_Zbit:inst bcd7seginst1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Counter27bit Cik cikbt23 cikbit23 cikbit24 cikbit25 cikbit25									
				1						
e Kessage	ολ Infoλ Warningλ Critical Warning λ ₽ [Location:	∖Error λ Suppr	essed à Flag /							

Double-click on the name of the signal.

Port Properties	X
General Font Format	
Name: clkbit23	
Alias: << <same as="" name="" port="">&gt;</same>	
Hide alias when symbol is instantiated in design file	
Type: OUTPUT	
Default status: Used	
OK	ut (
	~

Change the signal name and click "OK". Save the file.

#### Update symbols

🔏 Quartus II - E:/Arbets/teac				er_example - Cou	inter_example	e - [Counter_example.	
File Edit View Project Assi	ignments Pro	cessing Tools Window					- 8 ×
] 🗅 🚅 🖬 🎒 🎒 👗 🖻		Counter_example	- 💥 🖌 🤇	3 🎯 🛞 👘 🕨	• 🖻 🗖 🙋	) 🚯 👗 🕘 📎 🛛	<u>e</u> 🙆
Project Navigator ×	🕸 Counti	er27bit.vhd	🔡 Counte	_example.bdf		Counter27bit.bsf	1
Entity							
△ Cyclone II: EP2C20F484C7				· · · · · · · · · · · · · · · · · · ·			
	<b>A</b>		Ct	unter27bit bj0		. bcd7seg	
who bcd7seg;inst1	Ð 🗌	PIN L1	50WEUT	Clk clkbit23 .b[1	і <u>)</u> ібізі.ці і	:	
	77			clkbit24 .b[2 clkbit25 .b[3		bcd[30] display[0	
	7 👬	· · · · <del>· · · · · · · · · · · · · · · </del>		clkbit26			
	¶ ⊕					inst1	
	A		in	st			
	4						
	12		· · · · · · · · · · · · · · · · · · ·				
	$\Box \circ$			K Cut	Ctrl+X		
	1)			Ва Сору	Ctrl+C		
				🔁 Paste	Ctrl+V		
			· · · · · · · · · · · · · · · · · · ·	X Delete	Del		
				Update Symbo	Lor Plock		
< >				Zoom	•		
		<		Show	•		×
				· .			
* Type Message				Insert			
				Open Sy <u>m</u> bol F	ile		
				Open AHDL I <u>n</u>	clude File		
System (Processing ) Extr	ralnfo )∖Info	$\lambda$ Warning $\lambda$ Critical	Warning $\lambda$ Error $\lambda$ Suppressed	} Flag /			
v2	<b>1</b>	pation:					▼ Locate
Cuts the selection and puts it on the C	Ilipboard				175, 326	ѷ₊∟→	
and the second design of the s		Client t 👻 🕒 2 M	4icroso 👻 🖑 Quartus II	🗀 DE1_tutorials	×		

Right-click in the blank space of the Graphic Editor and click "Update Symbol or Block...".



Click "OK".

## 17. What to do after add/remove input/output signals in a VHDL file

If you add/remove input/output signals in a VHDL file, you should create the symbol again by clicking "File > Create/Update > Create Symbol Files for Current File" and adding the new symbol to the schematic file.

## 18. How to create a VHDL file for the schematic file

Click "File > Create/Update > Create HDL Design File for Current File".

Create HDL Design	File for Curre	nt File 🛛 🔀
File type		
O VHDL	Add VHDL Sta	atements
C Verilog HDL		
File name: E:/Arbets/t	eaching/Altera/So	che_VHDL_proje
	OK	Cancel

Click "OK".

Notice that the created file is not added in the project since this file is not needed for compilation of your design. The VHDL file is useful if you want to move your design to another design tool or software.

If you want to view it, you can open this file by clicking "File > Open...".

Öppna		
Leta i:	Count Tutorial_count	ter 💌 🗲 🖻 📸 📰 -
Senast använda dokument Skrivbord	b Counter27bit counter_examp Counter_examp Seven_seg	le l
Mina dokument		
Den här datorn		
<b>S</b>		
Mina nätverksplatser	Filnamn:	counter_example
	Filformat:	Device Design Files (*.tdf;*.vhd;*.vhdl;*.v;*.vlg;*  Avbryt
		Add file to current project
	Open as:	Auto

Select the VHDL file "counter\_example" and click "Öppna".

The code is an example of the structural style VHDL code. There are 2 components, "bcd7seg" and "counter27bit", in the code.

## **19.** How to copy a project

It is possible to copy an existing project and give the copied project a new project name. The copied project can be further improved by adding new components and VHDL codes.

Click "Project->Project copy...". When the "Copy Project" window pops up, change the "Destination directory" and the "New project name" and click "OK".

Destination and easy and the river project name and energy of .
Copy Project
Destination directory: C:/work/Teaching/TNE094/Lab_test/Demo_2/
New project name: demo_2
Open new project. (This option closes the current project.)
OK Cancel

If the "Destination directory" does not exist, the following window pops up. Click "Yes".

Quartus II	X
<b></b>	Destination directory "C:/work/Teaching/TNE094/Lab_test/Demo_2/" does not exist. Do you want to create it?
	Yes No

## 20. How to change top-level entity

Sometimes, you need to change top-level entity before compiling the design. For example, after copying a project, if you click "File->Save As..." to change the file name of the schematic to a new name, you need to change the top-level entity.

Click "Assignments-> Settings...". Click "General".



Select an entity from the pull-down list for "Top-level entity". Some entity names in the list are the entity names in the VHDL codes. (Notice that entity names may be different from the VHDL file names!) There is also an entity name for the schematic in the list. The entity name is the same as the file name of the schematic. If the new entity name for the schematic is not in the list, you should change the top-level entity by typing the new entity name.

If you only want to compile a VHDL code, you can select the entity name of the entity in the VHDL code.

If you want to compile the whole design, you should select the entity name for the schematic.

### 21. How to change revision name

A revision name is used to set the output file names after compilation.



If you want to change the revision name, click "Project->Revisions...".

Revisions				X
Specify the currer revision, or edit th	nt revision for the ne description of a	project, create a revision.	a new revision, delete	e an existing
Revisions:				
Revision Na	Top-level En	Family	Device	Set Current
✓ demo_1_1	demo_2	Cyclone II	EP2C20F48	Create
				Delete
				Compare
				Customize
Description for re-	vision 'demo_1_1	':		
			ОК	Cancel

Click the button "Create...". In other versions of Quartus II, the window may also look like the following one. Click <<new revision>> to create a new revision.

Revision Name	Top-level Entity	Family	Device	Meet Timing	Timing Model	Set Current
✓ lab1_t2	lab1_t4		EP2C20F484C7	Piece rinning	Timing Plotter	
ab1_t1	lab1_t2		EP2C20F484C7			Delete
< <new revision="">&gt;</new>	-					Compare

	Create Revision
	Specify a name and description for the new revision. You can base the revision on an existing revision, and specify the revision as the current revision.
	Revision name:
1	Based on revision: demo_1_1
	Description:
	Created on: Tuesday, February 26, 2013 Based on : demo_1_1
1	🔽 Copy database
	Set as current revision
	OK Cancel

Fill in a new revision name and click "OK".

Revisions						
Specify the current revision for the project, create a new revision, delete an existing revision, or edit the description of a revision.						
Revisions:						
Revision Na	Top-level En	Family	Device	Set Current		
	demo_2 demo_2	Cyclone II Cyclone II	EP2C20F48 EP2C20F48	Create		
				Delete		
				Compare		
				Customize		
Description for revision 'demo_2_1' :						
Revision na Created on: Based on :		demo_2_1 Tuesday, demo_1_1	February 26,	2013		
			ОК	Cancel		

Click "OK".

Notice that, in the above window, if you want to delete the old revision, you can click the revision name in the list and click the button "Delete". All the output files of the revision will be deleted.

## 22. How to use In-System Sources and Probes Editor

The In-System Sources and Probes Editor in the Quartus II software allows you to easily control any internal signal and provides you with a completely dynamic debugging environment. You can get more information on the In-System Sources and Probes Editor from the Quartus II Handbook, Chapter 16 (Volume 3: Verification, Section IV: System Debugging Tools).

The In-System Sources and Probes Editor consists of the ALTSOURCE\_PROBE megafunction and an interface to control the ALTSOURCE\_PROBE megafunction instances during run time. Each ALTSOURCE\_PROBE megafunction instance provides you with source output ports and probe input ports, where source ports drive selected signals and probe ports sample selected signals. When you compile your design, the ALTSOURCE\_PROBE megafunction sets up a register chain to either drive or sample the selected nodes in your logic design. During run time, the In-System Sources and Probes Editor uses a JTAG connection to shift data to and from the ALTSOURCE\_PROBE megafunction instances.

#### Configuring the ALTSOURCE\_PROBE Megafunction

To use the In-System Sources and Probes Editor in your design, you must first instantiate the ALTSOURCE\_PROBE megafunction variation file. You can configure the ALTSOURCE\_PROBE megafunction with the MegaWizard<sup>™</sup> Plug-In Manager. Each source or probe port can be up to 256 bits. You can have up to 128 instances of the ALTSOURCE\_PROBE megafunction in your design.

To configure the ALTSOURCE\_PROBE megafunction, performing the following steps: 1. On the Tools menu, click MegaWizard Plug-In Manager.

🧐 MegaWizard Plug-In Manager [page 1]
Image: A construction of the second of th
Cancel     < Back     Next >     Finish

2. Select Create a new custom megafunction variation.

#### 3. Click Next.

🔇 MegaWizard Plug-In Manager [page 2a]		<b>—</b>
Which megafunction would you like to customize? Select a megafunction from the list below	Which device family will you be using? Which type of output file do you want to AHDL Verilog HDL Verilog HDL What name do you want for the output ff C:/Teaching/TNE094/Lab_test/Lab1_2/ Return to this page for another creat Note: To compile a project successfully in files must be in the project directory, in a the Options dialog box (Tools menu), or a of the Settings dialog box (Assignments n Your current user library directories are:	file?  te operation In the Quartus II software, your design I library specified in the Libraries page of a library specified in the Libraries page
	Cancel < E	Back Next > Finish

4. On page 2a of the MegaWizard Plug-In Manager, make the following selections:

a. In the Installed Plug-Ins list, expand the JTAG-accessible Extensions folder and select In-System Sources and Probes. (You can also verify that the currently selected device family matches the device you are targeting.)

b. Select an output file type and enter the **name** (for example, source\_probe1) of the ALTSOURCE\_PROBE

megafunction. You can choose AHDL (.tdf), VHDL (.vhd), or Verilog HDL (.v) as the output file type.

5. Click Next.

べ MegaWizard Plug-In Manager [page 3 of 5]	? 💌
🤄 In-System Sources a	nd Probes
Parameter     2 EDA     3 Summary     Settings	
source_probe1 probe[0] source[0]	Currently selected device family: Cyclone II Match project/default Do you want to specify an Instance Index? No, assign it automatically Yes, use this number The 'Instance ID' of this instance (optional): NONE How wide should the probe port be? How wide should the source port be? Advanced Options
	Cancel < Back Next > Finish

6. On page 3 of the MegaWizard Plug-In Manager, make the following selections:

a. Under Do you want to specify an Instance Index?, turn on Yes. This index determines the position of the instance in the list of instances of the In-System Sources and probes Editor. b. Specify the 'Instance ID' of this instance.

c. Specify the width of the probe port. The width can be from 0 bit to 256 bits.

d. Specify the width of the source port. The width can be from 0 bit to 256 bits.

7. On page 3 of the MegaWizard Plug-In Manager, you can click Advanced Options and specify other options, including the following:

■ What is the initial value of the source port, in hexadecimal? — Allows you to specify the initial value driven on the source port at run time.

■ Write data to the source port synchronously to the source clock — Allows you to synchronize your source port write transactions with the clock domain of your choice.

• Create an enable signal for the registered source port—When turned on, creates a clock enable input for the synchronization registers. You can turn on this option only when the Write data to the source port synchronously to the source clock option is turned on. 8. Click Next.

MegaWizard Plug-In Manager [page 4 of 5]	? <mark>*</mark>
in-System Sources a	and Probes
Parameter 2 EDA 3 Summary     Settings	
source_probe1	Simulation Libraries The megafunction does not have any simulation model files and can not be simulated Cancel Sack Next > Finish
9. Click Next.	
MegaWizard Plug-In Manager [page 5 of 5]	
In-System Sources a	and Probes
source_probe1	Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish
← probe[30] source[70] →	to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions. The MegaWizard Plug-In Manager creates the selected files in the following directory:
	C:\Teaching\TNE094\Lab_test\Lab1_2\
	File Description
	source_probe1.vhd         Variation file           source probe1.inc         AHDL Include file
	source_probe1.mc AnoL Include me     Visource_probe1.cmp VHDL component declaration file
	source_probe1.bsf Quartus II symbol file
	source_probe1_inst Instantiation template file
	Cancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish

10. Select (tick) soure\_probe1.bsf to create a Quartus II symbol file. The symbol can be imported to the schematic of your design. (Since the file "source\_probe1.vhd" is always created, you can also create the symbol for the VHDL file. See Chapter 5, Create a symbol for a VHDL file,", of this document.) 11. Click Finish.



12. Click Yes.

#### Import the created symbol to the schematic of your project

Follow the instructions in Chapter 6, Importing symbols to the schematic file, of this document.

#### **Compile the project**

Click "Processing > Start Compilation". See Chapter 12, Compilation, of this document.

#### **Program FPGA Chip**

Click "Tools > Programmer". See Chapter 13, Programming FPGA Chip, of this document.

#### **Running the In-System Sources and Probes Editor**

1. Open the In-System Sources and Probes Editor. Click "Tools >In-System Sources and Probes Editor".

If you have not programed FPGA chip, you should do Steps 2 - 5 to program FPGA chip. Otherwise, you can skip Steps 2– 5.

2. In the JTAG Chain Configuration pane, point to Hardware, and then select the hardware communications device. You may be prompted to configure your hardware; in this case, click Setup.

3. From the Device list, select the FPGA device to which you want to download the design (the device may be automatically detected). You may need to click Scan Chain to detect your target device.

4. In the JTAG Chain Configuration pane, click to browse for the SRAM Object File (.sof) that includes the In-System Sources and Probes instance or instances. (The .sof may be automatically detected).

5. Click Program Device to program the target device.

#### **Instance Manager**

The Instance Manager pane provides a list of all ALTSOURCE\_PROBE instances in the design and allows you to configure how data is acquired from or written to those instances. The following buttons and sub-panes are provided in the Instance Manager pane:

■ Read Probe Data—Samples the probe data in the selected instance and displays the probe data in the In-System Sources and Probes Editor pane.

• Continuously Read Probe Data—Continuously samples the probe data of the selected instance and displays the probe data in the In-System Sources and

Probes Editor pane; you can modify the sample rate via the Probe read interval setting.

• Stop Continuously Reading Probe Data—Cancels continuous sampling of the probe of the selected instance.

■ Write Source Data—Writes data to all source nodes of the selected instance.

■ Probe Read Interval—Displays the sample interval of all the In-System Sources and Probe instances in your design; you can modify the sample interval by clicking Manual.

• Event Log—Controls the event log in the In-System Sources and Probes Editor pane.

■ Write Source Data—Allows you to manually or continuously write data to the system. The status of each instance is also displayed beside each entry in the Instance Manager pane. The status indicates if the instance is Not running Offloading data, Updating data, or if an Unexpected JTAG communication error occurs. This status indicator provides information about the sources and probes instances in your design.

#### **In-System Sources and Probes Editor Pane**

The In-System Sources and Probes Editor pane allows you to view data from all sources and probes in your design. The data is organized according to the index number of the instance. The editor provides an easy way to manage your signals, and allows you to rename signals or group them into buses. All data collected from in-system source and probe nodes is recorded in the event log and you can view the data as a timing diagram.

#### **Reading Probe Data**

You can read data by selecting the ALTSOURCE\_PROBE instance in the Instance Manager pane and clicking Read Probe Data. This action produces a single sample of the probe data and updates the data column of the selected index in the In-System

Sources and Probes Editor pane. You can save the data to an event log by turning on the Save data to event log option in the Instance Manager pane.

If you want to sample data from your probe instance continuously, in the Instance Manager pane, click the instance you want to read, and then click Continuously read probe data. While reading, the status of the active instance shows Unloading. You can read continuously from multiple instances.

You can access read data with the shortcut menus in the Instance Manager pane.

To adjust the probe read interval, in the Instance Manager pane, turn on the Manual option in the Probe read interval sub-pane, and specify the sample rate in the text field next to the Manual option. The maximum sample rate depends on your computer setup. The actual sample rate is shown in the Current interval box. You can adjust the event log window buffer size in the Maximum Size box.

#### Writing Data

To modify the source data you want to write into the ALTSOURCE\_PROBE instance, click the name field of the signal you want to change. For buses of signals, you can double-click the data field and type the value you want to drive out to the ALTSOURCE\_PROBE instance. The In-System Sources and Probes Editor stores the modified source data values in a temporary buffer. Modified values that are not written out to the ALTSOURCE\_PROBE instance instances appear in red. To update the ALTSOURCE\_PROBE instance, highlight the instance in the Instance Manager pane and click Write source data. The Write source data function is also available via the shortcut menus in the Instance Manager pane.

The In-System Sources and Probes Editor provides the option to continuously update each ALTSOURCE\_PROBE instance. Continuous updating allows any modifications you make to the source data buffer to also write immediately to the ALTSOURCE\_PROBE instances. To continuously update the ALTSOURCE\_PROBE instances, change the Write source data field from Manually to Continuously.

#### **Organizing Data**

The In-System Sources and Probes Editor pane allows you to group signals into buses, and also allows you to modify the display options of the data buffer.

To create a group of signals, select the node names you want to group, right-click and select Group. You can modify the display format in the Bus Display Format and the Bus Bit order shortcut menus.

The In-System Sources and Probes Editor pane allows you to rename any signal. To rename a signal, double-click the name of the signal and type the new name.

The event log contains a record of the most recent samples. The buffer size is adjustable up to 128k samples. The time stamp for each sample is logged and is displayed above the event log of the active instance as you move your pointer over the data samples.

You can save the changes that you make and the recorded data to a Sources and Probes File (.spf). To save changes, on the File menu, click Save. The file contains all the modifications you made to the signal groups, as well as the current data event log.

### 23. How to install USB driver

USB blaster is the USB device on Altera's FPGA board, DE1. When DE1 is connected to a PC through a USB cable, the USB driver for USB Blaster should be installed. The USB driver can be found in the folder "\altera\91sp2\quartus\drivers\usb-blaster", if Quartus II version 9.1 is installed on the PC.

When DE1 is connected to a PC with **Windows XP**, a pop-up window "Found New Hardware Wizard" will be shown to guide the installation of the driver. See the details in the manual "Getting started with Altera DE1.pdf".

When DE1 is connected to a PC with **Windows Vista**, a pop-up window will be shown to guide the installation of the driver. Similar steps as for Windows XP should be done.

When DE1 is connected to a PC with **Windows 7**, no pop-up window will be shown. One should follow the following steps in "Manual for installation of Quartus II and USB driver for Windows 7" in "Manual\_install\_Quartus\_USBdriver\_Windows\_7.pdf" to install the USB driver.