ARINC

Interface for PC/104

CEI-420A

FEATURES

- Up to 16 input discretes or 8 Rx and 8 Tx ARINC 429 channels
- Intelligent interface with large buffers
- Full featured API included for Windows XP, 2000, Me, NT, 98, 95, Linux Kernel (2.4 and 2.6), Visual Basic, Labview, VxWorks and LabWindows/CVI
- Easy-to-use *BusTools*/ARINC Windows-based GUI bus analyzer available
- PC/104-Plus pass-through connectors available
- Up to 16 input and 8 output discretes
- High-performance processor
- Fully independent channel operation
- Support for ARINC 573 or 717 optional

Hardware

Available in a range of configurations to match your needs, the intelligent CEI-420A provides complete, integrated databus functionality for ARINC 429/575 and related avionics protocols in embedded PC/104 applications. The 420A supports maximum data throughput on all channels while providing on-board message scheduling, label filtering, multiple buffering options, timetagging and I/O discretes that handle avionics-level voltages. Ruggedized configurations with extended operating temperatures and a configuration with PC/104-Plus pass-through connector are optional.

Software

Condor software tools and solutions significantly reduce the time required to integrate ARINC 429 and other avionics protocols into your application. Included with the CEI-420A is our flexible, high-level, API (Application Programming Interface) support for Windows XP, 2000, Me, NT, 98, 95, Linux Kernel (2.4 and 2.6), VxWorks, Labview, LabWindows/CVI and Visual Basic. This powerful API supports multiple cards, and is compatible with Condor API support on PCI, PC/AT, CompactPCI and PCMCIA platforms. Optional software includes LabVIEW support and *BusTools*/ARINC, Condor's easy-to-use, Windows-based GUI solution for ARINC 429 analysis, simulation and data logging.

Architecture

Controlled by a powerful Intel 80960 CPU, the CEI-420 features independent channels, selectable data rates and parity, along with automatic slew rate adjustment. Other standard features include error detection, small PC/104 bus memory footprint and latching, keyed I/O connections. Up to sixteen input discretes support TTL to avionics-level voltages, while up to eight low-side switched output discretes can handle up to 0.5 ampere.

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ARINC

Interface for PC/104

CEI-420A

SOFTWARE FEATURES

On-board firmware, large data buffers and a high-level API are integrated to provide total flexibility in receiving and generating ARINC bus traffic. Filter data by label and/or SDI for each receive channel. Three different methods are provided to buffer received data: Buffered Mode utilizes a separate circular buffer for each channel; Merged Mode combines all received data into a single, time-sequenced circular buffer; and Dedicated Mode provides a snapshot of the very latest data. Transmit messages are automatically scheduled on-board or transmitted from a FIFO.

SPECIFICATIONS

ARINC 429 Receive Channels

- Number of channels: up to 8
- Data rates: 12.5 KHz or 100 KHz
- Standard input levels: ± 6.5 to ±13 VDC (A to B)
- Buffering: 2 KB per channel
- Parity: odd, even or none
- Error reporting: parity

ARINC 429 Transmit Channels

- Number of channels: 8
- Data rates: 12.5 KHz or 100 KHz
- Standard output level: ±10 VDC (A to B)
- Buffering: 2 Kbyte per channel
- Parity: odd, even or none

Software

- API - Includes high-level API for Windows XP, 2000, Me, NT, 98, 95, Linux Kernel (2.4 and 2.6), VxWorks, Labview, LabWindows/CVI and Visual Basic
  - Source code API library included
- GUI - Optional *BusTools*/ARINC GUI bus analyzer
- LabVIEW - Support optional

Additional Protocol Support

- ARINC 573/717 Bi-Polar RZ and Harvard Bi-Phase

Architecture

- Processor: Intel 80960
- RAM: 64 Kbyte dual-port SRAM
- 4 KB PC/104 bus memory footprint
- Uses 16-bit PC/104 bus signals
- PC/104-Plus pass-through connector optional

Physical / Environmental

- Standard PC/104 card size (3.7" x 3.5")
- Standard operating temperature: 0°C to +70°C
- Extended temperature range available
- Latching I/O connectors

Discrete Inputs

- Number of inputs: 8
- Supports avionics-level (open/gnd or high/low) and TTL/CMOS

Multi-purpose Discrete Input/Output Channels

- Number of outputs: 8
- Each channel can be individually configured as an input or output
- Low side switches, each capable of sinking 0.5 ampere

Power (typical)

- +5 VDC:750 mA
- +12 VDC:100 mA
- -12 VDC:80 mA

Warranty: 3 year limited hardware warranty

TOOLS

API Support

Flexible, high-level utility libraries for Windows XP, 2000, Me, NT, 98, 95, Linux Kernel (2.4 and 2.6), VxWorks, Labview, LabWindows/CVI and Visual Basic are included with the CEI-420A. Our easy-to use API (Application Programming Interface) speeds application development by providing simplified access to all configuration, initialization, transmit and receive functionality. Contact Condor for a copy of the API User Manual to see how this robust and flexible C programming interface can reduce development, integration and life cycle maintenance efforts. LabVIEW VI support is also available.

Bus Analysis

BusTools/ARINC is an easy-to-use, Windows XP, 2000, Me, NT, 98, 95-based ARINC 429 Bus Analysis/Simulation/Data Logging solution available on the CEI-200, 220, 420A, 520, 620, 715 and PA-100 products for PC/AT, PC/104, PCI, CompactPCI, and PCMCIA platforms. Monitor multiple channels in real-time. Display time-tagged data in hex, binary or engineering units (standard or custom). Filter received data by label and/or SDI. View discrete descriptors and user-bit-encoded values. Quickly create and display historical and real-time charts of individual labels. Record and playback data over transmit buses.

See our on-line Commercial Products Configuration Guide for available configurations.
http://www.condoreng.com

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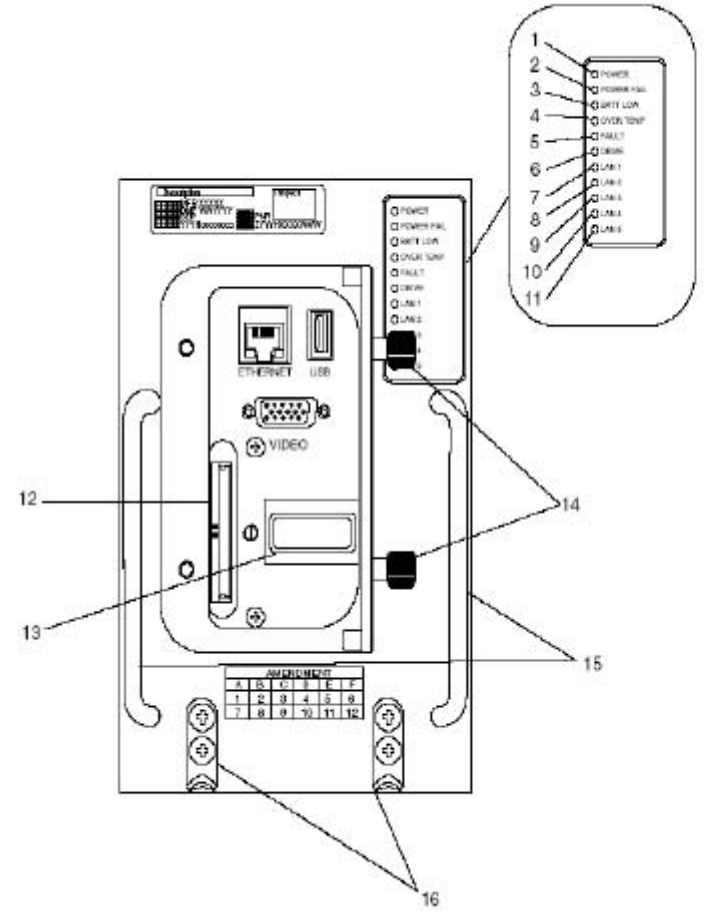
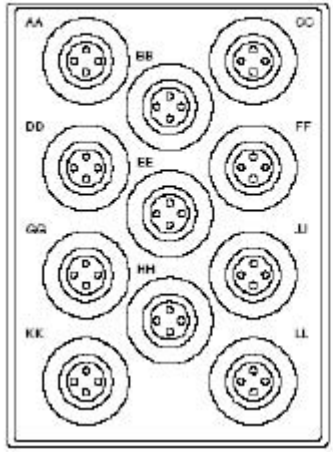


(FIGURE 5) INDEX NO.	CONTROL OR INDICATOR	FUNCTION
1	POWER Indicator	When lit, indicates AGS/CNSU is powered up.
2	POWER FAIL Indicator	When lit, indicates that loss of external power has been detected by the AGS/CNSU. (AGS/CNSU is operating under battery power.)
3	BATT LOW Indicator	When lit, indicates battery charge is low.
4	OVER TEMP Indicator	When lit, indicates an over temperature condition in the AGS/CNSU.
5	FAULT Indicator	When lit, indicates AGS/CNSU failed to boot.
6	DRIVE Indicator	When lit or blinking, indicates hard disk drive is being accessed.
7	LAN 1 Indicator	When lit or blinking, indicates activity on LAN 1 (rear panel connector section B-AA).
8	LAN 2 Indicator	When lit or blinking, indicates activity on LAN 2 (rear panel connector section B-BB).
9	LAN 3 Indicator	When lit or blinking, indicates activity on LAN 3 (rear panel connector section B-CC).
10	LAN 4 Indicator	When lit or blinking, indicates activity on LAN 4 (rear panel connector section B-DD/FF).
11	LAN 5 Indicator	When lit or blinking, indicates activity on LAN 5 (rear panel connector section B-GG/JJ).
12	Compact Flash Card Slot	Accepts Type I or Type II Compact Flash Card or Microdrive.
13	Hour Meter	Displays total number of hours AGS/CNSU has been in operation.
14	Access Door Latches	Rotated counterclockwise to unlatch access door. Rotated clockwise to latch door in closed position.
15	Handles	Used to assist in installation, removal, and transport of AGS/CNSU.
16	Hold-Down Hooks	Used to secure AGS/CNSU in equipment mounting tray.



The Server provides four separate Network Interface Controllers (NIC):

2x 10/100 BaseT (100Mb/s Ethernet)
(1 direct port, 2 ports via integrated Network Switch plus Front Panel connector, RJ-45)

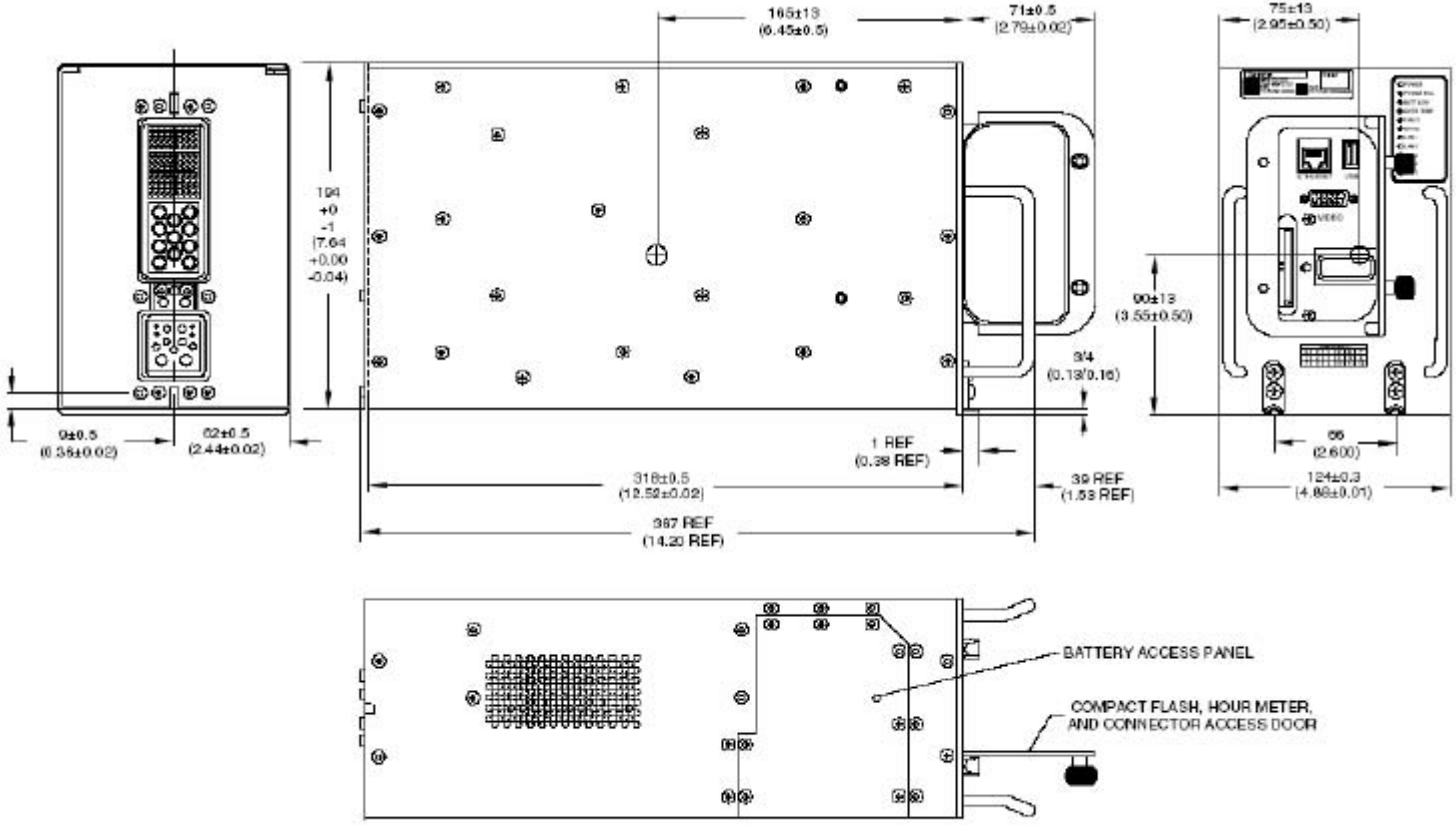
and

2x 1000 BaseT (Gigabit-Ethernet)

All Ethernet ports are autoranging.

Section B (Middle) of Rear Panel
ARINC 600 Type II Connector

PIN	SIGNAL	PIN	SIGNAL
Quadrax Section AA – 10/100BT_01			
1	TX+	3	TX–
2	RX+	4	RX–
Quadrax Section BB – 10/100BT_02			
1	TX+	3	TX–
2	RX+	4	RX–
Quadrax Section CC – 10/100BT_03			
1	TX+	3	TX–
2	RX+	4	RX–
Quadrax Section DD – 1000BT_01A Port 1			
1	Bidirectional Pair A+	3	Bidirectional Pair A–
2	Bidirectional Pair B+	4	Bidirectional Pair B–
Quadrax Section EE – No Connection			
Quadrax Section FF – 1000BT_02A Port 1			
1	Bidirectional Pair C+	3	Bidirectional Pair C–
2	Bidirectional Pair D+	4	Bidirectional Pair D–
Quadrax Section GG – 1000BT_01B Port 2			
1	Bidirectional Pair A+	3	Bidirectional Pair A–
2	Bidirectional Pair B+	4	Bidirectional Pair B–
Quadrax Section HH – No Connection			
Quadrax Section JJ – 1000BT_02B Port 2			
1	Bidirectional Pair C+	3	Bidirectional Pair C–
2	Bidirectional Pair D+	4	Bidirectional Pair D–
Quadrax Section KK – No Connection			
Quadrax Section LL – No Connection			



NOTE: Primary dimensions are in millimeters. Dimensions in parentheses are in inches.

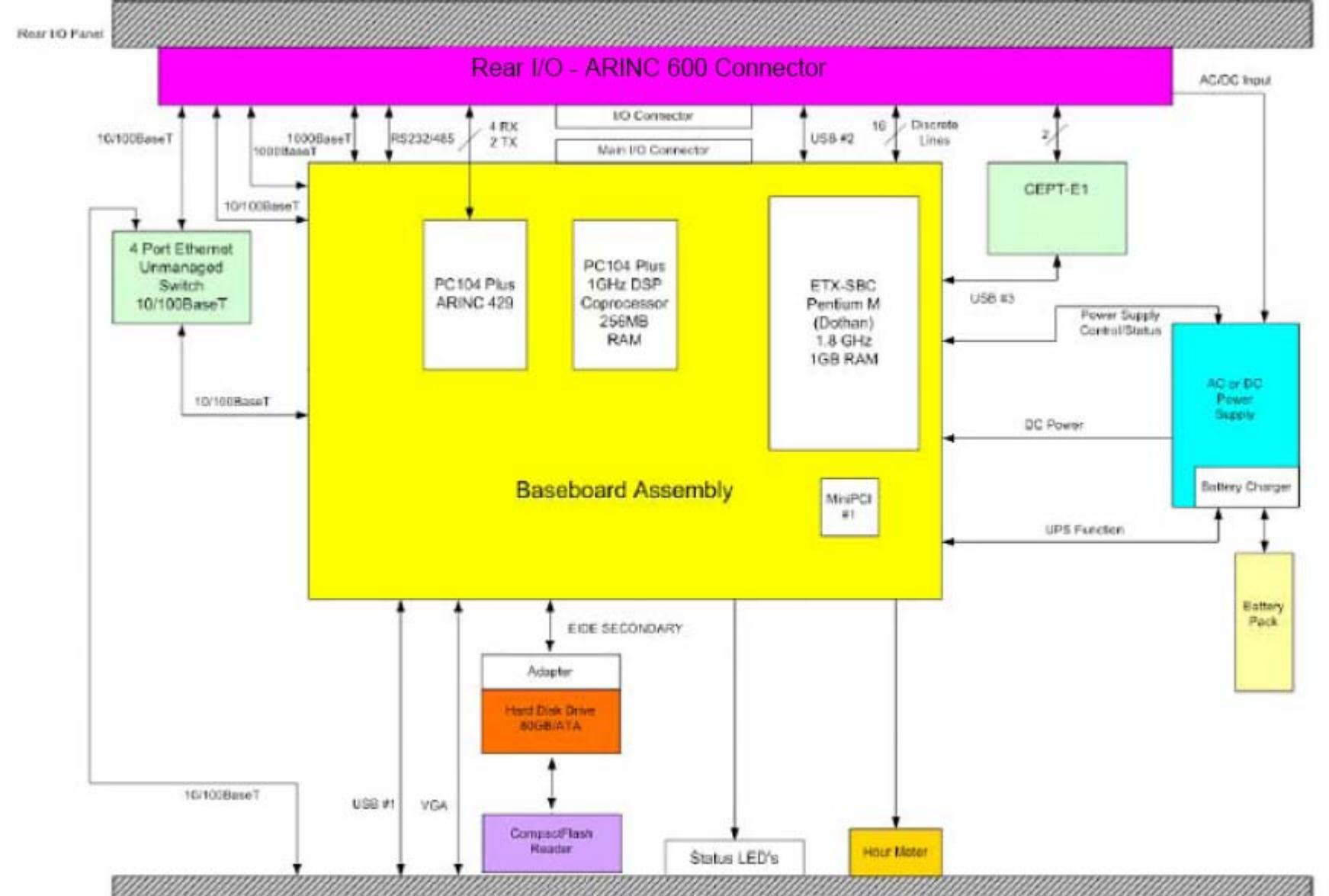
Compact Flash Card

The CF card is placed into the CNSU and holds the backup software and parameters.

In normal operation the **CNSU** operates from the internal Hard Disk.

Position

Note: It is mandatory to have the CF card installed to operate the CNSU


Rear I/O Panel
Rear I/O - ARINC 600 Connector
AC/DC Input
I/O Connector
Main I/O Connector
10/100BaseT
1000BaseT
1000BaseT
RS232/485
4 RX
2 TX
USB #2
16
Discrete
Lines
2
CEPT-E1
10/100BaseT
4 Port Ethernet
Unmanaged
Switch
10/100BaseT
PC104 Plus
ARINC 429
PC104 Plus
1GHz DSP
Coprocessor
256MB
RAM
ETX-SBC
Pentium M
(Dothan)
1.8 GHz
1GB RAM
USB #3
Power Supply
Control/Status
AC or DC
Power
Supply
10/100BaseT
DC Power
Baseboard Assembly
MiniPCI
#1
Battery Charger
UPS Function
Battery
Pack
EIDE SECONDARY
Adapter
Hard Disk Drive
80GB/ATA
10/100BaseT
USB #1
VGA
CompactFlash
Reader
Status LED's
Hour Meter

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A1	429_RX_01A (+)	C1	429_RX_02A (+)	E1	No Connection
A2	429_TX_01A (+)	C2	429_TX_02A (+)	E2	No Connection
A3	429_RX_03A (+)	C3	429_RX_04A (+)	E3	No Connection
A4	DIG_GND	C4	DIG_GND	E4	No Connection
A5	Reserved	C5	Reserved	E5	Reserved
A6	Reserved	C6	Reserved	E6	Reserved
A7	Reserved	C7	Reserved	E7	Reserved
A8	Reserved	C8	Reserved	E8	Reserved
A9	Reserved	C9	Reserved	E9	Reserved
A10	DISC_IN_01	C10	DISC_IN_03	E10	DISC_IN_05
A11	DISC_OUT_01	C11	DISC_OUT_03	E11	DISC_OUT_05
A12	No Connection	C12	No Connection	E12	No Connection
A13	Chassis Ground	C13	No Connection	E13	DIG_GND
A14	Chassis Ground	C14	No Connection	E14	Reserved
A15	Chassis Ground	C15	No Connection	E15	Reserved
B1	429_RX_01B (-)	D1	429_RX_02B (-)	F1	DIG_GND
B2	429_TX_01B (-)	D2	429_TX_02B (-)	F2	No Connection
B3	429_RX_03B (-)	D3	429_RX_04B (-)	F3	Reserved
B4	DIG_GND	D4	DIG_GND	F4	Reserved
B5	Reserved	D5	Reserved	F5	Reserved
B6	Reserved	D6	Reserved	F6	Reserved
B7	Reserved	D7	Reserved	F7	Reserved
B8	Reserved	D8	Reserved	F8	Reserved
B9	Reserved	D9	Reserved	F9	Reserved
B10	DISC_IN_02	D10	DISC_IN_04	F10	DISC_IN_06
B11	DISC_OUT_02	D11	DISC_OUT_04	F11	DISC_OUT_06
B12	No Connection	D12	No Connection	F12	No Connection
B13	Chassis Ground	D13	POWER_OFF_CTRL	F13	DIG_GND
B14	Chassis Ground	D14	POWER_OFF_RTN	F14	Reserved
B15	Chassis Ground	D15	DIG_GND	F15	Reserved

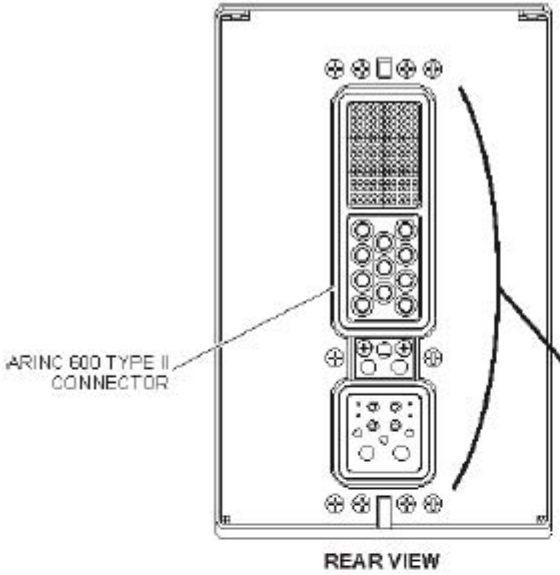
PIN	SIGNAL	PIN	SIGNAL
G1	Chassis Ground	J1	USB_+5V
G2	No Connection	J2	USB_RTN
G3	Reserved	J3	No Connection
G4	Reserved	J4	No Connection
G5	Reserved	J5	Reserved
G6	Reserved	J6	Reserved
G7	Reserved	J7	Reserved
G8	Reserved	J8	Reserved
G9	Reserved	J9	Reserved
G10	DISC_IN_07	J10	RS485_IN_01A (+)
G11	DISC_OUT_07	J11	RS485_OUT_01A (+)
G12	No Connection	J12	Reserved
G13	DIG_GND	J13	No Connection
G14	Reserved	J14	No Connection
G15	Reserved	J15	No Connection
H1	No Connection	K1	USB_DATA-
H2	No Connection	K2	USB_DATA+
H3	Reserved	K3	No Connection
H4	Reserved	K4	No Connection
H5	Reserved	K5	Reserved
H6	Reserved	K6	Reserved
H7	Reserved	K7	Reserved
H8	Reserved	K8	Reserved
H9	Reserved	K9	Reserved
H10	DISC_IN_08	K10	RS485_IN_01B (-)
H11	DISC_OUT_08	K11	RS485_OUT_01B (-)
H12	No Connection	K12	Reserved
H13	DIG_GND	K13	No Connection
H14	Reserved	K14	Chassis Ground
H15	Reserved	K15	Chassis Ground

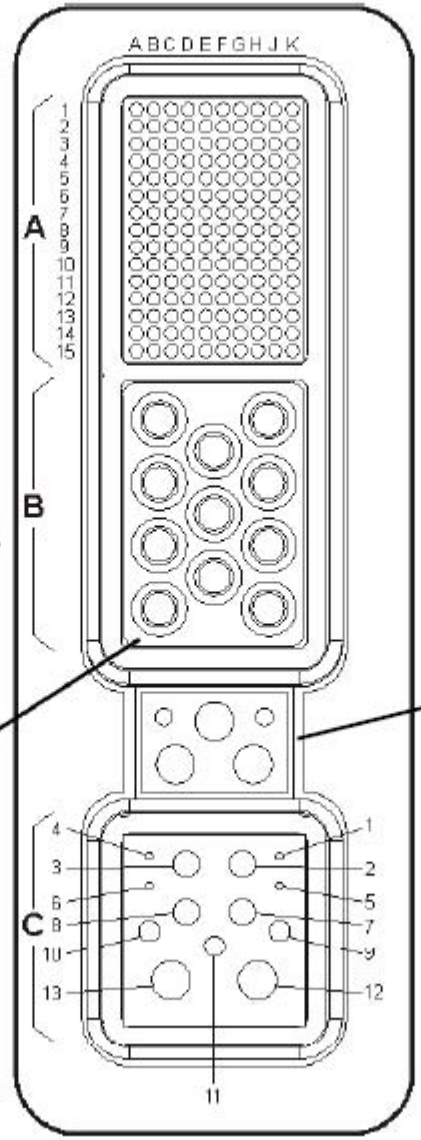
Section A (Top) of Rear Panel ARINC 600 Type II Connector

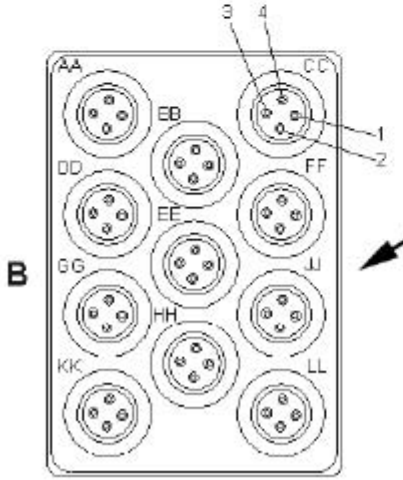
- ARINC 600 - 4 MCU Housing
- Intel™ Pentium®M 1.8 GHz
- 1 GB RAM
- 80 GB hard disk Drive
- 4 Ethernet ports
- One VGA Video Port (Shop Maintenance only)
- ARINC 429 & discrete I/O
- Linux operating system
- UPS capability

CHARACTERISTIC	SPECIFICATION
Nomenclature	AGS / CNSU, Z465H0000111
Processor	Intel™ Pentium®M 1.8 GHz
Memory (RAM)	1 GB
Data Storage	80 GB hard disk drive
Operating System	Linux
Battery	Rechargeable UPS battery operates AGS for 5 minutes upon loss of external AC power Non-Rechargeable CMOS- Battery (3.6 V Lithium) for storing basic settings
UPS battery Recharge Time	45 minutes
Input Power	97 – 134 VAC, 360 – 800 Hz, single phase, 100 W (140 VA) maximum
Size	19.4 cm (7.64") high x 13 cm (4.88") wide x 31.8 cm (12.52") deep (excluding handles and hold-down hooks)
Weight	5.445kg (12 pounds)
Temperature Range: Operating Non-operating	 -15°C to +55°C -55°C to +85°C
Altitude : Operating Non-operating	 Atmospheric Pressure Equivalent to 0 to 15,000 feet Atmospheric Pressure Equivalent to 0 to 40,000 feet
Humidity (operating)	20% to 90% relative humidity, non-condensing
Cooling: Air Flow Static Pressure Drop Inlet Air Temperature	 22 kg/hour supplied by external source 0.2 inches of water at 22 kg/hour air flow 40° C maximum

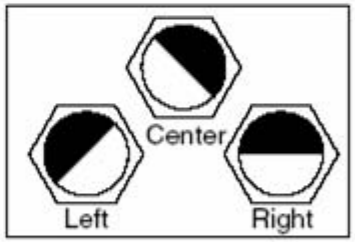
ARINC 600 Type II Connector







Key- section



Note: The dark part represents the key.

70050M5 - 800

120W MULTIPLE OUTPUT
PFC POWER SUPPLY (47 - 800Hz)

Providing six independent output voltages and up to 120W continuous output power, the **70050M5-800** is optimized for wide frequency (47 – 800Hz) operation. Nominal line efficiency exceeds 70% at ½ to full output load and the supply is capable of providing full load power during momentary input AC brown-out conditions for up to 50mSec. This time is expandable by inclusion of an external capacitor bank attached to a two-pin connector provided within the supply. Additionally, the supply houses an intelligent Nickel Cadmium battery charger and isolated low voltage DC/DC converter with the ability to operate for up to five minutes at full rated load from an external 24Vdc (20Vdc-30Vdc) battery.

Weighing less than 32 ounces, the **70050M5-800** is housed in an aluminum enclosure with outer dimensions of 7.25” x 5.00” x 1.40”. The top cover is perforated with two cover options: with or without recessed fan. The lower U-Chassis accepts five #4 screws to facilitate system mounting. Interconnection is accomplished with five Molex straight locking vertical connectors.

FEATURES

⋇	**Exceeds RTCA/DO-160E, section 16, and Airbus ABD0100.1.8, issue D for power factor and input current harmonic distortion levels over the wide operating frequency range of 360Hz to 8000Hz**
⋇	**Efficiency: 73% typical, ½ to full rated output load, nominal line (115Vrms)**
⋇	**Wide input range: 96Vrms – 134Vrms, 47Hz – 800Hz**
⋇	**Complies with RTCA/DO-160E, category M for conducted emissions and susceptibility**
⋇	**Active inrush current limiting: 7Apk**
⋇	**Size: 7.25” x 5.00” x 1.40”; weight: less than 32 ounces**
⋇	**Six standard outputs: +/-5V, +/-12V, 28Vdc, 24Vdc (battery charger)**
⋇	**Independent over current protection on each output**
⋇	**Built-in intelligent battery charger / operation from external 24Vdc battery**
⋇	**AC status line (TTL)**
⋇	**Output enable line (TTL)**

STANDARD OUTPUTS

PARAMETER	VALUE (TYPICAL)					
	+5.125V	+12V	-5V	-12V	+28V	+24Vbatt
Voltage Regulation	+/-2.5%	+/-5%	+/-5%	+/-5%	+/-5%	--
Output Current	10A	7A	1A	1A	300mA	600mA
Maximum Load	51W	84W	5W	12W	8W	16W
Minimum Load	1A	0	0	0	0	0
Pk-pk ripple + noise (20MHz)	100mVpp	120mVpp	50mVpp	120mVpp	120mVpp	120mVpp
Switched output	Yes	Yes	Yes	Yes	No	No
Over current trip-point	18A	7.5A	2.1A	2.1A	1A	600mA
Notes	(1), (4)	(2), (4)	(2), (4), (5)	(2), (4)	(2), (4)	(3), (4)

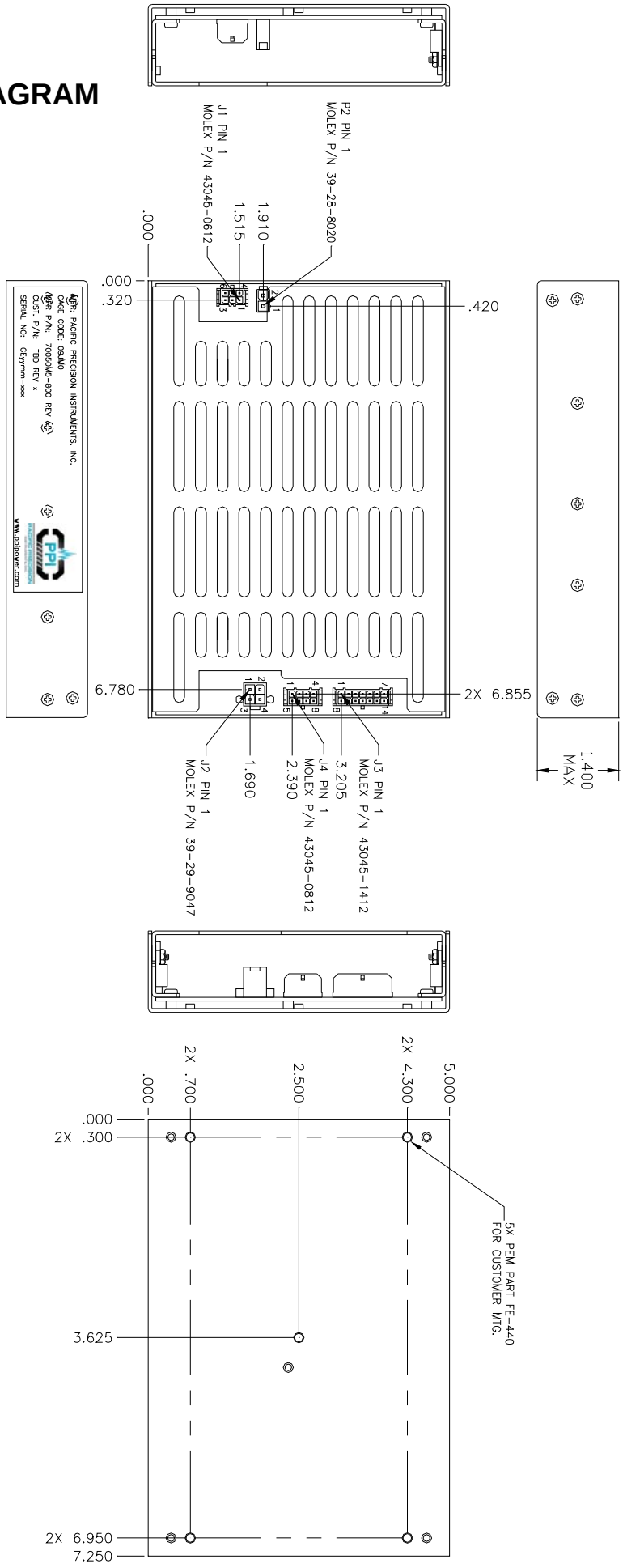
Notes:

1) Pulse-retry circuit limited to 3% duty cycle
2) Fold back current limited
3) 600mA constant current source
4) **Maximum supply (simultaneous) output power is limited to 120W using any combination of individual output current maximums provided.** A 5W minimum load is required on the 5V output in order to maintain proper cross-regulation.
5) -5V output voltage regulation is +/-5% for output current draw $\leq$ 750mA and is +/-10% for output currents > 750mA.

INTERCONNECTION

Connector	J1	J2	J3	J4	P2
Molex P/N Supply Side	**43045-0612**	**39-29-9047**	**43045-1412**	**43045-0812**	**39-28-8020**
1	AC Line	24Vbatt (+)	+5Vdc	Output Enable - H	+200Vdc
2	Chassis	24Vbatt (-)	+5Vdc	Battery Enable - H	+200V Return
3	AC Neutral	24Vbatt (+)	DC Return	Battery Low	
4	Chassis	24Vbatt (-)	+12Vdc	Ext Pwr Fail	`
5	Chassis		DC Return	+28Vdc	
6	Chassis		-12Vdc	DC Return	
7			DC Return	DC Return	
8			+5Vdc	DC Return	
9			DC Return		
10			DC Return		
11			+12Vdc		
12			DC Return		
13			-5Vdc		
14			DC Return		

MECHANICAL DIAGRAM



ELECTRICAL SPECIFICATIONS

UNLESS OTHERWISE SPECIFIED THE FOLLOWING TEST CONDITIONS APPLY: Ta=25°C. ACTIVE LOADS APPLIED TO OUTPUT, VIN=115Vrms, 400Hz, < 1.25% THD SINUSOID

INPUT CHARACTERISTICS

PARAMETER	*70050M5-800*	*REMARKS*
INPUT VOLTAGE RANGE	**96-134Vrms**	**COMPLIES WITH NORMAL/ ABNORMAL INPUT VOLTAGES PER RTCA/DO-160E, SECTION 16**
INPUT FREQUENCY RANGE	**360Hz – 800Hz. Exceeds RTCA/DO-160E and Airbus ABD0100.1.8, issue D for power factor and input current harmonic distortion levels over the wide operating frequency range for ½ to full output loading**	**OPERATES AT 47 – 360Hz WITH REDUCED DISTORTION PERFORMANCE**
LEAKAGE CURRENT	**< 5mA**	**AC LINE/NEUTRAL TO CHASSIS, @ 115Vrms / 400Hz**
INRUSH CURRENT	**< 7.0Apk**	**COLD START**
TOTAL HARMONIC DISTORTION (INPUT CURRENT)	**< 3.5% < 5.0%**	**1/2 TO FULL OUTPUT LOAD (60W-120W), 360Hz 1/2 TO FULL OUTPUT LOAD (60W-120W), 800Hz**
INDIVIDUAL HARMONICS, AC CLEAN, (Vthd < 1.25%)	**EVEN: < 1% I_f / n, (n<10) EVEN: <0.1% I_f (n ≥10) ODD: < 30% I_f / n ODD TRIPLENS: < 15% I_f / n**	**360-800Hz I_f = FUNDAMENTAL CURRENT Vthd ≤ 1.25%, n = 1 THRU 99, n = ORDER OF HARMONIC ½ TO FULL LOAD (60W-120W) DISREGARD HARMONIC CURRENTS < 5mArms**
INDIVIDUAL HARMONICS, DISTORTED INPUT, (Vthd > 10%)	**EVEN: < 1% I_f / n + Vn (n<10) EVEN: <0.1% I_f + Vn (n ≥10) ODD: < 30% I_f / n + Vn ODD TRIPLENS: < 15% I_f / n + Vn**	**360-800Hz Vthd ≥ 10%, n = 1 THRU 99, Vn = CORRESPONDING INPUT VOLTAGE HARMONIC n = ORDER OF HARMONIC ½ TO FULL LOAD (60W-120W) DISREGARD HARMONIC CURRENTS < 5mArms**
POWER FACTOR	**0.90 min**	**Pout > 50W**
CREST FACTOR (CURRENT)	**1.314 - 1.514**	**RATIO OF PEAK/ RMS**
START-UP TIME	**< 500mSec**	**OUTPUTS WITHIN REGULATION**
CONDUCTED EMISSIONS	**RTCA/DO-160E**	**CATEGORY M EQUIPMENT**
STORAGE TEMPERATURE RANGE	**-55°C TO +100°C**	**NON-OPERATIONAL**
OPERATING TEMPERATURE RANGE	**-25°C TO +70°C**	**REQUIRES EXTERNAL AIRFLOW TO ASSURE CASE TEMPERATURE DOES NOT EXCEED 100°C**
OUTPUT ENABLE - H	**TTL LEVEL, SECONDARY REFERENCED**	**DISABLES ALL OUTPUTS EXCEPT +28V and +24Vbattery WHEN ASSERTED LOW. REQUIRES 2.5V MIN LEVEL TO ENABLE SUPPLY OUTPUTS (NO INTERNAL PULL-UP PROVIDED). SHOULD BE PULLED HIGH THROUGH WITH A 33k - 68k RESISTOR ATTACHED TO 28V (CONTINUOUS) OUTPUT IF NOT USING OUTPUT ENABLE FUNCTION.**

OUTPUT CHARACTERISTICS

PARAMETER	70050M5-800	REMARKS
RATED OUTPUT POWER	120W	CONTINUOUS
RATED OUTPUT VOLTAGES		SEE "STANDARD OUTPUTS" TABLE
TEMPERATURE STABILITY COEF.	0.01% / °C	OUTPUT VOLTAGES
OUTPUT RIPPLE + NOISE (pk - pk)	< 1%	20MHz BANDWIDTH (EACH OUTPUT)
LINE REGULATION	< 0.5%	INDIVIDUAL OUTPUT DEVIATION FOR ± 20%, STEP CHANGE IN LINE VOLTAGE
LOAD REGULATION	OUTPUTS REMAIN WITHIN REGULATION	50% STEP CHANGE IN INDIVIDUAL OUTPUT LOAD
HOLD-UP TIME	50mSec MINIMUM	AT FULL 120W LOAD. REQUIRES EXTERNAL 250V RATED ELECTROLYTIC CAPACITORS CONNECTED TO P2, OR OPERATION FROM 24V BATTERY, FOR EXTENDING HOLD-UP TIME. CONTACT PPI ENGINEERING FOR MORE DETAIL.
ISOLATION VOLTAGE INPUT TO CHASSIS	1500Vac, 60Hz	NO ARCING OR DAMAGE FOR 60 SECOND TEST DURATION. LEAKAGE CURRENT < 10mArms.
ISOLATION VOLTAGE INPUT TO OUTPUT	1500Vac, 60Hz	NO ARCING OR DAMAGE FOR 60 SECOND TEST DURATION. LEAKAGE CURRENT < 10mArms.
OUTPUT VOLTAGE ADJUSTMENT	NONE	
EXTPWRFAIL-H STATUS LINE	HIGH STATE, 2.5Vmin LOW STATE, 0.5Vmax @ 16mA SINK CURRENT	LOW STATE (W/ RESPECT TO DC Return) UPON DETECTION OF INPUT AC > 96Vrms. ASSERTS HIGH WITHIN 10mSEC UPON DETECTION OF INPUT AC SOURCE FALLING BELOW 90Vrms

BATTERY CHARGER CHARACTERISTICS

PARAMETER	70050M5-800	REMARKS
RATED OUTPUT VOLTAGE	29V	0.6A CONSTANT CURRENT SOURCE
FAST CHARGE CURRENT	0.6A TYPICAL	SEE "BATTERY OPERATION SUMMARY" FOR TERMINATION OF FAST CHARGING MODE
TRICKLE CHARGE CURRENT	10mA TYPICAL	CONTINUOUS WHEN NOT IN FAST CHARGE MODE OF OPERATION
BATTERY ENABLE – H SIGNAL	2.5V MINIMUM	APPLY A TTL HIGH (W/RESPECT TO DCrtn) TO ACTIVATE BATTERY CHARGER AND BATTERY CHARGER CONVERTER, A TTL LOW WILL DISABLE BATTERY CONVERTER IF OPERATING FROM BATTERIES
BATTERY LOW – H STATUS LINE	2.5 V MINIMUM	ACTIVE HIGH OUTPUT UPON DETECTION OF BATTERY VOLTAGE AT 22 V ± 0.5V
OFF STATE LEAKAGE CURRENT	< 30uA MAXIMUM	LEAKAGE CURRENT FROM BATTERY WHEN POWER SUPPLY IS IN OFF STATE

BATTERY OPERATION SUMMARY

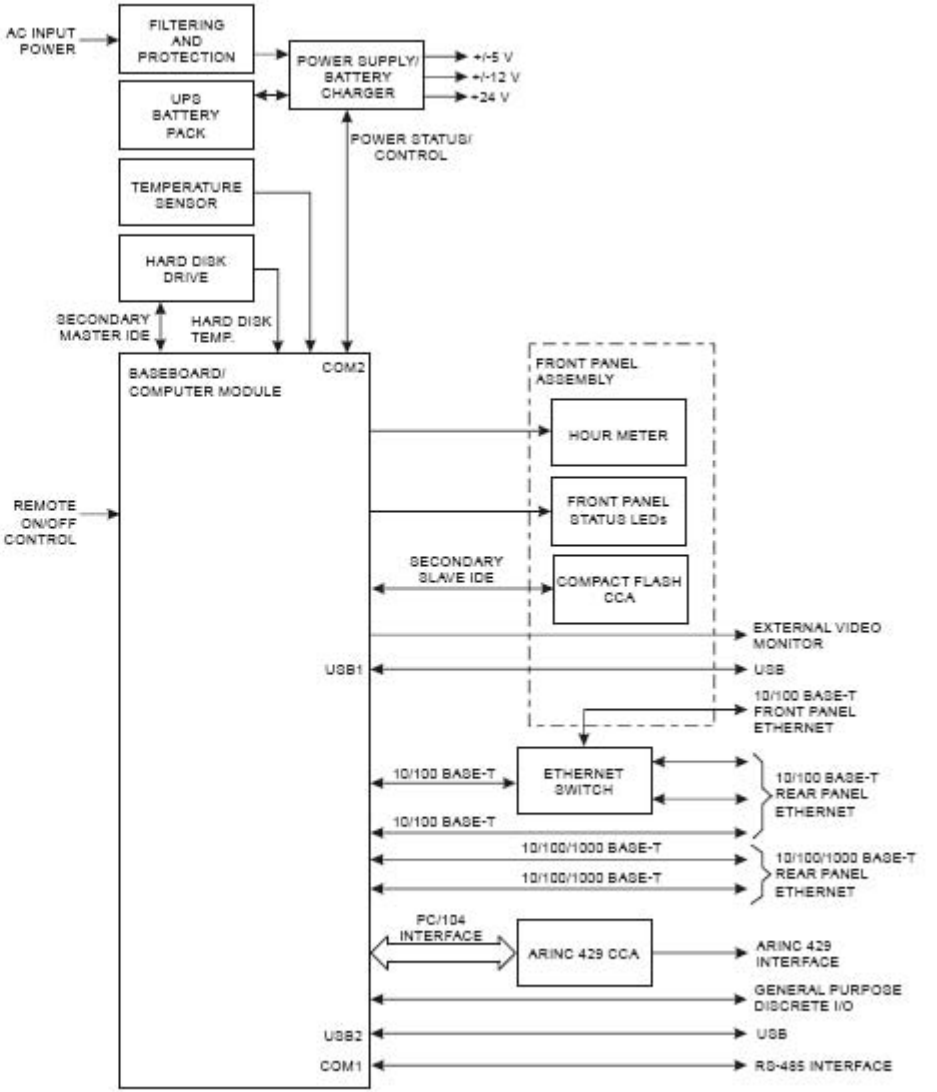
When an external rechargeable +24Vdc Nickel Cadmium battery is connected to J2, and AC is applied to the power supply (at J1), and BATTERY ENABLE is asserted high with respect to DC Return, the internal battery charger will begin the FAST CHARGE mode of operation. Provided the battery is capable of taking a charge (i.e., the initial battery voltage is greater than 18V), the FAST CHARGE mode will commence and will continue for no less than 7 minutes. Once the initial 7 minute time period has timed out, the FAST CHARGE mode will be terminated if the battery voltage is sensed to be higher than 29.3V or 90 minutes elapses - whichever occurs first. The charger circuit will then enter the TRICKLE CHARGE mode which will occur continuously to keep the battery "topped off". If the AC input power is removed, the power supply will automatically switch over to battery operation. The five DC outputs are guaranteed to remain in regulation during the switchover time period. If the AC input voltage is reapplied, battery operation will cease and the charger circuit will re-establish the FAST CHARGE mode of operation. The charger circuit is disabled while operating from batteries.

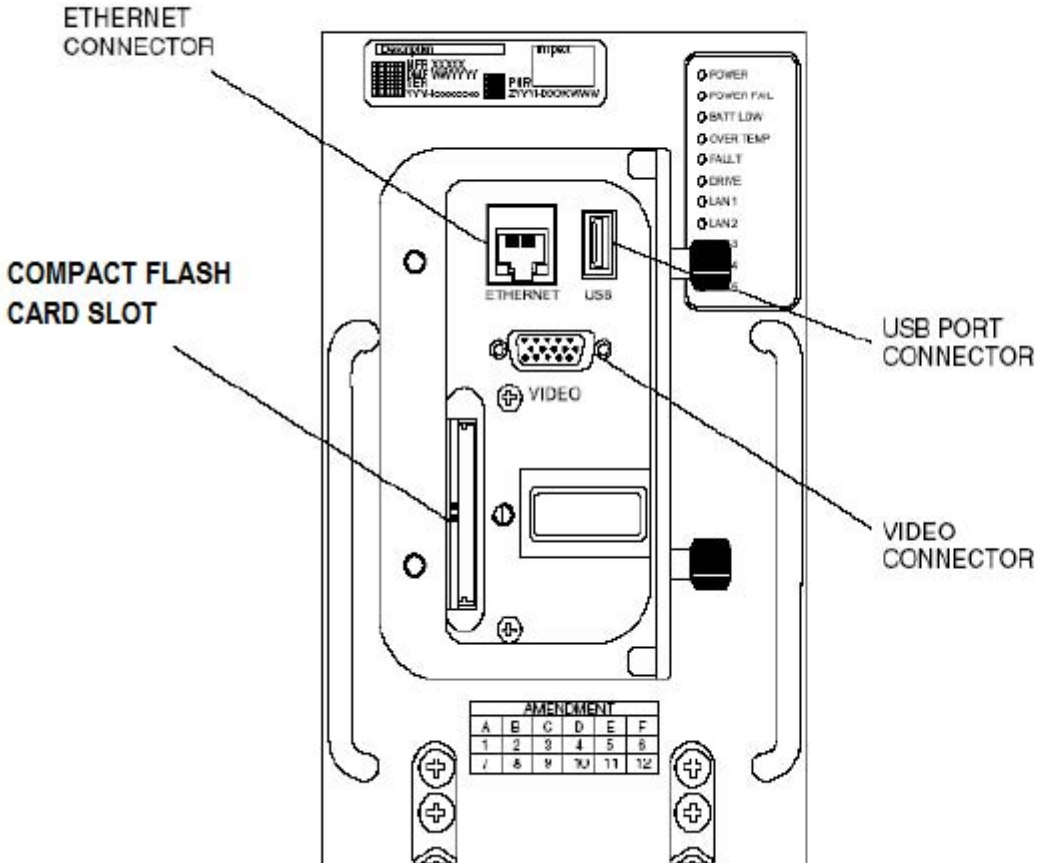
The power supply will operate from battery voltage as long as this voltage is larger than 18V. If the battery voltage discharges below 18V, the supply will automatically shutdown and remain latched off. Only application of AC input power will clear this latching mechanism. The **70050M5-800** supply cannot start from battery voltage, only AC input power.

Single Board Computer (SBC)

- System Control Functions and Sensors
- Discrete lines
- UPS function
- Ethernet I/O
- VGA Video
- USB
- RS-232/485 Serial Port
- Flash/EPROM

- Hard Disk Drive (HDD)
- Compact Flash Reader
- Front Panel Status Indicators
- Rear Panel I/O PWA
- Power Subsystem
- Power Supply
- Battery Pack
- ARINC 600 Rear Panel Connector (Size 2)
- ARINC 429 Interface
- Ethernet unmanaged switch





VIDEO Connector Pin Assignments

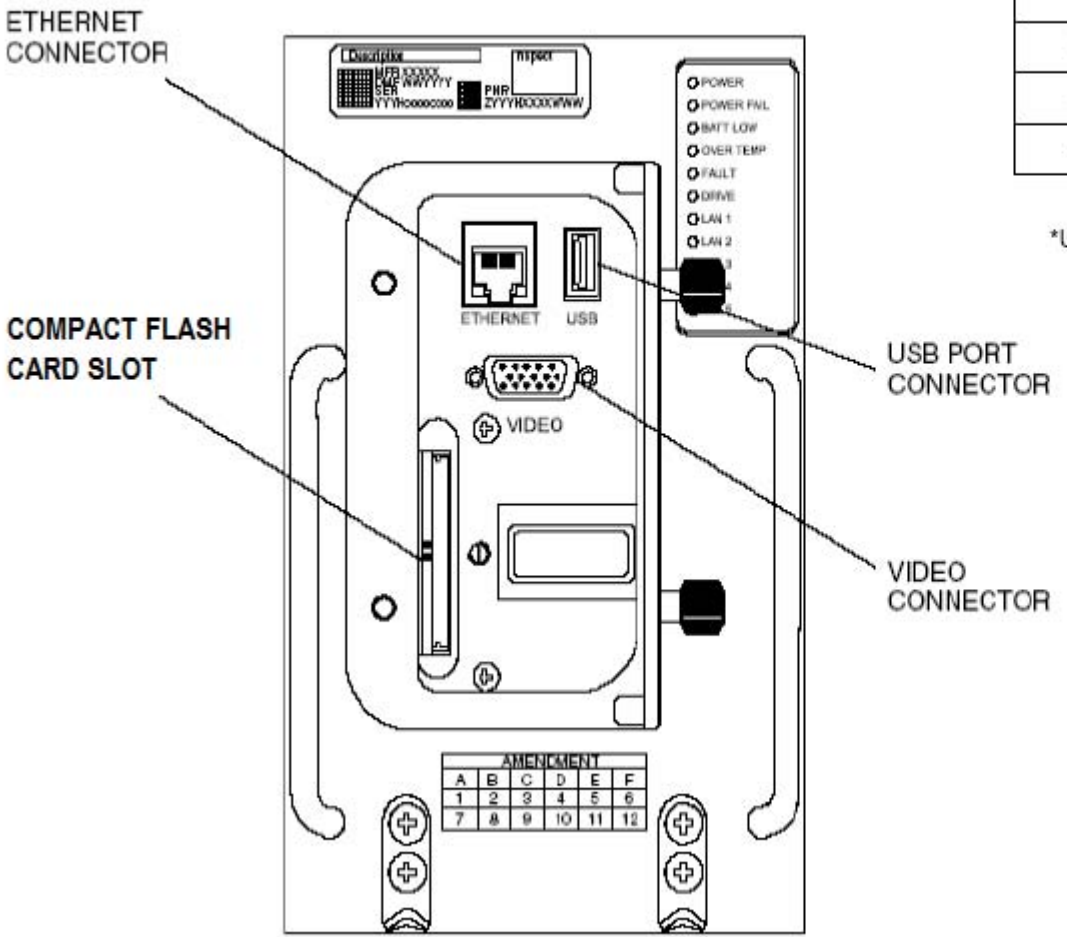
PIN*	SIGNAL	PIN*	SIGNAL
1	Red	9	Reserved
2	Green	10	Signal Ground
3	Blue	11	Reserved
4	Reserved	12	Reserved
5	Signal Ground	13	Horizontal Drive
6	Signal Ground	14	Vertical Drive
7	Signal Ground	15	Reserved
8	Signal Ground		

*Use HD15 Male for mating connector.

ETHERNET Connector Pin Assignments

PIN*	SIGNAL	PIN*	SIGNAL
1	Transmit Data +	5	No Connection
2	Transmit Data -	6	Receive Data -
3	Receive Data +	7	No Connection
4	No Connection	8	No Connection

*Use RJ-45 Male for mating connector.



USB Connector Pin Assignments

PIN*	FUNCTION
1	+5 VDC
2	Data -
3	Data +
4	Ground

*Use USB Type A Male for mating connector.

Diversified Technology, Inc.

ETX-LX15
Configuration and Maintenance Guide
Rev 1.1

ETX-LX15 ETX Board with an Intel® Pentium® M

Return Shipment Information

If service or repair is required, contact DTI's Service Department for a Return Material Authorization (RMA) number and shipping instructions. If the product is out of warranty, or was damaged during shipment, a purchase order will be required for the repair. The product should be returned in its original shipping materials. Contact DTI if replacement material is required. Seal the carton securely and ship prepaid to the following address with the RMA number on the label.

DIVERSIFIED TECHNOLOGY, INC.
Service Department
476 Highland Colony Parkway
P.O. Box 748
Ridgeland, MS 39158
RMA# _____

To contact the Service Department:

Telephone: (601) 856-4124
Fax: (601) 856-2888
Email: tech@dtims.com

Items determined to be covered under warranty will be returned freight prepaid. Items not in warranty will be returned freight collect, contact DTI's Service Department.

For Your Safety

CAUTION: DTI eTX-Lx15 baseboards use a lithium battery. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions.

Revision History

Date	Revision	Summary of Corrections
7/22/04	1.0	Initial Release
		Updated compliance section
1/10/05	1.1	Corrections to pin-out in section B.3.5
		Added note to section 1.3.20

Table of Contents

Tables

Figures

Document Organization

This document describes the operation and use of the ETX-LX15 Computer Processor Board with an Intel® Pentium® M. The following topics are covered in this document.

Chapter 1, "Introduction," introduces the key features of the ETX-LX15. This chapter includes a product definition, a list of product features, and a functional block diagram with a brief description of each block. This chapter can be used to compare the features of the ETX-LX15 against the needs of a specific application.

Chapter 2, "Getting Started," provides unpacking instructions and initial setup information for the ETX-LX15. This chapter summarizes configuration information and should be read before using the board.

Chapter 3, "Configuration," describes the jumper settings on the ETX-LX15. This chapter details factory default settings and provides information about tailoring the board to the needs of specific applications.

Chapter 4, "Reset," discusses the reset types and reset sources available on the ETX-LX15.

Chapter 5, "System Monitoring and Control," lists various system monitoring and control features available on the ETX-LX15.

Chapter 6, "IDE Controller," provides an introduction to the ETX-LX15's IDE Controller. This chapter covers drive configuration, IDE I/O mapping, device drivers, and the ETX-LX15's support for internal and external disk drives.

Chapter 7, "Watchdog Timer," explains the operation of the ETX-LX15's watchdog timer. Sample code is provided to illustrate how the watchdog's functions are used in an application.

Chapter 8, "System BIOS," discusses recovery from and correction of a corrupted BIOS.

Appendix A, "Specifications," contains the electrical, environmental, and mechanical specifications for the ETX-LX15.

Appendix B, “Connectors,” This chapter provides a connector location illustration and connector pin out tables. A detailed description and pin out for each connector is given.

Appendix C, "Thermal Considerations," describes the thermal requirements for reliable operation of the ETX-LX15.

Appendix D, "Datasheet Reference," provides links to Websites with information about many of the devices and technologies used in the ETX-LX15.

Appendix E, "Agency Approvals," presents UL, CE, and FCC agency approval and certification information for the ETX-LX15.

Chapter 1

1 Introduction

This chapter provides an introduction to the ETX-LX15 including a product definition, a list of product features, and a functional block diagram with descriptions of each block.

This embedded application will employ the Embedded Technology eXtended (ETX) compliant standard. The ETX-LX15 is ETX Specification V2.6 compliant and designed to operate within systems with ETX compliant Baseboards. The ETX-LX15 ECM, embedded computing module, will provide the scalability, flexibility, and stability of Applied Computing Platforms that utilize Pentium M processors. Along with CPU flexibility, the ETX-LX15 CPU module offers dual channel LVDS flat panel, PCI/ISA support, and on-board system monitoring. Other functionality includes ethernet integration using the Intel 82562EM 10/100 Base-T PCI Ethernet controller, dual channel IDE hard drives, serial ports, and USB2.0 ports.

1.1 Product Definition

The ETX-LX15 is an embedded computing module designed to decrease time to market for the end user. It is a modular implementation of processing power, (CPU, Chipset, etc.), that relies on an application specific ETX baseboard for accessibility to external I/O. The ETX-LX15 is an ideal solution for all form factors. It utilizes the Intel® Pentium® M processor in a micro-FCBGA package along with the Intel 855GME chipset and ICH4-M IO controller. The design offers the latest in memory and I/O technology to provide an inexpensive, yet fast and reliable ETX Specification V2.6 board. Coupled with Intel's mobile technology, the ETX-LX15 is ideal for most small form factor, low power applications. The ETX-LX15 includes hardware monitoring and a field upgradeable AMI Award BIOS.

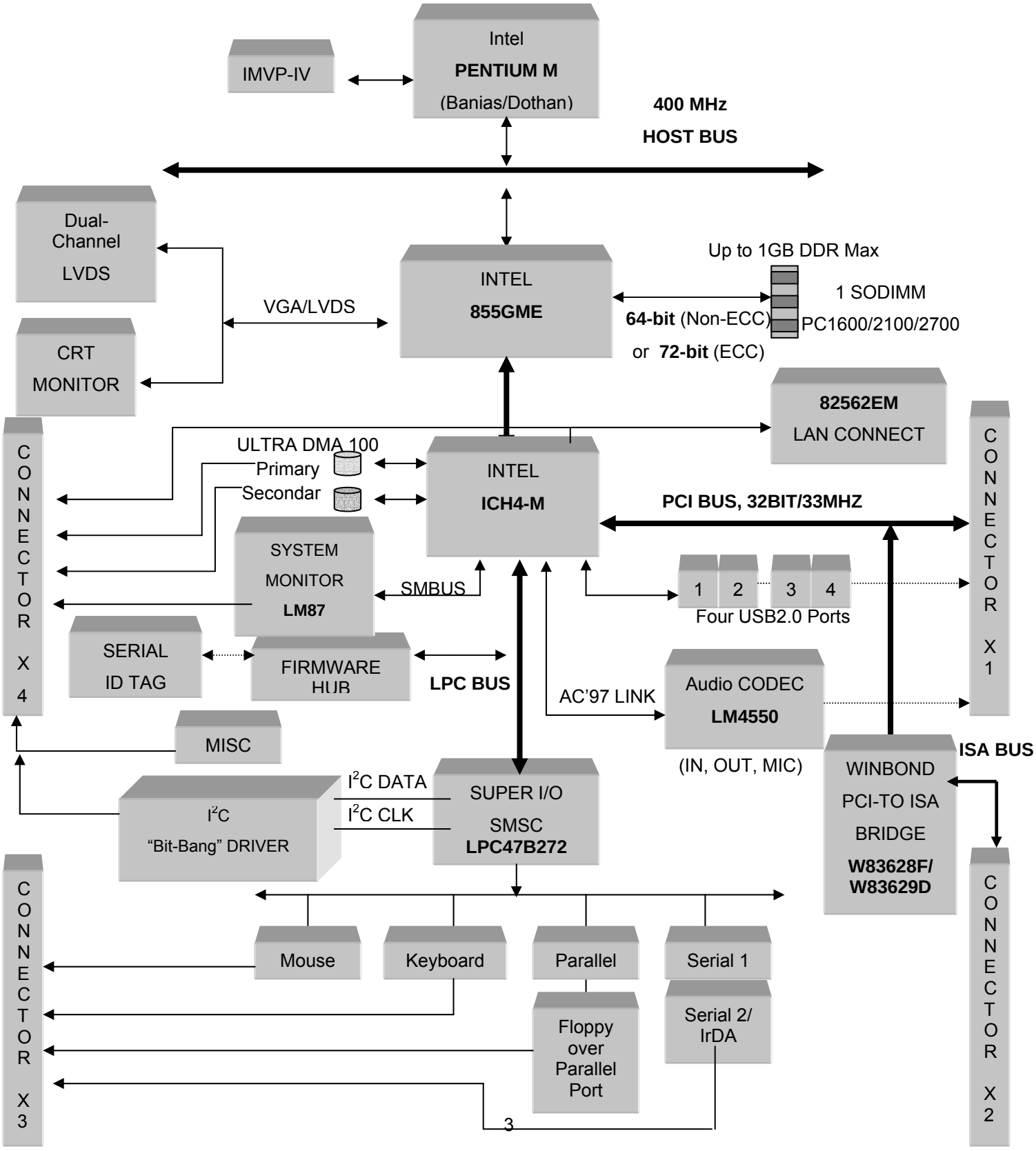
For more information about options and accessories, including the processor selection, memory sizing, and heat spreader, contact your DTI sales representative.

1.2 Features

- *ETX Specification 2.6* compliant
- Standard I/O via ETX baseboard
- Mobile Intel Pentium M, micro-FCBGA package
- 1 MB of Level 2 cache
- 400 MHz front side bus
- Intel® 855GME GMCH
- Integrated Intel Extreme Graphics 2 controller
- Supports 256 MB, 512 MB, or 1 GB of DDR SDRAM memory at 200, 266, or 333 MHz
- Dual Channel LVDS Flat Panel Support
- Intel ICH4-M I/O Controller
    - Integrated 10/100 Mb PCI Ethernet controller
    - 4-slot, 32/33-bit, PCI Bus support
    - Four Universal Serial Bus Ports (USB Revision 2.0 compliant)
    - Dual channel PCI ATA/100 EIDE
    - Integrated AC'97 2.1 Sound
    - Software Programmable Watchdog Timer
- PS2 Mouse and Keyboard Interfaces
- 3-slot ISA Bus support
- LM87 System Monitor
- Multifunctional IEEE 1284 enhanced parallel port and 360KB to 1.44MB floppy disk controller (selectable via ETX configuration pin from the baseboard)
- System BIOS in Boot Block Flash memory
- Two 16C550 RS-232 serial ports
- IrDA 1.1 support multiplexed on Serial Port 2
- Reset/Speaker
- Support for Microsoft Windows 2000/XP, Red Hat Linux, and Solaris 8/9
- Standard AT Systems include:
    - Two enhanced interrupt controllers (8259)
    - Three counter/timers (one 8254)
    - Real-time clock/CMOS RAM (146818B)
    - Two enhanced DMA controllers (8237)

1.3 Functional Blocks

The following topics provide overviews of the ETX-LX15's main features, some of which are shown in the functional block diagram below.



1.3.1 ETX Architecture

ETX, Embedded Technology Extended, is a form factor architecture whose primary purpose is to improve time-to-market. This architecture embeds most of the processing power onto a printed circuit board module that is at most 100mm x 114mm. That module then receives power from and passes its I/O to an ETX baseboard where one gains access to the necessary external connectors. ETX Specification v2.6 governs design of ETX modules and baseboards in order to insure physical interchangeability and electrical compatibility between modules; however, baseboard form factor is a completely custom arena. ETX modules are ideal for ATX, PICMG, CPCI, ISA, PCI, VME or any standalone application. The ETX-LX15 is designed to operate within any ETX Specification v2.6 baseboard.

1.3.2 Processor

The ETX-LX15 uses the Mobile Pentium M in a micro FCBGA package. The 1MB on-die transfer L2 cache is integrated with the CPU, eliminating the need for separate components and improving performance. The FCBGA package Pentium M processor also operates with a 400 MHz Processor Side Bus for fast access to memory and data. The eTX-LX15 may utilize either an Intel Pentium M Banias or Dothan processor. Supported Intel Pentium M processors are 1.1GHz at 400 MHz FSB with 1MB integrated L2 Cache and 1.6GHz at 400 MHz FSB with 1MB integrated L2 Cache. Dothan processor speeds are TBD.

The "Mobile Pentium M (FCBGA Package)" topic in Appendix D contains a link to the datasheet for the processor.

1.3.3 Chipset

The Intel 855GME chipset consists of two controller hubs. The 855GME Memory Controller Hub (MCH) supports a 400MHz system bus, DDR200/266/333 memory up to 1 GB via the one right-angled memory socket. The 855GME also offers integrated graphics support via Intel's Extreme Graphics 2 Technology. Video capabilities of the 855GME include high performance 2D/3D capability and support both CRT and flat panel displays. Coupled with the ICH4-M, the 855GME also offers an integrated AC'97 controller, integrated LAN capability, and four USB2.0 ports.

The following is a list of features of the 855GME chipset:

- Designed, validated, and optimized for the Intel Pentium M with NetBurst™ micro-architecture using proven and established building blocks
- 400MHz system bus delivers a high-bandwidth connection between the Intel Pentium M and the platform, providing 3x the bandwidth over platforms based on Intel® Pentium® III processors
- Support for DDR333 memory in addition to DDR200 and DDR266
- Extreme Graphics 2 technology for high performance, sharp 3D images while maintaining a balanced memory usage for graphics and system performance
- Dual Display Functionality (CRT and LVDS Flat Panel)

Coupled with the ICH4-M:

- USB 2.0 controllers provide high performance peripherals with 480Mbps of bandwidth. This results in a significant increase over previous integrated 1-4 port hubs at 12Mbps
- Integrated LAN connect and AC97 Functionality
- 32bit/33Mhz PCI bus
- Dual Ultra ATA/100 controllers, coupled with the Intel® Application Accelerator - a performance software package - support faster IDE transfers to storage devices

- The Intel® Application Accelerator software provides additional performance over native ATA drivers. The Intel Application Accelerator improves system performance by improving I/O transfer rates and enables faster O/S load time resulting in accelerated boot times
- Embedded lifecycle support

The "Intel 855GME Chipset" topic in Appendix D contains a link to information about the chipset.

1.3.4 PCI-to-PCI Bridge

The ETX-LX15 has a 32bit/33Mhz PCI bus to the ETX baseboard.ETX-LX15 can be the system host. All PCI I/O is driven at 3.3V and is 5V tolerant. This bus complies with PCI Specification 2.2.

1.3.5 Memory and I/O Addressing

The ETX-LX15 supports up to 1GB of DDR200/266/333 via one right-angled SODIMM socket. Memory does not come with the ETX-LX15 and must be installed by the customer or by DTI. Configurations choices are 128MB, 256MB, 512MB, or 1GB.

See the "Memory Configuration" and "I/O Configuration" topics in Chapter 2 for more information.

1.3.6 Power Ramp Circuitry

The ETX-LX15 features power monitoring circuitry that insures operation under adequate input power environments. The ETX-LX15 unconditionally resets the board when it detects that 5V is below an acceptable operating limit. Minimum voltage threshold for the ETX-LX15 is 4.5V (5V supply).

1.3.7 Video

The ETX-LX15 supports both CRT and LVDS flat panel video using Intel's 855GME high performance video interface. When using less than 512MB of installed DDR memory, the 855GME can share up to 32MB of system memory for graphics purposes. The 855GME can allocate up to 64MB of graphics memory if the total amount of system memory is greater than 512MB.

The onboard video from the Intel 855GME may be disabled by a jumper setting. This allows for the use of a PCI video card only. If the onboard video is enabled and a PCI video card is installed, the PCI video card will be the primary video source in DOS. Once the Windows drivers are loaded, either controller may be primary, and both dual display and dual application functionality can be utilized.

The "Video" topic in Appendix D contains a link to the datasheet for this device.

1.3.8 10/100 Base-T Ethernet

The fast ethernet on the ETX-LX15 ECM is provided by the Intel 82562EM PCI LAN connect device. The 82562EM controller supports 10/100 Base-TX ethernet implemented through the ETX interface to the baseboard. The 82562EM complies with the IEEE 802.3u Auto-Negotiation (and 100BASE-TX) standard and the IEEE 802.3x Full-Duplex Flow Control standard.

The "Ethernet" topic in Appendix D contains links to the datasheets for the Ethernet devices used on the ETX-LX15.

1.3.9 IDE Hard Drive

The ETX-LX15 ECM provides a PCI EIDE ATA/100 controller. This PCI IDE controller supports all DMA IDE and ATAPI compliant devices. The IDE interface is implemented using Intel's 82801DBM I/O Controller Hub (ICH4-M). The ATA100 interface supports two devices per connection. All IDE configurations are handled by the ETX-LX15 configuration utility. When enabled, the primary IDE interface utilizes IRQ14, and the secondary IDE interface utilizes IRQ15. The standard IDE drive is connected via a 40-pin, 40-wire ribbon cable and the ultra ATA100 drive is connected via a 40-pin, 80 wire ribbon cable (NOTE: An Ultra ATA100 cable should not exceed 18"). The EIDE interface is available through the "X4" ETX connector to the baseboard. .

See Chapter 6, "IDE Controller", for more information.

1.3.10 Serial I/O

The ETX-LX15 provides support for two full function, high-speed NS16C550 compatible serial ports. The serial port interfaces are implemented using SMSC's LPC47B272. Both ports, COM1 and COM2 are accessible through the "X3" ETX connector. COM2 is also configurable as an IRDA 1.0 compliant port.

1.3.11 Parallel Port

The ETX-LX15 also includes a standard parallel port. The address of the port may be set to any standard printer port address by using the ETX-LX15 configuration utility. It may also be disabled entirely through the same utility. Some parallel port signals are multiplexed with floppy signals; hence, the interface setup should be selected at boot-up by use of a jumper on the baseboard. The parallel port of the SIO chip is hardware strapped to act as a parallel port by default instead of a floppy port. This functionality is passed to the baseboard through the X3 connector. The selector signal LPT/FLPY~ is passed to the baseboard through the X4 connector.

Note: Since some signals are inputs from the printer (i.e. actively driven by the printer), it is advisable to not use the floppy interface with a printer still attached to the system.

1.3.12 Floppy Disk Interface

The ETX-LX15 supports /AT compatible floppy disk drives. The floppy disk interface supports 360k, 720k, 1.2M and 1.44MB disk drives. The floppy interface can be enabled or disabled using the ETX-LX15 configuration utility. When enabled, the floppy interface utilizes IRQ6 and DMA channel 2. The ETX-LX15 supports Floppy over Parallel Port; meaning, floppy and parallel port functionality are multiplexed; consequently, the desired functionality must be selected before boot-up using a jumper on ETX baseboards. This feature is passed to the baseboards through the X3 ETX connector. Note: The ETX-LX15 uses only floppy drive 1 signals (not drive 0); hence, when using the floppy interface, connect a **NON-TWISTED** cable to the floppy drive.

The implementation of the floppy disk interface as Drive 1 complies with the ETX Specification. Refer to the ETX Design Guide and Specification for additional information.

1.3.13 Audio

The ETX-LX15 utilizes the National LM4550 to provide a high quality audio path within the PC system. The LM4550 performs the analog intensive functions of the AC97 Rev 2.1 architecture. Audio is accessible only through the X1connector on an ETX baseboard. Supported features include line in, line out, and microphone in. Microphone Boost is not supported.

1.3.14 Interrupts

Two enhanced, 8259-style interrupt controllers provide the ETX-LX15 with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/Timers
- Serial I/O
- Keyboard
- Floppy disk
- IDE interface
- Real-Time Clock
- On-board PCI devices

Enhanced capabilities include the ability to configure each interrupt level for active high-going edge or active low-level inputs.

The ETX-LX15's interrupt controllers reside in the ICH4-M device. The "Intel ICH4-M Controller" topic in Appendix D provides a link to the datasheet for this device.

1.3.15 Counter/Timers

Three 8254-style counter/timers, as defined for the PC/AT, are included on the ETX-LX15. Operating modes supported by the counter/timers include:

- Interrupt on count
- Frequency divider
- Software triggered
- Hardware triggered
- Square wave output
- One shot

The ETX-LX15's Counter/Timers reside in the Intel ICH4-M device. The "Intel ICH4-M Controller" topic in Appendix D provides a link to the datasheet for this device.

1.3.16 DMA

Two cascaded 8237-style DMA controllers are provided on the ETX-LX15 for use by the on-board peripherals.

The ETX-LX15's DMA controllers reside in the Intel ICH4-M device. The "Intel ICH4-M Controller" topic in Appendix D provides a link to the datasheet for this device.

1.3.17 Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose, battery-backed, CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS setup information.

The ETX-LX15's Real-Time Clock resides in the Intel ICH4-M device. The "Intel ICH4-M Controller" topic in Appendix D provides a link to the datasheet for this device.

1.3.18 Reset

The push-button reset on the ETX-LX15's that is accessible through the “X4” ETX header functions as a "Hard Reset".

See Chapter 4, "Reset," for more information about reset sources for the ETX-LX15.

1.3.19 Watchdog Timer

The watchdog timer optionally monitors system operation and is programmable for different timeout periods (from 2.4 seconds to 38 seconds). It is a two-stage watchdog, meaning that it can be enabled to produce a system management interrupt (SMI) or an IRQ (APIC 1, INT 9) before it generates a Reset. Failure to strobe the watchdog timer within the programmed time period may result in an SMI, a reset request, or both. A register bit can be read to indicate if the watchdog timer caused the reset event. This watchdog timer register is not cleared on power-up, enabling system software to take appropriate action if the watchdog generated the reboot.

See Chapter 7, "Watchdog Timer," for more information, including sample code.

1.3.20 Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a common interface to slower-speed peripherals. Functions such as keyboard, serial ports, printer ports, and mouse ports can be consolidated into USB, simplifying cabling requirements. The ETX-LX15 provides four USB 2.0 ports to the ETX baseboard. All four ports are passed via the “X1” ETX header.

The ETX-LX15’s USB channels are controlled by the Intel ICH4-M device. The "Intel ICH4-M Controller" topic in Appendix D provides a link to the datasheet for this device.

Note: Windows 2000 and XP USB 2.0 drivers are obtained by installing the latest Windows service packs for the respective operating systems.

1.3.21 System Environmental Monitor

This board provides a serial interface system hardware monitor. This functionality is obtained via a National Semiconductor LM87 hardware monitor chip. Monitored voltages include 5V, 3.3V, 2.5V, the CPU core voltage, and the memory termination voltage, 1.25V. Ambient and CPU core temperatures are also monitored via the LM87.

For further information, see "System Monitoring and Control" in chapter 5 for more details.

1.4 Software

The ETX-LX15 includes a DTI enhanced AMI Embedded BIOS loaded into on-board 1Mb flash. The BIOS settings are user-configurable and can boot an operating system from a hard drive, CD-ROM drive, over network connection, or CompactFlash located on the baseboard. BIOS and firmware updates can be provided by DTI. User created custom CMOS settings are saved regardless of the state of the CMOS battery (i.e. non-volatile custom CMOS settings).

The ETX-LX15 is compatible with all major PC operating systems, including Microsoft* Windows* 2000/XP, Linux*, and VxWorks*. Chips may provide additional drivers for Intel peripherals, flash drives, and for supported operating systems. Software device drivers for the ETX-LX15 may be found on the DTI Product Documentation and Software CD.

Chapter 2

2 Getting Started

This chapter summarizes the information needed to make the ETX-LX15 operational. This chapter should be read before using the board.

2.1 Unpacking

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and DTI for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to DTI. Refer to the Return Shipment Information page for assistance.

CAUTION: This board must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the board. Wear a wrist strap grounded through one of the system's ESD Ground jacks when servicing system components.

2.2 System Requirements

The following topics briefly describe the basic system requirements and configurable features of the ETX-LX15. Links are provided to other chapters and appendices containing more detailed information.

2.2.1 BIOS Version

For proper operation, the ETX-LX15 must run the DTI enhanced AMI Embedded BIOS. The revision level is shown in the BIOS Identification string displayed during the Power-On Self Test (POST).

2.2.2 Connectivity

On the backside, the ETX-LX15 features four ***Hirose FX8-100P-SV*** headers for mating. The ETX-LX15 is designed to operate within any ETX baseboard providing ETX compliant X1, X2, X3, and X4 signaling.

The ETX-LX15 meets the following power requirements:

- +5VDC +5%, -5% @ 3.7A typical

Configuration	5V (Avg)	5V (peak)
1.7GHz / 512MB	3.62A	3.95A
Hard disk (add) (typical)	540mA	1.00A

*** Peak (short duration) power supply current may be significantly higher (up to 50%) and will vary depending upon the application. Readings were taken during low stress application.**

It is the users' responsibility to ensure that the ETX-LX15 is installed in a chassis capable of supplying adequate airflow or conductive cooling. The ETX-LX15 may come with a heat spreader that allows the processor to operate between 0° and approximately 50°C ambient with a minimum of 200 LFM (1 meter per second) of external airflow. The maximum power dissipation of the processor (FCPGA package) is 25W. External airflow **must** be provided at all times; except, if a conductive cooling application has been properly designed and analyzed.

See Appendix A, "Specifications," and Appendix C, "Thermal Considerations," for more details.

CAUTION: The processor "core" temperature must **never** exceed 100°C under any condition of ambient temperature or usage. This may result in permanent damage to the processor.

The ETX-LX15 may contain materials that require regulation upon disposal. Please dispose of this product in accordance with local rules and regulations.

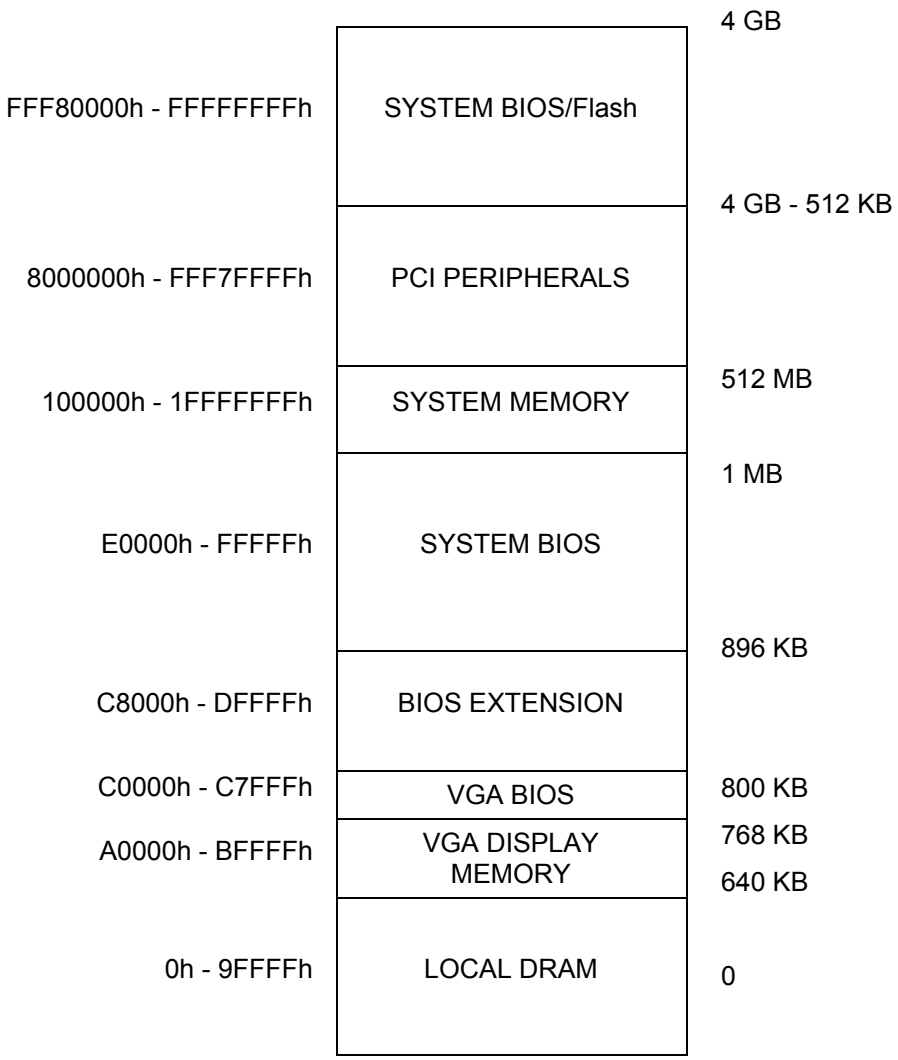
For disposal or recycling information, please contact your local authorities or the Electronic Industries Alliance at http://www.eiae.org/

2.3 Memory Configuration

The ETX-LX15 components can *address* up to 4 GB of memory, but the board only has one SO-DIMM socket; hence, can physically only hold one stick of memory. The address space is divided between memory local to the board and memory located on the Local PCI bus. Any memory not reserved or occupied by a local memory device (DRAM/flash) is available to PCI memory devices.

The ETX-LX15 can support one stick of 256 MB, 512 MB, or 1 GB DDR SDRAM. 1MB of L2 cache is integrated with the Pentium® –M processor.

Memory Address Map Example



2.4 I/O Configuration

The ETX-LX15 addresses up to 64 KB of I/O using a 16-bit I/O address. The ETX-LX15 is populated with many commonly used I/O peripheral devices. The I/O address location for each peripheral is shown in the "I/O Address Map" illustration.

I/O Address Map

*Onboard ISA peripherals addressed between 100h - 7FFh decode 11 bits of address (A0h - A10h). Therefore, these peripherals will alias throughout the 16-bit I/O space at the following ranges:

- x100-x3FFh
- x500-x7FFh
- x900-xBFFh
- xD00-xFFFh

PCI devices can fully utilize the address space from D00 - FFFFh, since subtractive decoding is used for the onboard ISA devices.

D00 - FFFFh	PCI*
CF8 - CFFh	PCI Config/RST Control
780 - CF7h	PCI Reserved
778 - 77Fh	LPT ECP Registers
400 - 777h	Reserved
3F8 - 3FFh	COM1
3F0 - 3F7h	Floppy / IDE Registers
3E0 - 3EFh	Reserved
3B0 - 3DFh	VGA Registers
380 - 3AFh	Reserved
378 - 37Fh	LPT
300 - 377h	Reserved
2F8 - 2FFh	COM2
200 - 2F7h	Reserved
1F8 - 1FFh	Reserved
1F0 - 1F7h	Primary IDE Registers
178 - 1DFh	Reserved
170 - 177h	Secondary IDE Registers
100 - 16Fh	Reserved
F0 - FFh	Coprocessor
E0 - EFh	Reserved
C0 - DFh	On-board Slave DMA Controller
B4 - BFh	Reserved
B2 - B3h	APM Registers
B0 - B1h	Reserved
A0 - AFh	On-board Slave Interrupt Controller
93 - 9Fh	Reserved
92h	Fast RESET and Gate A20
90 - 91h	Reserved
81 - 8Fh	On-board DMA Page Registers
80h	Diagnostic Port

78 - 79h	Reserved
70 - 77h	On-board Real-Time Clock
60 - 6Fh	Keyboard and System Ports
50 - 5Fh	Reserved
40 - 4Fh	On-board Timer/Counters
30 - 3Fh	Reserved
2E - 2Fh	Super I/O Configuration
22 - 2Dh	Reserved
20 - 21h	On-board master Interrupt Controller
0 - 1Fh	On-board Master DMA Controller

2.5 Connectors

The ETX-LX15 includes several connectors to interface to application-specific devices. Refer to the "Connectors" topic in Appendix B for complete connector descriptions and pin outs.

2.6 Jumper Options

The ETX-LX15 provides two jumper configuration options for features that cannot be provided through the BIOS Setup Utility. Location figures and descriptions are provided in Chapter 3, "Configuration."

2.7 BIOS Configuration Overview

This topic presents an introduction to the ETX-LX15's BIOS.

The BIOS has many separately configurable features. These features are selected by running the built-in Setup utility. System configuration settings are saved in a portion of battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot-up or reset. The configuration is protected by a checksum word for system integrity.

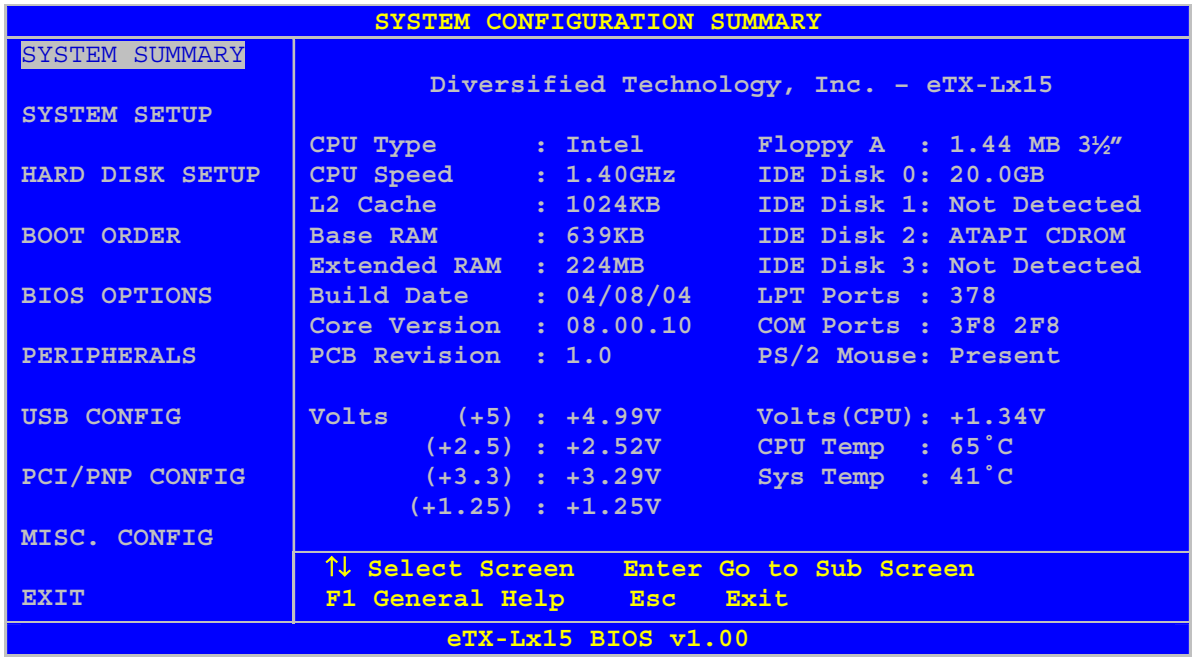
To access the Setup utility, press **F2** during the system RAM check at boot-up. When Setup runs, an interactive configuration screen displays. Refer to the following "Setup Screen" illustration for an example.

Setup parameters are divided into different categories. The available categories are listed in a menu down the left side of the setup screen. The parameters within the highlighted (current) category are listed in the main (right) portion of the Setup screen. Context sensitive help can be displayed for each parameter by highlighting the parameter and pressing F1. A legend of keys is listed at the bottom of the Setup screen.

Use the up and down arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the **+/–** or ↔keys to change the value of a parameter.

Solid arrows next to menu items in the main screen indicate submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press **Enter**.

Setup Screen



2.8 Operating System Installation

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor.

1. Install peripheral devices. Devices are automatically configured by the BIOS during the boot sequence.
2. Most operating systems require initial installation on a hard drive from a floppy or CD-ROM drive. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.
3. Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.
4. Select the appropriate boot device order in the SETUP boot menu depending on the OS installation media used. For example, if the OS includes a bootable installation floppy, select **Removable Media** as the first boot device and reboot the system with the installation floppy installed in the floppy drive. (Note that if the installation requires a non-bootable CD-ROM, it is necessary to boot an OS with the proper CD-ROM drivers in order to access the CD-ROM drive).
5. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of DTI products.
6. When installation is complete, reboot the system and set the boot device order in the SETUP boot menu appropriately.

Chapter 3

3 Configuration

The ETX-LX15 has been designed for maximum flexibility. Many features can be configured by the user for specific applications. Most configuration options are selected through the BIOS Setup utility (discussed in the "BIOS Configuration Overview" topic in Chapter 2). Some options cannot be software controlled and are configured with jumpers.

3.1 Jumper Options and Locations

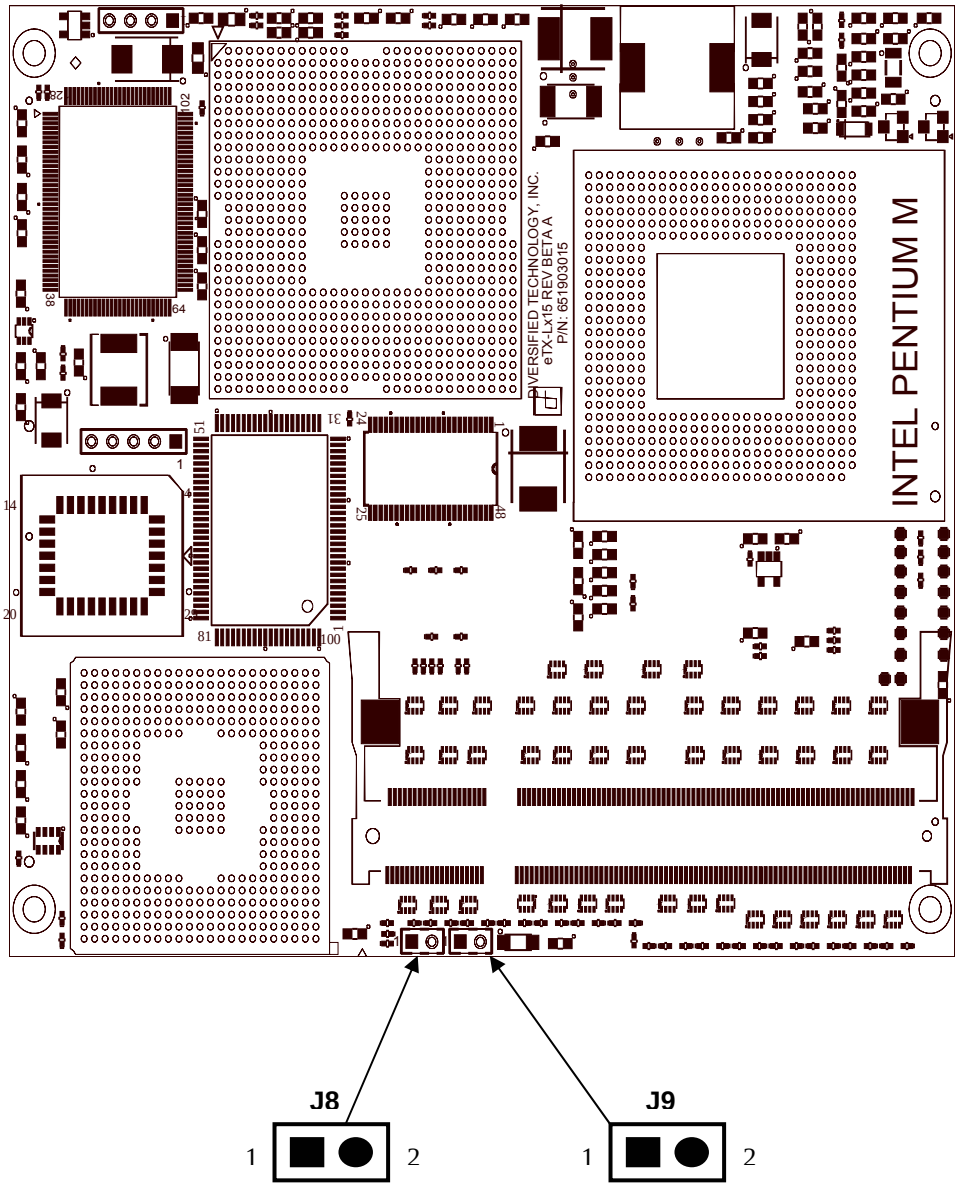
The ETX-LX15 contains a push-button switch on the faceplate and eight jumpers on the component side of the board. The jumpers are listed and briefly described in the "Jumper Cross-Reference" table below.

Factory default switch settings are shown in the "Default Jumper Settings" figure.

Jumper Cross-Reference Table

Jumper	Function
J8	Manufacture Test Mode
J9	Disable Onboard Video

Default Jumper Configuration



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3.1.1 J8 (Manufacturing Test Mode)

Used by the manufacturer for testing purposes. Do not install a jumper at this location.

SW3-4		Function
Open	Default	Normal operation
Closed		Board in manufacture test mode.

3.1.2 J9 (Disable Onboard Video)

Installing this jumper will disable the onboard video. Install this jumper if using a PCI video card only.

SW3-3		Function
Open	Default	Onboard video is enabled.
Closed		The onboard video is disabled.

Chapter 4

4 Reset

This chapter discusses the reset types and reset sources on the ETX-LX15. If necessary, the ETX-LX15's board reset characteristics can be tailored to the requirements of a specific system.

4.1 Reset Types and Sources

The ETX-LX15's reset types are listed below. The sources for each reset type are detailed in the following topics.

- **Hard Reset:** All devices are held in reset.
- **Soft Reset:** CPU initialization only. Other devices are not reset.

4.1.1 Hard Reset Sources

System Register CF9h (ICH4-M Reset Control Register)

Bits 1 and 2 in this register are used by the ICH4-M to generate a hard reset or a soft reset. During a hard reset, the ICH4-M asserts CPURST, PCIRST#, and RSTDRV. Additionally, it resets its core and suspends well logic.

4.1.2 Soft Reset Sources

System Register CF9h (ICH4-M Reset Control Register)

Bits 1 and 2 in this register are used by the ICH4-M to generate a hard reset or a soft reset. During a soft reset, the ICH4 asserts INIT to the CPU for 16 PCICLK. This causes the processor to enter "real mode", initialize its internal registers, and begin instruction execution from FFFFFFF0h (the boot vector).

Keyboard Controller Reset

The keyboard controller generates a keyboard controller reset when FEh is written to port 64h. This causes the ICH4-M to assert INIT to the CPU.

Keyboard CTRL-ALT-DEL

Simultaneously pressing these keys calls a BIOS function that reboots the system.

Note: **This method does not work under operating systems that trap calls to this BIOS function.**

Watchdog Timer

The watchdog timer may be programmed to generate a system reset if it is not updated within a given time-out period. This function is discussed in Chapter 7, "Watchdog Timer."

Chapter 5

5 System Monitoring

The ETX-LX15 allows onboard voltages and temperatures to be monitored via an onboard *National Semiconductor LM87* hardware monitor. The LM87 is software accessible via the SMBUS controller integrated in the *Intel ICH4-M*. The following section will outline necessary information to allow reading voltage and temperature values from the LM87. For more detailed descriptions see the *National Semiconductor LM87* and *Intel ICH4-M* datasheets obtainable via the links in Appendix D.

5.1 Monitoring and Control Functions

The LM87 voltage and temperature registers are accessible via the SMBUS.

5.2 LM87 SMBUS Data Format

A three-byte packet is needed to read values from the LM87. The table below outlines the contents of the packets.

Byte Number	Name	Value	Description
1	Device Address	5Dh	The first byte is the device address for the LM87. Bit 0 is 1 since this is a read operation.
2	Register	xxh	Register within the LM87 to read.
3	Data	xxh	Data read from the LM87.

5.3 LM87 Voltage Registers

The following table lists the LM87 registers that hold voltage readings. The value read from the register must be multiplied by the Voltage Multiplier to obtain the voltage value in Volts.

Example:

For a +5Volt reading of C0h: C0h = 192 192 x .026V = 4.992Volts

LM87 Register	Voltage Name	Voltage Multiplier
20h	+2.5	13mV
21h	CPU	14.1mV
22h	+3.3	17.2mV
23h	+5	26mV
25h	+1.25	14.1mV

5.4 LM87 Temperature Registers

The following table lists the LM87 registers that hold temperature readings.

LM87 Register	Temperature Name
26h	CPU
27h	System

The temperature readings are encoded as 2's compliment hex numbers. The following table gives some example readings and their corresponding temperatures.

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1.0°C	0000 0001	01h

+0°C	0000 0000	00h
-1.0°C	1111 1111	FFh
-25°C	1110 0111	E7h

5.5 SMBUS Registers

The following registers are used to issue commands on the SMBUS. These register locations are offsets from the value of the base address register. The SMBUS base IO address (SMB_BASE) is obtained from PCI Configuration Register Bus:0 Dev:1F Func:3 Reg:20-23h.

5.5.1 HST_STS - Host Status Register (SMB-BASE+00h)

Offset:	SMB_BASE+00h	Size:	8 bits
Default Value:	00h	Attribute:	R/WC

Bit	Description
7:5	Reserved
4	**FAILED – (R/WC)** 0 = This bit is cleared by writing a 1. 1 = Set in response to issuing a KILL command.
3	**BUS_ERR – (R/WC)** 0 = This bit is cleared by writing a 1. 1 = Indicates a transaction collision on the SMBUS.
2	**DEV_ERR – (R/WC)** 0 = This bit is cleared by writing a 1. 1 = Indicates an “Illegal Command Field”, “Unclaimed Cycle”, or a “Host Device Time-out” on the SMBUS.
1	Reserved
0	**HOST_BUSY – (RO)** 0 = Indicates that the current SMBUS transaction is complete. 1 = Indicates that the SMBUS is currently processing a transaction.

5.5.2 HST_CNT – Host Control Register (SMB-BASE+02h)

Offset:	SMB_BASE+02h	Size:	8 bits
Default Value:	00h	Attribute:	R/W

Bit	Description
7	Reserved
6	**START – (WO)** 0 = Always returns 0. Check the HOST_BUSY bit to determine if a SMBUS transaction is in progress. 1 = Setting this bit to a 1, initiates the SMBUS transaction specified by the SMB_CMD field.
5	Reserved
4:2	**SMB_CMD – (RW)** These bits contain the encoding for the format of the desired SMBUS transaction. **010 = Byte Data**: This command used the XMIT_SLVA, HST_CMD, and HST_D0 registers.
1	**KILL – (R/W)** 0 = Normal SMBUS functionality 1 = When set, any pending SMBUS transaction is terminated and the FAILED bit is set. Software must clear this bit once it is set.
0	Reserved

5.5.3 HST_CMD – Host Command Register (SMB-BASE+03h)

Offset:	SMB_BASE+03h	Size:	8 bits
Default Value:	00h	Attribute:	R/W

Bit	Description
7:0	This byte is transmitted during the command phase of the SMBUS transaction.

5.5.4 XMIT_SLVA – Transmit Slave Address Register (SMB-BASE+04h)

Offset:	SMB_BASE+04h	Size:	8 bits
Default Value:	00h	Attribute:	R/W

Bit	Description
7:1	Upper 7 bits of the SMBUS slave address.
0	Read/Write Control – (R/W) 0 = Write. Data is supplied via HST_D0. 1 = Read. Data is retrieved via HST_D0.

5.5.5 HST_D0 – Host Data 0 Register (SMB-BASE+05h)

Offset:	SMB_BASE+05h	Size:	8 bits
Default Value:	00h	Attribute:	R/W

Bit	Description
7:0	This byte is the data returned from or supplied to an SMBUS transaction.

5.6 SMBUS Programming Algorithms

This section provides basic SMBUS read and write algorithms that can be used to assess the LM87 system monitoring device.

5.6.1 SMBUS Read Algorithm

1. Program the XMIT_SLVA register with the slave devices address. Bit 0 must be 1 for a read.
2. Program the HST_CMD register with the device command or register offset value.
3. Program the HST_CNT Register with a 48h. [Start] + [SMB_CMB=Byte Data]
4. Wait for the HOST_BUSY bit to be set to indicate the transaction has begun.
5. Wait for the HOST_BUSY bit to be cleared to indicate the transaction is finished.
6. Read the returned data from HST_D0.
7. If any HST_STS[4:2] bits are set, an error occurred. Clear the bits by setting them to 1 and return an error code.

5.6.2 SMBUS Write Algorithm

1. Program the XMIT_SLVA register with the slave devices address. Bit 0 must be 1 for a read.
2. Program the HST_CMD register with the device command or register offset value.

3. Program the HST_D0 register with the data to be written.
4. Program the HST_CNT Register with a 48h. [Start] + [SMB_CMB=Byte Data]
5. Wait for the HOST_BUSY bit to be set to indicate the transaction has begun.
6. Wait for the HOST_BUSY bit to be cleared to indicate the transaction is finished.
7. If any HST_STS[4:2] bits are set, an error occurred. Clear the bits by setting them to 1 and return an error code.

5.7 SMBus Address Map

The table below lists the location, function, and address of each SMBus device used on the ETX-LX15.

Device	**ETX-LX15 Function**	**Address**
ICH SMBus (slave)	ICH4-M ICH	1000 100x
Board clock generator (CK409B)	Board clock generator (CK409B)	1101 001x
SO-DIMM0	SO-DIMM0	1010 000x
LM87	Hardware Monitor	0101 110x

Chapter 6

6 IDE Controller

The ETX-LX15 has an on-board IDE controller that provides two IDE channels for interfacing with up to four IDE devices. The IDE controller is incorporated into the Intel ICH4-M, which supports ATA-100. Both IDE channels are accessible via the “X4” ETX header.

The "Intel ICH4-M Controller" topic in Appendix D provides a link to the ICH4-M datasheet.

6.1 Features of the IDE Controller

8. Primary and Secondary channels for interfacing up to four devices
9. IBM-AT compatible
10. Supports PIO and Bus Master IDE
11. "Ultra ATA/33/66/100" Synchronous DMA Operation
12. Bus Master IDE transfers up to 100 MB/sec.
13. Individual software control for each IDE channel

6.2 Disk Drive Support

The ETX-LX15 supports internal and external IDE devices. These configurations are described below.

6.2.1 Primary IDE Channel

The ETX-LX15's primary IDE channel is directed to the X4 ETX connector, J11.

6.2.2 Secondary IDE Channel

The ETX-LX15's Secondary IDE channel is directed via the X4 ETX connector, J11.

6.3 IDE I/O Mapping

The I/O map for the IDE interface varies depending on the mode of operation. The default mode is "compatibility mode," meaning that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h and interrupt IRQ15. No memory addresses are used.

6.4 IDE Device Drivers

The IDE interface works with all applications by default. To fully utilize the IDE interface, additional software drivers need to be installed. Contact the vendor of your intended operating system to receive the latest drivers

Chapter 7

7 Watchdog Timer

This chapter explains the operation of the ETX-LX15's watchdog timer. It provides an overview of watchdog operation and features, as well as sample code to help you learn how the watchdog timer works with applications.

7.1 Watchdog Timer Overview

The watchdog timer is implemented by using the ICH4-M ICH integrated watchdog timer. The primary function of the watchdog timer is to monitor the ETX-LX15's operation and take corrective action if the software fails to function as programmed. The major features of the watchdog timer are:

14. Two-stage operation (meaning that it can be enabled to produce a system management interrupt [SMI] or an IRQ (APIC 1, INT 9) before it generates a reset)
15. Enabled and disabled through software control
16. Armed and updated through software control

The watchdog timer drives the First and Second Stages as follows:

1. The watchdog times out (First Stage) after the selected timeout interval.
2. SMI or IRQ is driven high.
3. A hard reset occurs (Second Stage) after the selected timeout interval.

The watchdog timer can have a range from 2.5 seconds to 38 seconds. The timer uses a 6 bit down counter. The counter is loaded with the initial value register. The timer is then enabled and it starts counting down. This is called the first stage. If the counter reaches zero before being reloaded, the watchdog timer generates an internal interrupt. The counter is then loaded with the initial value register and starts counting down. This is called the second stage. If the counter reaches zero before being reloaded, the watchdog timer resets the system.

More information can be obtained from the Intel ICH4-M Datasheet. The "Intel 855GME Chipset" topic in Appendix D provides a link to the ICH4-M datasheet.

7.2 PCI Configuration Registers

The two-stage watchdog timer controller appears in PCI configuration space at Bus:0 Dev:1F Func:0 and in IO address space 0460h.

The following registers are the primary PCI registers to control the watchdog timer.

7.2.1 Watchdog Control Register (Bus:0h Dev:1Fh Func:0h Reg:54h)

Offset:	54h	Size:	8 bits
Default Value:	00h	Attribute:	R/W

Bit	Description
7:4	Reserved
3	**Watchdog Interrupt Enable – (R/W)** 0 = Disables Watchdog interrupt. 1 = Enabled Watchdog interrupt.
2:0	**Watchdog Interrupt Select – (R/W)** This sets which interrupt line the watchdog interrupt will appear on. When the watchdog interrupt is mapped to IRQ 10-11 The signal is active high and cannot be shared with other interrupts. When the watchdog interrupt is mapped to IRQ 20-23, the signal is active low and can be shared with other PCI interrupts 000 = Reserved 001 = IRQ10 010 = IRQ11 011 = Reserved 100 = IRQ20 (Only available in APIC mode) 101 = IRQ21 (Only available in APIC mode) 110 = IRQ22 (Only available in APIC mode) 111 = IRQ23 (Only available in APIC mode)

7.2.2 General Status Register (Bus:0h Dev:1Fh Func:0h Reg:D4h)

Offset:	D4h	Size:	8 bits
Default Value:	0Xh	Attribute:	R/W

Bit	Description
7:2	Reserved
1	**NO_REBOOT – (R/W)** When this bit is set, the watchdog is not allowed to reboot the system.
0	Reserved

7.3 IO Registers

The following registers control the counter values and status of the watchdog timer controller. These register locations are offsets from the value of the base address register. The watchdog base IO address is derived by adding 060h to Bus:0 Dev:1F Func:0 Reg:40-41h. For the ETX-LX15, WDBASE is 0460h.

7.3.1 RLD - Timer Reload and Current Value Register (WDBASE+00h)

Offset:	WDBASE+00h	Size:	8 bits
Default Value:	00h	Attribute:	R/W

Bit	Description
7:6	Reserved
5:0	Reading the register returns the current timer value. Any write to this register will prevent a timeout.

7.3.2 TMR - Timer Initial Value Register (WDBASE+01h)

Offset:	WDBASE+01h	Size:	8 bits
Default Value:	04h	Attribute:	R/W

Bit	Description
7:6	Reserved
5:0	Value that is loaded into the watchdog timer when the RLD register is written. Values 0 and 1 should not be used as they are too small to obtain predictable results. The timer is clocked about every 0.6 seconds, and allows timeouts from 2.4 seconds to 36 seconds.

7.3.3 STS1 - Status Register 1 (WDBASE+04h)

Offset:	WDBASE+04h	Size:	8 bits
Default Value:	00h	Attribute:	R/WC

Bit	Description
7:4	Reserved
3	**Timeout – (R/WC)** This bit is set when the timer reaches 0. It can be cleared by writing a 1.
2:0	Reserved

7.3.4 STS2 - Status Register 2 (WDBASE+06h)

Offset:	WDBASE+06h	Size:	8 bits
Default Value:	00h	Attribute:	R/WC

Bit	Description
7:3	Reserved
2	**BOOT_STATUS – (R/WC)** This bit is set when a system boots with SECOND_TIMEOUT set. It can be cleared by writing a 1.
1	**SECOND_TIMEOUT – (R/WC)** This bit is set when the watchdog timer times out for a second time. It can be cleared by writing a 1.
0	Reserved

7.3.5 CTRL - Control Register (WDBASE+08h)

Offset:	WDBASE+09h	Size:	8 bits
Default Value:	00h	Attribute:	R/W

Bit	Description
7:4	Reserved
3	**TIMER_HALT (R/W)** 0 = The watchdog timer is enabled to count. 1 = The watchdog timer is halted.
2:0	Reserved

7.4 Using the Watchdog in an Application

The following topics are provided to aid you in learning to use watchdog in an application.

7.4.1 Watchdog Reset

An application using the reset feature sets the preload values, enables the watchdog reset, and then periodically reloads the watchdog to keep it from resetting the system. If a reload is missed, the watchdog times out and resets the system hardware.

7.4.2 Watchdog Programming Algorithm

1. Enable the watchdog to cause a reset by clearing bit 1 of Bus:0h Dev:1Fh Func:0h Reg:D4
2. Write the desired watchdog timeout to the Timer Initial Value Register (WDBASE + 1)
3. Write any value to the Timer Reload and Current Value Register (WDBASE + 0) to load the initial watchdog timeout value.
4. Enable the watchdog timer to count by clearing bit 3 of the watchdog Control Register (WDBASE + 9)
5. Write any value to the Timer Reload and Current Value Register (WDBASE + 0) periodically to keep the system from rebooting.

Chapter 8

8 System BIOS

The embedded BIOS on the ETX-LX15 is implemented as firmware that resides in the on-board flash read-only memory (ROM). The BIOS contains standard PC-compatible basic input/output (I/O) services and standard DTI server features.

Support for applicable SBC peripheral devices (SCSI, NIC, video adapters, etc.), that are also loaded into the SBC flash ROM, will not be specified in this document. Hooks are provided to support adding BIOS code for these adapters.

8.1 BIOS Upgrade and Recovery

To reprogram or update the BIOS if it becomes corrupted, use the DTIFLASH.EXE utility available from DTI and discussed later in this chapter.

8.1.1 Flash Utility Program

DTIFLASH.EXE is a utility program that can be obtained from DTI in the event a BIOS should be updated. Run DTIFLASH.EXE to modify the BIOS in the on-board flash memory. DTIFLASH.EXE eliminates the need for a PROM programmer and for removing boards and chips from the system.

To reprogram the BIOS, you should do the following:

1) The latest flash will be distributed via a Customer Service Alert Notification. Normally, the BIOS zip file also contains the DTIFLASH.EXE utility you need.
2) Create a DOS 6.2 boot disk and add the BIOS file and flash utility to the disk. Usually other Windows* boot disks will work fine as well, but use DOS if you run into any problems.
3) Boot the board from the DOS boot disk you just created. You can do this via a USB Floppy. If your system does not boot off the floppy you may need to enter the BIOS setup in order to move the floppy to the first item in the boot order.
4) Use the following syntax at a DOS prompt:
   DTIFLASH

The BIOS zip file should also contain a Readme file or installation file to help guide you through BIOS installation.

8.1.2 BIOS Recovery

In the event that the contents of the BIOS ROM are corrupted, there is a mechanism to recover the BIOS ROM using the BIOS recovery code.

To reprogram corrupted BIOS, you should do the following:

1) The latest flash will be distributed via a Customer Service Alert Notification.
2) Format a disk and copy only the BIOS ROM file to the disk.
3) Power on the board with the disk installed.
4) Press CTRL+HOME keys during power on. The board will enter automatic update mode and program the file from the disk. There will be no video displayed, but activity should be seen on the disk and the POST LEDs.
5) The board will automatically reboot after complete.

8.2 BIOS Configuration Overview

This topic presents a brief introduction to the DTI Embedded BIOS.

The DTI BIOS Software supports all of the IBM /AT standard functions and several unique functions and features. Features of the DTI BIOS include built-in utilities, help windows, and system monitoring functions.

Upon initial power up or after a hardware reset, the processor begins executing code out of the onboard BIOS. The BIOS contains all of the software needed to boot the board to a working state so an operating system can be loaded. The first order of business for the BIOS is to initialize crucial system components, such as timers and chipset parts. The BIOS then performs basic components checks to ensure their presence and then sets them to a default state. Next, the cache and memory controllers must be initialized and configured for the type and configuration of the cache and memory found in the system.

Once the memory is present, the compressed portions of the BIOS are de-compressed into the shadow memory occupying the standard BIOS memory ranges. The BIOS can now scan for and initialize other interfaces such as I/O devices and items on the PCI or ISA busses.

If a video adapter is in the system it is located and initialized. The video adapter will sign-on and its manufacturer, chip type, and creation date will appear on the screen. The BIOS will then display its sign-on information giving copyright information, the board name, and the version of the BIOS present in the system. At this point the following message will appear at the bottom of the screen giving the hotkey that will invoke the setup engine.

<F2> Enter Setup <SPACE> Skip Memory <ESC> BOOT Menu

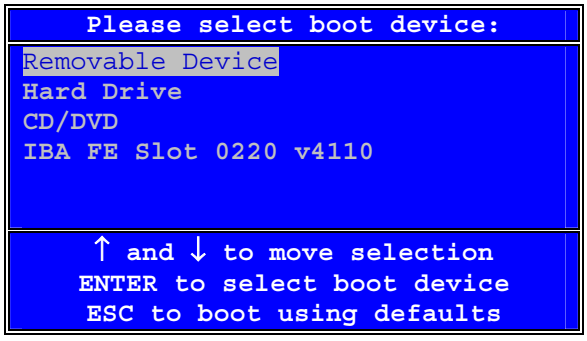
If the F2 key is pressed, the message below will be displayed and the ROM UTILITIES will be entered after the option ROM scan.

Entering Setup…..

The BIOS now starts to size and clear all system memory, displaying its progress on the screen. The BIOS will then sign-on any ISA or PCI option ROMs found on devices in the system. If the F2 key was pressed during POST; the ROM Utilities will be executed.

8.2.1 Boot Menu

During POST display, the ESC key can be pressed to invoke the multi-boot menu. The menu will appear near the end of POST, before the system summary screen is displayed, and after the option ROMs have signed on. The multi-boot menu allows interactive selection of the boot device. The list is typically in the following categorical order:



The up and down arrows on the keyboard can be used to highlight the device to boot from, and then press <Enter> to boot from it. Removable devices are the floppy drive, or other installed removable

media, e.g., ZIP drives. Hard drives are any fixed disk (IDE, SCSI) in the system. Other devices may appear in the list, such as Ethernet boot ROM agents from add-in cards. To change the boot order of devices within a category (such as to boot from IDE hard drive instead of SCSI), or to permanently change the boot order, you will have to enter SETUP and change the boot options.

If any errors are detected up to this point they will now be displayed on the screen along with the following prompt to direct further actions. Pressing F1 will ignore the errors and continue with the boot process. The F2 key can be pressed to enter the ROM UTILITIES and possibly resolve any configuration error that may have been made.

Press F2 to Run SETUP

Press F1 to load default values and continue

If the F2 key was not pressed, and no errors were detected, the system summary screen will be displayed. After 10 seconds or upon a key press the BIOS will attempt to boot the installed operating system.

The System BIOS is compatible with the Plug and Play Specification Version 1.0A. The two areas that are addressed by the System BIOS are Resource Management and Runtime Services.

Resource Management provides the ability to manage the fundamental system resources, which include DMA, Interrupt Request Lines (IRQs), I/O and Memory addresses. These resources, termed system resources, are in high demand and commonly are over allocated or allocated in a conflicting manner in ISA systems, leading to system configuration failures.

The resource manager takes on the responsibility for configuring Plug and Play cards, as well as system board devices during the power up phase. After the Power-On Self Test (POST) process is complete, control of the Plug and Play device configuration passes from the system BIOS to the system software. The BIOS does, however, provide configuration services for system board devices even after the POST process is complete. These services are known as Runtime Services.

Runtime Services provide a mechanism whereby a Plug and Play operating system, such as Windows 2000, may perform resource allocation dynamically at runtime. The operating system may directly manipulate the configuration of devices that have traditionally been considered static.

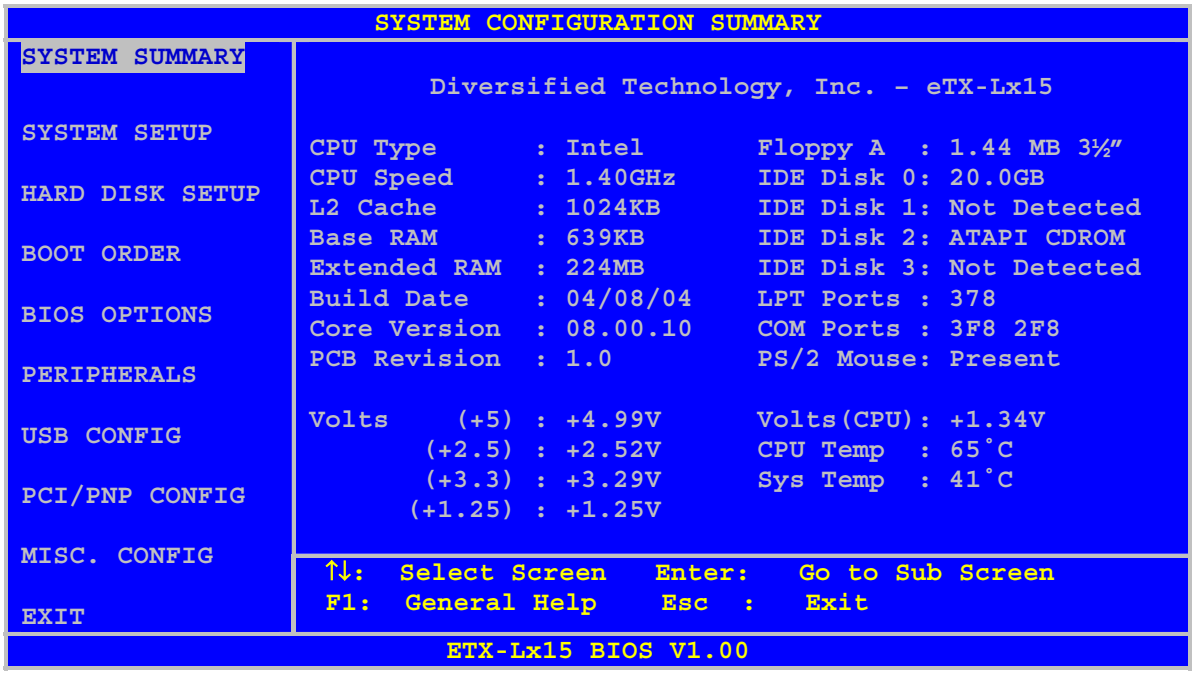
8.2.2 ROM Utilities

The ROM Utilities consist of various easy-to-use utilities required in the configuration of the board. The function of each utility is briefly described below. Battery backed CMOS RAM is used to store the configuration/setup parameters selected in the ROM Utilities. On power-up the CMOS RAM parameters are used to configure the system. If the CMOS RAM is corrupt, default parameters stored in ROM are used to configure the system. If no errors occurred during the POST, the System Configuration Summary Screen will be displayed as shown on the next page. Else, ROM Utility configuration errors detected during the POST will be displayed and the default values loaded. As each utility is selected using the arrow keys, the contents of the utility will be displayed. This allows the user to view the current settings of each utility without having to actually execute the utility. To execute a specific utility, either press the function key associated with the utility or move the highlighted bar onto the utility and press <ENTER>.

ROM Utilities	
SYSTEM SUMMARY	Displays various information about the system installed
SYSTEM SETUP	Used to configure the time/date and floppy drive types
HARD DISK SETUP	Used to configure the hard drive types
BOOT ORDER	Used to specify boot device ordering
BIOS OPTIONS	Used to setup various BIOS features
PERIPHERALS	Used to enable/disable onboard I/O devices
USB CONFIG	Used to configure USB devices
PCI/PNP CONFIG	Configure PCI interrupt lines
PNP EXCLUSIONS	Specify used non-PNP ISA resources
EVENT LOGGING	Used to view and control the system event log
SECURITY/VIRUS	Used to set system passwords and anti-virus options
EXIT	Used to exit ROM utilities

8.2.3 System Summary

The System Configuration Summary utility provides valuable information about the system. The information supplied can also be useful in determining items that are present in the systems and how they are configured. The System Configuration Summary screen is shown below, followed by a brief description of information supplied.

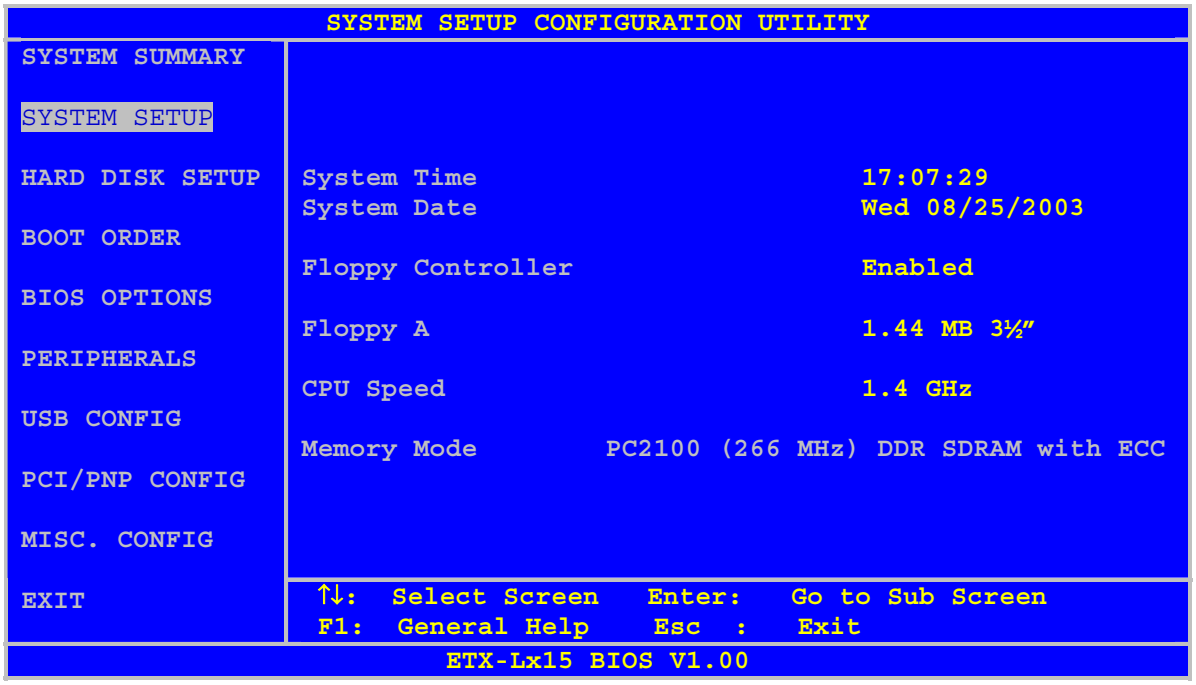


System Summary Descriptions

CPU Type:	Displays the type of processor installed.
CPU Speed:	Displays the speed of logical processor installed.
L2 Cache:	Displays the amount of L2 cache detected.
Base RAM:	Displays the amount of installed system RAM up to 640KB.
Extended RAM:	Displays the amount of installed extended RAM beyond 1024 KB.
Build Date:	Displays the date on which the BIOS was generated.
Core Version:	Displays the version of the AMI BIOS core.
PCB Revision:	Displays the PCB board revision level.
Floppy A:	Displays the media type selected for the floppy drive.
IDE Disk 0 - 3:	Displays the drive type selected for the IDE drive.
COM Ports:	Displays the I/O addresses of all installed serial ports.
LPT Ports:	Displays the I/O addresses of all installed parallel ports.
PS/2 Mouse:	Displays whether or not a mouse was detected by the BIOS during the POST.
Volts	Displays the current status of the system and CPU voltage sources.
Temperatures:	Displays the current CPU and ambient temperatures of the board.

8.2.4 System Setup

The System Setup Configuration Utility is used to configure the system time/date and the type of floppy disk installed.

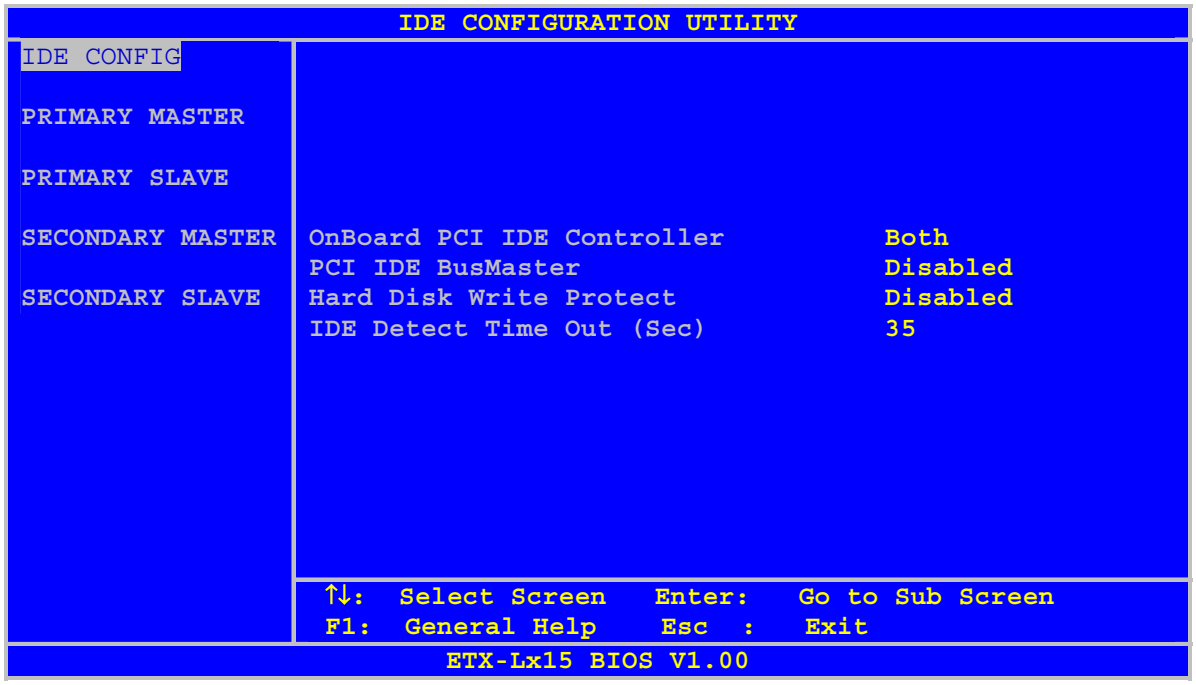


System Setup Descriptions

System Time:	A new time is set by typing in the HOUR, MINUTE, and SECONDS each followed by pressing < ENTER >. The time is displayed in 24-hour format; therefore, AM hours range from 0 through 11 and the PM hours range from 12 through 23. Invalid times cannot be entered.
System Date:	A new date is set by tying in the MONTH, DAY, and YEAR each followed by pressing <ENTER >. If one of the parameters is out of range, the new date will not be entered.
Floppy Controller:	This option enables or disables the onboard floppy controller. It will also allow enabling certain baseboard SIO floppy controllers.
Floppy A:	Drive types 360K, 720K, 1.2M, and 1.44M are supported. A DISABLED option is also available for diskless workstations. No floppy error messages will be displayed if DISABLED is selected.
CPU Speed	This item sets the operating speed for the processor. Higher speed requires more power, lower speeds requires less power.
Memory Mode	Displays the type, operating frequency, and ECC availability of the installed memory.

8.2.5 IDE Configuration

The IDE Configuration Utility is used to configure the hard drive controller and interface properties for the system. The following page describes the configuration options.

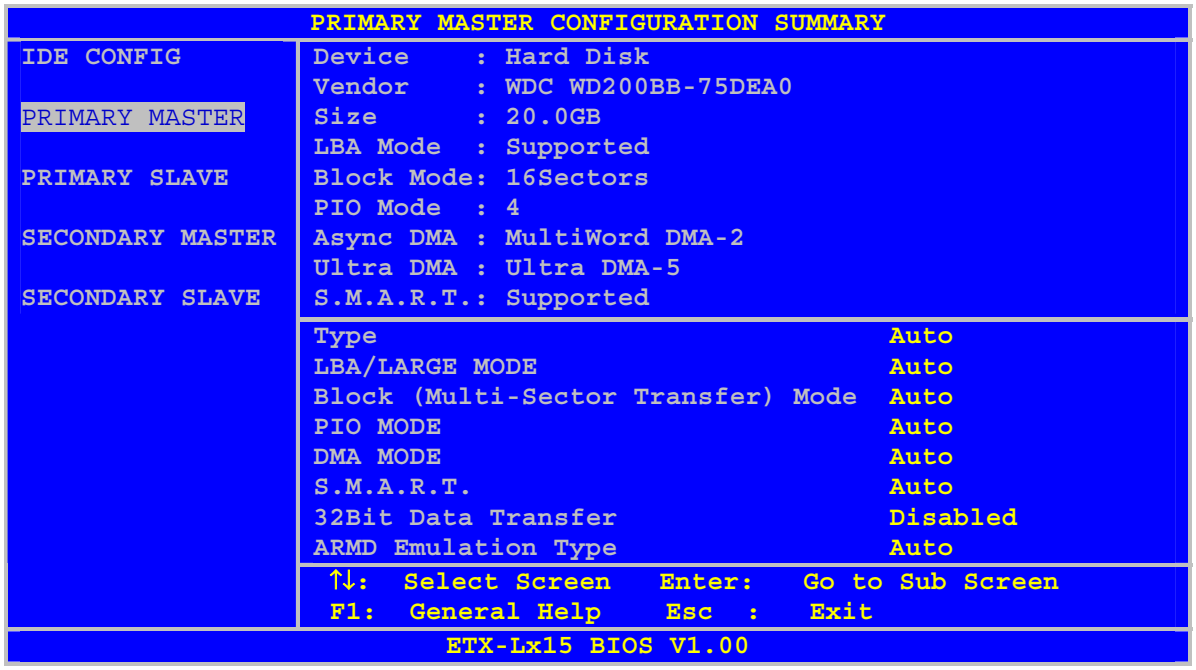


IDE Configuration Descriptions

Onboard PCI IDE Controller:	This item enables or disables the onboard PCI IDE controllers. Supported options include disabled, enable primary only, enable secondary only, and enable both controllers.
PCI IDE BusMaster:	When this item is enabled, the BIOS uses PCI bus mastering for accesses to IDE drives.
Hard Disk Write Protect:	When this item is enabled, the BIOS protects the IDE drives from write accesses. This is only effective for operating systems that access the hard drives using BIOS interfaces.
IDE Detect Time Out:	This item specifies the maximum amount of time that the BIOS will attempt to search for IDE devices.

8.2.6 Hard Disk Setup

The Hard Drive Configuration Utility is used to configure the hard drives installed in the system. The following page describes the configuration options.



Hard Drive Setup Descriptions

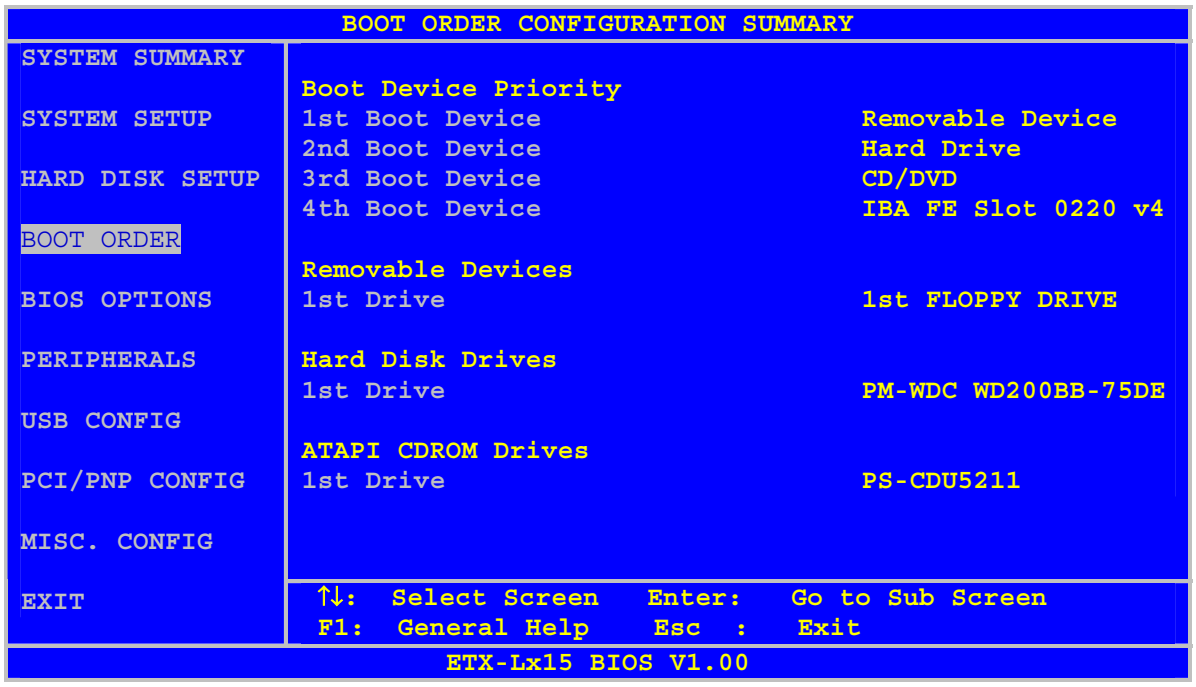
The configuration options described below work identically for HARD DRIVES 0 - 3.

Device:	Displays the type of IDE device currently installed. Type choices include Not Installed, Hard Disk, ATAPI CDROM, and ARMD.
Vendor:	Displays the manufacturer device identification information.
Size:	Displays the storage capacity of the device.
LBA Mode:	Displays support for Logical Block Accessing. LBA uses 28-bit addressing of the hard disk instead of CHS (Cylinder/Head/Sector) addressing for supporting drives up to 137GB.
Block Mode:	Displays the maximum Block Mode transfer for the device.
PIO Mode:	Displays the maximum PIO supported by the device.
Async DMA:	Displays the highest support Asynchronous DMA Mode.
Ultra DMA:	Displays the highest support Synchronous DMA Mode.
S.M.A.R.T.:	Displays device support for Self-Monitoring Analysis and Reporting Technology. This protocol allows detection of drive errors.

Type:	Selects the type of IDE device. Type choices include Not Installed, Auto, CDROM, and ARMD. If AUTO type is selected, the hard drive parameters are read during boot-up, and are configured automatically. The hard drive information, such as manufacturer and model number, is displayed during POST. The CDROM type will enable bootable CD-ROM support for an IDE CDROM drive attached as a master or slave. An IDE CD-ROM can be made the boot device through the BOOT OPTIONS screen. The ARMD type is selected when an ATAPI Removable Media Device is present. This includes drives for high capacity floppies that can be formatted as floppies or hard disks, e.g., LS120, IOMega Zip, Fujitsu MO, and certain FLASH devices.
32BIT Data Transfer:	Controls support for 32Bit IDE transfers.
ARMD Emulation Type:	Specifies the type of emulation used.

8.2.7 Boot Order

The Boot Order Configuration Utility is used to determine the order in which the BIOS attempts to boot from devices. The BIOS attempts to boot from the devices at the top of the list first. If the device is not bootable, then the next item down in the list is tried. Removable Devices and Hard Disks have further ordering within their category. The following page describes the configuration options. The ESC key can be pressed during POST to display a boot device menu. This will over-ride the boot order chosen in the CMOS Setup Utility and boot from the device selected.

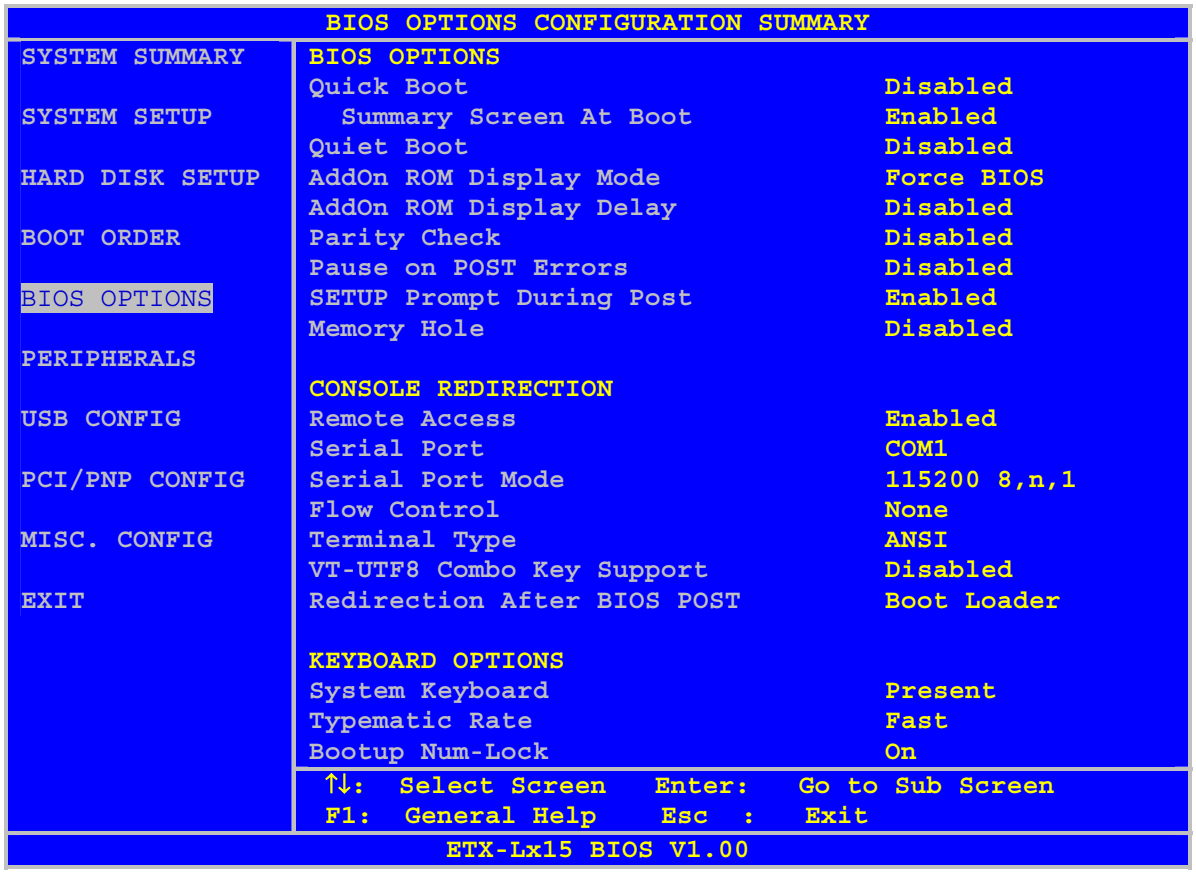


Boot Order Descriptions

Boot Device Priority:	Selects the boot order for installed boot devices. The BIOS attempts to boot from items at the top of the list first.
Removable Devices:	Boot from legacy floppy diskette, removable LS-120, or ZIP drives. The desired removable device must be selected.
Hard Disk Devices:	Boot from hard disk drive. The desired hard drive must be selected through Hard Disk Drives.
ATAPI CDROM Drives:	Boot from an IDE CDROM.

8.2.8 BIOS Options

The BIOS Options Configuration Utility provides various features which affect features provided by the BIOS.



BIOS Options Descriptions

Quick Boot:	Allows the BIOS to skip certain tests while booting. This decreases the amount of time needed to boot the system.
Summary Screen At Boot:	When this option is enabled, the system summary information will be displayed before the system boots.
Quiet Boot:	When enabled displays a graphic during POST instead of the normal POST information.
AddOn ROM Display Mode:	Selects the display mode used by the BIOS when signing on option ROMs.
AddOn ROM Display Delay:	When this item is enabled, the BIOS will insert a brief pause after each option ROM signs on. This is useful to allow viewing any errors or messages that may otherwise be missed.

Parity Check:	Enable system support for parity error checking.
Pause On Post Errors:	This option determines whether the POST will pause and wait for user input when an error occurs.
Prompt During Post:	When this option is enabled, the prompt that displays the key needed to enter SETUP will be displayed during the POST.
After Power Loss:	This option will determine the power state after a total power loss. The possible states include power on, last state, and stay off.
Memory Hole:	This item enables a 1MB memory hole to the ISA bus in the 15-16 MB range.

Console Redirection Descriptions

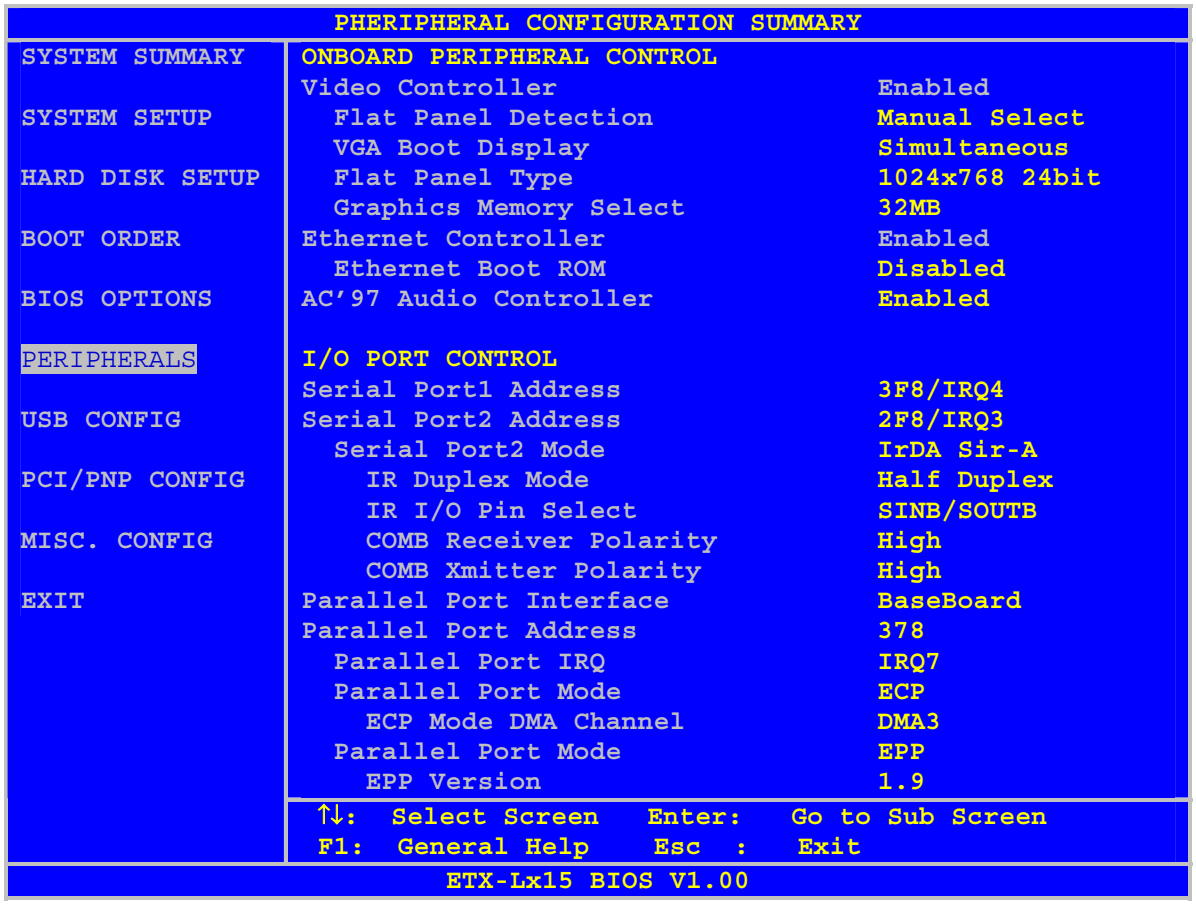
Remote Access:	This item allows serial console redirection to be enabled. This allows all video output to be redirected through the serial port during the POST and DOS. In addition, input through the serial port will be used through the POST and DOS.
Serial Port:	Specifies the serial port to be used for console redirection.
Serial Port Mode:	Selects the baud rate for console redirection. The possible baud rates are: 9600, 19200, 38400, and 115200.
Flow Control:	This item allows hardware flow control to be used.
Terminal Type:	Selects between ANSI and VT100 terminal types.
VT-UTF8 Combo Key Support:	This item allows VT-UTF8 Combination Key support for ANSI/VT100 terminals.
Redirection After BIOS Post:	Control if console redirection is to be used after POST.

Keyboard Options Descriptions

System Keyboard:	Used to specify if a keyboard is present to the system.
Typematic Rate:	Specifies the rate at which keys repeat if a key is held down.
Bootup Num-Lock:	Specifies the state of the Num-Lock key to be set when the system boots.

8.2.9 Peripherals

The Peripheral Configuration Utility allows onboard devices to be enabled, disabled, or configured. The onboard programmable I/O adapter includes a floppy disk interface, two serial ports, and a parallel printer port.



Onboard Peripheral Control Descriptions

Video Controller:	This item displays the current state of the onboard video controller. This onboard video controller can be disabled via a hardware jumper.
Flat Panel Detection	This item specifies the method used for determining the flat panel type. The available options are No Flat Panel, Manual Select, and Jili EEPROM.
VGA Boot Display:	Selects the boot display used by the video controller. The available options are CRT, Flat Panel, and Simultaneous.
Flat Panel Type:	If the Flat Panel Detection item is set for Manual Select, this item is used to specify the type of flat panel installed.
Ethernet Controller:	This item displays the current state of the onboard Ethernet controller. The onboard Ethernet controller cannot be disabled.
Ethernet Boot ROM:	Controls the embedded Ethernet boot ROM allowing for remote network booting.
AC'97 Audio Controller:	Controls whether the onboard AC'97 Audio controller is enabled.

I/O Port Control Descriptions

Serial Port 1 & 2 Address: The two serial ports can be configured to one of four possible settings or disabled.

I/O Address	Interrupt	COM Port
3F8h	IRQ4	COM1
2F8h	IRQ3	COM2
3E8h	IRQ4	COM3
2E8h	IRQ3	COM4

Serial Port 2 Mode: This item allows the user to select the mode for serial port 2. Options include Normal, IrDA Sir-A, ASK IR, IrDA Sir-B, Consumer, and Raw Ir.

IR Duplex Mode: This item allows for the selection of full or half duplex for serial port 2.

IR I/O Pin Select: This item allows for receive and transmit pin selection for serial port 2. SINB/SOUT selects the serial port TXD2 and RXD2 pins. IRRX/IRTX selects the alternate IRRX and IRTX pins.

ComB Receiver Polarity: This item allows for the selection of active high or active low for serial port 2 receiver polarity.

ComB Xmitter Polarity: This item allows for the selection of active high or active low for serial port 2 transmitter polarity.

Parallel Port Interface: The parallel port interface can be used to function as a parallel interface or a floppy interface. Both onboard interfaces cannot function at the same time. Options include force to floppy, force to parallel, and Baseboard. The Baseboard option allows the parallel interface functionality to be configured by an ETX defined jumper on the baseboard.

Parallel Port Address: Use this item to enable or disable the onboard parallel port. Three possible I/O base addresses are 378h, 3BCh, or 278h.

Parallel Port IRQ: Use this item to select the interrupt for the parallel port. The possible interrupts are IRQ5 or IRQ7.

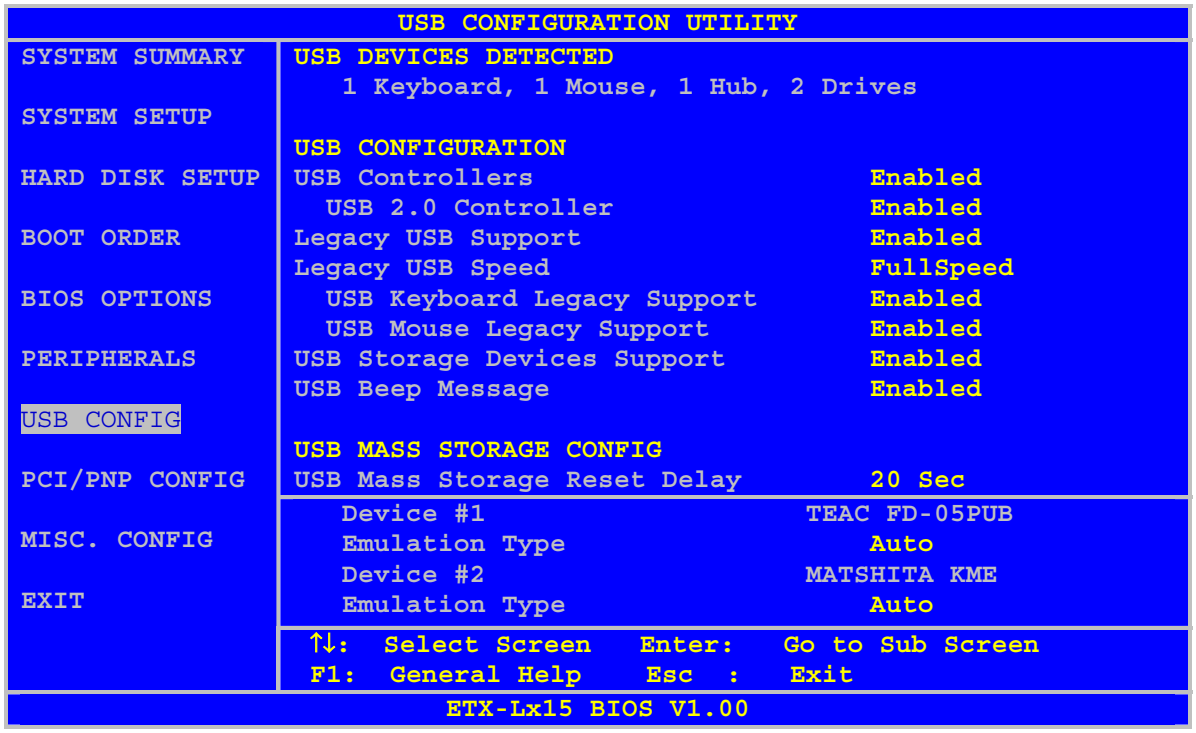
Parallel Port Mode: In “Output Only” mode the LPT port functions like a standard printer port. Three other available modes are Bi-Directional, ECP, and EPP.

ECP Mode DMA Channel: The DMA channel used in ECP mode can be routed to DMA channel 0, 1, or 3.

EPP Version: When in EPP mode the EPP version can be selected. The possible options are 1.7 and 1.9.

8.2.10 USB Configuration

The USB Configuration Utility allows control of the board's USB features.



USB Devices Detected Descriptions

USB Devices Detected:	Displays a list of the USB devices that have been detected.

USB Control Descriptions

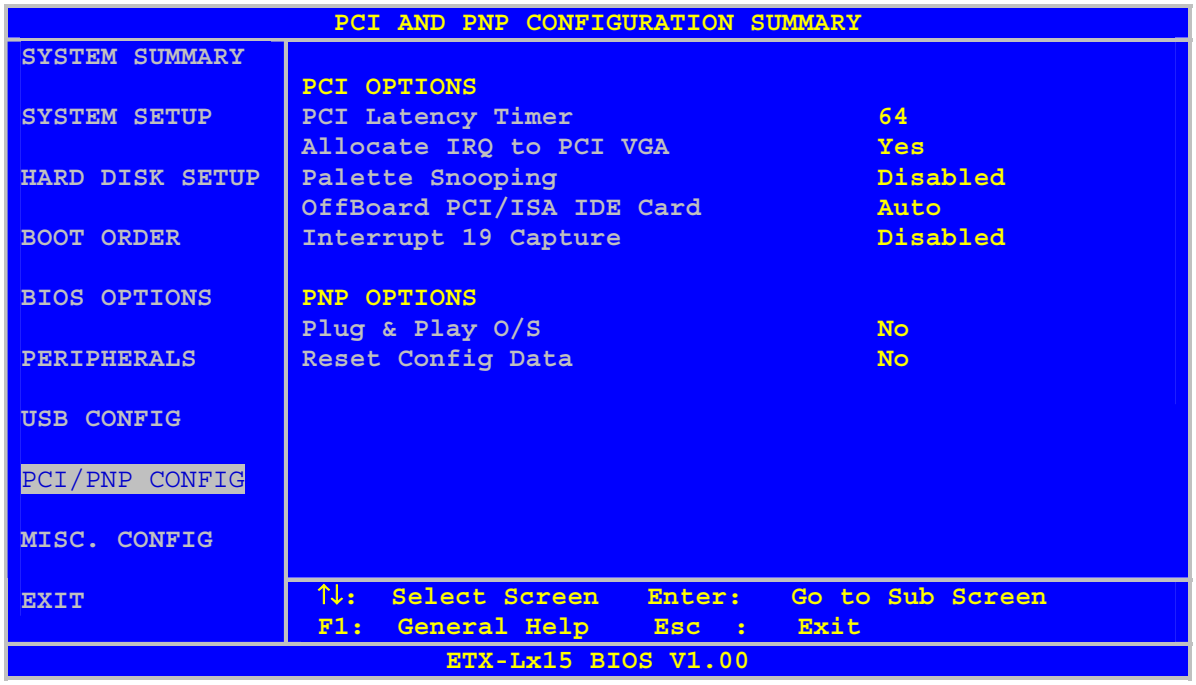
USB Controllers	This item controls the onboard USB functions. The USB ports are not usable when this item is disabled.
USB 2.0 Controllers	This item controls the onboard USB 2.0 function. USB 2.0 is not supported when this item is disabled.
Legacy USB Support:	Enables support for legacy USB devices.
Legacy USB Speed	Selects the operating speed for USB legacy devices. Options are HiSpeed (480Mbps) and FullSpeed (12Mbps). Use FullSpeed if problems are encountered with a USB device running at HiSpeed.
USB Keyboard Legacy Support:	Controls legacy support for USB keyboard.
USB Mouse Legacy Support:	Controls legacy support for USB mouse.
USB Storage Device Support:	Controls support for USB mass storage devices.
USB Beep Message:	Enables a beep during USB device enumeration.

USB Mass Storage Configuration Descriptions

USB Mass Storage Reset Delay:	Number of seconds to wait for a USB mass storage device after sending the start unit command.
Emulation Type:	Specifies the method used to determine the type of USB mass storage devices connected.

8.2.11 PCI/PNP Configuration

The PCI and PNP Configuration Utility allows configuration of the PCI bus, PNP options, as well as ACPI related items.



PCI Options Descriptions

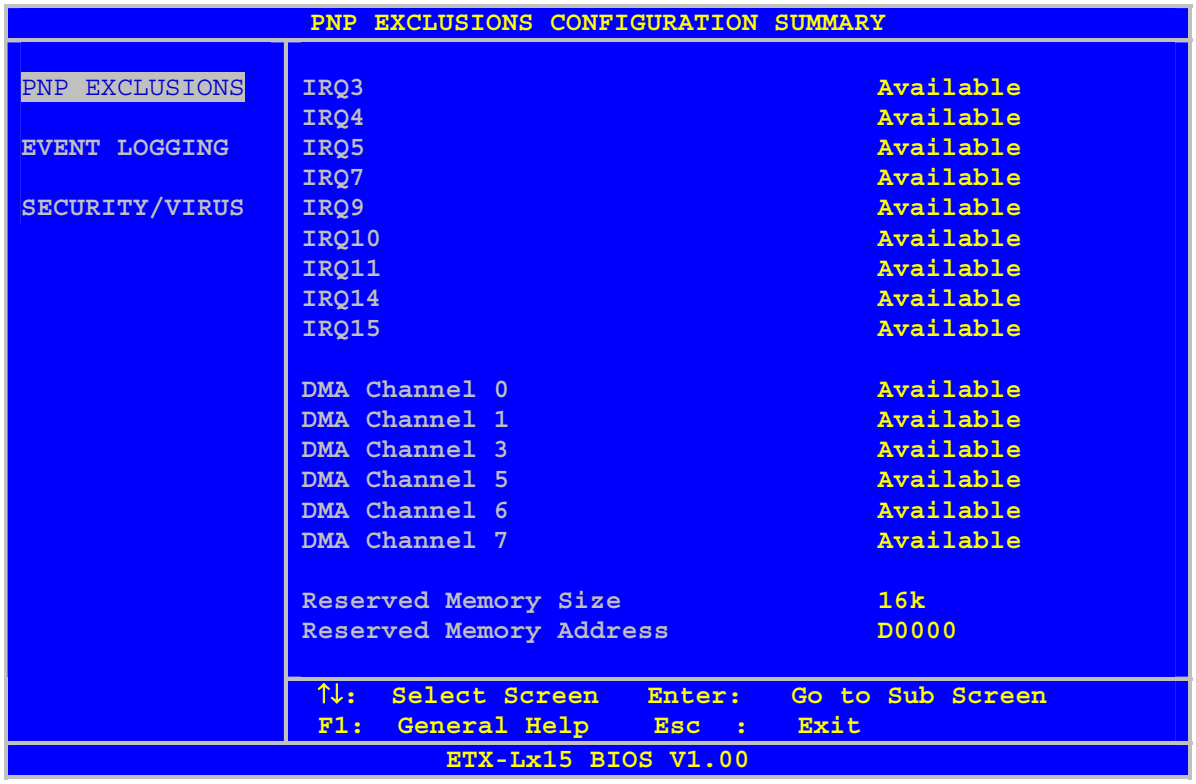
PCI Latency Timer:	This option is used to set the desired PCI latency for all devices on the PCI bus.
Allocate IRQ to PCI VGA:	This item allows the system to restrict PCI video from being assigned an interrupt.
Palette Snooping:	This item allows some PCI video cards to operate in combination with an ISA video card. Only enable this item if instructed to by the video card manufacturer.
OffBoard PCI/ISA IDE Card:	Use this item to specify the presence of an offboard PCI IDE card.
Interrupt 19 Capture:	This item allows option ROMs to capture interrupt 19 for use in booting.

PNP Options Descriptions

Plug & Play O/S:	If disabled (default), the BIOS will set up any plug & play devices. If enabled, the operating system is assumed to configure plug & play devices.
Reset Configuration Data:	If set to “Yes”, the plug & play configuration is reset after leaving SETUP. This option is automatically reset to “No”.

8.2.12 PNP Exclusions

The PCI EXCLUSIONS CONFIGURATION UTILITY is used to tell the BIOS which resources are used by non-PNP ISA cards. This information is used by the BIOS to inform the user of resource conflicts. If non-PNP ISA resources are not specified, the BIOS could give resources to a PNP or PCI device that are already in use by some non-PNP ISA card. Set any memory, interrupts, or DMA resources used by non-PNP ISA cards to reserved.

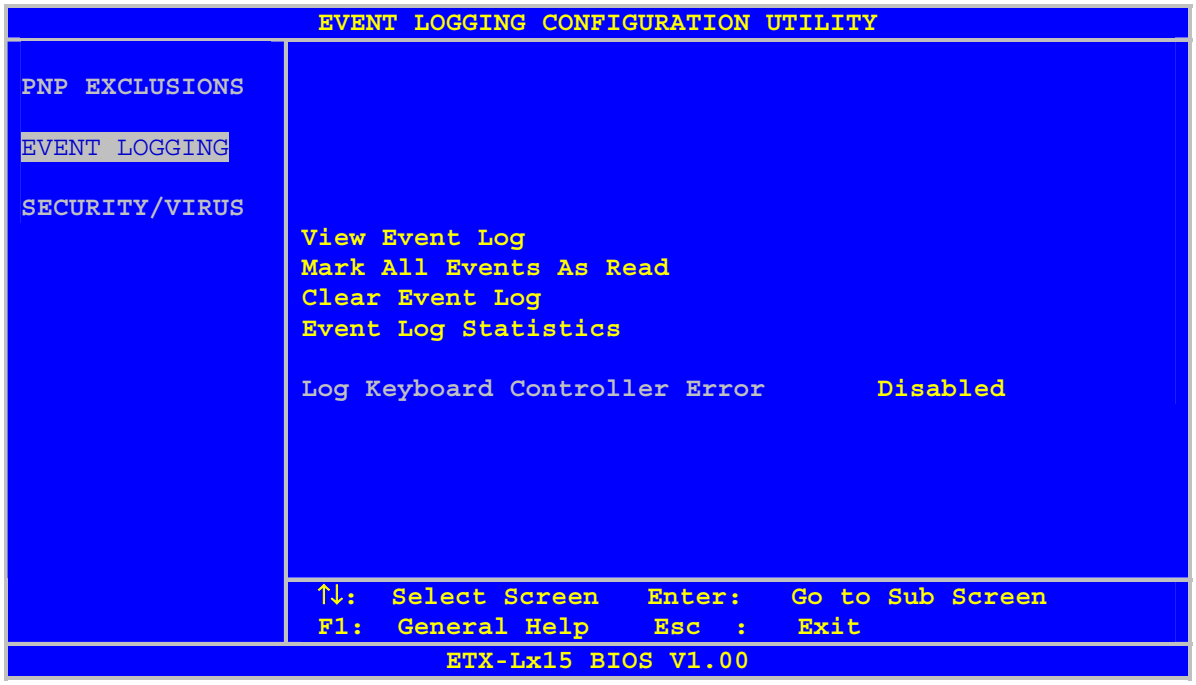


PNP Exclusions Descriptions

ISA IRQS:	This section is used to reserve interrupts for use by non-PNP ISA cards.
ISA DMA:	This section is used to reserve DMA channels for use by non-PNP ISA cards.
Reserved Memory:	This section is used to reserve upper memory blocks (UMBs) for use by non-PNP ISA cards. A block can be reserved in 16K increments from C000h to DFFFh.

8.2.13 Event Logging

The Event Logging Configuration Utility is used to configure and view system events that have been logged.

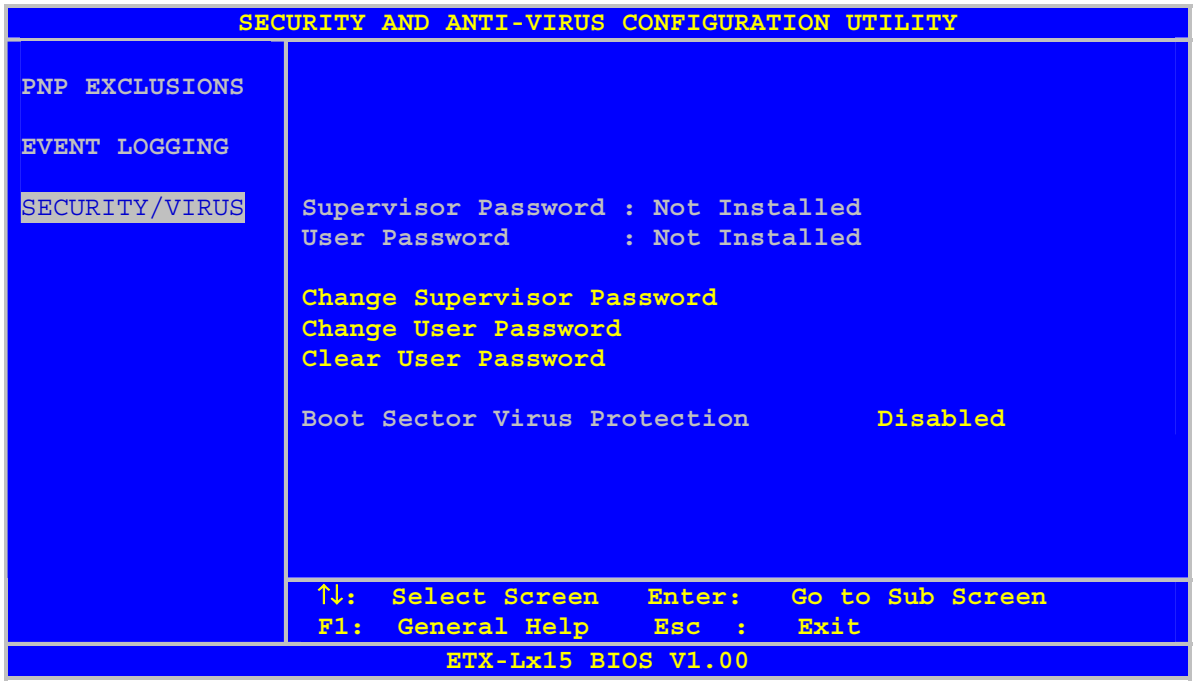


Event Logging Descriptions

View Event Log:	This item is used to open a window containing a list of the currently logged system events.
Mark All Events As Read:	This item is used the mark all system events in the log as read.
Clear Event Log:	This item is used to erase all events from the system log.
Event Log Statistics:	This item is used to view statistics about the system event log.
Log Keyboard Controller Error:	This option controls whether or not keyboard controller errors are recorded in the event log. Keyboard controller errors typically occur when a keyboard is not plugged in. By disabling this option, the event log will not be filled with keyboard controller errors if a system will normally not have a keyboard attached.

8.2.14 Security/Virus

The Security and Anti-Virus Configuration Utility is used to set system passwords and control system anti-virus items.

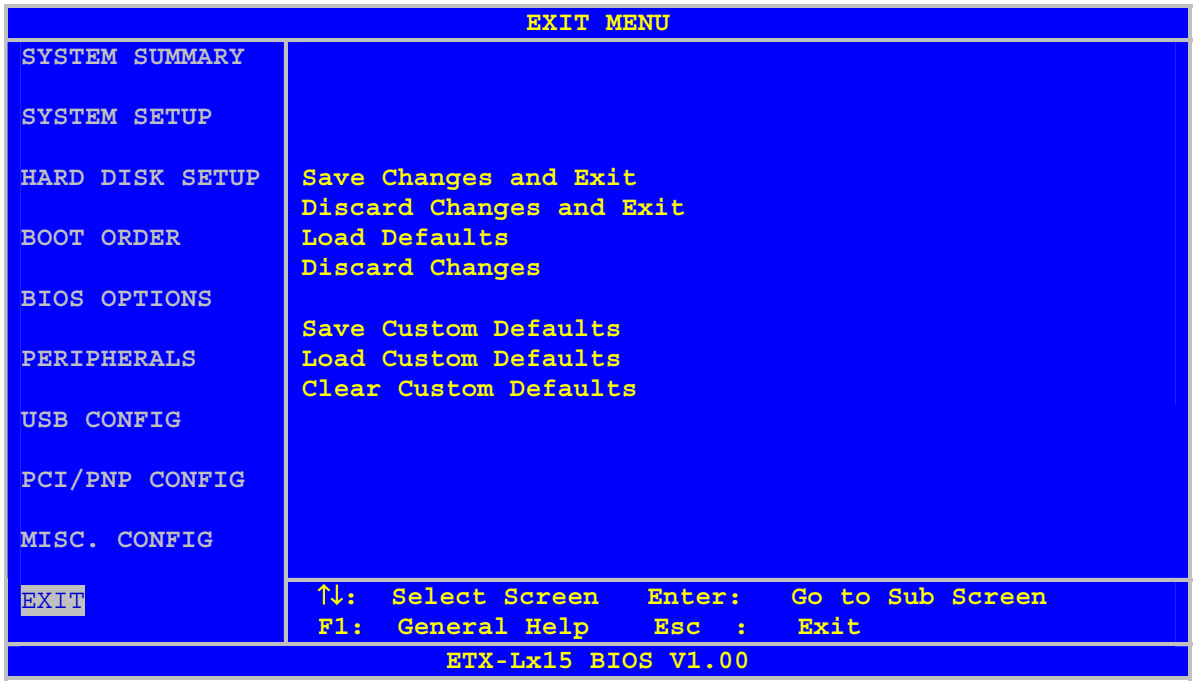


Security/Virus Descriptions

Supervisor Password:	This item indicates whether a supervisor password has been set.
User Password:	This item indicates whether a user password has been set.
Change Supervisor Password:	This item allows setting the supervisor password.
Change User Password:	This item allows setting the user password.
Clear User Password:	This item is used to clear the user password.
Boot Sector Virus Protection:	When this item is enabled, a warning message is displayed before any program tries to access the boot sector.

8.2.15 Exit

The Exit Menu provides a way to exit setup and save or discard changes. It also provides a way to load the default settings stored in the BIOS. Custom Defaults allows CMOS default settings to be saved in non-volatile storage. These Custom Defaults override the standard defaults whenever the CMOS battery is lost.



Exit Description

Save Changes and Exit:	Exits SETUP and saves all changes to CMOS.
Discard Changes and Exit:	Exits SETUP and discards any changes.
Load Defaults:	Loads the SETUP factory default values.
Discard Changes:	Discard any changes made during SETUP.
Save Custom CMOS:	Save current CMOS settings into non-volatile storage.
Load Custom CMOS:	Load previously stored CMOS settings from non-volatile storage.
Clear Custom CMOS:	Clear custom CMOS non-volatile storage area.

8.3 Plug and Play (PnP)

The system BIOS supports the following industry standards for making the system “Plug and Play ready” such as ACPI, PCI local bus specification rev 2.1 and SMBIOS 1.

8.3.1 Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with industry specifications. The BIOS scans, in order, for the following:

ISA devices: Resources for ISA devices that are PNP compatible will be automatically assigned by the BIOS. Resources that are required by non-PNP compatible ISA devices need to be specified in the BIOS Setup utility.

Add-in video graphics adapter (VGA) devices: If found, the BIOS initializes and allocates resources to these devices.

PCI Devices: The BIOS allocates resources according to the parameters set up by the SSU and as required by the *PCI Local Bus Specification*, Revision 2.1.

The system BIOS Power-on Self Test (POST) guarantees that there are no resource conflicts prior to booting the system. Please note that PCI device drivers are required to support the sharing of IRQs. Sharing PCI IRQs should not be considered a resource conflict. Note that only four legacy IRQs are available for use by PCI devices; as a result, most PCI devices will share an IRQ.

8.3.2 PnP ISA Auto-configuration

The system BIOS:

Supports relevant portions of the *Plug and Play ISA Specification*, Revision 1.0a and the *Plug and Play BIOS Specification*, Revision 1.0A.

Assigns I/O, memory, direct memory access (DMA) channels, and IRQs from the system resource pool to the embedded PnP Super I/O device.

8.3.3 PCI Auto-configuration

The system BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the *PCI Local Bus Specification*, Revision 2.1. The system BIOS also supports the 16 and 32-bit protected mode interfaces as required by the *PCI BIOS Specification*, *Revision 2.1*.

Beginning at the lowest device, the BIOS uses a “depth-first” scan algorithm to enumerate the PCI buses. Each time a bridge device is located, the bus number is incremented and scanning continues on the secondary side of the bridge before all devices are scanned on the current bus. The BIOS then scans for PCI devices using a “breadth-first” search – all devices on a given bus are scanned from lowest to highest before the next bus number is scanned.

System BIOS POST maps each device into memory and/or I/O space, and assigns IRQ channels as required. The BIOS programs the PCI-ISA interrupt routing logic in the chipset hardware to steer PCI interrupts to compatible ISA IRQs.

The BIOS dispatches any option ROM code for PCI devices to the DOS compatibility hole (C0000h to DFFFFh) and transfers control to the entry point. The DOS compatibility hole is a limited resource; therefore, system configurations with a large number of PCI devices may result in a shortage of this resource. If the BIOS runs out of option ROM space, some PCI option ROMs are not executed and a POST error is generated.

Drivers and/or the OS can detect the installed devices and determine resource consumption using the defined PCI, legacy PnP BIOS, and/or ACPI BIOS interface functions.

8.3.4 Legacy ISA Configuration

ISA devices that are PNP compatible will be recognized by the BIOS and assigned resources automatically. Non-PNP compatible ISA device resources need to be specified in the BIOS Setup section "PNP EXCLUSIONS". This allows the BIOS to reserve these resources so on-board devices do not use them.

8.3.5 Automatic Detection of Video Adapters

The BIOS detects video adapters in the following order:

Off-board PCI

Onboard PCI

The onboard (or offboard) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to off-board devices.

8.4 Console Redirection

Console redirection allows users to monitor the ETX-LX15's boot process and to run the ETX-LX15's Setup utility from a remote serial terminal. Connection is made either directly through a serial port or through a modem.

The console redirection feature is most useful in cases where it is necessary to communicate with a processor board, such as the ETX-LX15, in an embedded application without video support.

The BIOS supports redirection of both video and keyboard via a serial link (COM 1 or COM 2). When console redirection is enabled in BIOS setup, local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Setup and any other text-based utilities can be accessed via console redirection.

8.5 System Management BIOS (SMBIOS)

The ETX-LX15 follows the criteria outlined in the *System Management BIOS Reference Specification, Version 2.3*. Refer to this specification for details on SMBIOS.

8.6 POST CODE LEDS (DTI Baseboard Only)

Four surface-mounted LEDS are located on DTI baseboards for the ETX-LX15 that indicate the post/board status. The LEDS are arranged from the most significant bit (MSB) to the least significant bit (LSB), and a color scheme is used to identify the bit values. For instance, the LED will be lit RED when one of the upper four bits is high and will be lit GREEN when one of the lower bits is high. The upper and lower bits will be represented simultaneously by the LEDS. Thus, the LED will appear ORANGE if one of the upper and lower bits is both high in the same bit location. These eight bits represent a binary number, and if that binary number is converted into a hexadecimal number you'll have the failing code if the board fails to boot. An example illustrating this is provided below.

LED Color Description

R=RED G=GREEN O=ORANGE F=OFF

Bit in the *upper nibble* is high:

POST CODE 20 --- BIT values (MSB to LSB) 0010 0000

I I

Upper Nibble Lower Nibble

LEDS Status MSB to LSB

Visible colors: FFRF (Off Off Red Off)

Bit in the *lower nibble* is high:

POST CODE 02--- BIT values (MSB to LSB) 0000 0010

I I

Upper Nibble Lower Nibble

LEDS Status MSB to LSB

Visible colors: FFGF (Off Off Green Off)

Bits in the *same location* are both high:

POST CODE 33 --- BIT values (MSB to LSB) 0011 0011

I I

Upper Nibble Lower Nibble

LEDS Status MSB to LSB

Visible colors: FFOO (Off Off Orange Orange)

The following table is provided to show the most important POST CODES:

POST CODE	LED COLORS (MSB->LSB)	DESCRIPTION
E1	RRRG	MEMORY SIZE RAM
E9	ORRG	LOAD BB FROM FLOPPY
08	GFFF	CPU INIT
38	GFRR	USB INIT
0C	GGFF	KEYBOARD CONTLR TEST
2A	GFOF	PCI INIT
2A	GFOF	VIDEO
3A	GFOR	MEMORY SIZE RAM
28	GFRF	OPTION ROM SCAN
00	FFFF	INT19 (SWITCHES TO OS)

If the board fails to boot or hangs-up at any of these POST codes, please follow these steps.

Step1: Check all power connections and cables to verify they are fully inserted and there are not any loose connections.

Step2: Observe the indicating POST code and refer to the following section pertaining to the failure.

POST CODE	TROUBLESHOOTING HINT
08	Check the CPU to see if it is fully seated in its socket.
E1, 3A	Check the memory module to see if it is fully seated and that it is not inserted at an angle. The board may stay at post code 60 for a long time depending on the memory size; attach a monitor and confirm the board continues to count memory.
2A, 78	Check all PCI cards to verify they are fully seated in the backplane. Remove and replace any newly added PCI cards.
0C	Check keyboard.
38	Check USB for USB keyboard or mouse.
E1	If BIOS has been recently flashed or changed out, check to see if it is fully seated in the BIOS socket or if a wrong size device has been used.
00	Board has attempted to load OS. Ensure OS is properly installed on boot media. If the OS is successfully loaded, this code may remain; however, differing Operating Systems may map the LED port for floppy access, and C0 will be overwritten with random codes. This occurrence is normal, and floppy functionality will not be affected.

Step3: If board problems persist, contact Diversified Technology's Service Department.

Appendix A

A Specifications

This appendix describes the electrical, environmental, and mechanical specifications of the ETX-LX15. It includes connector descriptions and pin outs, as well as illustrations of the board dimensions and connector locations.

A.1 Electrical and Environmental

The topics listed below provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

A.2 Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ETX-LX15 at these maximums. See the "DC Operating Characteristics" section in this appendix for operating conditions.

Supply Voltage, Vcc:	6.5V
Storage Temperature (no hard disk):	-40° to +85° Celsius
Storage Temperature (with hard disk):	-40° to +65° Celsius
Non-Condensing Relative Humidity:	<95% at 40° Celsius

A.2.1 DC Operating Characteristics

Supply Voltage, Vcc:	4.75 minimum to 5.25V maximum
Supply Current, Icc:	3.7A average (typical with 1.1 GHz processor and 512 MB SDRAM. Peak (short duration) power supply current may be significantly higher (up to 50%) and will vary depending upon the application.

A.2.2 Battery Backup Characteristics

Battery Voltage:	3V
Real-Time Clock Requirements:	2.56µA maximum (Vbat = 3V, Vcc=0V)

CAUTION: DTI ETX baseboards use a lithium battery. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions.

A.2.3 Operating Temperature

The ETX-Lx15 may be operated in a maximum ambient temperature of 65°C. Operation at this temperature is highly dependant on the thermal solution. A heat spreader is available for the ETX-Lx15, which may help in designing either a forced air or conduction-cooled solution. With forced air cooling, the ETX-LX15's heat spreader allows a maximum ambient air temperature of 40°C with 200 LFM (linear feet per minute) of airflow. Refer to the "Electrical and Environmental" topic in Chapter 2 for additional information. Also refer to the topic "Temperature Monitoring" in Appendix C, "Thermal Considerations", for details on monitoring the processor temperature.

A.2.4 Baseboard Connector Characteristic

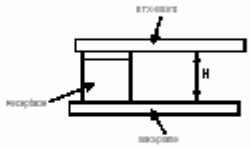
The following excerpt from the ETX Specification v2.6 provides further mechanical and electrical information on the ETX-LX15's I/O headers.

ETX Component SBC™ Specification *Mechanical Characteristics*

5.3. Specification of baseboard connector

To achieve various stacking heights, the receptacles for ETX baseboards are available in two heights.

Manufacturer	Order number	Resulting height H between backplane and ETX-Board
HIROSE	FX8-100S-SV	3 +0.3/-0.2mm
	FX8C-100S-SV5	9.5 +0.3/-0.2mm



Current capacity	0.4A per pin
Rated voltage	100V AC
Insulation resistance	100MΩ or greater @ 250V DC
Withstand voltage	300V AC r.m.s.
Contact resistance	45mΩ or less @ 100mA DC
Insulation	PPS resin (Light brown, UL94V-0)
Contacts	Phosphor bronze (Contacts and leads – gold plating)

A.3 Reliability

MTBF:

ETX-LX15 : TBD

ETX-Lx15 (with DTI's baseboard): TBD

MTTR: 2 minutes (based on board replacement), plus system startup

A.4 Mechanical

This section includes the following mechanical specifications:

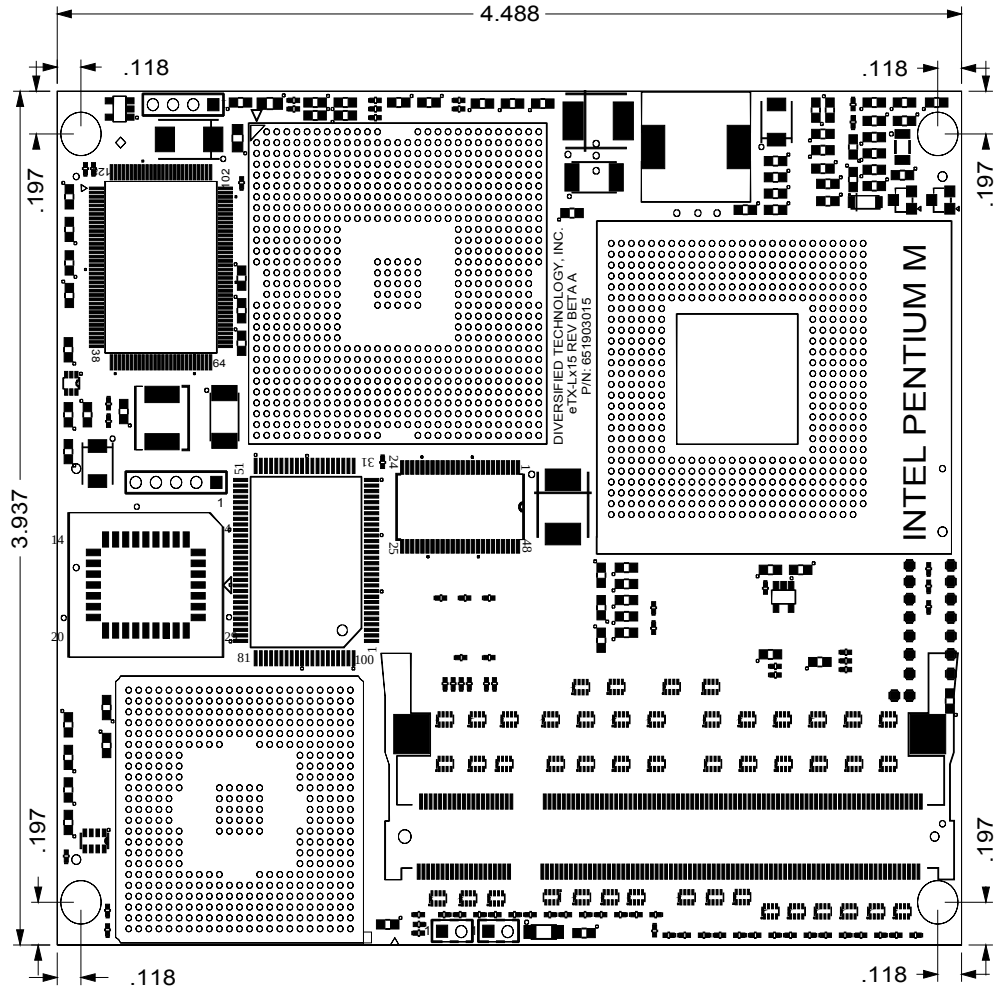
- Dimensions and weight
- Connector locations, descriptions, and pin outs

A.4.1 Board Dimensions and Weight

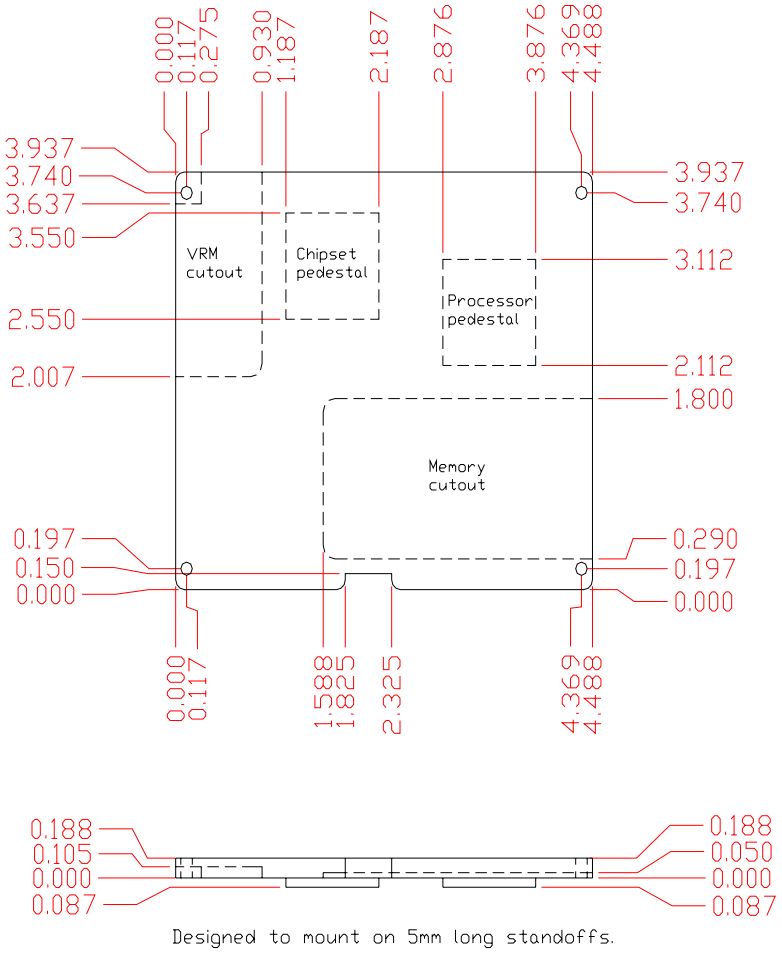
The ETX-LX15's mechanical dimensions are shown in the "PCB Dimensions" illustration and are outlined below.

PCB Dimensions:	100mm x 114 mm x 8 mm
Weight:	226.8 grams (8 ounces) w/ processor, heat spreader, 512MB memory

PCB Dimensions:



A.4.2 Heat Spreader Dimensions

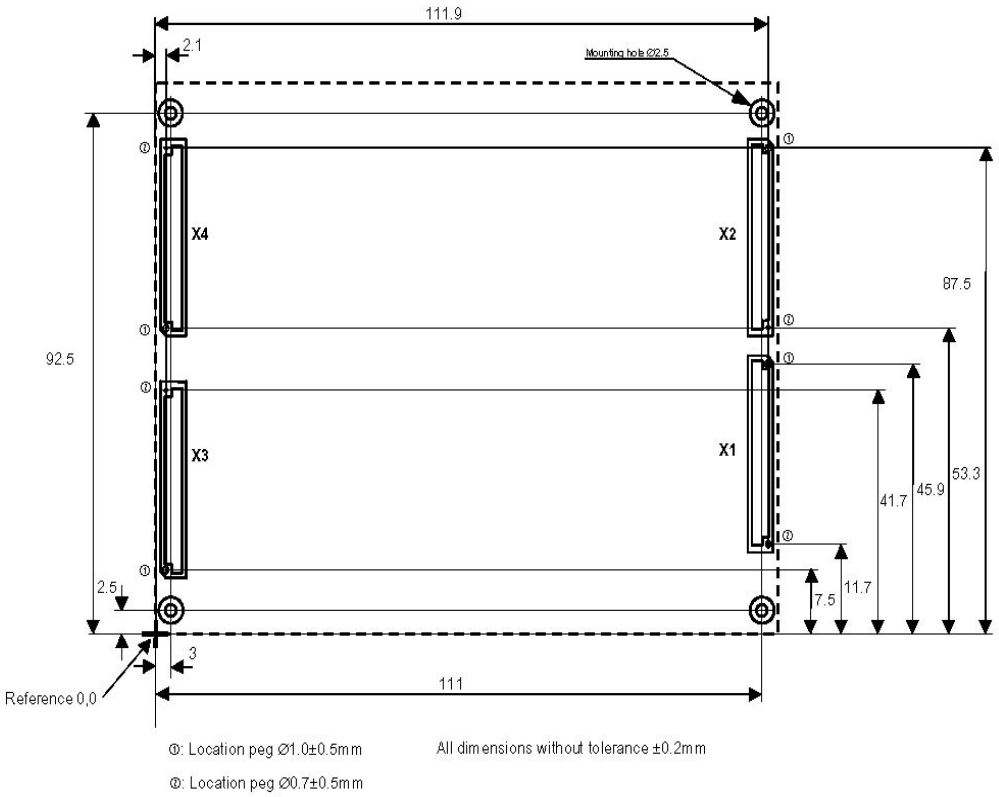


A.4.3 Baseboard Compatibility

The ETX-LX15 has fully ETX Specification V2.6 compliant I/O. Nominal operation of the ETX-LX15 should be easily obtained for all ETX compliant baseboards. Baseboard designers should reference the ETX Component SBC Design Guide V1.0 and ETX Specification V2.6 for baseboard design assistance.

The following is an excerpt from the ETX specification detailing the recommended backplane layout pattern:

5.4. Backplane layout



The outline shown here is for modules with a Y dimension of 95mm. Note that in order to accommodate both 95mm and 100mm ETX modules, the 95mm outline shown here should be expanded by 2.5mm on the top and 2.5mm on the bottom.

The relative mounting hole and connector locations on the 95mm and 100mm modules are the same – only the Y envelope dimension varies. Therefore a given baseboard design can accommodate both 95mm and 100mm modules provided sufficient clearance is allowed for the 100mm module.

Appendix B

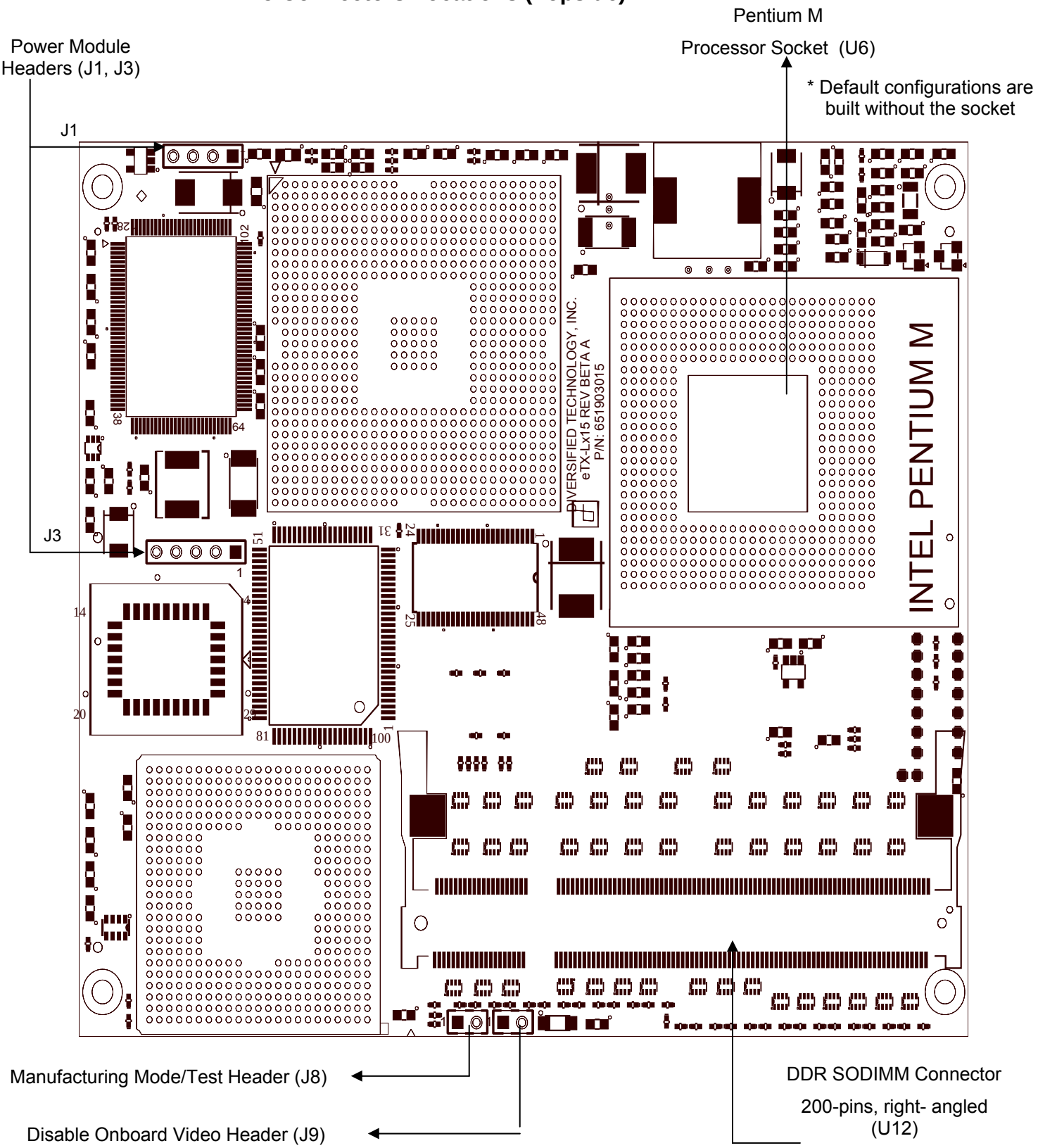
B Connectors

As shown in the "Connector Locations" figure, the ETX-LX15 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table below. A detailed description and pin out for each connector is given in the following topics.

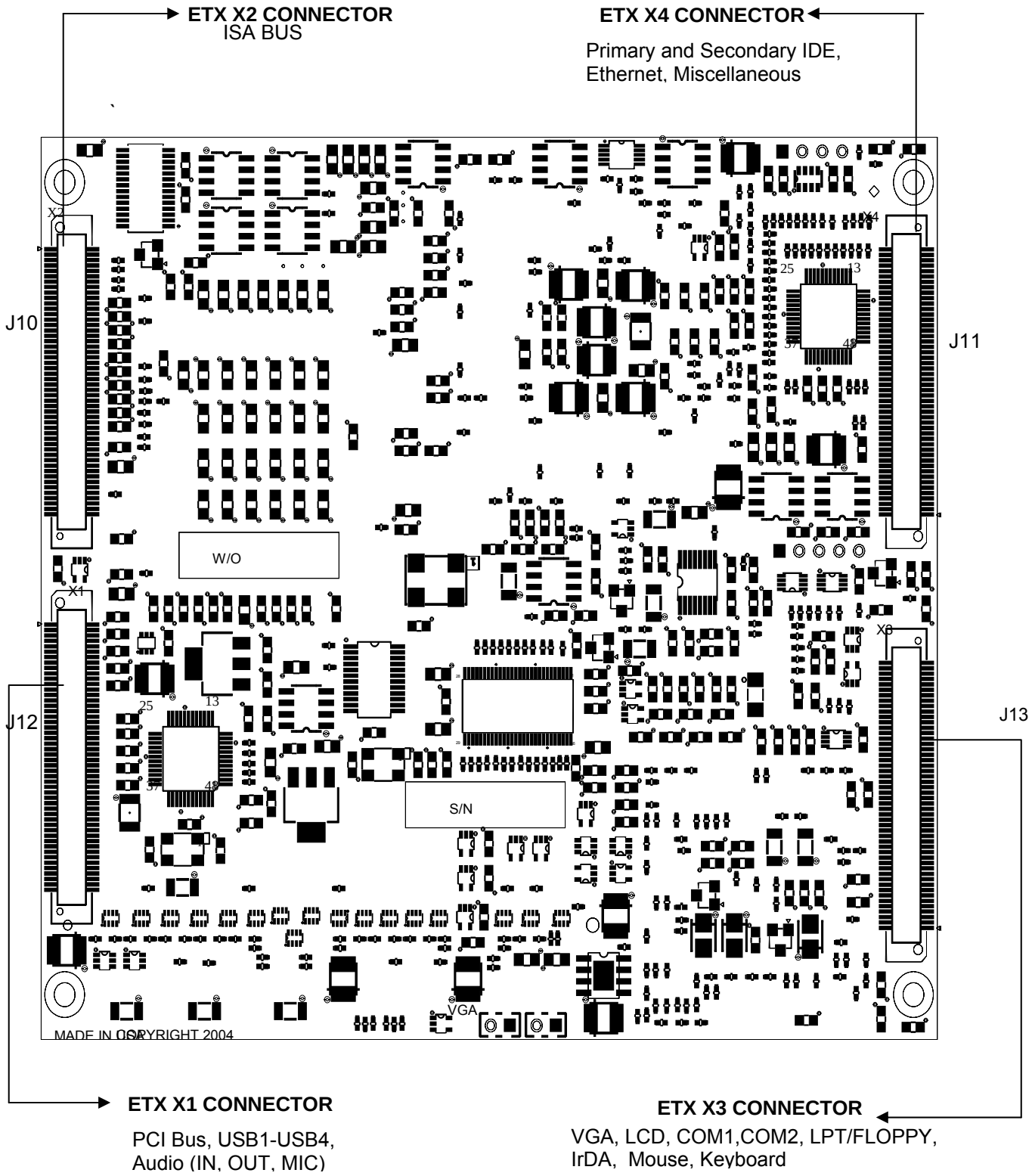
Connector Assignments

Connector	Function
J10	ETX X2 Header (Hirose FX8-100P-SV)
J11	ETX X1 Header (Hirose FX8-100P-SV)
J12	ETX X3 Header (Hirose FX8-100P-SV)
J13	ETX X4 Header (Hirose FX8-100P-SV)
J1	Power Entry
J3	Power Entry
U12	Right angle DIMM connector
U7	Pentium M Processor (socket able upon request)

B.1 ETX-LX15 Connectors Locations (Topside)



B.2 ETX-LX15 BACKSIDE CONNECTORS



B.3 ETX-LX15 Connector Pin-outs

This section lists the connector pin-outs on the ETX-LX15.

B.3.1 Header Pin-outs

J8 – Manufacturing Mode	
1	GND
2	MMode_GPI

J9 – Disable Onboard Video	
1	GND
2	VIDEO Disable

B.3.2 X1 ETX CONNECTOR (J12)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3V
13	REQ2#	14	GNT1#
15	REQ1#	16	3V
17	GNT0#	18	RESERVED
19	VCC	20	VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3V
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SNDL
47	AD15	48	ASGND
49	CBE1#	50	SNDR

Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	PAR	54	SERR#
55	GPERR#	56	RESERVED
57	PME#	58	USB2#
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3#
63	IRDY#	64	STOP#
65	FRAME#	66	USB2
67	GND	68	GND
69	AD16	70	CBE2#
71	AD17	72	USB3
73	AD19	74	AD18
75	AD20	76	USB0#
77	AD22	78	AD21
79	AD23	80	USB1#
81	AD24	82	CBE3#
83	VCC	84	VCC
85	AD25	86	AD26
87	AD28	88	USB0
89	AD27	90	AD29
91	AD30	92	USB1
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

B.3.3 X2 ETX CONNECTOR (J10)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	MASTER#
7	SD12	8	DREQ7
9	SD11	10	DACK7#
11	SD10	12	DREQ6
13	SD9	14	DACK6#
15	SD8	16	DREQ5
17	MEMW#	18	DACK5#
19	MEMR#	20	DREQ0
21	LA17	22	DACK0#
23	LA18	24	IRQ14
25	LA19	26	IRQ15
27	LA20	28	IRQ12
29	LA21	30	IRQ11
31	LA22	32	IRQ10
33	LA23	34	IO16#
35	GND	36	GND
37	SBHE#	38	M16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA2	44	TC
45	SA3	46	DACK2#
47	SA4	48	IRQ3
49	SA5	50	IRQ4

Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	REFSH#
63	SA11	64	DREQ1
65	SA12	66	DACK1#
67	GND	68	GND
69	SA13	70	DREQ3
71	SA14	72	DACK3#
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	VCC	84	VCC
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	NOWS#
91	DREQ2	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	IOCHK#	98	RSTDRV
99	GND	100	GND

B.3.4 X3 ETX CONNECTOR (J13)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#	10	DDDA
11	LCDDO16/B4	12	LCDDO18/SHFCLK
13	LCDDO17/B5	14	LCDDO19/EN
15	GND	16	GND
17	LCDDO13/B1	18	LCDDO15/B3
19	LCDDO12/B0	20	LCDDO14/B2
21	GND	22	GND
23	LCDDO8/G2	24	LCDDO11/G5
25	LCDDO9/G3	26	LCDDO10/G4
27	GND	28	GND
29	LCDDO4/R4	30	LCDDO7/G1
31	LCDDO5/R5	32	LCDDO6/G0
33	GND	34	GND
35	LCDDO1/R1	36	LCDDO3/R3
37	LCDDO0/R0	38	LCDDO2/R2
39	VCC	40	VCC
41	JILI_DAT	42	LTGIO0/VSNYC
43	JILI_CLK	44	BLON#
45	BIASON/HSYNC	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	VCC	54	GND
55	STB#/RSVD	56	AFD#/DENSEL
57	RESERVED	58	PD7/RSVD
59	IRRX	60	ERR#/HDSEL#
61	IRTX	62	PD6/RSVD
63	RXD2	64	INIT#/DIR#
65	GND	66	GND
67	RTS2#	68	PD5/RSVD
69	DTR2#	70	SLIN#/STEP#
71	DCD2#	72	PD4/DSKCHG#
73	DSR2#	74	PD3/RDATA#
75	CTS2#	76	PD2/WP#
77	TXD2#	78	PD1/TRK0#
79	RI2#	80	PD0/INDEX#
81	VCC	82	VCC
83	RXD1	84	ACK#/DRV
85	RTS1#	86	BUSY#/MOT
87	DTR1#	88	PE/WDATA#
89	DCD1#	90	SLCT#/WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

B.3.5 X4 ETX CONNECTOR (J11)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH	10	LILED
11	RSMRST#	12	ACTLED
13	ROMKBCS#	14	SPEEDLED
15	EXT_PRG	16	I2CLK
17	VCC	18	VCC
19	OVCR#	20	GPCS#
21	EXTSMI#	22	I2DAT
23	SMBCLK	24	SMBDATA
25	SIDE_CS3#	26	SMBALRT#
27	SIDE_CS1#	28	DASP_S
29	SIDE_A2	30	PIDE_CS3#
31	SIDE_A0	32	PIDE_CS1#
33	GND	34	GND
35	PDIAG_S	36	PIDE_A2
37	SIDE_A1	38	PIDE_A0
39	SIDE_INTRQ	40	PIDE_A1
41	BATLOW#	42	GPE1#
43	SIDE_AK#	44	PIDE_INTRQ
45	SIDE_RDY	46	PIDE_AK#
47	SIDE_IOR#	48	PIDE_RDY
49	VCC	50	VCC

Pin	Signal	Pin	Signal
51	SIDE_IOW#	52	PIDE_IOR#
53	SIDE_DRQ	54	PIDE_IOW#
55	SIDE_D15	56	PIDE_DRQ
57	SIDE_D0	58	PIDE_D15
59	SIDE_D14	60	PIDE_D0
61	SIDE_D1	62	PIDE_D14
63	SIDE_D13	64	PIDE_D1
65	GND	66	GND
67	SIDE_D2	68	PIDE_D13
69	SIDE_D12	70	PIDE_D2
71	SIDE_D3	72	PIDE_D12
73	SIDE_D11	74	PIDE_D3
75	SIDE_D4	76	PIDE_D11
77	SIDE_D10	78	PIDE_D4
79	SIDE_D5	80	PIDE_D10
81	VCC	82	VCC
83	SIDE_D9	84	PIDE_D5
85	SIDE_D6	86	PIDE_D9
87	SIDE_D8	88	PIDE_D6
89	GPE2#	90	CBLID_P#
91	RXD#	92	PIDE_D8
93	RXD	94	SIDE_D7
95	TXD#	96	PIDE_D7
97	TXD	98	HDRST#
99	GND	100	GND

Appendix C

C Thermal Considerations

This appendix describes the thermal requirements for reliable operation of an ETX-LX15 using the Mobile Pentium 4 processor - M. It covers basic thermal requirements and provides specifics about monitoring the board and processor temperature.

C.1 Thermal Requirements

The maximum processor core temperature ***must not exceed 100°C***. The ETX-LX15 can be ordered with a heat spreader to help in designing a cooling solution for the processor module. Either forced air or conduction cooling solutions are possible. When used with forced air, the heat spreader allows a maximum ambient air temperature of 40°C with 200 linear feet per minute (LFM) of airflow. The maximum power dissipation of the CPU is 25 W at 1.2 GHz and 1.20V. The "Thermal Requirements" table below shows the relationship between ambient air temperature, board temperature, and processor core temperature.

Thermal Requirements

External Ambient Air Temperature (°C)	Temperature Around the Board (°C)	Pentium M processor Core Temperature (°C)
0	13	44
5	18	49
10	22	54
15	27	60
20	33	65
25	37	69
30	42	74
35	47	79
40	52	84
45	57	89
50	63	95
55	68	100 = maximum

C.2 Temperature Monitoring

Because reliable long-term operation of the ETX-LX15 depends on maintaining proper temperature, DTI strongly recommends verifying the operating temperature of the processor module and processor core in the final system configuration.

The Pentium M processor incorporates an on-die thermal diode that can be used to monitor the processor's die temperature. The ETX-LX15 includes an LM87 Hardware Monitor to check the die temperature of the processor for thermal management purposes.

When checking airflow conditions, let the Processor Core Temperature Test dwell for at least 30 minutes and verify that the core temperature does not exceed 65°C. The processor "core" temperature must **never** exceed 100°C under any condition of ambient temperature or usage.

WARNING: Temperatures over 100°C may result in permanent damage to the processor.

Refer to the "Thermal Requirements" table for more information.

Appendix D

D Datasheets

This appendix provides links to datasheets, standards, and specifications for the technology designed into the ETX-LX15.

D.1 ETX

Refer to ETX Specification V2.6 for more information.

Website at:

http://www.jumptec.de/product/data/etx/pdf/ETXSpecV2.6.pdf

D.2 Ethernet

Refer to the *Intel 82562em Fast Ethernet PCI Controller* datasheet for more information on the Ethernet 10/100 LAN Controller. The datasheet is available from Intel's Website at:

http://www.intel.com/design/network/products/lan/controllers/82562.htm

D.3 Intel 855GME Chipset and ICH4-M Controller

For more information on the following ETX-LX15 functions, refer to the *Intel 855GM/855GME Chipset Graphics and Memory Controller Hub* datasheets.

- Integrated Intel Extreme Graphics 2 video

For more information on the following ETX-LX15 functions, refer to the *Intel ICH4-M* datasheet.

- USB 2.0
- Counter/Timers
- DMA controllers
- Real-Time Clock
- Interrupt controllers
- Reset Control register
- IDE Interface Controller

Datasheets and other information available online at:

http://developer.intel.com/design/chipsets/embedded/855gme.htm

D.4 Pentium M processor (FCBGA Package)

For more information about the Intel Pentium M processor in FCBGA Package, see the *Mobile Intel Pentium 4 processor - M in FCPGA* datasheet. This document is available online at:

http://developer.intel.com/products/notebook/processors/pentiumm/index.htm

D.5 Video

For more information about Intel's Extreme Graphics 2 supported integrated into the 855GME, visit the following site:

http://www.intel.com/design/graphics2/index.htm

D.6 Super I/O

Refer to the SMSC *LPC47B27x Super I/O* datasheet for more information on the following ETX-LX15 functions:

- Floppy Port
- Serial Ports
- Parallel Port

The datasheet is available online from the SMSC Website at:

http://www.smsc.com/main/catalog/lpc47b27x.html

D.7 System Monitor

Refer to the *National Semiconductor LM87* datasheet for more information on the following ETX-LX15 functions:

- Voltage Monitoring
- Temperature Monitoring

The datasheet is available online from the National Semiconductor Website at:

http://www.national.com

Appendix E

E Agency Approvals

E.1 CE Certification

The eTX-Lx15 meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility [EN55024:1998, EN55022:1998] and Low-Voltage Directive 73/23/EEC for Product Safety [EN60950-1:2001]. The final product configuration may need further testing. DTI is ready to work with you to get your product through the CE certification process.

E.2 Safety

UL/cUL 60950-1:2003	Safety for Information Technology Equipment (UL File # E139737)
EN/IEC 60950-1:2001	Safety for Information Technology Equipment

E.3 Electro-magnetic Compatibility

FCC Part 15, Subpart B:2003	Class A Commercial Equipment
CISPR 22:1997	Class A Radiated, Power line Conducted
EN 50081-1:1992	Emissions- Residential, Commercial
EN 55022:1998	Class A Radiated, Power line Conducted
EN 61000-3-2:1995	Power Line Conducted Emissions
EN 61000-3-3:1995	Power Line Fluctuation and Flicker
EN 55024:1998	Immunity- Information Technology Equipment
EN 61000-4-2:1995	Electro-Static-Discharge (ESD)
EN 61000-4-3:1997	Radiated Susceptibility
EN 61000-4-4:1995	Electrical Fast Transient Burst

E.4 Regulatory Information

E.4.1 FCC (USA)

This product has been tested and found to comply with the limits for a Class A digital device pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This product generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.

Note: This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

CAUTION: If you make any modification to the equipment not expressly approved by DTI, you could void your authority to operate the equipment.

E.4.2 Industry Canada (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadien des Communications.

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: "Digital Apparatus," ICES-003 of the Canadian Department of Communications.