NEC

MOS INTEGRATED CIRCUITS

μPD78F9842

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F9842 is a member of μPD789842 Subseries of the 78K/0S Series product.

The μPD78F9842 is a product that has expanded the internal ROM of the μPD789841 and 789842, and replaced it with flash memory.

Flash memory can be written or erased electrically on board, making the μPD78F9842 best suited for prototypes in system development, small-scale production, or systems likely to be upgraded frequently.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

μPD789842 Subseries User's Manual: U13776E

78K/0S Series User's Manual Instructions: U11047E

FEATURES

- Pin-compatible with mask ROM versions (other than the V_{PP} pin)
- Flash memory: 16 Kbytes
- Internal high-speed RAM: 256 bytes
- Selectable minimum instruction execution time: High speed (0.24 μs) and low speed (0.96 μs) (with the system clock operating at 8.38 MHz)
- I/O ports: 30
- Timer: 6 channels
  - 10-bit inverter control timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer counter: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- A/D converter with 8-bit resolution: 8 channels
- Serial interface (UART00): 1 channel
- Multiplier: 10 bits × 10 bits = 20 bits
- SWAP: contents of the high-order 4 bits and the low-order 4 bits of the 8-bit register are switchable.
- Vectored interrupt sources: 14
- Power supply voltage: V_{DD} = 4.0 V to 5.5 V

APPLICATIONS

Inverter air conditioners, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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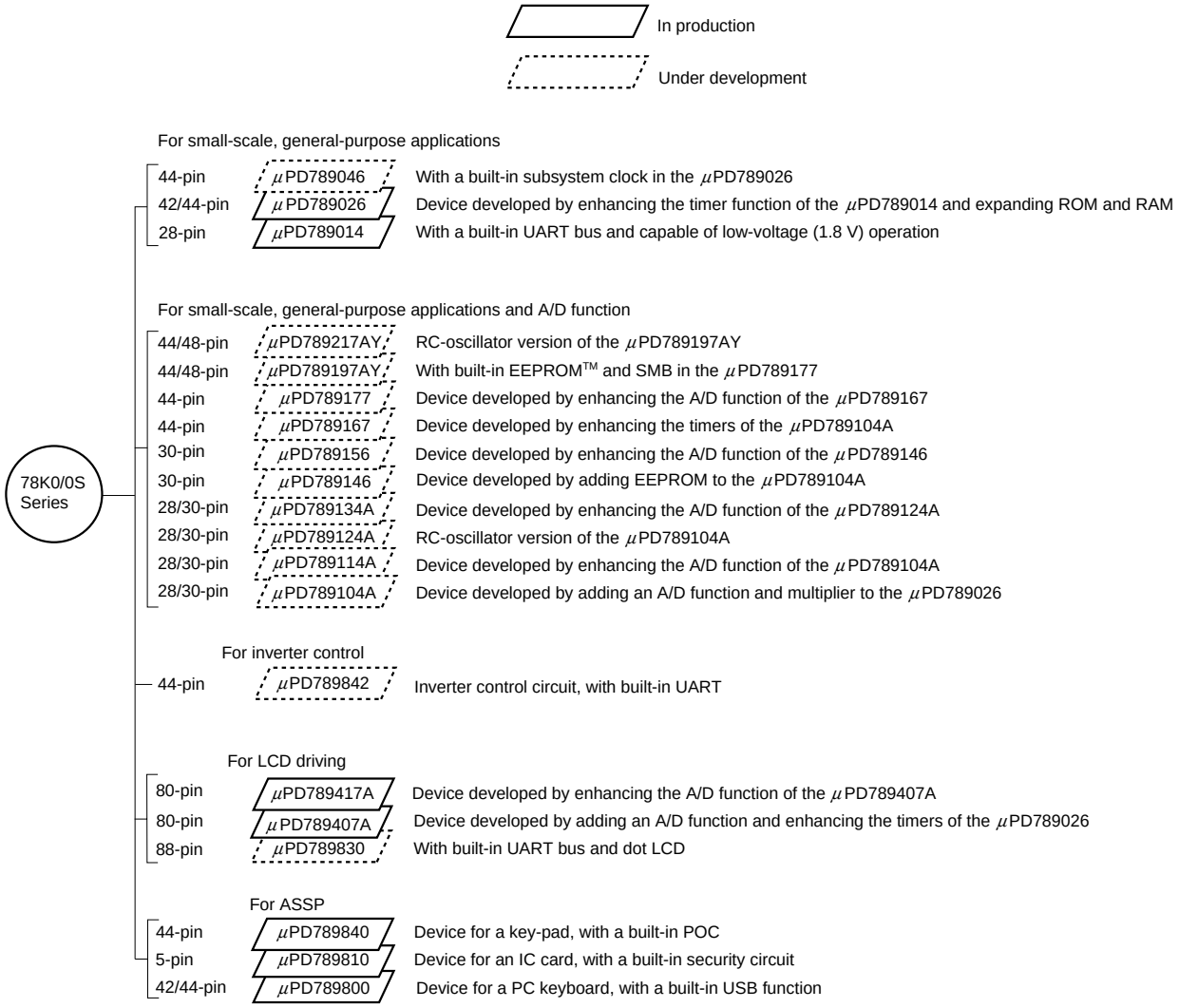
ORDERING INFORMATION

Part number	Package
PD78F9842GB-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 2.7 mm resin thickness)
PD78F9842GB-8ES	44-pin plastic QFP (10 × 10 mm, 1.4 mm resin thickness)

78K/0S SERIES DEVELOPMENT

The products of the 78K/0S Series are shown below. The subseries names are indicated in the frames.



The following table lists the major differences in functions between the subseries.

Subseries \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	Serial Interface	I/O	Remarks
			8-bit	16-bit	Watch	WDT					
Small-scale, general-purpose applications	μPD789046	16K	1ch	1ch	1ch	1ch	–	–	1ch (UART: 1ch)	34 pins	–
	μPD789026	4K to 16K			–						
	μPD789014	2K to 4K	2ch	–						22 pins	
Small-scale, general-purpose applications with A/D function	μPD789217AY	16K to 24K	3ch	1ch	1ch	1ch	–	8ch	2ch (UART: 1ch, SMB: 1ch)	31 pins	RC-oscillator version, with on-chip EEPROM
	μPD789197AY										With on-chip EEPROM
	μPD789177								1ch (UART: 1ch)		–
	μPD789167						8ch	–			
	μPD789156	4K to 16K	1ch		–		–	4ch		20 pins	With on-chip EEPROM
	μPD789146						4ch	–			
	μPD789134A	2K to 8K					–	4ch			RC-oscillator version
	μPD789124A						4ch	–			
	μPD789114A						–	4ch			–
	μPD789104A						4ch	–			
Inverter control	μPD789842	8K to 16K	3ch	**Note**					1ch (UART: 1ch)	30 pins	–
LCD driving	μPD789417A	12K to 24K	3ch	1ch	1ch	1ch	–	7ch	1ch (UART: 1ch)	43 pins	–
	μPD789407A						7ch	–			
	μPD789830	24K	1ch				–			30 pins	
ASSP	μPD789840	8K	2ch	–	–	1ch	4ch	–	1ch	29 pins	
	μPD789810	6K	–				–		–	1 pin	With on-chip EEPROM
	μPD789800	8K	2ch						2ch (USB:1ch)	31 pins	

Note 10-bit timer: 1 channel

FUNCTIONS

Item		Function
Internal memory	Flash memory	16 Kbytes
	High-speed RAM	256 bytes
Minimum instruction execution time		0.24 μs/0.96 μs (with system clock operating at 8.38 MHz)
General-purpose register		8 bits × 8 registers
Instruction set		16-bit operations Bit manipulations (such as set, reset, and test)
I/O ports		Total : 30 CMOS input/output pins : 22 CMOS input pins : 8
Timers		10-bit inverter control timer : 1 channel 8-bit timer/event counter : 2 channels 8-bit timer counter : 1 channel Watch timer : 1 channel Watchdog timer : 1 channel
A/D converters		8-bit resolution × 8 channels
Serial interface		UART: 1 channel
Multiplier		10 bits × 10 bits = 20 bits
SWAP		Contents of the high-order 4 bits and the low-order 4 bits of the 8-bit register are switchable
Vectored interrupt sources	Maskable	11 internal and 2 external interrupts
	Nonmaskable	One internal interrupt
Power supply voltage		V_{DD} = 4.0 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		44-pin plastic QFP (10 × 10 mm)

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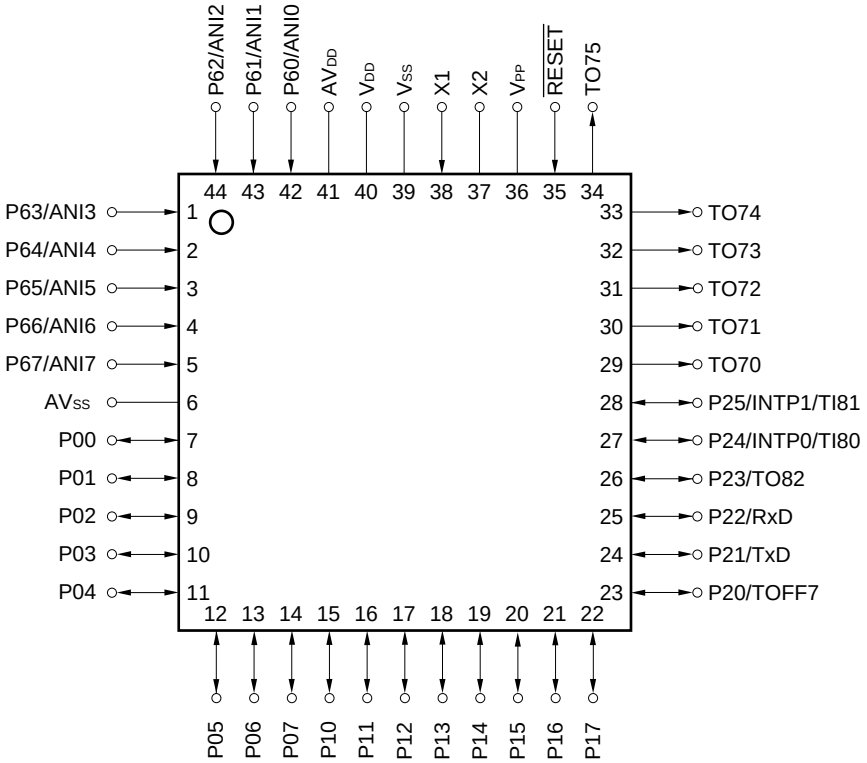
1. PIN CONFIGURATION (TOP VIEW)

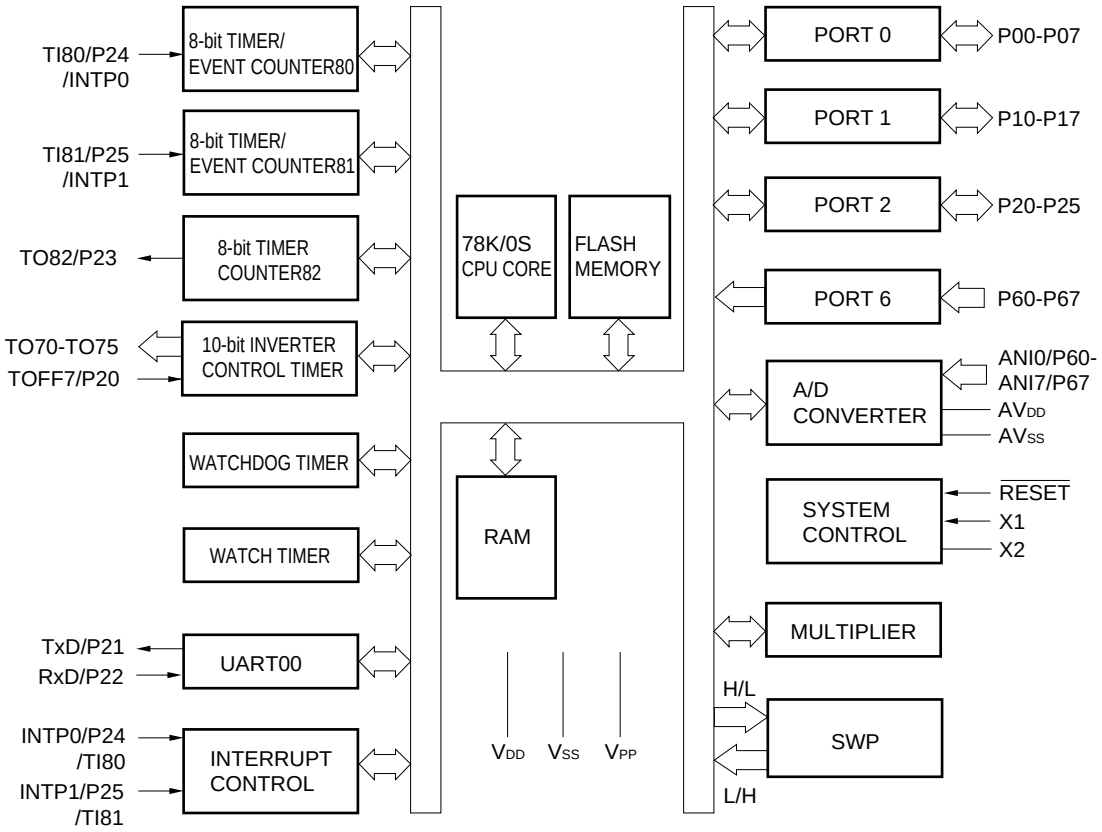
- **44-pin plastic QFP**
  μPD78F9842GB-3BS-MTX (10 × 10 mm, 2.7 mm resin thickness)
  μPD78F9842GB-8ES (10 × 10 mm, 1.4 mm resin thickness)



Cautions 1. Connect the V_{PP} pin directly to the V_{SS} pin.
2. Connect the AV_{DD} pin to the V_{DD} pin.
3. Connect the AV_{SS} pin to the V_{SS} pin.

ANI0 to ANI7	: Analog Input	RxD	: Receive Data
AV_{DD}	: Analog Power Supply	TI80, TI81	: Timer Input
AV_{SS}	: Analog Ground	TI70 to TO75, TO82	: Timer Output
INTP0, OMTP1	: Interrupt from Peripherals	TOFF7	: Timer Output Off
P00 to P07	: Port0	TxD	: Transmit Data
P10 to P17	: Port1	V_{DD}	: Power Supply
P20 to P25	: Port2	V_{PP}	: Programming Power Supply
P60 to P67	: Port6	V_{SS}	: Ground
$\overline{\text{RESET}}$	: Reset	X1, X2	: Crystal

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit input/output port Input/output can be specified in 1-bit units When used as an input port, on-chip pull-up resistor connection can be specified by means of software.	Input	–
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified in 1-bit units When used as an input port, on-chip pull-up resistor connection can be specified by means of software.	Input	–
P20	I/O	Port 2 6-bit input/output port Input/output can be specified in 1-bit units On-chip pull-up resistor connection can be specified by means of software.	Input	TOFF7
P21				TxD
P22				RxD
P23				TO82
P24				INTP0/TI80
P25				INTP1/TI81
P60 to P67	Input	Port 6 8-bit input-only port	Input	ANI0-ANI7

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt inputs for which effective edges (rising and/or falling edges) can be specified	Input	P24/TI80
INTP1				P25/TI81
RxD	Input	Serial data input for asynchronous serial interface	Input	P22
TxD	Output	Serial data output for asynchronous serial interface	Input	P21
TO70 to TO75	Output	Timer output from timer for 10-bit inverter control timer	Output	–
TOFF7	Input	External input to stop timer output (TO70 to TO75)	Input	P20
TI80	Input	External count clock input of TM80	Input	P24/INTP0
TI81		External count clock input of TM81		P25/INTP1
TO82	Output	Timer output of TM82	Input	P23
ANI0 to ANI7	Input	A/D converter analog input	Input	P60 to P67
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}		A/D converter analog power supply	–	–
X1	Input	Crystal resonator connection for system clock oscillation	–	–
X2	–		–	–
$\overline{RESET}$	Input	System reset input	Input	–
V_{DD}	–	Positive power supply for ports	–	–
V_{SS}	–	Ground potential ports	–	–
V_{PP}	–	This pin is used to set the flash memory programming mode and applies a high voltage when a program is written or verified. In normal operation mode, connect this pin directly to the V_{SS} pin.	–	–

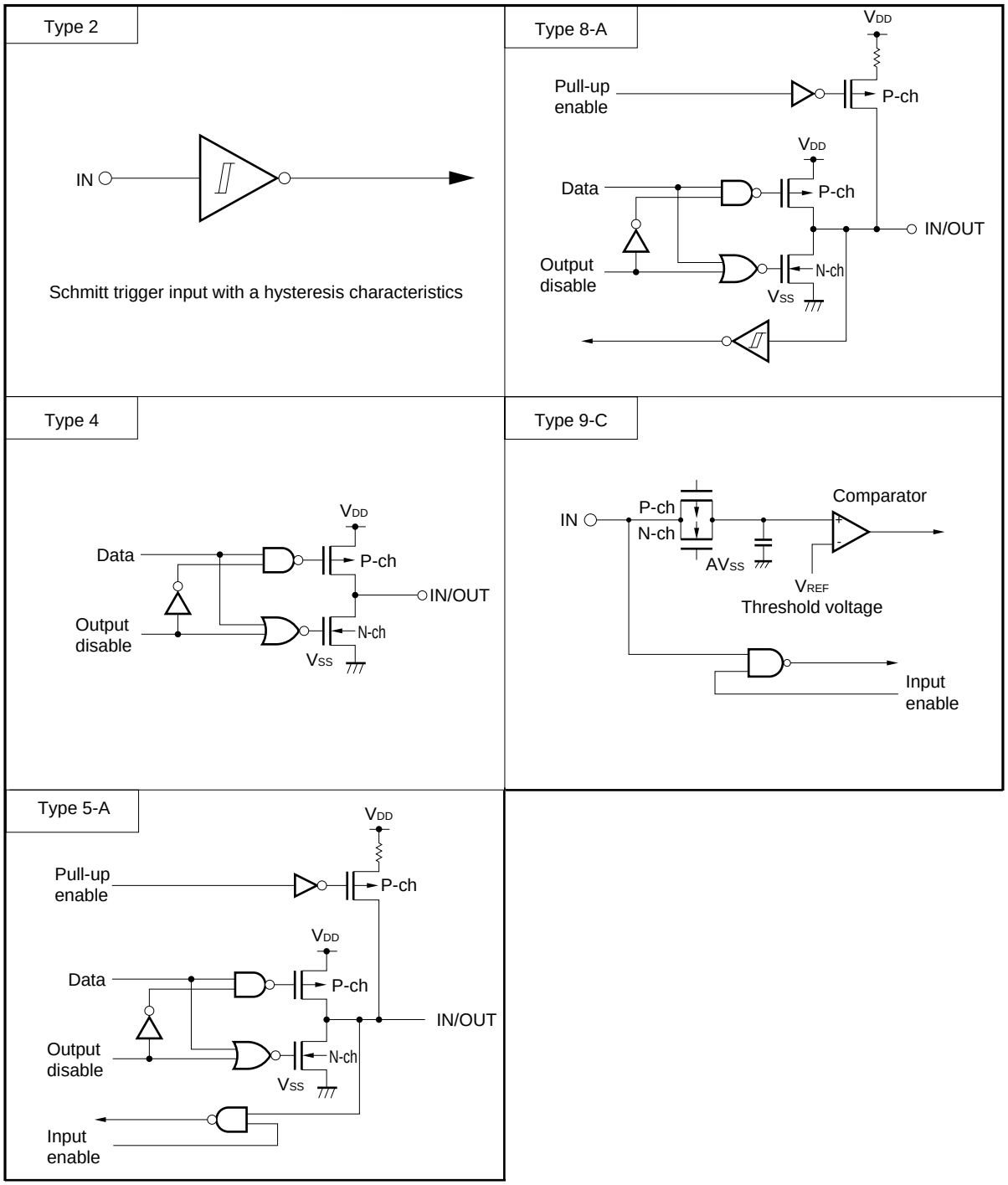
3.3 Pin Input/Output Circuits and Connection of Unused Pins

Table 3-1 lists the input/output circuit-type for each pin and explains how unused pins are handled.
Figure 3-1 shows the configuration of each type of input/output circuit.

Table 3-1. Type of Input/Output Circuit for Each Pin and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-A	I/O	When used as inputs: individually connect these pins to the V_{DD} or V_{SS} pin via resistors. When used as outputs: leave these pins open.
P10 to P17			
P20/TOFF7	8-A		
P21/TxD			
P22/RxD			
P23/TO82			
P24/INTP0/TI80			
P25/INTP1/TI81			
P60/ANI0 to P67/ANI7	9-C	Input	Connect these pins directly to the V_{DD} or V_{SS} pin.
TO70 to TO75	4	Output	Individually connect these pins to the V_{DD} or V_{SS} pin via resistors.
RESET	2	Input	–
V_{PP}	–	–	Connect this pin directly to the V_{SS}.

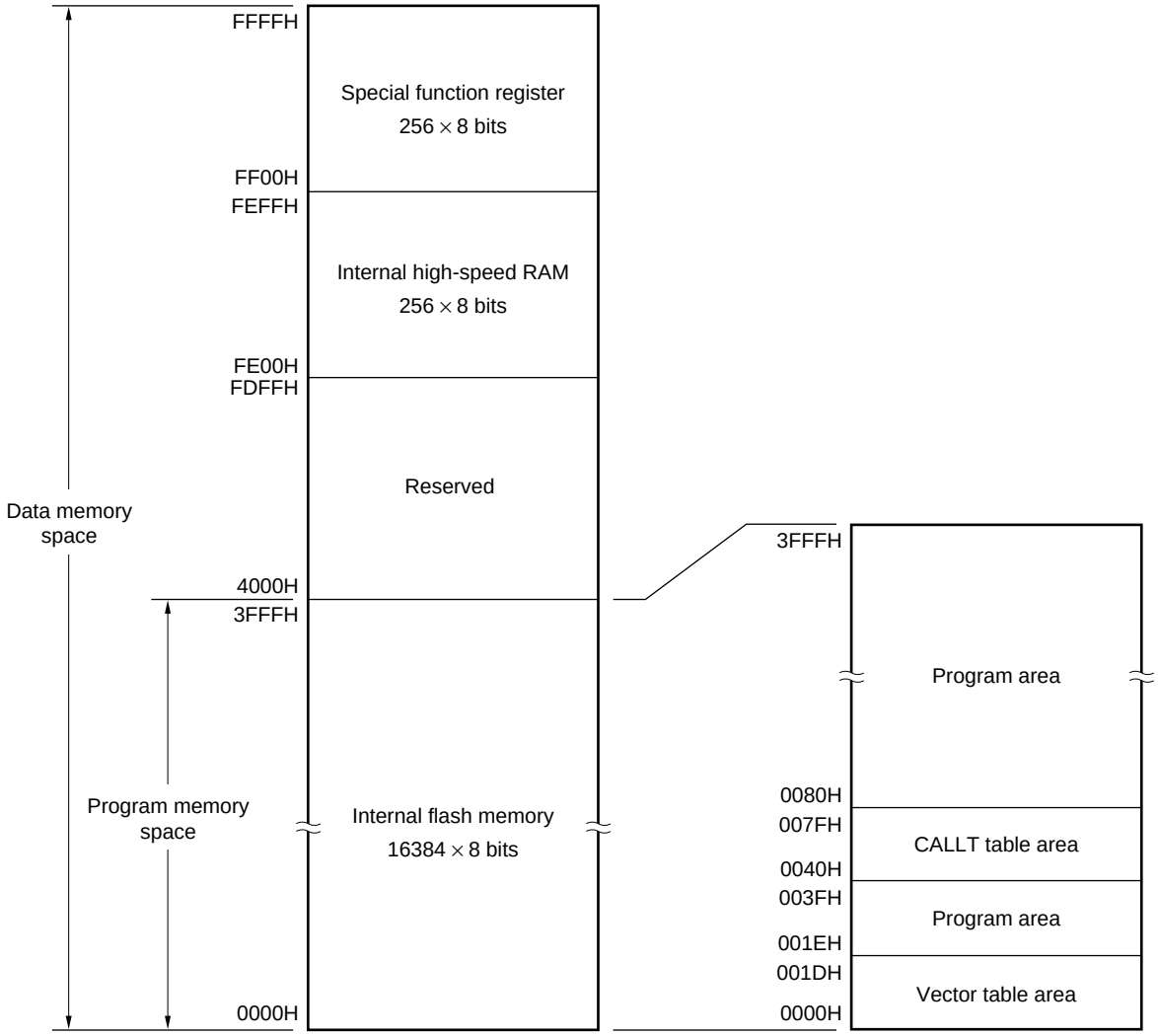
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The μPD78F9842 can access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. FLASH MEMORY PROGRAMMING

The internal program memory of the μPD78F9842 is flash memory.

Flash memory can be written to even while the device is mounted in the target system (on-board write). To write a program to flash memory, connect the dedicated flash programmer (Flashpro III (Model number: FL-PR3 and PG-FP3)) to both the host machine and target system.

Remark The FL-PR3 is manufactured by Naito Densei Machidaseisakusho.

5.1 Selecting Transmission Method

The Flashpro III writes to flash memory by means of serial transmission. The transmission method to be used for writing is selected from those listed in Table 5-1. To select a transmission method, use the format shown in Figure 5-1, according to the number of V_{PP} pulses listed in Table 5-1.

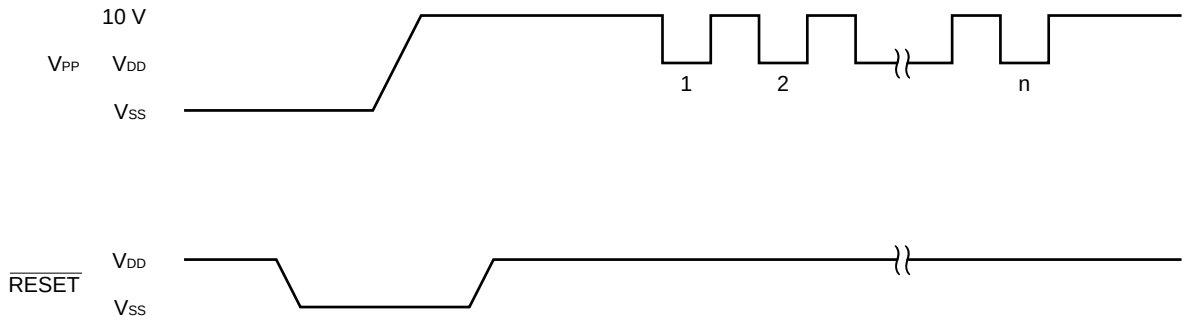
Table 5-1. Transmission Methods

Transmission Method	Pins	Number of V_{PP} pulses
UART	TxD/P21 RxD/P22	8
Pseudo three-wire mode [Note]	P00 (serial clock input) P01 (serial data output) P02 (serial data input)	12

Note Serial transfer is performed by controlling the ports using software.

Caution To select a transmission method, always use the corresponding number of V_{PP} pulses listed in Table 5-1.

Figure 5-1. Format of Transmission Method Selection



5.2 Flash Memory Programming Function

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected transmission method. Table 5-2 lists the main flash memory programming functions.

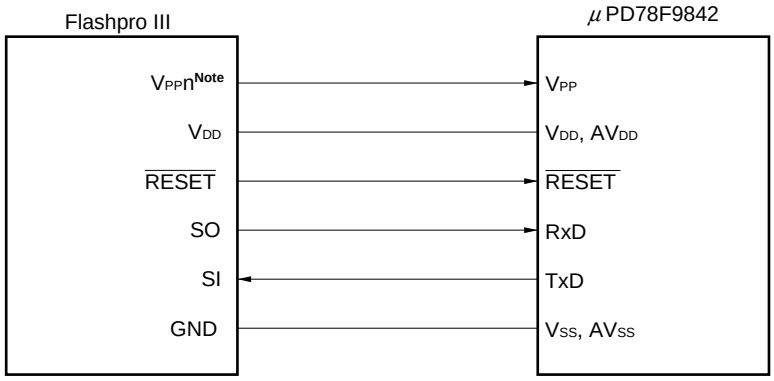
Table 5-2. Main Flash Memory Programming Functions

Function	Description
Batch erase	Erases the entire memory contents.
Batch blank check	Checks that the entire memory contents have been erased.
Data write	Writes to the flash memory according to the specified write start address and number of bytes of data to be written.
Batch verify	Compares the entire memory contents with the input data.

5.3 Connecting Flashpro III

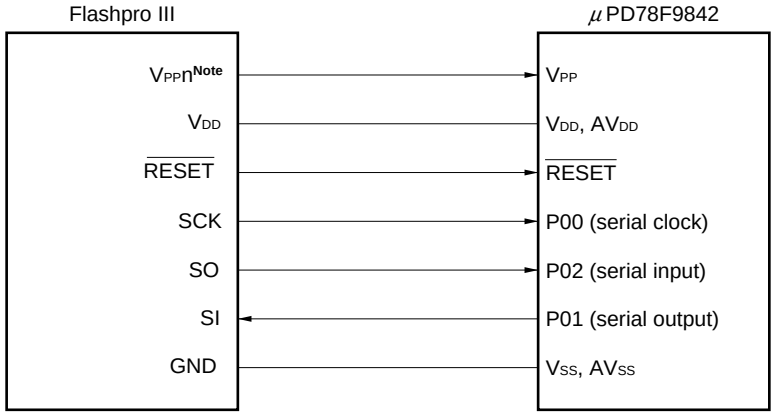
The connection between the Flashpro III and the μPD78F9842 varies with the transmission method (UART or pseudo 3-wire). Figures 5-2 and 5-3 show the connection for each transmission method.

Figure 5-2. Flashpro III Connection in UART Mode



Note n: 0 or 1

Figure 5-3. Flashpro III Connection in Pseudo 3-Wire Mode



Note n: 0 or 1

5.4 Settings for Flashpro III

When using the Flashpro III to write to flash memory, set the Flashpro III as listed in Table 5-3.

Table 5-3. Settings for the Flashpro III

Transmission Method	Settings for the Flashpro III		Number of V_{PP} Pulses[Note 1]
UART	Type	78 K(2)	8
	RAM	128	
	ROM	Flash	
	START ADDRESS	0	
	END ADDRESS	3FFF	
	COMM PORT	UART ch-0	
	CPU CLK	On Target Board	
	On Target Board	4.1943 MHz	
	UART BPS	9600 bps [Note 2]	
Pseudo 3-wire mode	Type	78 K(2)	12
	RAM	128	
	ROM	Flash	
	START ADDRESS	0	
	END ADDRESS	3FFF	
	COMM PORT	Port A	
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.00 MHz	
	In Flashpro	4.00 MHz	
	SIO CLK	1.00 MHz	

Notes 1. The number of V_{PP} pulses supplied from the Flashpro III during the initialization of serial transmission. Pins to be used in transmission depend on this number.

2. Select one of the following: 9,600, 19,200, 38,400, or 76,800 bps.

Remark COMM PORT : Selection of the serial port
SIO CLK : Selection of the serial clock frequency
CPU CLK : Selection of the input CPU clock source

6. INSTRUCTION SET OVERVIEW

The instruction set for the μPD78F9842 is listed later.

6.1 Conventions

6.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform to assembly specifications). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and square parentheses ([ ]) are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

# : Immediate data specification	$: Relative address specification
! : Absolute address specification	[ ] : Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or [ ].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 6-1).

Table 6-1. Operand Formats and Descriptions

Format	Description
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H-FF1FH Immediate data or label
saddrp	FE20H-FF1FH Immediate data or label (even-addresses only)
addr16	0000H-FFFFH Immediate data or label
	(only even-addresses for 16-bit data transfer instructions)
addr5	0040H-007FH Immediate data or label (even-addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

6.1.2 Descriptions of the operation field

A	: A register; 8-bit accumulator
X	: X register
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
AX	: AX register pair; 16-bit accumulator
BC	: BC register pair
DE	: DE register pair
HL	: HL register pair
PC	: Program counter
SP	: Stack pointer
PSW	: Program status word
CY	: Carry flag
AC	: Auxiliary carry flag
Z	: Zero flag
IE	: Interrupt request enable flag
NMIS	: Flag to indicate that a nonmaskable interrupt is being processed
( )	: Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L	: High-order and low-order 8 bits of a 16-bit register
∧	: Logical product (AND)
∨	: Logical sum (OR)
$\overline{\vee}$	: Exclusive OR
——	: Inverted data
addr16	: 16-bit immediate data or label
jdisp8	: Signed 8-bit data (displacement value)

6.1.3 Description of the flag operation field

(Blank)	: No change
0	: Cleared to 0
1	: Set to 1
×	: Set or cleared according to the result
R	: Restored to the previous value

6.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL+byte]	2	6	A ← (HL + byte)			
	[HL+byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL+byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note3	1	4	AX ← rp			
	rp, AX Note3	1	4	rp ← AX			
XCHW	AX, rp Note3	1	8	AX ↔ rp			

Notes 1. Except when r = A

2. Except when r = A or X

3. Only when rp = BC, DE, or HL

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock controller register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark The instruction clock is based on the CPU clock (f_{CPU}), specified in the processor clock controller register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) –byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×

Remark The instruction clock is based on the CPU clock (f_{CPU}), specified in the processor clock controller register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3 NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp$_H$, (SP – 2) ← rp$_L$, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$, ← (SP + 1) ← rp$_L$, ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark The instruction clock is based on the CPU clock (f_{CPU}), specified in the processor clock controller register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark The instruction clock is based on the CPU clock (f_{CPU}), specified in the processor clock controller register (PCC).

7. ELECTRICAL SPECIFICATIONS

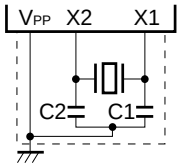
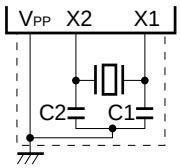
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Rated Value	Unit
Power supply voltage	V_{DD}		–0.3 to +6.5	V
	V_{PP}		–0.3 to +11.0	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Each pin	–10	mA
		Total for all pins	–30	mA
Low-level output current	I_{OL}	Each pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

CHARACTERISTICS OF THE SYSTEM CLOCK OSCILLATION CIRCUIT (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx)[Note 1]	V_{DD} = oscillation voltage range	8.0	8.38	8.5	MHz
		Oscillation stabilization time[Note 2]	Time after the V_{DD} has reached the minimum value in the oscillation voltage range			4	ms
Crystal oscillator		Oscillator frequency (fx) [Note 1]		8.0	8.38	8.5	MHz
		Oscillation stabilization time[Note 2]				10	ms

Notes 1. Only the characteristics of the oscillation circuit are indicated. See the description of the AC characteristics for the instruction execution time.

2. Time required for oscillation to stabilize once a reset sequence ends or STOP mode is released. Use a resonator that will become stable within the oscillation wait time.

Caution When using the system clock oscillation circuit, observe the following conditions for the wiring of the sections enclosed in dotted lines in the above diagrams so as to avoid the effects of wiring capacitance, etc.

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as the V_{SS}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output current	I_{OH}	Each pin				–1	mA
		Total for all pins				–15	mA
Low-level output current	I_{OL}	Each pin				10	mA
		Total for all pins				80	mA
High-level input voltage	V_{IH1}	P00 to P07, P10 to P17, P60 to P67		0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20 to P25		0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	P00 to P07, P10 to P17, P60 to P67		0		0.3V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P20 to P25		0		0.2V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
High-level output voltage	V_{OH}	I_{OH} = –1mA		V_{DD} – 1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 10mA				1.0	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1 and X2			3	μA
	I_{LIH2}		X1, X2			20	μA
Low-level input leakage current	I_{ILI1}	V_{IN} = 0 V	Pins other than X1 and X2			–3	μA
	I_{ILI2}		X1, X2			–20	μA
High-level output leakage current	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software-specified pull-up resistor	R	V_{IN} = 0 V		50	100	200	kΩ
Power supply current [Note 1]	I_{DD1}	8.38-MHz crystal oscillation operating mode [Note 2]			Undefined	Undefined	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode			Undefined	Undefined	mA
	I_{DD3}	STOP mode			Undefined	Undefined	μA
	I_{DD4}	8.38-MHz crystal oscillation A/D operating mode			Undefined	Undefined	mA

Notes 1. The power supply current does not include the current flowing through the on-chip pull-up resistor.

2. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H.)

Remark Unless otherwise specified, the characteristics of alternate function pins are the same as those of port pins.

AC CHARACTERISTICS

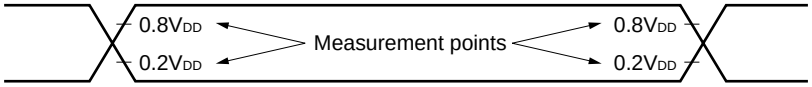
(1) Basic operations (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	When the PCC is set to 00H	0.24		0.25	μs
		When the PCC is set to 02H	0.94		1.00	μs
TI input frequency	f_{TI}		0		4.0	MHz
TI input high/low level width	f_{TIH}, f_{TIL}		0.1			μs
Interrupt input high/low level width	f_{INTH}, f_{INTL}	INTP0, INTP1	10			μs
$\overline{\text{RESET}}$ input low level width	f_{RSL}		10			μs

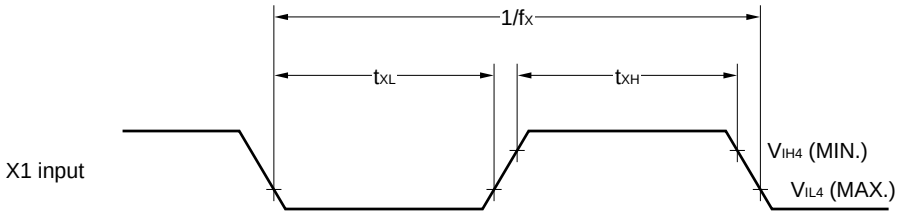
(2) Serial interface (UART) (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		At fx = 8.38 MHz operation			115200	bps

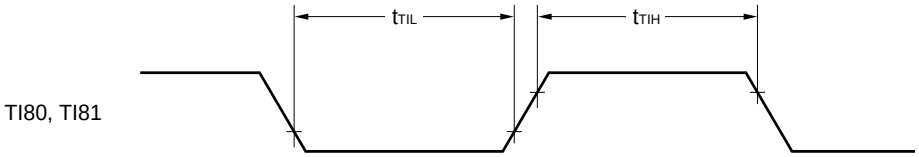
AC TIMING MEASUREMENT POINTS (except the X1 input)



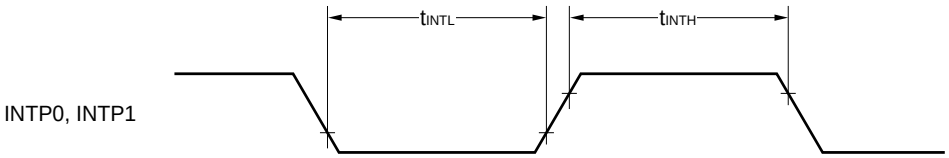
CLOCK TIMING



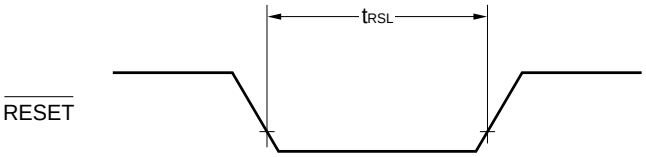
TI TIMING



INTERRUPT INPUT TIMING



$\overline{\text{RESET}}$ INPUT TIMING



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]					1.5	LSB
Conversion time	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Note No quantization error (±1/2 LSB) is included.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA-HOLD CHARACTERISTICS (T_A = –40 to +85°C)

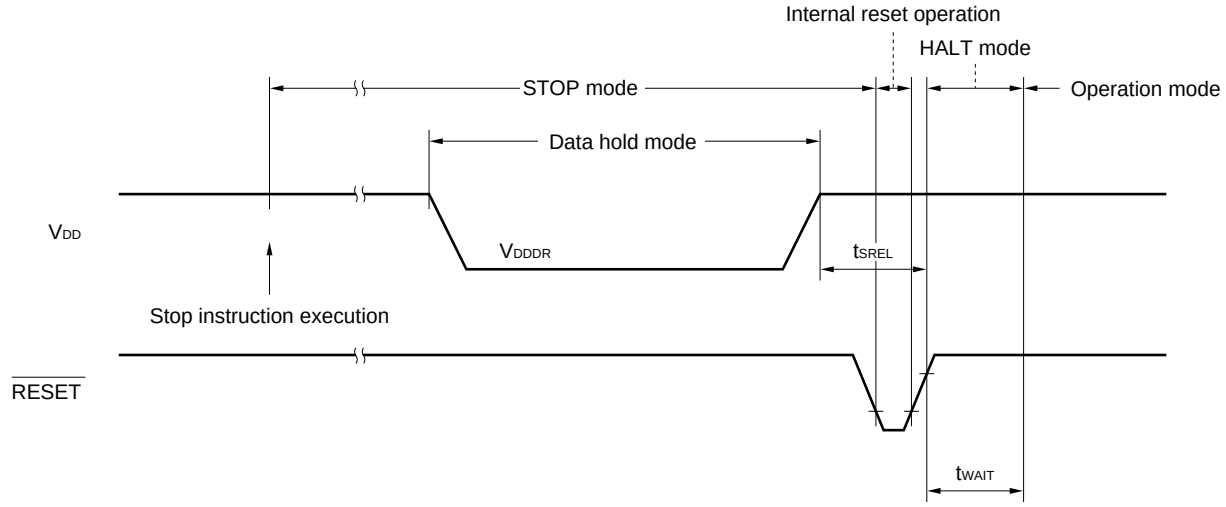
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data-hold supply voltage	V_{DDDR}		4.0		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Cleared by $\overline{\text{RESET}}$		2^{15}/fx		ms
		Cleared by an interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization time is a period in which the operation of the CPU is stopped in order to avoid unstable operation at the start of oscillation.

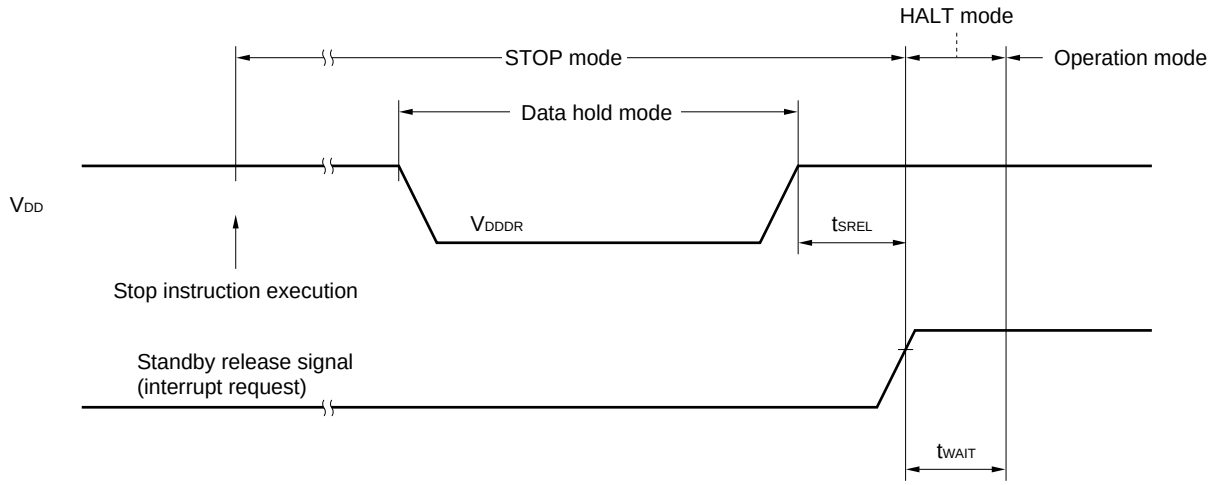
2. The typical (TYP) value can be selected from 2^{12}/fx, 2^{15}/fx, or 2^{17}/fx by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register.

Remark fx: system clock oscillation frequency

DATA HOLD TIMING (STOP mode release by $\overline{\text{RESET}}$)



DATA HOLD TIMING (Standby release signal: STOP mode release by interrupt signal)



FLASH MEMORY PROGRAMMING CHARACTERISTICS

(1) Basic characteristics (T_A = –20 to +60°C, V_{DD} = 4.0 to 5.5 V)

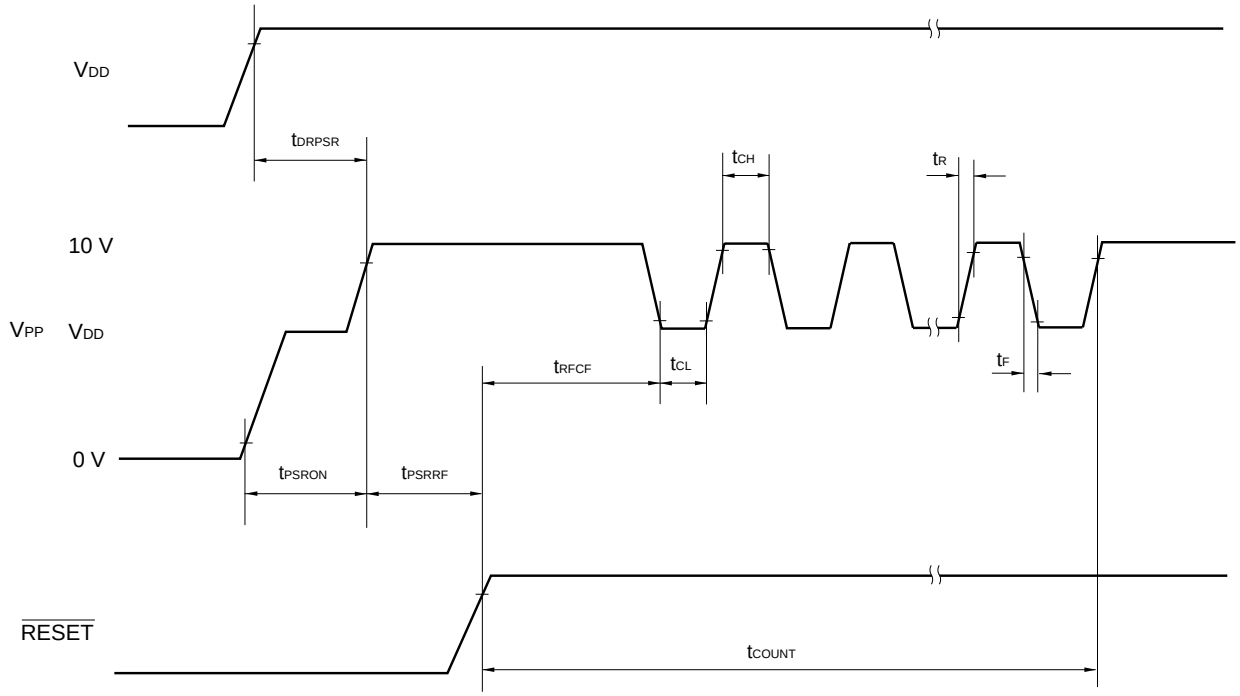
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	f_X		8.0		8.5	MHz
Power supply voltage	V_{PPL}	During V_{PP} low-level detection	0		$0.2V_{DD}$	V
	V_{PPH}	During V_{PP} high-level detection	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PP}	During V_{PP} high-voltage detection	9.7	10.0	10.3	V
V_{DD} power supply current	I_{DD}				50	mA
V_{PP} power supply current	I_{PP}	V_{PP} = 10 V			100	mA
Write time	T_{WRT}	1 byte		50	500	μs
Number of rewrite times	C_{WRT}				20	Times
Erase time	T_{ERASE}			6		s

(2) AC CHARACTERISTICS (T_A = –20 to +60°C, V_{DD} = 4.0 to 5.5 V)

Flash memory write mode

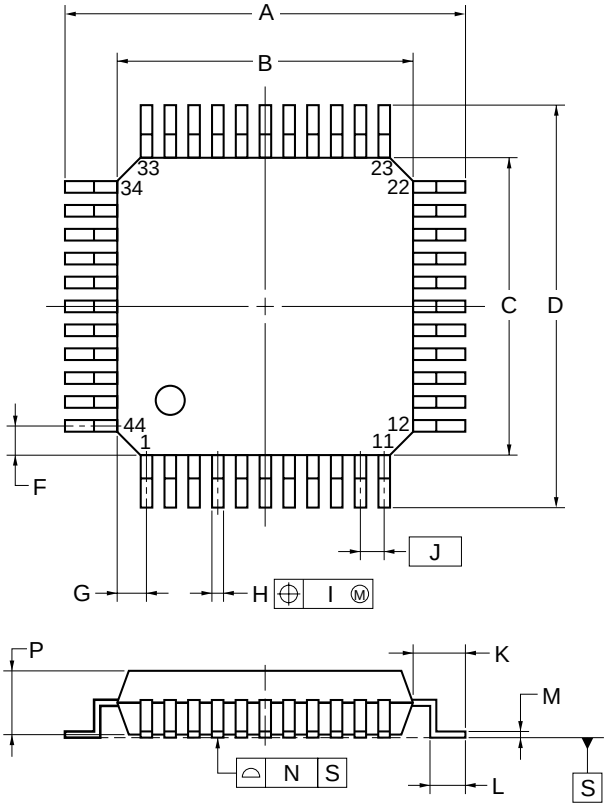
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
V_{DD} ↑→ V_{PP} ↑ set time	t_{DRPSR}	V_{PP} high voltage	1.0			μs
V_{PP} ↑→ $\overline{\text{RESET}}$ ↑ set time	t_{PSRRF}	V_{PP} high voltage	1.0			μs
$\overline{\text{RESET}}$ ↑→ V_{PP} count start time	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} pulse high-level width and low-level width	t_{CH}, t_{CL}		8.0			μs
V_{PP} pulse rising time and falling time	t_R, t_F				Undefined	μs

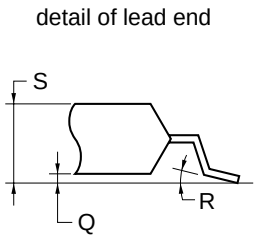
FLASH MEMORY WRITE MODE



8. PACKAGE DRAWINGS

44 PIN PLASTIC QFP (10 × 10 mm) PACKAGE DRAWING





NOTE

1. Controlling dimension — millimeter.
2. Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.	0.119 MAX.

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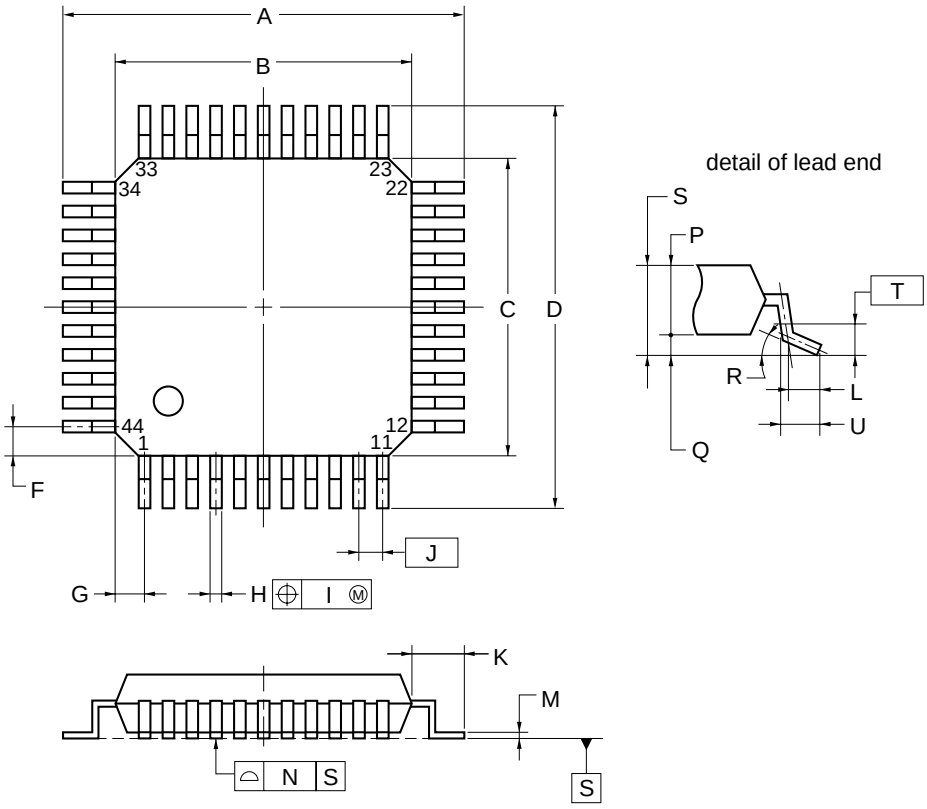
44 PIN PLASTIC QFP (10 × 10 mm) PACKAGE DRAWING



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

APPENDIX A DIFFERENCES BETWEEN THE μPD78F9842 AND MASK ROM VERSIONS

The μPD78F9842 is produced by replacing the internal ROM of a mask ROM version with flash memory. Table A-1 lists the differences between the μPD78F9842 and mask ROM versions.

Table A-1. Differences between the μPD78F9842 and Mask ROM Versions

Item		Flash Memory Version	Mask ROM Version	
		μPD78F9842	μPD789841	μPD789842
Internal memory	ROM	16 Kbytes	8 Kbytes	16 Kbytes
	High-speed RAM	256 bytes		
IC pin		Not provided	Provided	
V_{PP} pin		Provided	Not provided	
Electrical specifications		May differ between the flash memory and mask ROM versions		

Caution There are differences in the amount of noise tolerance and noise radiation between flash memory versions and mask ROM versions. When considering changing from a flash memory product to a mask ROM version during process from experimental manufacturing to mass production, make sure to sufficiently evaluate the flash memory versions using commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

APPENDIX B DEVELOPMENT TOOLS

The following development tools are available for developing systems that use the μPD78F9842.

LANGUAGE PROCESSING SOFTWARE

RA78K0S Notes 1, 2, 3	Assembler package common to the 78K/0S Series
CC78K0S Notes 1, 2, 3	C compiler package common to the 78K/0S Series
DF789842 Notes 1, 2, 3, 5	Device file for the μPD789842 Subseries

FLASH MEMORY WRITE TOOLS

Flashpro III (Model number: FL-PR3 Note 4, PG-FP3)	Dedicated flash programmer for on-chip flash memory
FA-44GB Note 4	Flash memory write adapter for 44-pin plastic QFP. Connection is required according to the target product.
Flashpro III controller	A program controlled by a PC is included in the Flashpro III. Can be operated in Windows™ 95.

DEBUGGING TOOLS

IE-78K0S-NS In-circuit emulator	This in-circuit emulator is used to debug hardware or software when application systems that use the 78K/0S Series are developed. The IE-78K0S-NS supports the integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter	This adapter is used to supply power from a 100- to 240-V AC outlet.
IE-70000-98-IF-C Interface adapter	This adapter is required when a PC-9800 series computer (other than a notebook type) is used as the host machine for the IE-78K0S-NS. (C bus supported)
IE-70000-CD-IF-A Note 5 PC card interface	This PC card and interface cable are required when a PC-9800 series computer is used as the host machine for the IE-78K0S-NS. (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter	This adapter is required when IBM PC/AT™ or compatibles are used as the host machine for the IE-78K0S-NS. (ISA bus supported)
IE-70000-PCI-IF Note 5 Interface adapter	This adapter is required when a PCI bus embedded computer is used as the host machine for the IE-78K0S-NS.
IE-789842-NS-EM1 Emulation board	This board is used to emulate the peripheral hardware specific to the device. The IE-789842-NS-EM1 is used in combination with the in-circuit emulator.
NP-44GB Note 4	This board is used to connect the in-circuit emulator to the target system. The NP-44GB is for the 44-pin plastic QFP.
SM78K0S Notes 1, 2	System simulator common to all 78K/0S series units
ID78K0S-NS Notes 1, 2, 5	Integrated debugger common to all 78K/0S series units
DF789842 Notes 1, 2, 5	Device file for the μPD789842 Subseries

REAL-TIME OS

MX78K0S Notes 1, 2	OS for the 78K/0S Series

Notes 1. Based on the PC-9800 series (MS-DOS™ + Windows)

2. Based on IBM PC/AT and compatibles (Japanese/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™, (SunOS™ and Solaris™), and NEWS™ (NEWS-OS™)

4. Product manufactured by Naito Densei Machidaseisakusho. (+81-44-822-3813). Consult an NEC sales representative regarding purchase.

5. Under development

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789842.

APPENDIX C RELATED DOCUMENTS

DOCUMENTS RELATED TO DEVICES

Document Name	Document No.	
	Japanese	English
μPD789841, 789842 Preliminary Product Information	U13790J	U13790E
μPD78F9842 Preliminary Product Information	U13901J	This manual
μPD789842 Subseries User's Manual	U13776J	To be prepared
78K/0S Series User's Manual Instruction	U11047J	U11047E

DOCUMENTS RELATED TO DEVELOPMENT TOOLS (USER'S MANUALS)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows Base	Reference	U11489J	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger Windows Base	Reference	U12901J	U12901E
IE-78K0S-NS In-circuit Emulator		U13549J	U13549E
IE-789742-NS-EM1 Emulation Board		To be prepared	To be prepared

DOCUMENTS RELATED TO SOFTWARE TO BE INCORPORATED INTO THE PRODUCT (USER'S MANUALS)

Document Name		Document No.	
		Japanese	English
OS for 78K/0S Series MX78K0S	Basics	U12938J	U12938E

OTHER DOCUMENTS

Document Name	Document No.	
	Japanese	English
IC Package Manual (CD-ROM)	–	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Quality Assurance for Semiconductor Devices	–	MEI-1202
Microcomputer Product Series Guide	U11416J	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest documents when designing application systems.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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