PENDER
ELECTRONIC DESIGN

GR-TMTC Mezzanine

User Manual

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GR-TMTC Mezzanine User Manual

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REVISION HISTORY

Revision	Date	Page	Description
0.1	2006-09-07	All	First issue

1 INTRODUCTION

1.1 Overview

The *GR-TMTC* equipment provides a hardware platform for the implementation of LEON3 systems together with IP cores which implement TMTC (RS422) and SPACEWIRE interfaces.

The assembly (Figure 1-1) consists of the following hardware elements:

- *GR-CPCI-XC4V* FPGA Development Board
- *GR-TMTC* Mezzanine Interface Board with Front Panel and wiring Harness

The FPGA development board must be programmed with an suitable FPGA configuration.

Although the equipment can be used 'stand-alone' on the bench top, it is intended to be installed in a Compact PCI rack. The *GR-TMTC* assembly requires one Compact PCI back plane slot. However, the width of the front panel requires two slot widths (8 TE).

It is also possible to add the optional *GR-CPCI-RS232* accessory board to the assembly. This accessory board provides two UART (serial RS232) interfaces connected by ribbon cable to J4, and a Reset switch which can be connected to the JP5 reset header on the *GR-CPCI-XC4V* board.

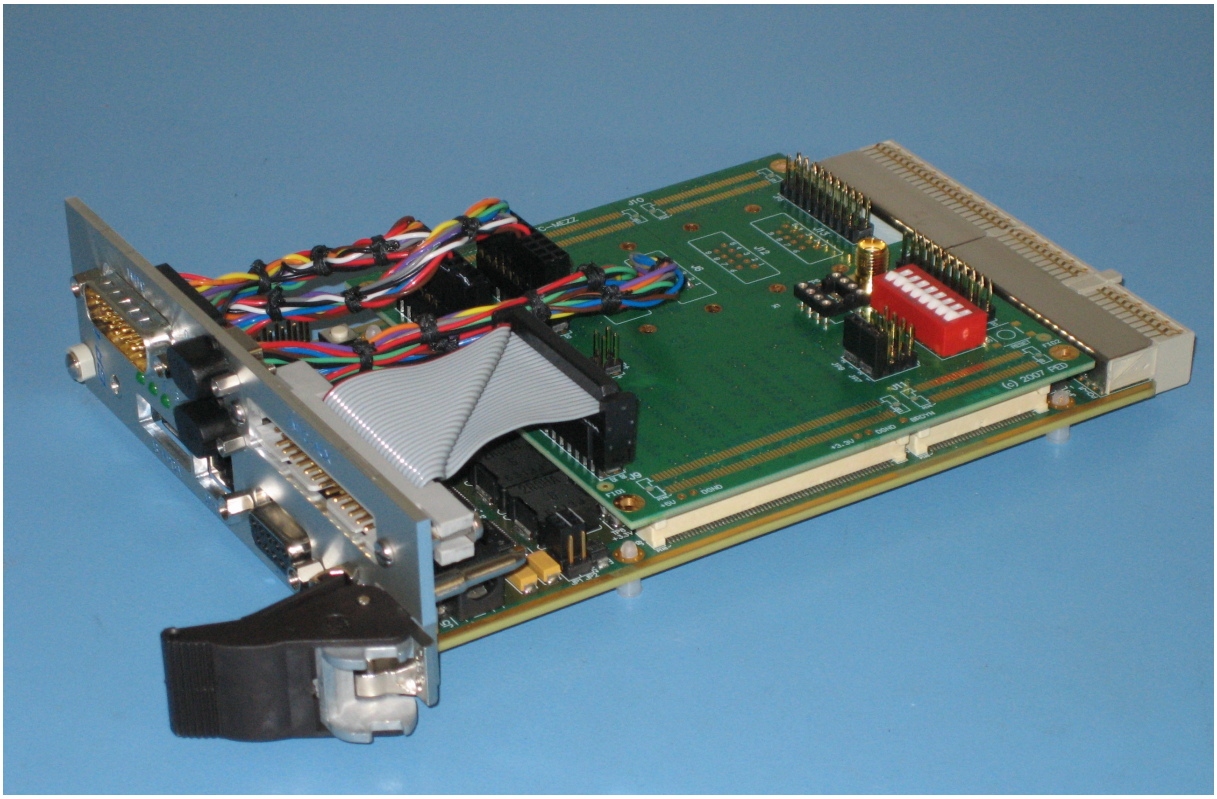

Figure 1-1: *GR-TMTC* Assembly

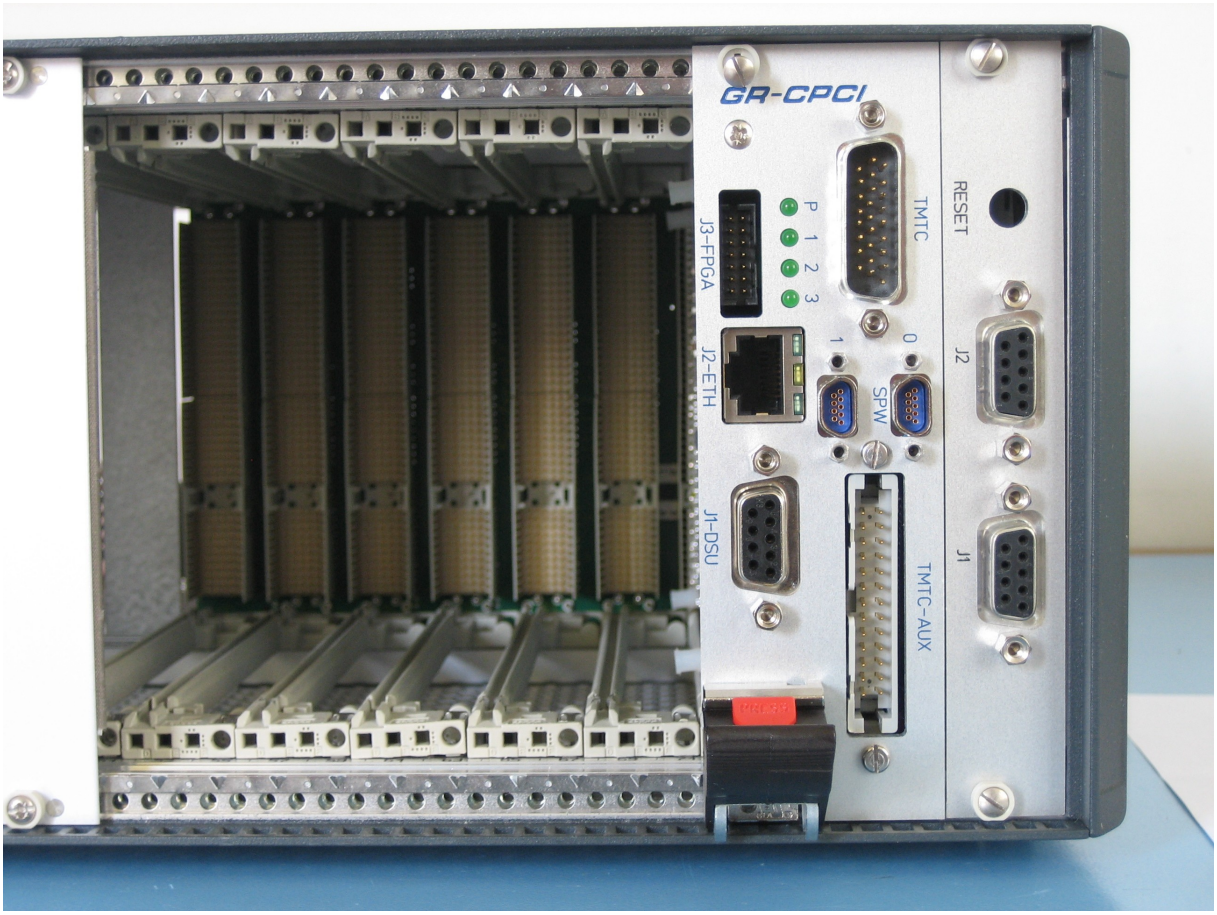

Figure 1-2: *GR-TMTC* Assembly mounted in Compact PCI rack

The *GR-TMTC* mezzanine front panel provides circuits and connectors for:

- serial Debug Support Unit interface (D9 Female connector)
- Ethernet interface (RJ45 connector)
- JTAG connector for FPGA programming
- two LVDS (Spacewire type) electrical interfaces (Microminiature MDM9S connectors)
- TMTC RS422 interfaces (HDD26 Male connector)
- Auxilliary TMTC RS422 and TTL signals (0.1” Shrouded Headers)
- power indicator (LED) and three user definable LED indicators

The *GR-CPCI-RS232* front panel provides circuits and connectors for:

- two serial RS232 interfaces (D9 Female connectors)
- push button for system reset

To enable convenient connection to the interfaces, the connector types and pin-outs are compatible with the standard connector types for these types of interfaces. The pin out information is listed in section 3 of this document.

1.2 References

More detailed information concerning the implementation and configuration of the elements making up the *GR-TMTC* assembly is provided in the following documents:

RD-1 GR-CPCI-XC4V Leon Development Board Users Manual

RD-2 GR-CPCI-XC4V_schematic.pdf, Schematic

RD-3 GR-CPCI-XC4V_assy_drawing.pdf, Assembly Drawing

RD-4 GR-TMTC-MEZZ_schematic.pdf, Schematic

RD-5 GR-TMTC-MEZZ_assy_drawing.pdf, Assembly Drawing

RD-6 GR-TMTC-Harness_schematic.pdf, Schematic

1.3 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This board contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the board observe appropriate precautions and ESD safe practices.

When not in use, store the board in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the board is in an unpowered state.

1.4 Abbreviations

ESD	Electro-Static Discharge
FPGA	Field Programmable Gate Array
FT	Fault-Tolerant
GPIO	General Purpose Input / Output
I/O	Input/Output
LVDS	Low Voltage Digital Signaling
PCB	Printed Circuit Board
SPW	Spacewire

2 ELECTRICAL DESIGN

2.1 Block Diagram

The *GR-TMTC* assembly provides the electrical functions and interfaces as represented in the block diagram, Figure 2-1.

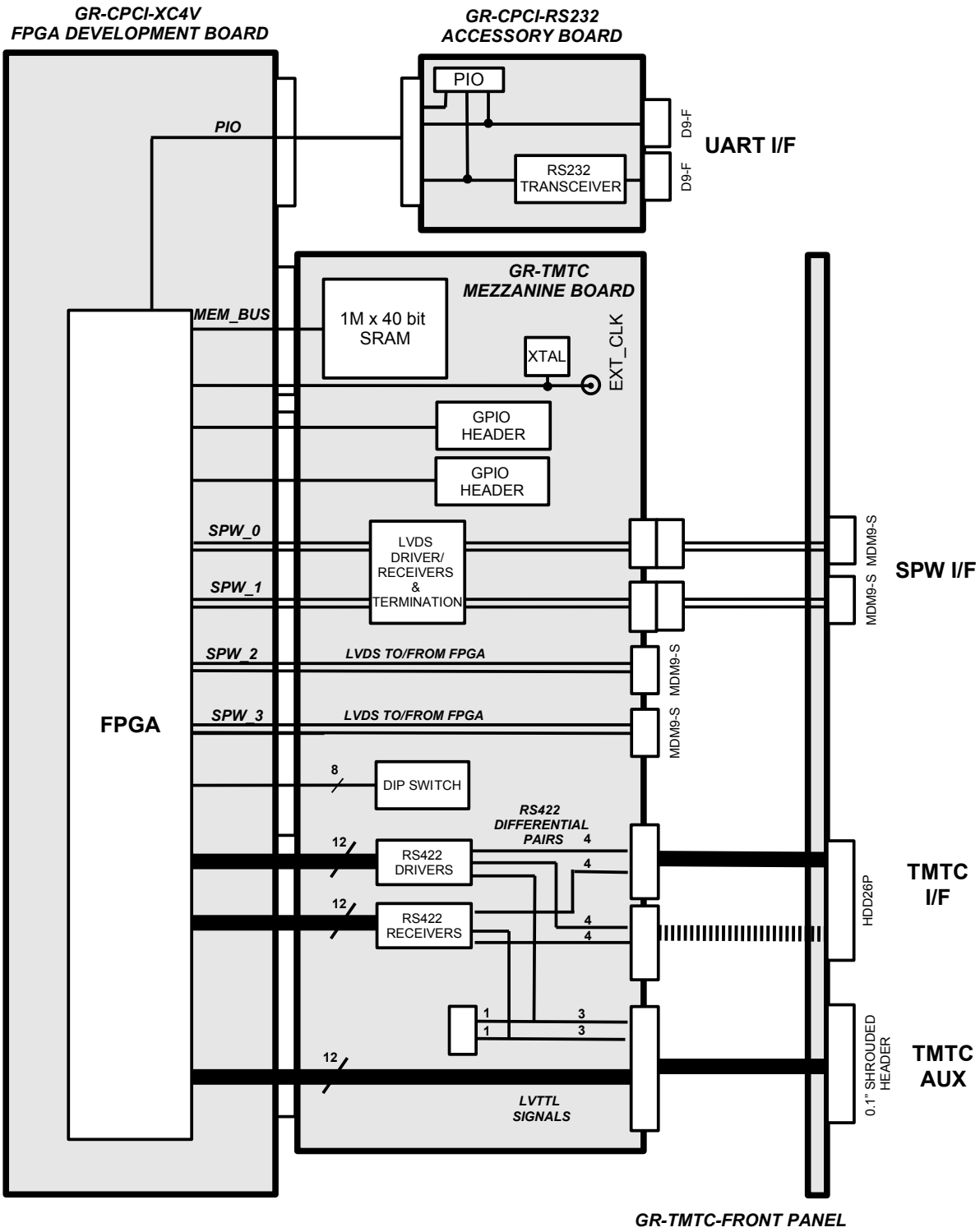

Figure 2-1: Block Diagram of *GR-TMTC* assembly and harness

As shown in the block diagram, the GR-TMTC Mezzanine contains the following circuits:

- 40Mbit (1MWord x 40 bit) SRAM memory (10ns)
- 8 pin DIL socket and SMA connector for user defined oscillator
- Headers for 2 x 16 General Purpose I/O signals (LVTTL)
- 8 pole DIP Switch for general purpose use
- Two sets of SPW signals: These signals are LVTTL input/ouputs to the FPGA and are provided with driver/receiver IC's on the mezzanine to provide the level conversion from single ended LVTTL to/from LVDS differential signals
- Two sets of SPW signals: These signals are LVDS input/ouputs directly to the FPGA. No driver/receiver circuits are required on the Mezzanine. However, the FPGA design must be appropriately configured for LVDS levels and termination on these inputs/outputs (more information in section 2.2).
- RS422 differential drivers for 12 signal pairs
- RS422 differential receivers for 12 signal pairs
- 12 single-ended LVTTL signals which can be defined as inputs or outputs
- Wiring from two front panel MDM9S connectors
- two 20 pin headers each providing an additional 16 general purpose LVTTL I/O signals connected directyl to the FPGA
- Wire and ribbon cable harness connecting from headers on mezzanine to connectors on GR-TMTC Front Panel

Figure 2-2 shows the completed *GR-TMTC* assembly including the cabling and harness to the front panel.

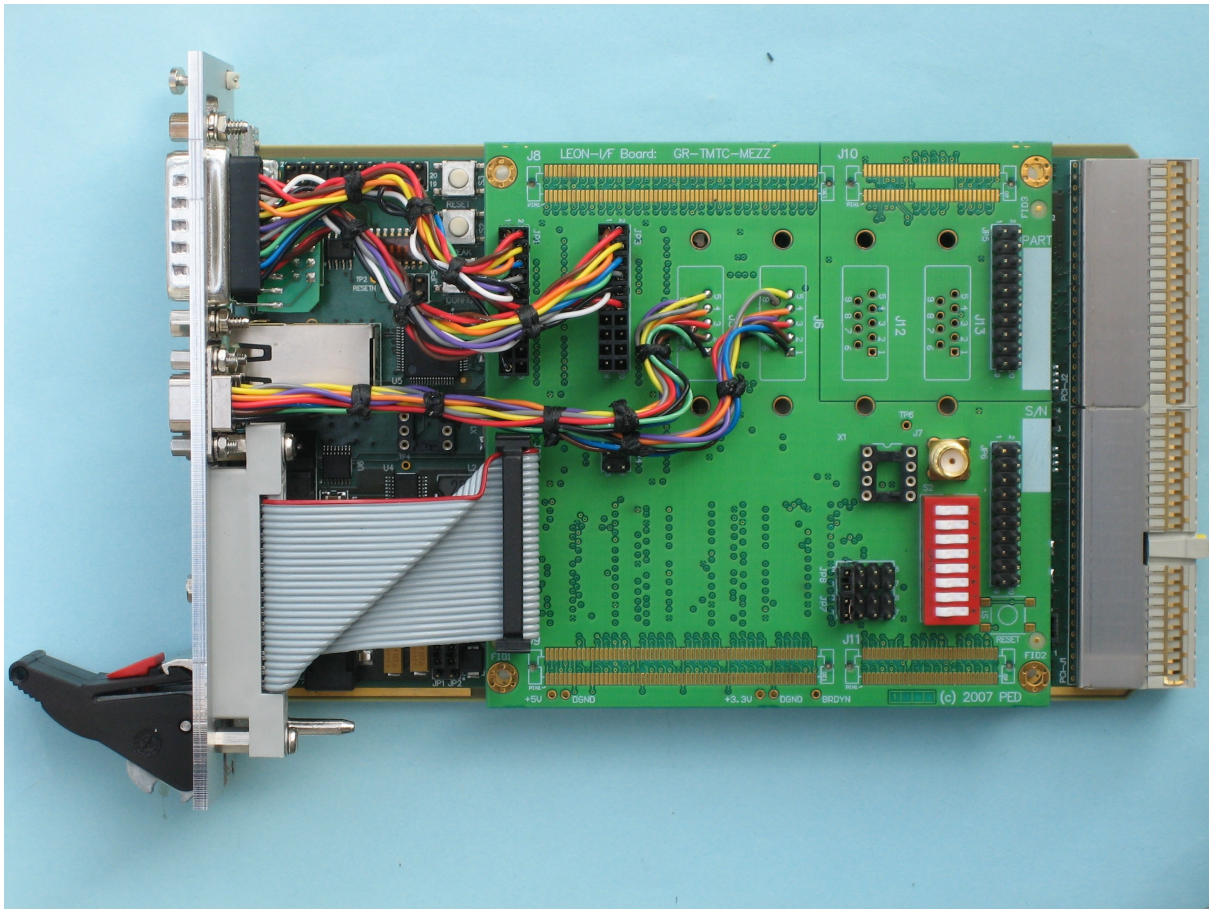

Figure 2-2: GR-CPCI-XC4V board with GR-TMTC-FLEX Mezzanine and front-panel

2.2 Configuration for FPGA VLDS signals

In the GR-TMTC kit, for two of the SPW interfaces the LVDS receiver and transmitter pairs are provided directly from LVDS pairs of the FPGA, and there are no discrete LVDS receiver/transmitter devices on the mezzanine board. For these sets of signals.

This requires that the FPGA design must be appropriately configured for LVDS input/outputs on the appropriate pins and that the FPGA bank voltage for the LVDS signals is set for 2.5V (This is the default configuration for the GR-CPCI-XC4V board),

Also, the Virtex4 FPGA on the GR-CPCI-XC4V board provides the possiblity to provide 100 Ohm termination for the LVDS receiver pairs internally to the FPGA, eliminating the need to provide termination on the mezzanine board itself. However, for this to operate, the following resistors are require to be installed on the GR-CPCI-XC4V board: R112, (50Ohms) and R137 (50 Ohms) which are not normally fitted in the default configuration for the GR-CPCI-XC4V board.

3 INTERFACES AND CONFIGURATION

3.1 List of Front Panel Connectors

Name	Function	Type	Description
J1	DSU	D9S	
J2	ETHERNET	RJ45	Ethernet network connector
J3	JTAG-FPGA	2x7 pin shrouded 2mm header	FPGA configuration and programming
SPW-0	SPW-0	MDM9-S (female)	LVDS connections for Spacewire Interface-0
SPW-1	SPW-1	MDM9-S (female)	LVDS connections for Spacewire Interface-1
TMTC	TMTC	HDDP26	The connector pinning and naming for this connector has been defined to be compoatible with the
TMTC-AUX	TMTC-AUX	26 pin shrouded 0.1” header	

Table 3-1: List of Front Panel Connectors

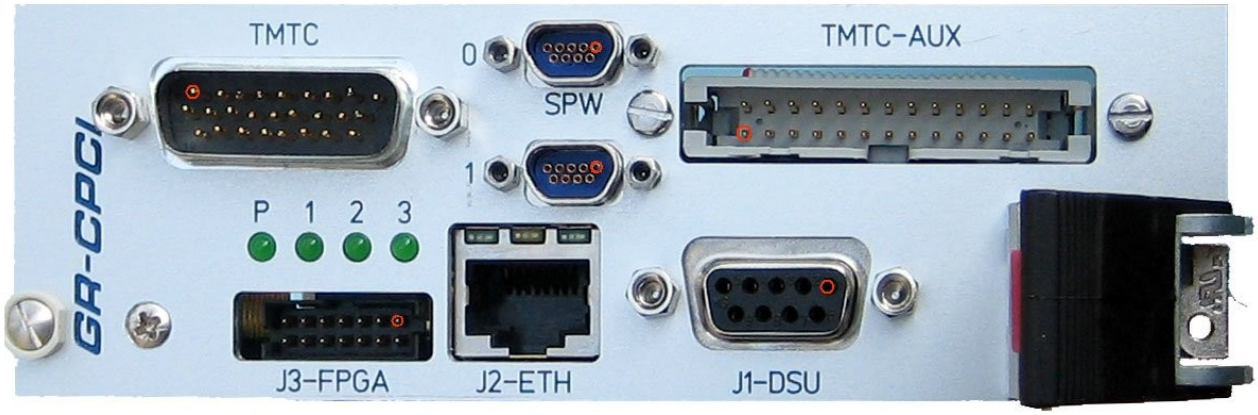

Figure 3-1: Front Panel view (Pin1's marked with red circle)

Pin	Name	Comment
1		No connect
6		No connect
2	DSU-TX	Transmit pin from DSU UART
7		No connect
3	DSU-RX	Receive pin to DSU UART
8		No connect
4		No connect
9		No connect
5	GND	Ground

Table 3-2: J1 DSU - Debug Support Unit connections

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output center-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input Center-tap
8		No connect

Table 3-3: J2 RJ45-ETHERNET Connector

Pin	Name	Comment
1	DGND	Ground
2	VREF / VREF	3.3V
3	DGND	Ground
4	TMS / PROG	JTAG: TMS or Slave serial: PROG
5	DGND	Ground
6	TCK / CCLK	JTAG: TCK or Slave serial: CCLK
7	DGND	Ground
8	TDO / DONE	JTAG: TDO or Slave serial: DONE
9	DGND	Ground
10	TDI / DIN	JTAG: TDI or Slave serial: DIN
11	DGND	Ground
12	NC / NC	No connect
13	DGND	Ground
14	NC / INIT	JTAG: no connect or Slave serial: INIT

Table 3-4: J3 FPGA – Programming Connector

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 3-5: SPW-0 : Spacewire interface connections

Pin	Name	Comment
1	DIN1+	Data In +ve
6	DIN1-	Data In -ve
2	SIN1+	Strobe In +ve
7	SIN1-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT1+	Strobe Out +ve
4	SOUT1-	Strobe Out -ve
9	DOUT1+	Data Out +ve
5	DOUT1-	Data Out -ve

Table 3-6: SPW-1 : Spacewire interface connections

Pin	Name	Comment
10	N/C	Not connected
1	TC-CLK_N	TC Clock -ve (RS422) Prime
19	TC-CLK_N'	TC Clock -ve (RS422) Redundant
11	TM-CLK_N'	TM Clock -ve (RS422) Redundant
2	TC-CLK_P	TC Clock +ve (RS422) Prime
20	TC-CLK_P'	TC Clock +ve (RS422) Redundant
12	TM-CLK_P'	TM Clock +ve (RS422) Redundant
3	TC-DATA_P	TC Data +ve (RS422) Prime
21	TC-DATA_P'	TC Data +ve (RS422) Redundant
13	TM-CLK_P	TM Clock +ve (RS422) Prime
4	TC-DATA_N	TC Data -ve (RS422) Prime
22	TC-DATA_N'	TC Data -ve (RS422) Redundant
14	TM-CLK_N	TM Clock -ve (RS422) Prime
5	TC-Spare_P	TC Spare +ve (RS422) Prime
23	TC-Spare_N'	TC Spare -ve (RS422) Redundant
15	TM-DATA_N	TM Data -ve (RS422) Prime
6	TC-Spare_N	TC Spare -ve (RS422) Prime
24	TC-Spare_P'	TC Spare +ve (RS422) Redundant
16	TM-DATA_P	TM Data +ve (RS422) Prime
7	TC-Active_P	TC Active +ve (RS422) Prime
25	TC-Active_P'	TC Active +ve (RS422) Redundant
17	TM-Data_P'	TM Data +ve (RS422) Redundant
8	TC-Active_N	TC Active -ve (RS422) Prime
26	TC-Active_N'	TC Active -ve (RS422) Redundant
18	TM-Data_N'	TM Data -ve (RS422) Redundant
9	DGND	Ground

Table 3-7: TMTC : TMTC interface connections

Pin	Name	Comment
1	CLCWIn_P0	CLCWIn0 +ve (RS422)
2	CLCWIn_N0	CLCWIn0 -ve (RS422)
3	CLCWIn_P1	CLCWIn1 +ve (RS422)
4	CLCWIn_N1	CLCWIn1 -ve (RS422)
5	CLCWOut_P0	CLCWOut0 +ve (RS422)
6	CLCWOut_N0	CLCWOut0 -ve (RS422)
7	CLCWOut_P1	CLCWOut1 +ve (RS422)
8	CLCWOut_N1	CLCWOut1 -ve (RS422)
9	CPDU_Clk	CPDU_Clk (LVTTL)
10	CPDU_Data	CPDU_Data (LVTTL)
11	CPDU_Arm	CPDU_Arm (LVTTL)
12	CPDU_Strobe	CPDU_Strobe (LVTTL)
13	TW_In_P	TW_In +ve (RS422)
14	TW_In_N	TW_In -ve (RS422)
15	TW_Out_P	TW_Out +ve (RS422)
16	TW_Out_N	TW_Out -ve (RS422)
17	Datation_0	Datation_0 (LVTTL)
18	Pulses_0	Pulses_0 (LVTTL)
19	Datation_1	Datation_1 (LVTTL)
20	Pulses_1	Pulses_1 (LVTTL)
21	Datation_2	Datation_2 (LVTTL)
22	Pulses_2	Pulses_2 (LVTTL)
23	Datation_3	Datation_3 (LVTTL)
24	Pulses_3	Pulses_3 (LVTTL)
25	DGND	DGND
26	+3.3V	+3.3V

Table 3-8: TMTC-AUX : TMTC Auxilliary interface connections

LED	FPGA signal	FPGA Pin	Comment
LED P	+3.3V	--	3.3V power present on board
LED 1	LED1		User definable LED – e..g connect to processor signal 'DSUACT'
LED 2	LED2		User definable LED – e..g connect to processor signal 'ERRORN'
LED 3	LED2		User definable LED – e..g connect to processor signal 'WATCHDOG'

Table 3-9: List of Front Panel LED's and their driving signals

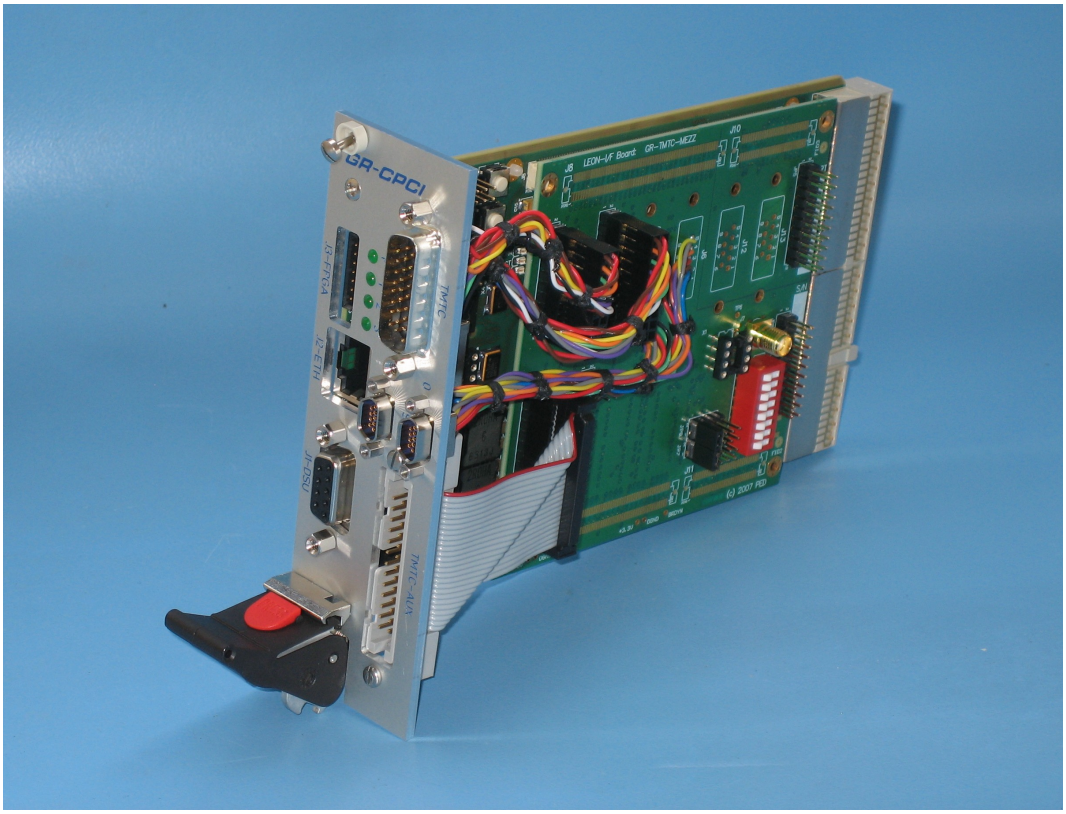

Figure 3-2: Assembly Photo Top view Oblique

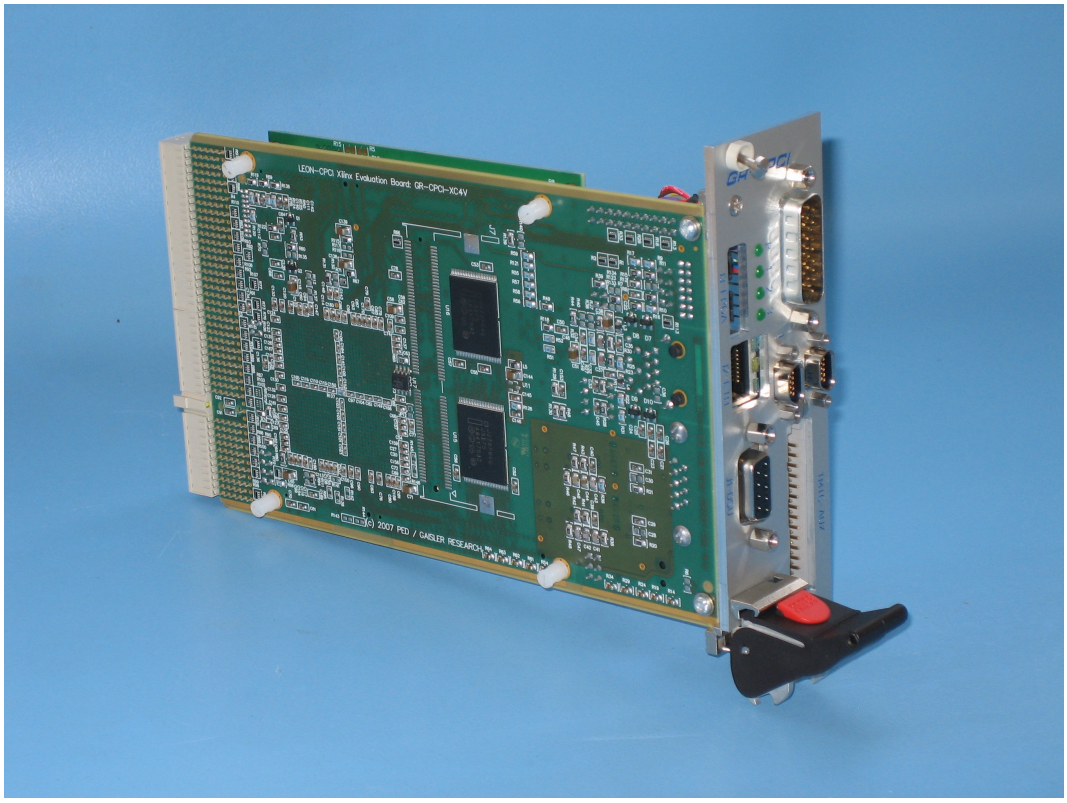

Figure 3-3: Assembly Photo Bottom view Oblique

3.2 List of Mezzanine Connectors

Figure 3-4 And Figure 3-5 show views of the Mezzanine board which is mounted to the GR-CPCI-XC4V board. The following tables list

In the default configuration, only connectors JP1, JP2, J5 and J6 are connected to the front panel. The connections from the mezzanine board to the front panel are described by the schematic, RD-6.

The mezzanine board also provided a number of other headers which, if appropriate could be used in other configurations to provide additional signal input/outputs

The following table list the headers and signals on the Mezzanine board.

In the tables, the name of the corresponding GENIO signal on the FPGA which drives the function of the pin and its pin number are indicated in the tables. Note that signals which are the negative pin of an differential pair driver/receiver are shown in brackets as they are driven/receive the same effective signal as its corresponding positive pin of the pair.

In the event of discrepancies, please refer to the schematic drawings.

Name	Function	Type	Description
JP1	TMTC - Prime	2 row x 10 pin 0.1” Header	RS422 TMTC signals (Prime set)
JP2	TMTC - AUX	2 row x 13 pin 0.1” Header	Auxilliary RS422 and TTL signals
JP3	TMTC – Redun.	2 row x 10 pin 0.1” Header	RS422 TMTC signals (Redundant set)
JP4	AUX	2 row x 2 pin 0.1” Header	2 Auxilliary RS232 signals
JP5	GPIO Signal Header-1	2 row x 10 pin 0.1” Header	General purpose TTL signals
JP6	GPIO Signal Header-2	2 row x 10 pin 0.1” Header	General purpose TTL signals
JP7	RAMSN bank config.	2 row x 4 pin 0.1” Header	Jumpers to select RAM bank
JP8	RAMOEN bank config.	2 row x 4 pin 0.1” Header	Jumpers to select RAM bank
J5	SPW-0	MDM9S footprint	SPW interface with LVDS driver/receivers
J6	SPW-1	MDM9S footprint	SPW interface with LVDS driver/receivers
J12	SPW-2	MDM9S footprint	SPW interface direct to FPGA
J13	SPW-3	MDM9S footprint	SPW interface direct to FPGA

Table 3-10: List of Mezzanine Headers

FUNCTION		FPGA signal	FPGA Pin	CONNECTOR PIN			FPGA Pin	FPGA signal		FUNCTION
TC_Clk0_P	IN	GENIO50	F28	1	■ □	2		(GENIO50)	IN	TC_Clk0_N
TC_Data0_P	IN	GENIO51	A26	3	□ □	4		(GENIO51)	IN	TC_Data0_N
TC_Active0_P	IN	GENIO52	G25	5	□ □	6		(GENIO52)	IN	TC_Active0_N
TC_Spare0_P	IN	GENIO53	E27	7	□ □	8		(GENIO53)	IN	TC_Spare0_N
TM_Clk0_P	OUT	GENIO54	G26	9	□ □	10		(GENIO54)	OUT	TM_Clk0_N
TM_Data0_P	OUT	GENIO55	D27	11	□ □	12		(GENIO55)	OUT	TM_Data0_N
TM_Spare1_P	OUT	GENIO57	D29	13	□ □	14		(GENIO57)	OUT	TM_Spare1_N
TM_Spare2_P	OUT	GENIO59	E29	15	□ □	16		(GENIO59)	OUT	TM_Spare2_N
n.c.		---		17	□ □	18		---		n.c.
DGND		---		19	□ □	20		---		DGND

Table 3-11: JP1 - TMTC-Prime Header

FUNCTION		FPGA signal	FPGA Pin	CONNECTOR PIN			FPGA Pin	FPGA signal		FUNCTION
CLCWIn_P0	IN	GENIO28	L34	1	■ □	2		(GENIO28)	IN	CLCWIn_N0
CLCWIn_P1	IN	GENIO29	M33	3	□ □	4		(GENIO29)	IN	CLCWIn_N1
CLCWOut_P0	OUT	GENIO24	N34	5	□ □	6		(GENIO24)	OUT	CLCWOut_N0
CLCWOut_P1	OUT	GENIO25	P35	7	□ □	8		(GENIO25)	OUT	CLCWOut_N1
CPDU_Clk	BIDI	GENIO32	K33	9	□ □	10		GENIO33	BIDI	CPDU_Data
CPDU_Arm	BIDI	GENIO35	U37	11	□ □	12		GENIO34	BIDI	CPDU_Strobe
TW_In_P	IN	GENIO30	L33	13	□ □	14		(GENIO30)	IN	TW_In_N
TW_Out_P	OUT	GENIO26	M35	15	□ □	16		(GENIO26)	OUT	TW_Out_N
Datation_0	BIDI	GENIO139	AM5	17	□ □	18		GENIO135	BIDI	Pulses_0
Datation_1	BIDI	GENIO138	AN3	19	□ □	20		GENIO134	BIDI	Pulses_1
Datation_2	BIDI	GENIO137	AP4	21	□ □	22		GENIO133	BIDI	Pulses_2
Datation_3	BIDI	GENIO136	AN4	23	□ □	24		GENIO132	BIDI	Pulses_3
DGND				25	□ □	26				+3.3V

Table 3-12: JP2 - TMTC Aux I/O Header

FUNCTION		FPGA signal	FPGA Pin	CONNECTOR PIN			FPGA Pin	FPGA signal		FUNCTION
TC_Clk0_P	IN	GENIO47	N37	1	■ □	2		(GENIO47)	IN	TC_Clk0_N
TC_Data0_P	IN	GENIO46	J37	3	□ □	4		(GENIO46)	IN	TC_Data0_N
TC_Active0_P	IN	GENIO45	P37	5	□ □	6		(GENIO45)	IN	TC_Active0_N
TC_Spare0_P	IN	GENIO44	K36	7	□ □	8		(GENIO44)	IN	TC_Spare0_N
TM_Clk0_P	OUT	GENIO43	P36	9	□ □	10		(GENIO43)	OUT	TM_Clk0_N
TM_Data0_P	OUT	GENIO42	L36	11	□ □	12		(GENIO42)	OUT	TM_Data0_N
TM_Spare1_P	OUT	GENIO41	R37	13	□ □	14		(GENIO41)	OUT	TM_Spare1_N
TM_Spare2_P	OUT	GENIO40	M36	15	□ □	16		(GENIO40)	OUT	TM_Spare2_N
n.c.		---		17	□ □	18		---		n.c.
DGND		---		19	□ □	20		---		DGND

Table 3-13: JP3 - TMTC-Redundant Header

FUNCTION		FPGA signal	FPGA Pin	CONNECTOR PIN			FPGA Pin	FPGA signal		FUNCTION
AUX_OUT_P	OUT	GENIO27	N33	1	■ □	2		(GENIO27)	OUT	AUX_OUT_N
AUX_IN_P	IN	GENIO31	V37	3	□ □	4		(GENIO31)	IN	AUX_IN_N

Table 3-14: JP4 – Auxilliary (Spare) Signal Header

FUNCTION	FPGA signal	FPGA Pin	CONNECTOR PIN		FPGA Pin	FPGA signal	FUNCTION
GPIO0	GENIO95	AD37	1	2	AL38	GENIO94	GPIO1
GPIO2	GENIO92	AL39	3	4	AC37	GENIO93	GPIO3
GPIO4	GENIO90	AM38	5	6	AD36	GENIO91	GPIO5
GPIO6	GENIO88	AM37	7	8	AD35	GENIO89	GPIO7
GPIO8	GENIO86	AC32	9	10	AF36	GENIO87	GPIO9
GPIO10	GENIO84	AB31	11	12	AE36	GENIO85	GPIO11
GPIO12	GENIO82	AB30	13	14	AG36	GENIO83	GPIO13
GPIO14	GENIO80	AC30	15	16	AG35	GENIO81	GPIO15
+3.3V	---		17	18		---	+3.3V
DGND	---		19	20		---	DGND

Table 3-15: JP5 – GPIO Signal Header -1

FUNCTION	FPGA signal	FPGA Pin	CONNECTOR PIN		FPGA Pin	FPGA signal	FUNCTION
GPIO16	GENIO151	AM2	1	2	AG8	GENIO150	GPIO17
GPIO18	GENIO149	AP1	3	4	AK4	GENIO148	GPIO19
GPIO20	GENIO147	AL5	5	6	AL4	GENIO146	GPIO21
GPIO22	GENIO145	AK6	7	8	AM3	GENIO144	GPIO23
GPIO24	GENIO143	AP2	9	10	AL3	GENIO142	GPIO25
GPIO26	GENIO141	AN2	11	12	AL6	GENIO140	GPIO27
GPIO28	GENIO131	AT3	13	14	AR2	GENIO130	GPIO29
GPIO30	GENIO129	AU3	15	16	AR3	GENIO128	GPIO31
+3.3V	---		17	18		---	+3.3V
DGND	---		19	20		---	DGND

Table 3-16: JP6 – GPIO Signal Header -2

FUNCTION	FPGA signal	FPGA PIN	OPEN	SWITCH	CLOSED
SWITCH0	GENIO159	AG7	'1'	1	'0'
SWITCH1	GENIO158	AK3	'1'	2	'0'
SWITCH2	GENIO157	AK1	'1'	3	'0'
SWITCH3	GENIO156	AH3	'1'	4	'0'
SWITCH4	GENIO155	AL1	'1'	5	'0'
SWITCH5	GENIO154	AH7	'1'	6	'0'
SWITCH6	GENIO153	AM1	'1'	7	'0'
SWITCH7	GENIO152	AK2	'1'	8	'0'

Table 3-17: DIP Switch S1 definition

1-2	RAM Bank 0
3-4	RAM Bank 1
5-6	RAM Bank 2
7-8	RAM Bank 3

Jumpers JP7 & JP8: RAM Bank selection

(Both jumpers must be set the same)

Pin	Name	FPGA Signal	FPGA Pin	Comment
1	DIN0+	GENIO110	AF38	Data In +ve
6	DIN0-	(GENIO110)		Data In -ve
2	SIN0+	GENIO111	AG37	Strobe In +ve
7	SIN0-	(GENIO111)		Strobe In -ve
3	SHIELD			Inner Shield
8	SOUT0+	GENIO109	AG38	Strobe Out +ve
4	SOUT0-	(GENIO109)		Strobe Out -ve
9	DOUT0+	GENIO108	AF39	Data Out +ve
5	DOUT0-	(GENIO108)		Data Out -ve

Table 3-18: J5 : Spacewire interface connections

Pin	Name	FPGA Signal	FPGA Pin	Comment
1	DIN1+	GENIO106	AH39	Data In +ve
6	DIN1-	(GENIO106)		Data In -ve
2	SIN1+	GENIO107	AB28	Strobe In +ve
7	SIN1-	(GENIO107)		Strobe In -ve
3	SHIELD			Inner Shield
8	SOUT1+	GENIO105	AB27	Strobe Out +ve
4	SOUT1-	(GENIO105)		Strobe Out -ve
9	DOUT1+	GENIO104	AJ39	Data Out +ve
5	DOUT1-	(GENIO104)		Data Out -ve

Table 3-19: J6 : Spacewire interface connections

Pin	Name	FPGA Signal	FPGA Pin	Comment
1	DIN2+	GENIO126	AA34	Data In +ve
6	DIN2-	GENIO124	AA35	Data In -ve
2	SIN2+	GENIO127	AA31	Strobe In +ve
7	SIN2-	GENIO125	Y31	Strobe In -ve
3	SHIELD			Inner Shield
8	SOUT2+	GENIO120	AC35	Strobe Out +ve
4	SOUT2-	GENIO122	AB35	Strobe Out -ve
9	DOUT2+	GENIO121	Y29	Data Out +ve
5	DOUT2-	GENIO123	AA30	Data Out -ve

Table 3-20: J12 : Spacewire interface connections

Pin	Name	FPGA Signal	FPGA Pin	Comment
1	DIN3+	GENIO118	AC38	Data In +ve
6	DIN3-	GENIO116	AC39	Data In -ve
2	SIN3+	GENIO119	AE34	Strobe In +ve
7	SIN3-	GENIO117	AD34	Strobe In -ve
3	SHIELD			Inner Shield
8	SOUT3+	GENIO112	AE39	Strobe Out +ve
4	SOUT3-	GENIO114	AD39	Strobe Out -ve
9	DOUT3+	GENIO113	AD31	Data Out +ve
5	DOUT3-	GENIO115	AD32	Data Out -ve

Table 3-21: J13 : Spacewire interface connections

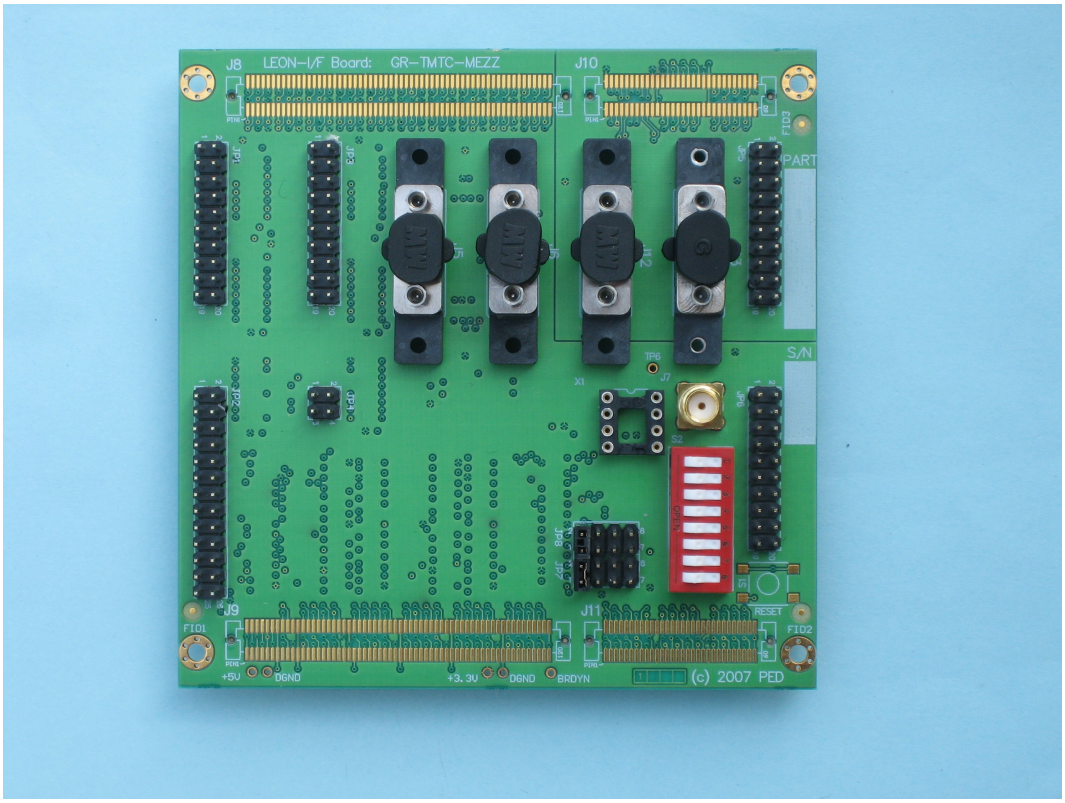

Figure 3-4: Mezzanine Photo Top view

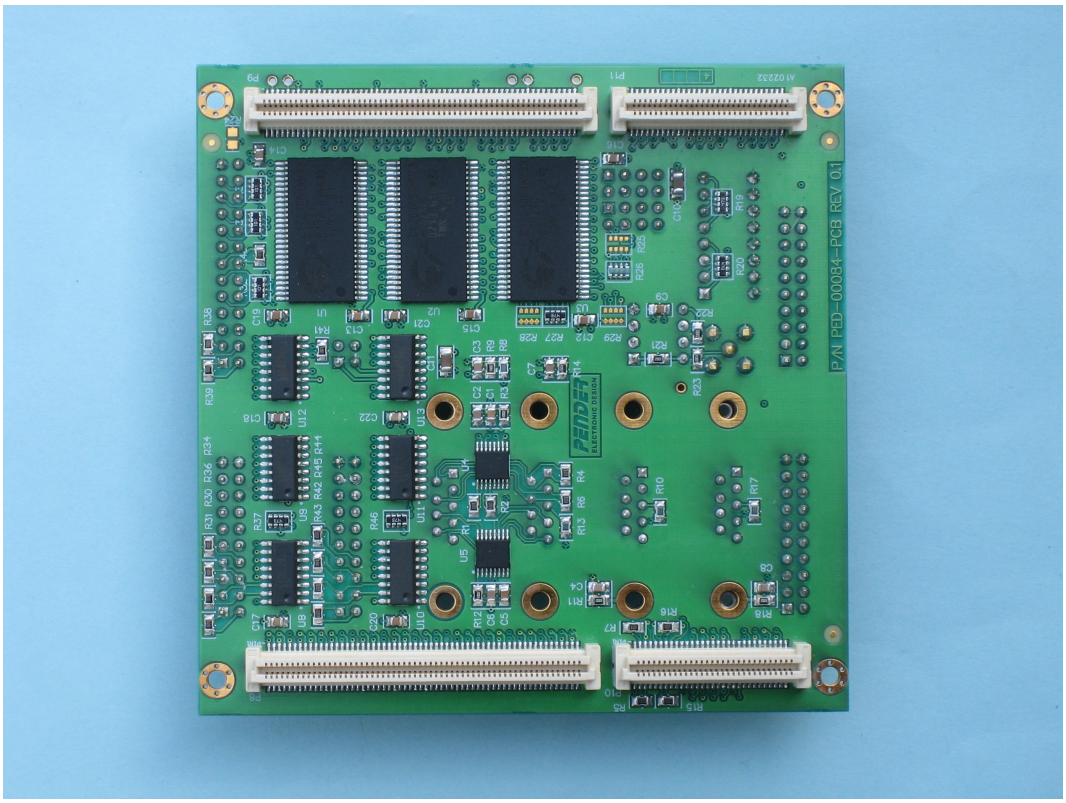

Figure 3-5: Mezzanine Photo Bottom view