logiREF-VIDEO-ISP-EVK

Xylon logicBRICKS™ Image Signal Processing (ISP) Reference Design for Xilinx® Zynq®-7000 AP SoC based MicroZed Embedded Vison Development Kit

User‘s Manual

Version: 1.00.a

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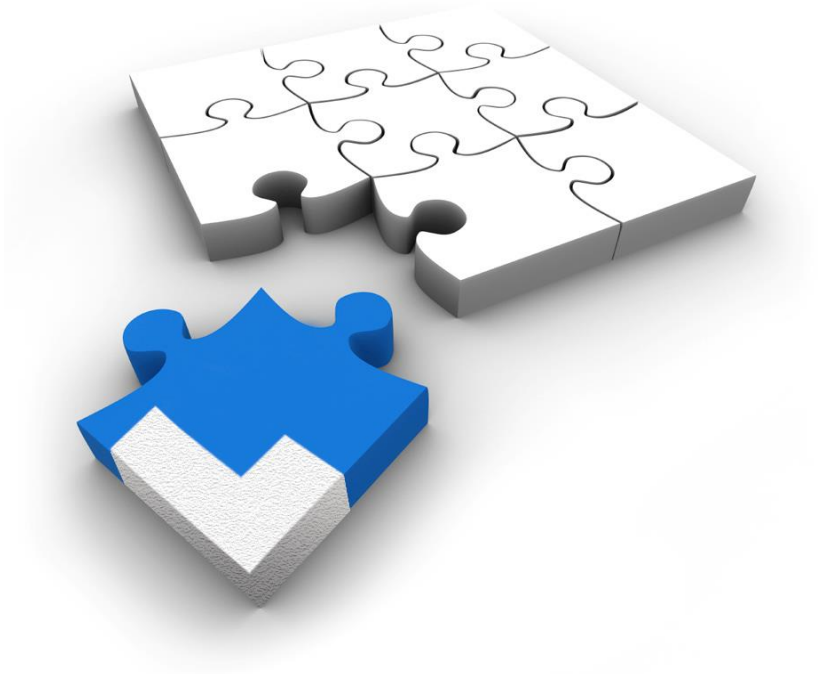


1 INTRODUCTION

Xylon's logiISP Image Signal Processing (ISP) Pipeline IP core is a full high-definition ISP pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx® Zynq®-7000 All Programmable SoC and 7 Series FPGA devices.

The logiISP IP core accepts diversely formatted video inputs generated by different sensors and removes defective pixels, de-mosaics Bayer encoded video, makes image color and gamma corrections, filters the noise from the video, collects video analytics data for various control algorithms and manipulates video data formats and color domains. IP core deliverables include the software driver, documentation and technical support. The IP core can be used with processor-based control algorithms for Auto White Balancing (AWB) and Auto Exposure (AE) that can be licensed from Xylon.

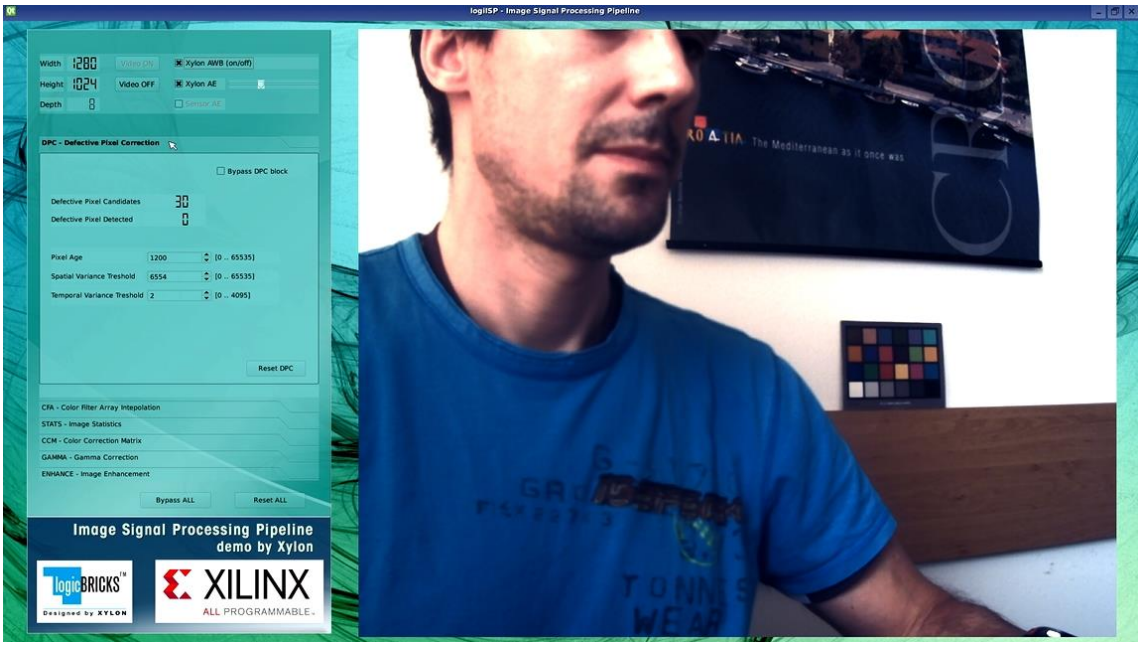


Figure 1 Screenshot from the Xylon Image Sensor Processing Pipeline (logiISP) Demo

Figure 2 and Figure 3 illustrate video quality enhancements achievable by the logiISP ISP pipeline IP core. Figure 3 shows the logiISP video output after the processing of the low-quality video input image shown on Figure 2.

This user's manual describes Xylon's logiREF-VIDEO-ISP-EVK ISP pipeline reference design for the MicroZed™ Embedded Vision Development Kit from Avnet Electronics Marketing and the ON Semiconductor's PYTHON-1300 1.3 MP video camera. This free and pre-verified logicBRICKS reference design includes evaluation logicBRICKS IP cores and hardware design files prepared for Xilinx Vivado® Design Suite. It also includes the complete Linux OS image, software drivers, demo applications and documentation.

The offered evaluation hardware design is customizable. logicBRICKS IP cores can be setup through the Vivado IP Integrator (IPI) and design users can evaluate different logiISP features, make changes on the logicBRICKS graphics sub-system and add third-party IP cores required by the target application.

Figure 2: Example logiISP Video Input

Figure 3: Example logiISP Video Output

1.1 Hardware Platform

The logiREF-VIDEO-ISP-EVK Image Signal Processing (ISP) Reference Design works with the the MicroZed Embedded Vision Kit from Avnet Electronics Marketing. A full evaluation requires the following hardware components:

Figure 4: Avnet MicroZed Embedded Vision Kit

- MicroZed Embedded Vision Development Kit
  (Part Number*: AES-MBCC-EMBV-DEV-KIT)
  or the equivalent combination built of:
  - MicroZed 7020 SOM
    (Part Number*: AES-Z7MB-7Z020-SOM-G)
  - MicroZed Embedded Vision Carrier Card Kit
    (Part Number*: AES-MBCC-EMBV-G)

and:

- ON Semiconductor PYTHON-1300-COLOR Camera
  (Part Number*: AES-CAM-ON-P1300C-G)

* Avnet Electronics Marketing part number – for more details visit www.microzed.org

1.2 Design Deliverables

1.2.1 Hardware Design Files

- Configuration bitstream file for the programmable logic
- MicroZed Embedded Vision Kit reference design prepared for Vivado Design Suite
- Xylon evaluation logicBRICKS IP cores:
    - logiISP Image Signal Processing (ISP) Pipeline
    - logiWIN Versatile Video Input
    - logiCVC-ML Compact Multilayer Video Controller
    - logiCLK Programmable Clock Generator
- Avnet IP cores: FMC Imageon Vita Receiver

1.2.2 Software

- standalone (bare metal) driver with the logiISP driver example and Linux user space driver
- standalone (bare metal) and Linux user space libraries (OSlib)
- Linux Framebuffer driver for the logiCVC-ML IP core (display controller IP core)

1.2.3 Binaries

- Linux binaries containing precompiled SD Card image for the fastest demo startup:
    - logiISPDemoQt - logiISP demo application with the GUI designed by the Linux Qt
    - uboot, dtb(dts), root file system
    - uImage - kernel with framebuffer driver for logiCVC-ML
    - qt.image - compressed precompiled Qt application framework
- Standalone binaries (zynq_fsbl, logiISP_demo)
- FPGA bitstream

1.3 Usage Modes

The logiREF-VIDEO-ISP-EVK reference design can be used in different ways, which are listed in this paragraph and thoroughly explained through this document.

1.3.1 Quick Evaluation with no HW and/or SW Changes

- Download and install the logiREF-VIDEO-ISP-EVK reference design (chapter 2.5 GET AND INSTALL THE REFERENCE DESIGN)
- Setup the demo hardware and use the provided SD card image to run precompiled demo applications (paragraph 6.1 Set Up the MicroZed EVK kit for Use with the Precompiled Linux Demo From the SD Card)

1.3.2 Develop Standalone and Linux Software, no HW Changes

- Download and install the logiREF-VIDEO-ISP-EVK reference design (chapter 2.5 GET AND INSTALL THE REFERENCE DESIGN)
- Setup the demo hardware (paragraph 6.1 Set Up the MicroZed EVK kit for Use with the Precompiled Linux Demo From the SD Card)
- Use the provided Zynq-7000 AP SoC as it is (binaries)
- Follow instructions for working with logicBRICKS standalone (bare-metal) or Linux drivers (please get the full instructions in the *start.html* file from your installation root directory)
- Develop software applications prior to the availability of the actual target system

1.3.3 Full ISP Customization, HW and SW Changes

- Download and install the logiREF-VIDEO-ISP-EVK reference design (chapter 2.5 GET AND INSTALL THE REFERENCE DESIGN)
- Setup the demo hardware (paragraph 6.1 Set Up the MicroZed EVK kit for Use with the Precompiled Linux Demo From the SD Card)
- Obtain logicBRICKS evaluation licenses from Xylon (chapter 4 GETTING LOGICBRICKS EVALUATION LICENSES)
- Use the provided Zynq-7000 AP SoC to add or remove more logicBRICKS IP cores and/or third-party IP cores, or to change logicBRICKS IP settings through the GUI
- Implement new Zynq-7000 AP SoC design
- Develop software by following instructions listed in the *start.html* file from your installation root directory

1.4 Xilinx Development Software

The logiREF-VIDEO-ISP-EVK reference design and Xylon logicBRICKS IP cores are fully compatible with Vivado Design Suite 2014.2. Future design releases shall be synchronized with the newest Xilinx development tools.

1.5 ISP Demo Preview

Please check Xylon's Video Gallery web pages (http://www.logicbricks.com/logicBRICKS-IP-Library/Video-Galleries/logicBRICKS-Demos-Xilinx-ISP-Processing.aspx) to preview the Image Signal Processing (ISP) demo provided with the logiREF-VIDEO-ISP-EVK installation for your MicroZed EVK development kit.

2 LOGICBRICKS IP CORES

2.1 About logicBRICKS IP Library

Xylon's logicBRICKS IP core library provides IP cores optimized for Xilinx FPGAs and Zynq-7000 All Programmable SoC. logicBRICKS IP cores shorten development time and enable fast design of complex embedded systems based on Xilinx All Programmable devices. The key features of the logicBRICKS IP cores are:

- Compatibility* with the Xilinx Vivado and ISE Design Suites – logicBRICKS can be used in same ways as Xilinx IP cores and require no skills beyond general tools knowledge. IP core feature sets and programmable logic utilization can be setup through Xilinx tool GUI.
- Each logicBRICKS IP core comes with the extensive documentation, reference design examples and can be evaluated on reference hardware platforms. Xylon provides evaluation logicBRICKS IP cores to enable risk-free evaluation prior to purchase.
- Broad software support – from bare-metal software drivers to standard software drivers for different operating systems (OS).
- Xylon assures skilled technical support.

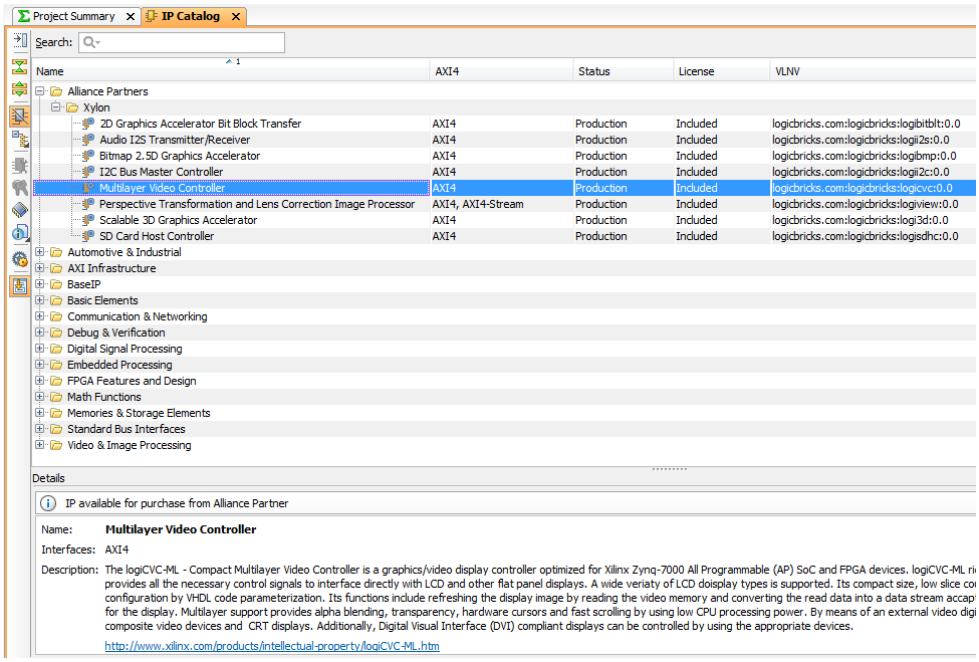


Figure 5: logicBRICKS IP Cores in the Vivado IP Catalog

** logiISP IP Core is provided in the Vivado compatible version only. Please visit our web site, or contact Xylon to learn more about the tools compatibility of the specific logicBRICKS IP core.*

The Figure 5 shows imported logicBRICKS IP cores into Vivado Design Suite, while the Figure 6 shows a typical logicBRICKS IP core's configuration GUI.

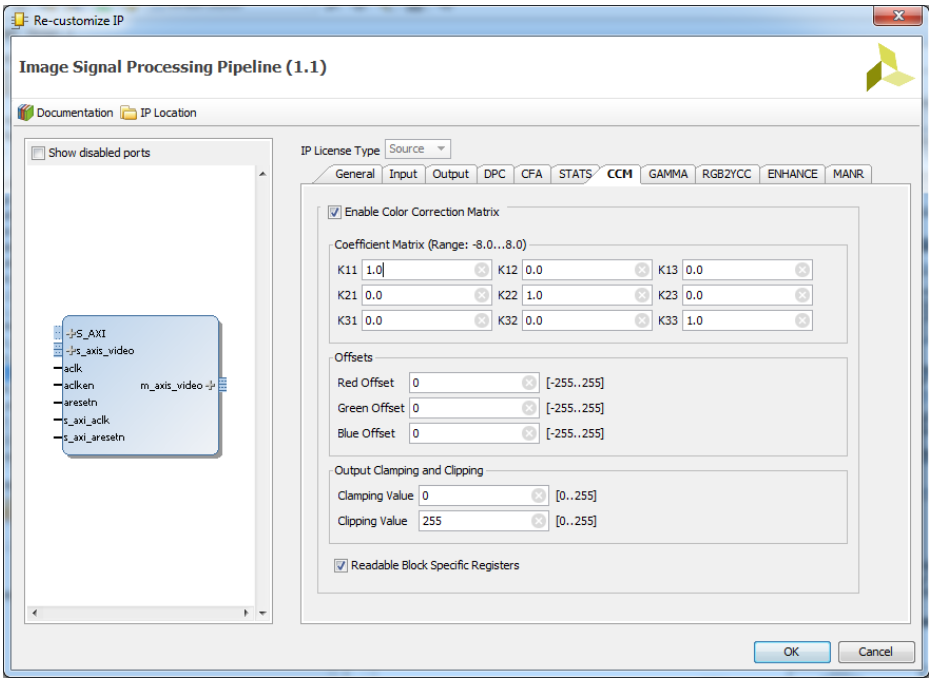


Figure 6: Example of logicBRICKS IP Configuration GUI

Click on the Documentation icon in the GUI opens the User's Manual of the logicBRICKS IP core!

2.2 Evaluation logicBRICKS IP Cores

Xylon offers free evaluation logicBRICKS IP cores which enable full hardware evaluation:

- Imported into the Xilinx ISE Platform Studio (XPS) and/or Vivado IP Integrator (IPI)
- IP parameterization through the tool GUI interface
- Bitstream generation
- If you need to simulate logicBRICKS IP cores, please contact Xylon

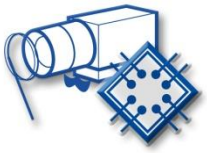
The logicBRICKS evaluation IP cores are run-time limited and cease to function after some time. Proper operation can be restored by reloading the bitstream. Besides this run-time limitation, there are no other functional differences between the evaluation and fully licensed logicBRICKS IP cores.

Evaluation logicBRICKS IP cores are distributed as parts of the Xylon reference designs: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx.

Specific IP cores can be downloaded from Xylon's web shop: http://www.logicbricks.com/Products/IP-Cores.aspx.

2.3 logicBRICKS IP Cores Used in This Design

2.3.1 logiISP Image Signal Processing (ISP) Pipeline



The logiISP Image Signal Processing Pipeline IP core is a full high-definition ISP pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx Zynq-7000 All Programmable SoC and 7 Series FPGA devices.

- Supports Xilinx Zynq-7000 AP SoC and 7 Series FPGA
- Complete and configurable ISP pipeline includes:
    - Defective Pixel Correction
    - Color Filter Array Interpolation
    - Image Statistics (+ AWB & AE Support)
    - Color Correction Matrix
    - Gamma Corrections
    - Image Enhancement
    - Motion Adaptive Noise Reduction
    - YCbCr to RGB Color-Space Converter
    - RGB to YCbCr Color-Space Converter
    - Chroma Resampler
- Digitally processes and enhances the quality of an input video stream and collects video statistics data for use in video control algorithms, i.e. Auto White Balance (AWB) and Auto Exposure (AE)
- Supports up to 1080p60 (1920x1080@60fps) and up to 7680x7680 at lower refresh rates
- Supports video input formats: Raw Bayer, RGB and YCbCr; color depth 8/10/12-bit
- Video input and output are ARM AMBA AXI4-Stream protocol compliant
- Optional registers are AMBA AXI4-Lite protocol compliant
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepackaged for Xilinx Vivado Design Suite and fully controllable through the IP Integrator GUI interface
- Evaluation IP core available online and the bit-accurate C model for evaluations available on request
- IP deliverables include the software driver, documentation and technical support
- Available fee-based license extension for the AWB&AE libraries, which are verified with the logiISP IP core

More info: http://www.logicbricks.com/Products/logiISP.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiISP_hds.pdf

2.3.2 logiCVC-ML Compact Multilayer Video Controller

The logiCVC-ML IP core is an advanced display graphics controller for LCD and CRT displays, which enables an easy video and graphics integration into embedded systems with Xilinx Zynq-7000 All Programmable SoC and FPGAs.

This IP core is the cornerstone of all 2D and 3D GPUs. Though its main function is to provide flexible display control, it also includes hardware acceleration functions: three types of alpha blending, panning, buffering of multiple frames, etc.

- Supports all Xilinx FPGA families
- Supports LCD and CRT displays (easily tailored for special display types)
- 64x1 to 2048x2048 display resolutions
- Available SW drivers for: Linux, Android, QNX and Microsoft Windows Embedded Compact OS
- Support for higher display resolutions available on request
- Supports up to 5 layers; the last one configurable as a background layer
- Configurable layers' size, position and offset
- Alpha blending and Color keyed transparency
- Pixel, layer, or Color Lookup Table (CLUT) alpha blending mode can be independently set for each layer
- Packed pixel layer memory organization:
  - RGB – 8-bpp, 8-bpp using CLUT, 16bpp Hi-color RGB 565 and True-color 24bpp
  - YCbCr – 16bpp (4:2:2) and 24bpp (4:4:4)
- Configurable CoreConnect™ PLBv4.6, Xylon XMB or ARM® AMBA® AXI4 memory interface data width (32, 64 or 128)
- Programmable layer memory base address and stride
- Simple programming due to small number of control registers
- Support for multiple output formats:
  - Parallel display data bus (RGB): 12x2-bit, 15-bit, 16-bit, 18-bit or 24-bit
  - YCbCr 4:4:4 or 4:2:2 output format
  - Digital Video ITU-656: PAL and NTSC
  - LVDS output format: 3 or 4 data pairs plus clock
  - Camera link output format: 4 data pairs plus clock
  - DVI output format
- Supports synchronization to external parallel input
- Versatile and programmable sync signals timing
- Double/triple buffering enables flicker-free reproduction
- Display power-on sequencing control signals
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Available for Xilinx Vivado IP Integrator and ISE XPS implementation tools

More info: http://www.logicbricks.com/Products/logiCVC-ML.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiCVC-ML_hds.pdf

2.3.3 logiWIN Versatile Video Input

The logiWIN IP core enables easy implementation of video frame grabbers. Input video can be decoded, real-time scaled, de-interlaced, cropped, anti-aliased, positioned on the screen…

- Supports Xilinx Zynq-7000 AP SoC and FPGAs
- Maximum input and output resolutions 2048x2048
  - Supports different input interface standards: ITU656 and ITU1120 (PAL and NTSC), RGB, YUV 4:2:2
- Built-in YCrCb to RGB, YUV to RGB and RGB to YCrCb converters
- Real-time scale-up to 64x and scale-down to 16x; lossless scaling down to 2x or 4x in the cascade scaling mode
- Supports video de-interlacing, cropping, positioning, pixel alpha blending...
- Embedded image color enhancements: brightness, contrast, hue, saturation
- ARM AMBA AXI4 and AXI4-Lite bus compliant
- Available for Xilinx Vivado IP Integrator and ISE XPS implementation tools

More info: http://www.logicbricks.com/Products/logiWIN.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiWIN_hds.pdf

2.3.4 logiCLK Programmable Clock Generator

The logiCLK is a programmable clock generator IP core featuring twelve independent and fully configurable clock outputs. While six clock outputs can be fixed by generic parameters prior to the implementation, the other six clock outputs can be either fixed by generics or dynamically reconfigured in a working device.

- Supports Xilinx Zynq-7000 All Programmable SoC, 7 series and Spartan®-6 FPGAs
- Provides 12 independent clock outputs that can be configured by generic parameters:
  - 6 outputs can be dynamically configured through the DRP interface
  - 6 outputs can be configured by generics only
- Input clock frequency range*:
  - Spartan-6: 19 – 540 MHz
  - 7 series: 19 – 1066 MHz
- Output clocks frequency range*:
  - Spartan-6: 3.125 – 400 MHz
  - 7 series: 6.25 – 741 MHz
- Configurable ARM AMBA AXI4-Lite and CoreConnect PLBv46 compliant registers interface
- Software support for Linux and Microsoft Windows Embedded Compact operating systems
- Available for Xilinx Vivado IP Integrator and ISE Platform Studio

** Depending on the used device's speed grade*

More info: http://www.logicbricks.com/Products/logiCLK.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiCLK_hds.pdf

2.4 logicBRICKS IP Cores for Graphical User Interface (GUI) Implementations

Xylon's logicBRICKS library of IP cores optimized for Xilinx All Programmable devices includes several graphics logicBRICKS IP cores for full range implementation of 2D and 3D Graphics Processing Units (GPU) on Xilinx Zynq-7000 All Programmable SoC and FPGAs.

Xylon's graphics logicBRICKS IP cores can be quickly combined with the video processing IP cores when it is necessary to support complex GUI interfaces. Graphics logicBRICKS IP cores are well supported by Xylon provided software drivers for the most popular operating systems: Linux, Android™, QNX® and Microsoft® Windows® Embedded Compact. A number of Xilinx partners who provide BSPs (Board Support Package) for different operating systems support Xylon logicBRICKS IP cores for graphics.

Figure 7: Screenshots from Some Demos Provided with the Reference Designs (logiREF-ZGPU-ZED, logiREF-ZGPU-ZC702 and logiREF-ZGPU-ZC706)

To get Xylon free GUI reference designs, please visit:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

To learn more about the available software support for graphics logicBRICKS IP cores, please visit:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/OS-IP-Core-Support.aspx

logiBITBLT Bit Block Transfer 2D Graphics Accelerator

This 2D graphics accelerator speeds up the most common GUI operations and off-loads the processor. The logiBITBLT transfers graphics objects from one to another part of system's on-screen or off-screen video memory, and performs different operations during transfers, such as ROP2 raster operations, bitmap scaling (stretching) and flipping, Porter & Duff compositing rules or transparency.

More info: http://www.logicbricks.com/Products/logiBITBLT.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiBITBLT_hds.pdf

logi3D Scalable 3D Graphic Accelerator

The logi3D* Scalable 3D Graphics Accelerator IP core is a 3D Graphics Processing Unit (GPU) IP core developed for embedded systems based on the Xilinx Zynq-7000 All Programmable SoC. The IP is designed to support the OpenGL ES 1.1 API specifications – a royalty-free, cross-platform API for full-function 2D and 3D graphics on embedded systems – including consoles, phones, appliances and vehicles.

** Product is based on a published Khronos specification, and is expected to pass the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.*

2.5 Complementary logicBRICKS Reference Design – Face Tracking

The face detection and tracking is a computer technology that uses video images captured by the video camera to determine and track distinctive facial features. The technology significantly improves human-machine interaction and opens a very wide range of applications, such as adriver drowsiness detection in automotive safety systems that prevent accidents, speaker detection in video conferencing systems capable to automatically zoom to the current speaker, hands-free interfacing helping disabled people to improve their daily lives, character animations in virtual reality entertainment and gaming, health, robotics, audio processing and others.

To learn more about this technology and to evaluate Xylon's solution designed for Xilinx All Programmable, please check Xylon's free downloadable logiREF-FACE-TRACK-EVK Face Detection and Tracking reference design for the MicroZed™ Embedded Vision Development Kit from Avnet Electronics Marketing and the ON Semiconductor's PYTHON-1300 1.3 MP video camera:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Face-Detection-for-Zynq-AP-SoC.aspx

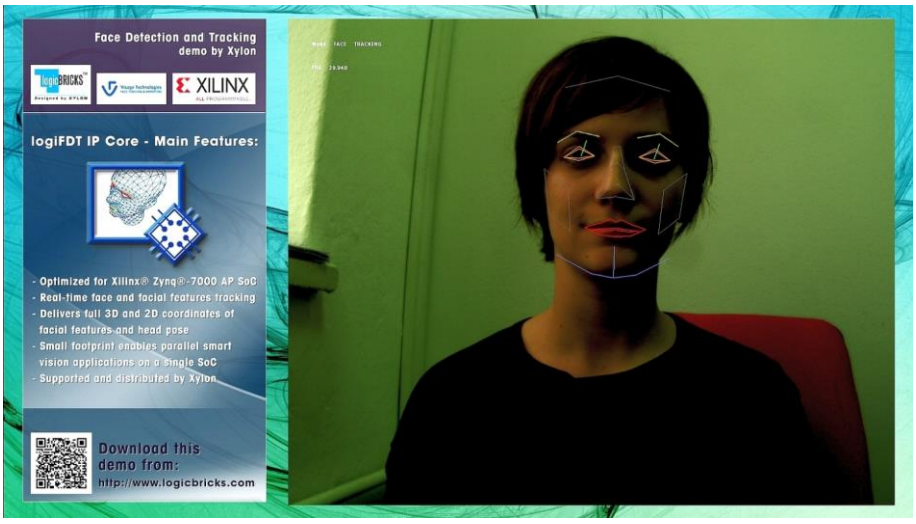


Figure 8: Screenshot from the Xylon Face Tracking Demo

3 GET AND INSTALL THE REFERENCE DESIGN

Xylon offers several logicBRICKS reference designs for different hardware platforms. Short descriptions of all Xylon logicBRICKS reference designs can be found at:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

A quick access to specific reference design is also possible through the main downloads navigation page: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx

Only registered logicBRICKS users can download logicBRICKS reference designs. Unregistered users will be re-directed to the User Login page. The download link is automatically sent by an e-mail, which means that the registration process requires access to the e-mail account. Xylon reference logicBRICKS designs can be downloaded as cross-platform Java JAR self-extracting installers.

For quick registration and other general instructions, please visit:

http://www.logicbricks.com/logicBRICKS/logicBRICKS-Quick-Info.aspx

3.1 Registration Process

Registration is very quick and simple. If you experience any troubles during the registration process, please contact Xylon Technical Support Service – support@logicbricks.com.

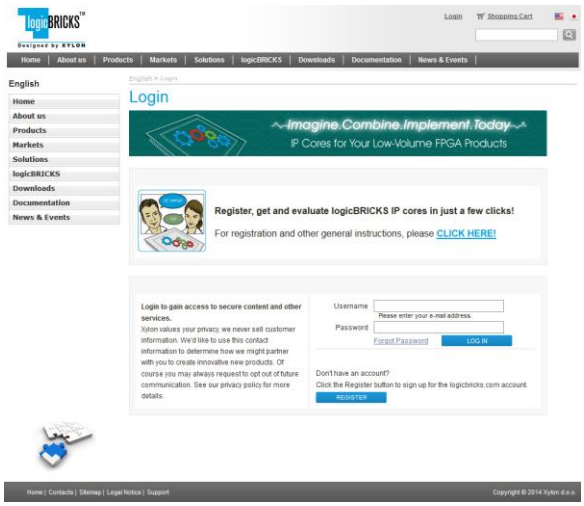


Figure 9: Registration Process – Step 1

Step 1

If you are the registered logicBRICKS user, please type-in your Username and Password. Unregistered users should click on the Register button, which will open the registration form.

Figure 10: Registration Process – Step 2

Step 2

Unregistered users should fill-in the registration form from the Fig 10. Please take care on required form's fields. Your Username is an actual e-mail account used for communication with Xylon logicBRICKS. Xylon accepts only valid company e-mail accounts.

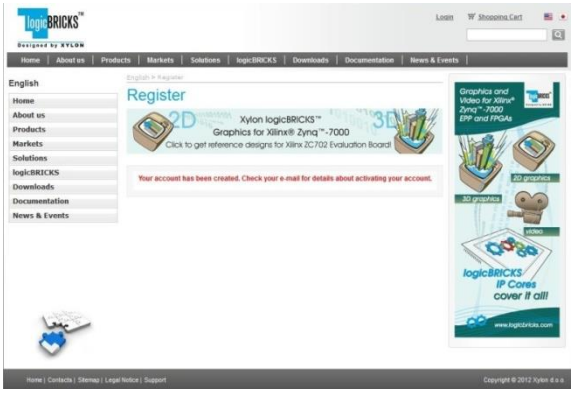


Figure 11: Registration Process – Step 3

Step 3

As soon as your registration form gets accepted by Xylon, you get a confirmation message. Please check your e-mail to find a link that activates your logicBRICKS account. If you do not get the confirmation message in several minutes, please check your Spam Filter or Junk Mail Folder. If you have not received the confirmation message, please contact Xylon support.

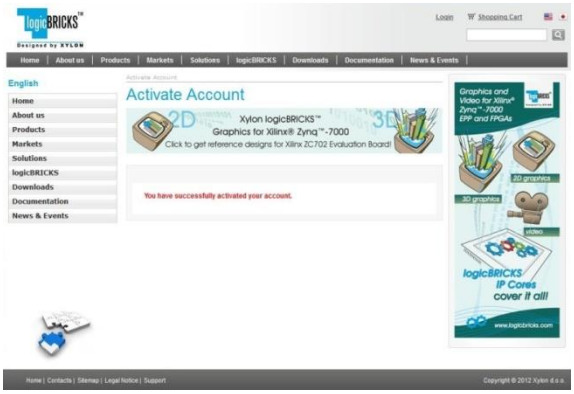


Figure 12: Registration Process – Step 4

Step 4

Click on the logicBRICKS web account activation link in the received e-mail, and you will get the confirmation status message. Please login to proceed.

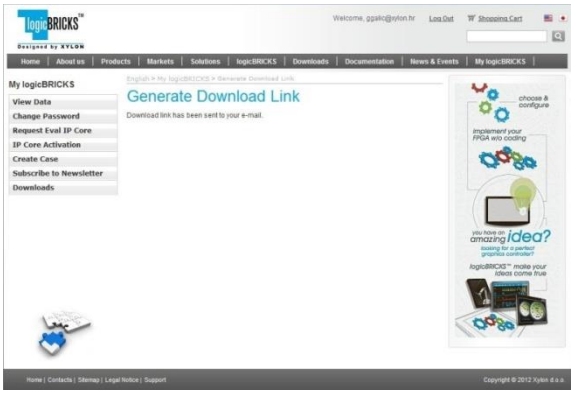


Figure 13: Registration Process – Step 5

Step 5

As soon as you select an appropriate logicBRICKS reference design and installer for your operating system from the Downloads Navigation Page (link bellow), you will get an e-mail with the download link for the selected reference design installation.

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx

3.2 Installation Process

Installation process is quick and easy. Each logicBRICKS reference design can be downloaded as a cross-platform Java JAR self-extracting installer. Please make sure that you have a copy of the JRE (Java Runtime Environment) version 6 or higher on your system to run Java applications and applets.

Double-click on the installer's icon to run the self-installing executable to unpack and install the reference design on your PC.

At the beginning, you will be requested to accept two evaluation licenses – Figure 14 and Figure 15.

For installation in Linux OS, please follow instructions:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Linux-Installation.aspx.

If you agree with the conditions from the evaluation licenses, click NEXT and select the installation path for your logicBRICKS reference design – Figure 16.

The installation process takes several minutes. It generates the directory structure described in the paragraph 3.3 Directory Structure.

3.2.1 Filesystem permissions of the installed directory (Windows 7)

The reference design installed in the default path `C:\Program Files\xylon` will inherit read-only filesystem permissions from the parent directory. This will block you in opening the hardware project file in Xilinx Vivado tools. Therefore it is necessary to change the filesystem permissions for the current user to "Full control" preferably.

To change the user permissions for `C:\Program Files\xylon` directory and all of it's subdirectories, right click on the `C:\Program Files\xylon` directory and select "Properties". Under "Security" tab select "Edit". Select "Users" group in the list and check "Full control" checkbox in the "Allow" column.

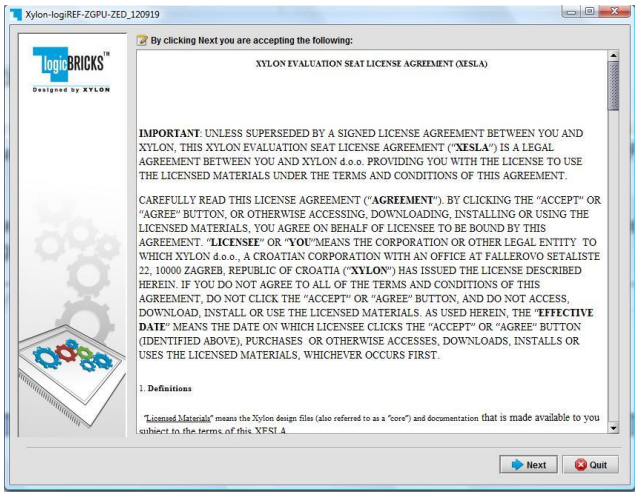


Figure 14: Installation Process – Step 1

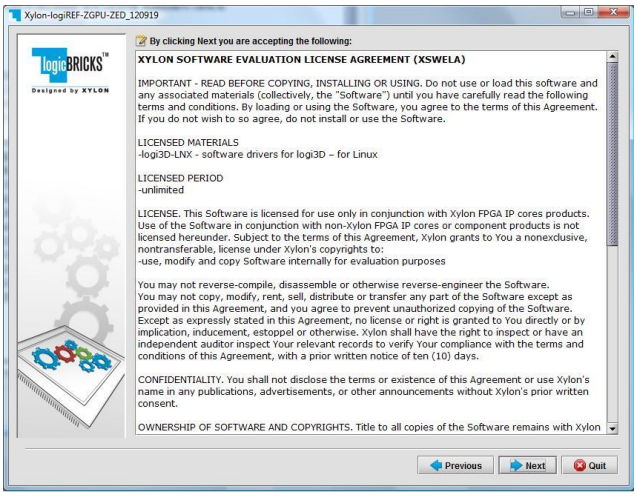


Figure 15: Installation Process – Step 2

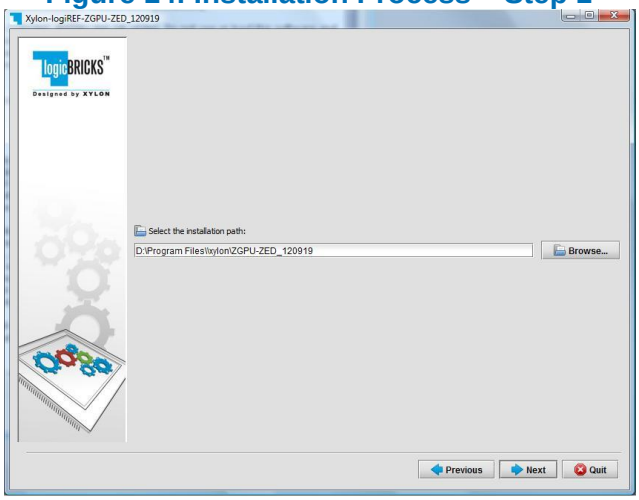


Figure 16: Installation Process – Step 3

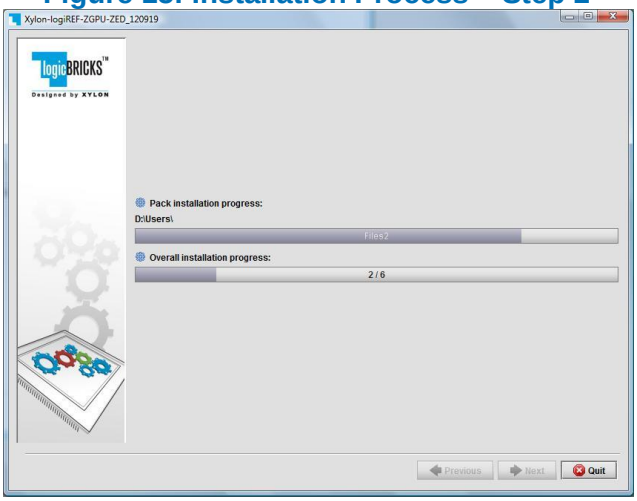


Figure 17: Installation Process – Step 4

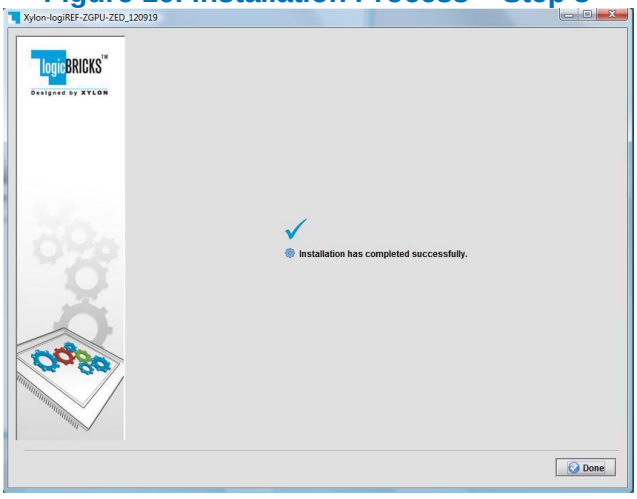


Figure 18: Installation Process – Step 5

3.3 Directory Structure

Figure 19 gives a top level view of the directories and files included with the logiREF-VIDEO-ISP-EVK reference design for the MicroZed Embedded Vision development kit. Table 1 explains the purpose of directories.

Please use the `start.html` file located in the installation root directory as a jump-start navigation page for exploring the reference design.

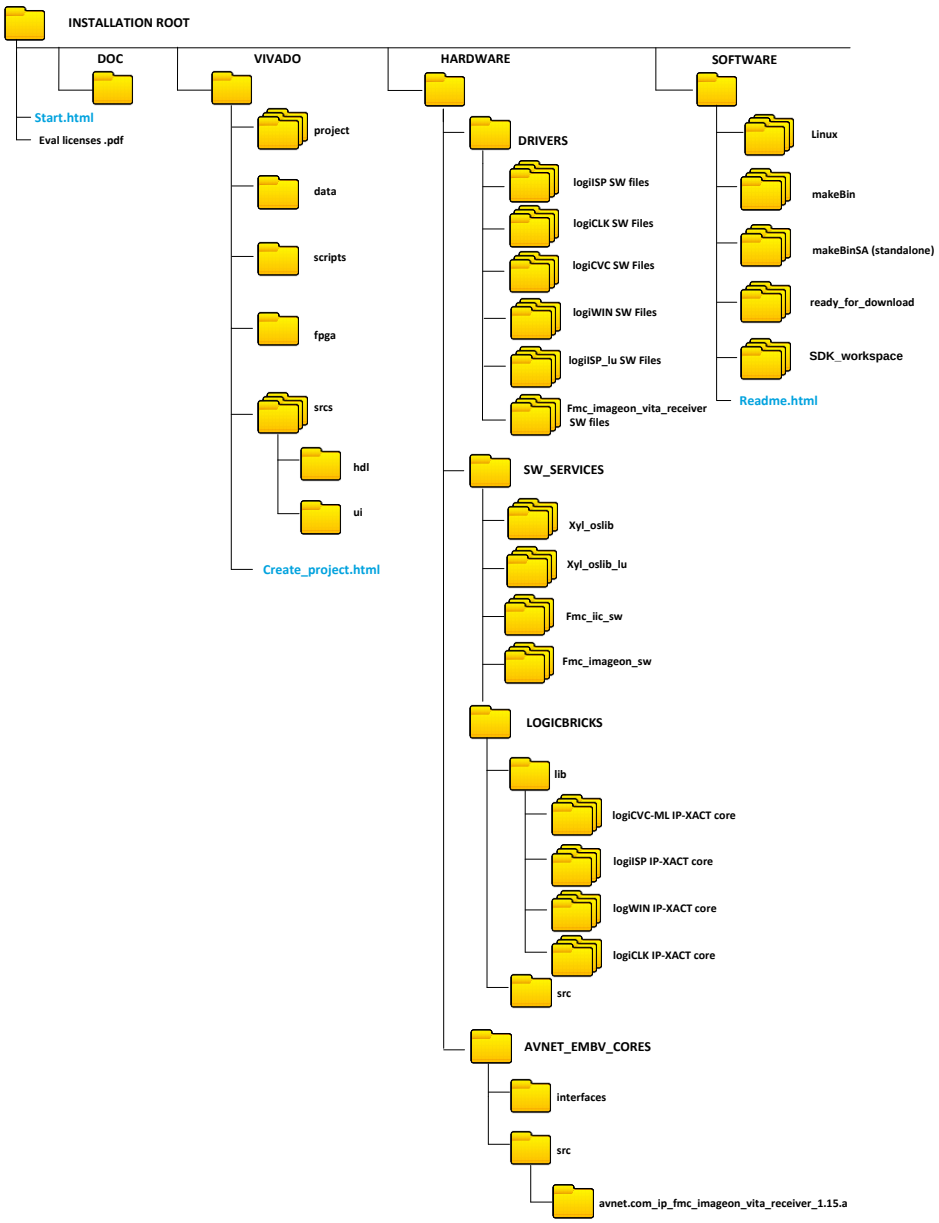


Figure 19: Installed Reference Design – The Directory Structure

Directory		Purpose
Installation Root		This directory contains the *start.html* page – the jump-start navigation page through the reference design.
Doc		Project documentation (Users Manual).
Vivado		This directory contains the complete Vivado project and files necessary for regenerating project from TCL scripts.
	Data	Design constraints files.
	hp433ab	Vivado project directories – recreated with TCL scripts.
	Srcs	Block design GUI script and HDL wrappers.
	Scripts	TCL scripts to create block design from scratch.
	fpga	MicroZed reference design bitstream.
	create_project.html	Instructions for building Vivado project from scratch.
Hardware		
	Drivers	Standalone (bare-metal and linux userspace) drivers for logicBRICKS IP cores with documentation and examples and Avnet's standalone driver for Vita Receiver.
	logicbricks/lib	Evaluation logicBRICKS IP-XACT cores (zip archives).
	logicbricks/src	Evaluation logicBRICKS IP-XACT extracted IP cores. IP cores' User's Manuals are stored in doc subdirectories.
	Logicbricks/if	logicBRICKS IPs' interface definitions for Vivado.
	avnet_embv_cores	Avnet provided IP cores.
	sw_services	xyl_oslib Xylon OS abstraction library for Linux applications and Avnet IIC libraries.
Software		
	readme.html	Navigation page through the software files and instructions for building binaries.
	Linux/kernel	Linux kernel and device tree configuration files.
	Linux/libraries	Scripts and patches for building Qt
	makeBin	Utility script for creating boot.bin file (for Linux)
	makeBinSA	Utility script for creating boot.bin file (for StandAlone)
	ready_for_download	Prepared SD binaries ready for download.
	SDK_workspace	Xilinx SDK workspace folder for building of bare-metal logiISP application and linux userspace logiISP driver.

Table 1: Explanation of Directories in logiREF-VIDEO-ISP-EVK Reference Design

4 GETTING LOGICBRICKS EVALUATION LICENSES

Please note that the logiREF-VIDEO-ISP-EVK reference design installation provides you with everything needed to run the provided demo applications or to use/change the provided software source code. However, if you wish to make any changes on the hardware design files, such as to remove, add or reconfigure some of the provided IP cores, you have to obtain evaluation IP licenses from Xylon.

The following pages describe the procedure for getting and licensing evaluation logicBRICKS IP cores that takes several minutes to complete. If you experience any troubles during this process, please contact Xylon Technical Support Service – support@logicbricks.com.

You must be logged in to the Xylon website using your logicBRICKS user name and password to get an access to evaluation logicBRICKS IP cores. Unregistered users will be re-directed to the User Login page. Paragraph 3.1 Registration Process explains this simple registration procedure.

Step 1 – Logged in users get the "My logicBRICKS" tab in the main www.logicbricks.com navigation menu. Click on it, and you will be directed to your main web page for communication with Xylon logicBRICKS – Figure 20. Please select the "**Request Eval IP Core**" tab in the left menu.

Figure 20: Step 1 – My logicBRICKS Navigation Page

Step 2 – Select the evaluation logicBRICKS IP core and click on "**Obtain evaluation license key**" link – Figure 21. If you are entitled to get the evaluation logicBRICKS IP core, you will be immediately asked (Figure 24) your Ethernet MAC ID number or Sun Host ID – as described in the Step 3.

If the evaluation logicBRICKS IP cores' list looks differently from the one shown on Figure 21, for example as the list presented by the Figure 22, please fill in and submit the request form (Figure 23), and allow us some time to process your request. Scroll down to get to the request form.

For instructions how to find your Ethernet MAC or host ID, please visit:
http://www.logicbricks.com/Documentation/Article.aspx?articleID=KBA-01186-M0JXKD

Figure 21: Step 2 – Selecting logicBRICKS IP Core for Licensing

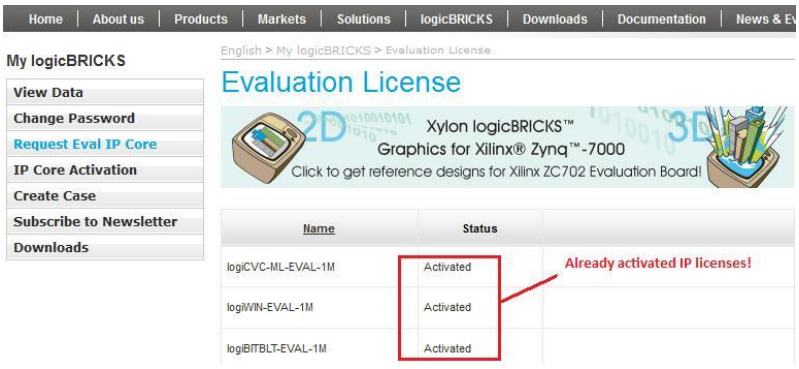


Figure 22: Step 2 – A List of Already Activated logicBRICKS IP Licenses

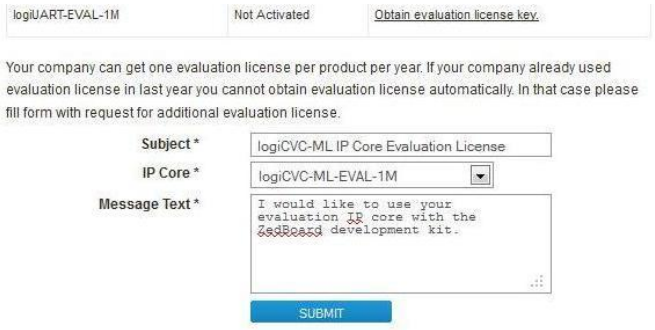


Figure 23: Step 1 – Licensing logicBRICKS Evaluation IP Cores

Step 3 – Evaluation logicBRICKS IP licenses are tied to your Ethernet MAC address or Sun Host ID (Figure 24), and can be used on a single working station only. Fill in this address and click on the "**Request License Key**" button. You should get the confirmation message – Figure 25. If you do not get the confirmation message, please contact Xylon technical support – support@logicbricks.com.

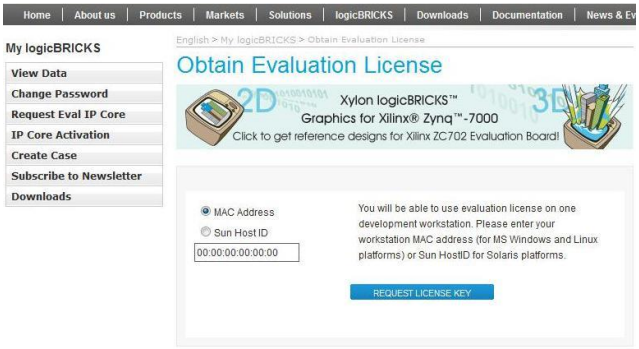


Figure 24: Step 3 – Licensing logicBRICKS Evaluation IP Cores

Figure 25: Step 3 – Confirmation Message

Step 4 – You will get an e-mail with the license key (file) and full instructions for setting up the license key and downloading the logicBRICKS IP core. Please follow the provided instructions.

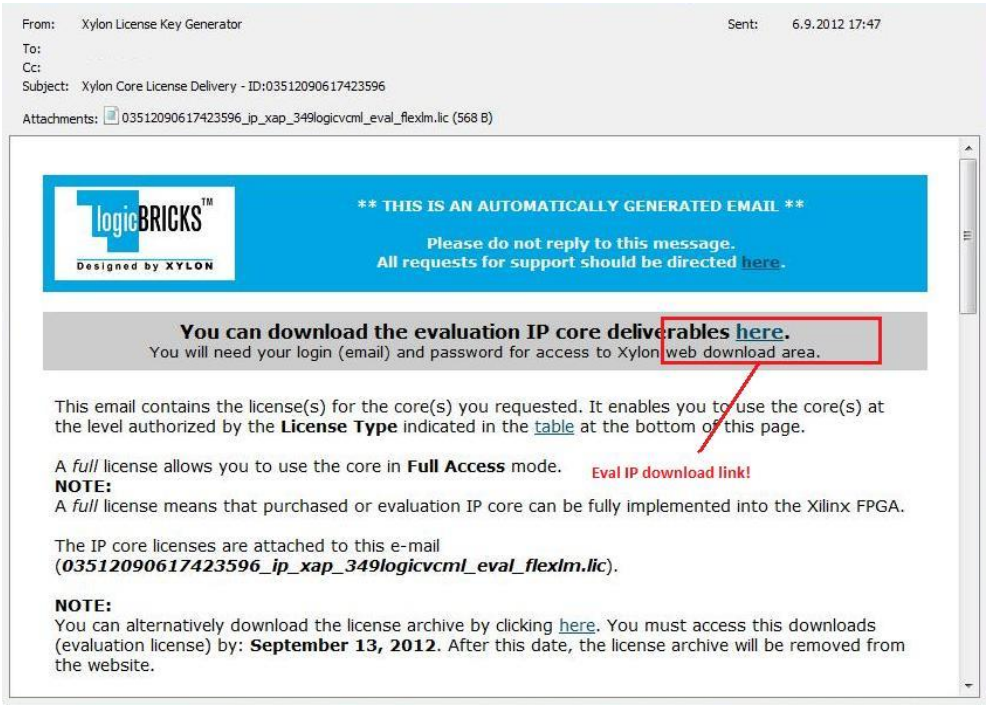


Figure 26: Step 4 – E-mail with logicBRICKS License and Download Instructions

5 LOGIREF-VIDEO-ISP-EVK DESIGN

Figure 27 shows the simplified block diagram of the logiREF-VIDEO-ISP-EVK reference design. Design clocking structures are not shown in detail. Please read the chapter 5.2.1 PL Clocking and explore the design files to understand the clocking structure.

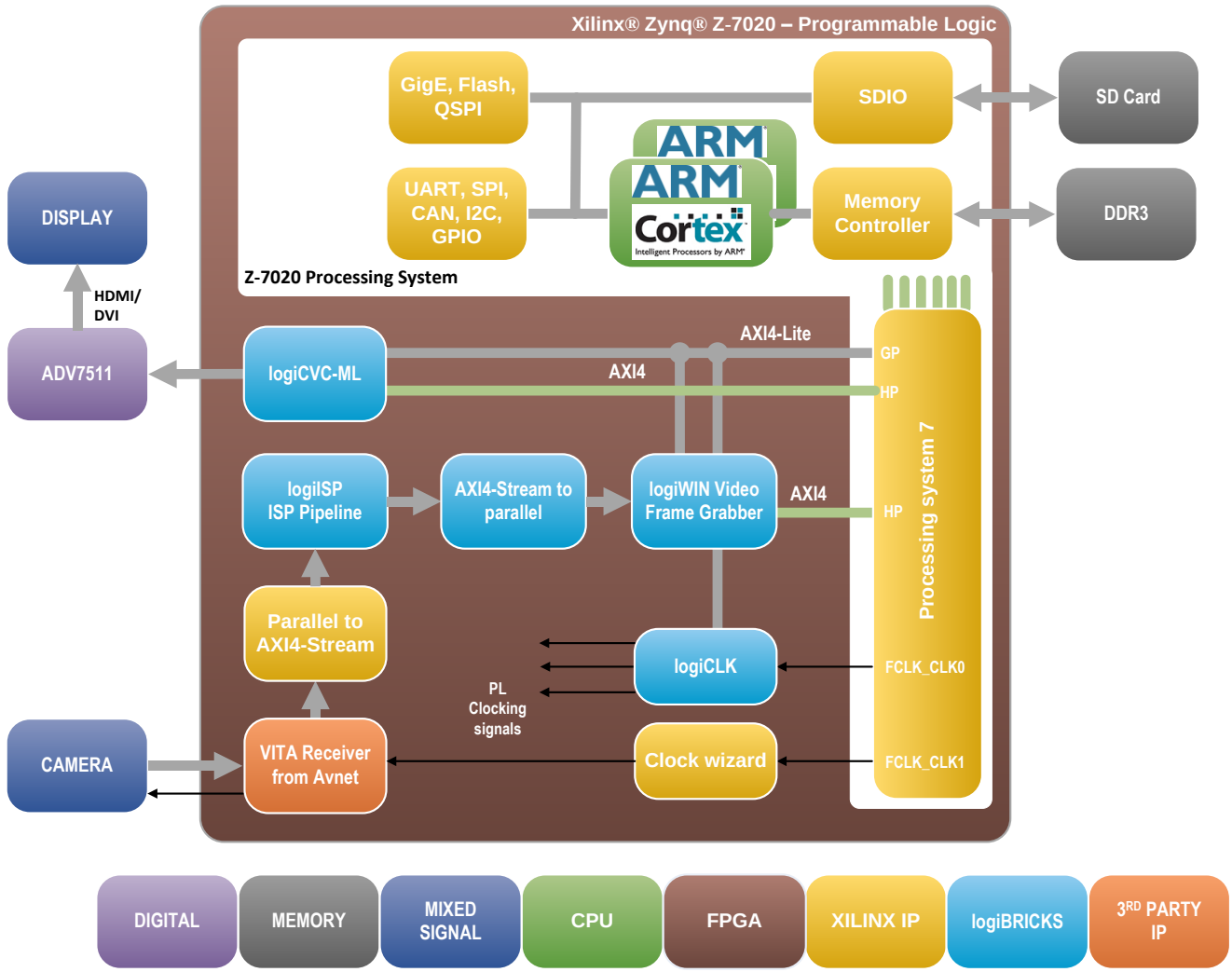


Figure 27: logiREF-VIDEO-ISP-EVK Reference SoC Block Diagram

The VITA Receiver IP core from Avnet Electronics Marketing receives the video data from the ON Semiconductor PYTHON-1300 camera module (LVDS data) and provides parallel RGB video data and video sync signals at its outputs.

The logiISP Image Signal Processing Pipeline IP core accepts the VITA Receiver sourced parallel RGB video converted into the streaming AXI4-Stream video input by an auxiliary Xilinx's Parallel to

AXI4-Stream converter IP core. The logiISP pipeline outputs the quality enhanced AXI4-Stream formatted streaming video, which is converted to the parallel RGB format prior to entering the logiWIN Versatile Video Input frame grabbing IP core. Demo users can evaluate different logiISP IP core's hardware configurations and re-programm the setup IP configuration through the provided Xylon GUI demo application.

In this referent design the logiISP IP core is configured to include the following image processing modules shown on the below Figure 28.

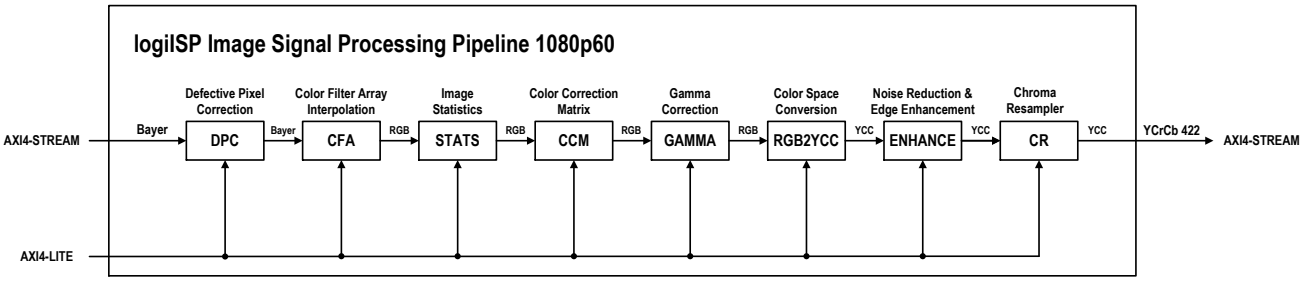


Figure 28 logiISP configuration for reference design

The camera supplies the image in the raw (Bayer) format, which is at first converted into the parallel RGB format, and further into the AXI4-Stream format as required by the logiISP IP core. The logiISP IP core outputs the processed YCbCr 422 formated video through the AXI4-Stream interface. The video output is converted into a standard parallel interface with sync signals and supplied to the logiWIN frame grabber IP. The resolution of the camera image is 1280 x 1024 pixels.

The logiWIN frame grabber stores the video in video frame buffers implemented in an external DDR3 memory. The logiWIN is AXI4 bus protocol compliant and can be easily connected to Zynq-7000 AP SoC memory controller. The logiWIN works synchronously with the logiCVC-ML Compact Multilayer Video Controller to enable implementation of the triple buffering video storage method that assures a flicker-free video output.

The memory subsystem is an essential part of any video and graphics based system. It must ensure enough storage space for video buffers, GUI elements and application code, as well as a fast interface to assure enough memory bandwidth for a smooth and uninterrupted SoC operation. The MicroZed board includes two 16-bit DDR3 memory devices, totalling 1GB of random access memory. The memory is connected to the hard memory controller in the Zynq-7000 AP SoC Processor Subsystem (PS).

The logiCVC-ML Compact Multilayer Video Controller IP core drives a common PC monitor through the ADV7511 – High-Definition Multimedia Interface (HDMI®) transmitter available on the MicroZed Embedded Vision Carrier Card Kit. The logiCVC-ML automatically handles the full HD graphics background layer and the live video overlay. The demo GUI has been implemented by the Qt cross-platform application framework.

5.1 Design Customization

The provided reference design can be customized in different ways. Please note that any changes in the provided reference design require evaluation IP licenses for logicBRICKS IP cores. The licensing process is described in the chapter 4 GETTING LOGICBRICKS EVALUATION LICENSES.

Possible design changes include:

- Change logicBRICKS IP settings, i.e. logiISP pipeline configuration in order to fit the application requirements and reduce programmable logic utilization, number of graphics layers controlled by the logiCVC-ML display controller IP core, etc.
- Add or remove logicBRICKS IP cores, i.e. add graphics accelerators to speed up the GUI interface and offload the processing system, etc.
- Add your own or third-party IP cores to various combinations of logicBRICKS IP cores
- ...

5.2 Memory Layout

Reference design's memory layout is shown on the bellow Figure 29.

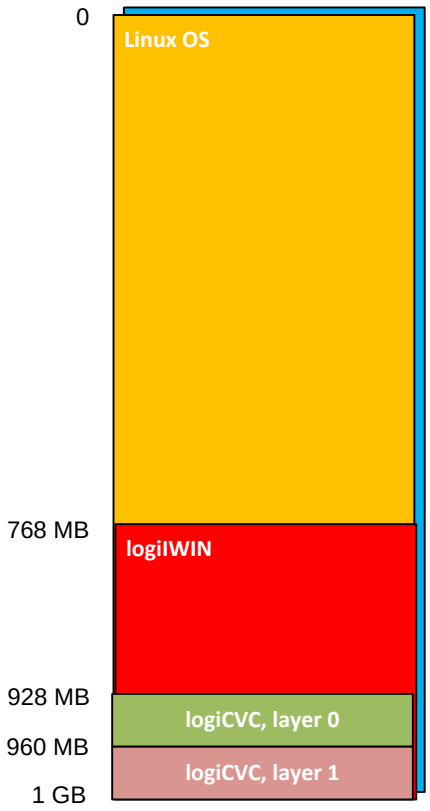


Figure 29: logiREF-VIDEO-ISP-EVK Memory Layout

IP Core	Memory Access [MB]	Memory Stride [pixels]	Display Memory [HxV pixels]
logiCVC	768 – 1024	2048	1920x1080
logiWIN	768 – 1024	2048	-
			-

Table 2: logicBRICKS IP Cores' Memory Addressing

Top video layer (layer 0) is used for camera image refresh, while bottom video layer (layer 1) is used for GUI.

logiCVC video layer	Type	Layer data width	Layer memory address	Double buffer address offset
0	YCbCr 422	16	0x3a000000	2048 lines
1	RGB	24	0x3c000000	2048 lines

Table 3 logiCVC-ML video layer settings

5.2.1 PL clocking

Figure 30 explains generation of the required PL clocks.

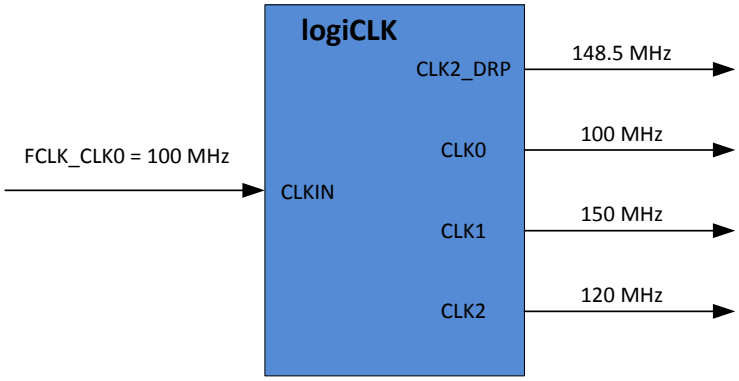


Figure 30 PL clocks generation using logiCLK

The logiCLK IP core is sourced by 100 MHz clock generated in the Zynq-7000 AP SoC Processing System and supplied to the FCLK_CLK0 PS output.

The CLK2_DRP output clock frequency can be dynamically adjusted during device's operation. It is used to generate source clock for logiCVC-ML video controller and for the video output. It's frequency is by default set to 148.5 MHz due to full-HD display resolution 1920x1080 and refresh rate 60 Hz (1080p).

CLK0, CLK1 and CLK2 outputs' frequencies can be changed only prior to the design implementation and are fixed during device's operation.

The CLK0 output clock is used as a source clock for AXI4-Lite interfaces in the programmable logic such as register interfaces and interconnects. Its frequency is set to 100 MHz.

The CLK1 output clock is used as a source clock for logiCVC-ML's AXI4 memory interface and interconnect. Its frequency is set to 150 MHz.

The CLK2 output clock is used as a source clock for logiISP video path, which comprises Parallel to AXI4-Stream converter, logiISP, AXI4-Stream to parallel converter and logiWIN. Its frequency is set to 120 MHz.

Besides above mentioned clocks few more are needed by the Vita receiver IP core provided by Avnet – 27 MHz and 108 MHz. To generate those clocks, the Clock wizard is used as shown by Figure 31. Ratio between those clocks is 1:4. The Clock wizard is sourced by 200 MHz clock generated in the Processing System (PS) and supplied to the FCLK_CLK1 PS output.

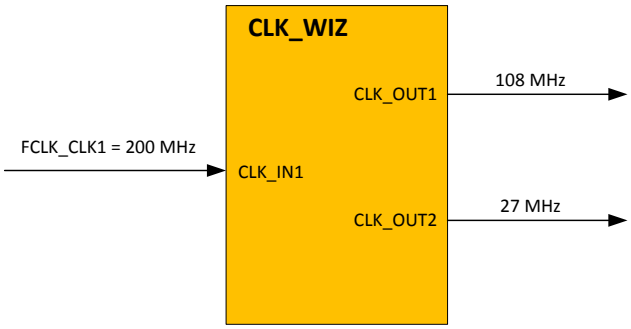


Figure 31 PL clocks generation using Clock Wizard

5.3 Restoring Full SoC Design from Xylon Deliverables

Xylon provides all necessary design files and TCL scripts to enable full Vivado Design Suite 2014.2 project restore. Full guidelines can be found in the `vivado/create_project.html` file.

The `hp433ab.xpr` file from your installation directory is the Vivado Design Suite project file that opens the project. Open this file with the Vivado and explore the design – Figure 32.

In order to re-implement or change the provided reference design, please go to Xylon's web site www.logicbricks.com and acquire evaluation licenses for the logicBRICKS IP cores (see chapter 4 GETTING LOGICBRICKS EVALUATION LICENSES).

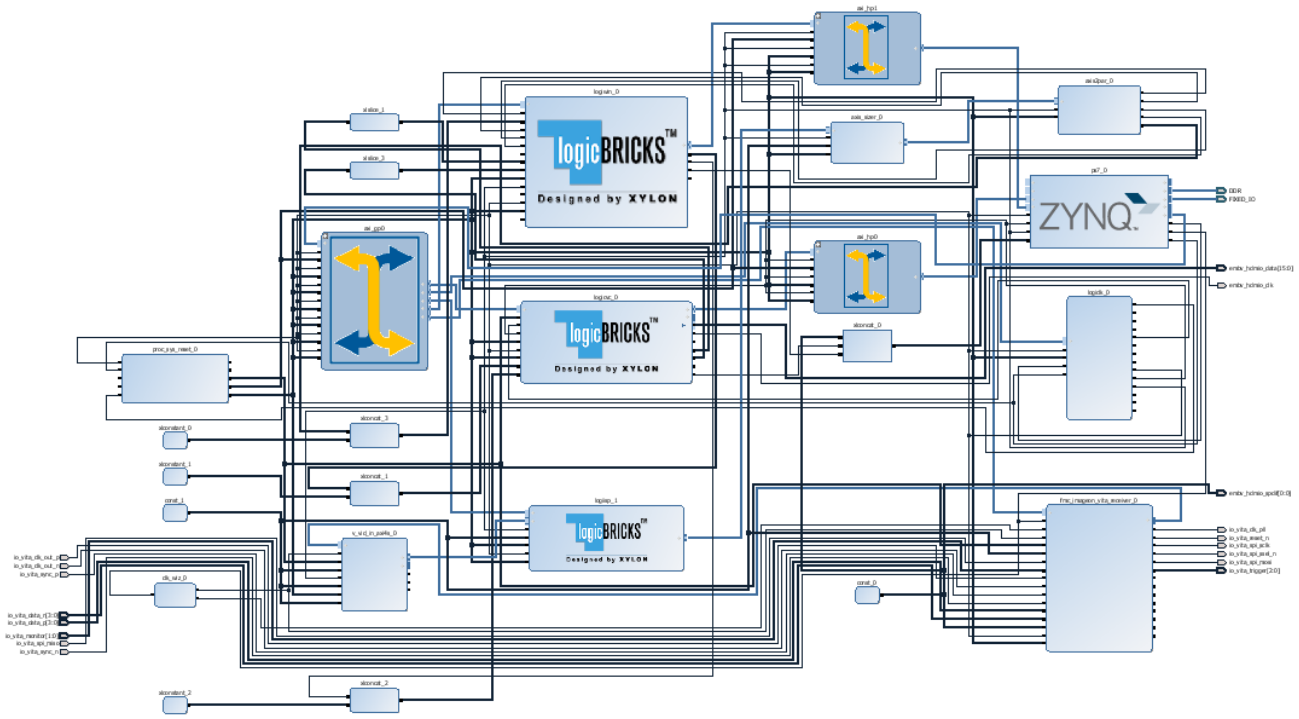


Figure 32: Vivado Block Design Diagram – logiREF-VIDEO-ISP-EVK Project

To access logicBRICKS IP cores' user's manuals, double-click on the specific IP core's to open the GUI, and click on the Documentation icon to open the document.
logicBRICKS User's Manuals contain all necessary information about the IP cores' features, architecture, registers, modes of operation, etc.

6 QUICK START

6.1 Set Up the MicroZed EVK kit for Use with the Precompiled Linux Demo From the SD Card

Xylon provides the demo binaries in the `software/ready-for-download/linux_sd` directory of the delivery. In order to quickly run the precompiled Xylon demo, please copy the contents of the `linux_sd` directory to the **root** directory on the FAT32 formatted SD card and use it with the hardware kit.

Note: there should be no `linux_sd` directory on the SD card, but only the contents of that directory.

Set up your MicroZed Embedded Vision Kit as follows:

- Plug the programmed SD card into the micro SD card connector J6 on the MicroZed board.
- Select the MicroZed configuration mode by setting up JP1-JP3 jumpers as shown on Figure 33. The presented setup selects the SD card as the boot device.
- Plug the MicroZed board into the Carrier Card board, as shown on Figure 34.
- Attach the On Semiconductor PYTHON-1300 camera module to the MicroZed Carrier Card, as shown on Figure 35.
- Connect the Full HD (1920x1080) PC monitor and the Carrier Card (HDMI OUT: CON3) by the micro-HDMI-to-HDMI video cable.
- Connect the USB mouse to the MicroZed USB connector J1.
- Connect the 5VDC power supply to the Carrier Card to connector CON8.

Figure 33: The MicroZed Board Jumpers Settings

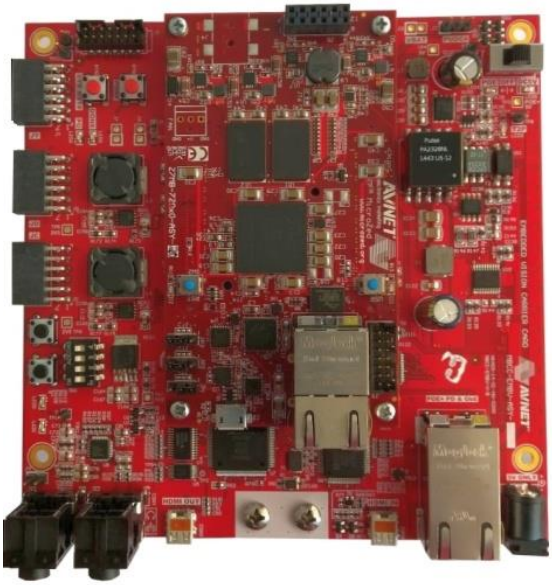


Figure 34: The MicroZed Board Plugged In the Carrier Card

Figure 35: The PYTHON-1300 Camera Module Plugged In the Carrier Card

6.2 Running the Precompiled Demo from the SD Card Image

To quickly start the precompiled ISP demo, make sure that you have the SD card with the precompiled image plugged in the board's slot, and all jumpers setup as described in the previous paragraph.

Connect USB mouse to the J1 connector on the MicroZed board. It is used for interaction with logiISP demo application.

Power up the board. After some time (cca 30s) logiISP demo Qt application will automatically start. Instructions how to use demo can be found in chapter 8.

7 SOFTWARE DOCUMENTATION

Please use the `start.html` file, which is located in your logiREF-VIDEO-ISP-EVK installation directory or open directly `software/readme.html` file to find relevant documentation for using logiREF-VIDEO-ISP-EVK software deliverables. This file contains links to software documents and instructions related to :

- Standalone (Bare Metal) software
- Linux software

7.1 Software Instructions – Standalone Software

Described chapters are:

- FSBL application
- Standalone (Bare-Metal) SW drivers and logiISP example (code and documentation)
- Building logiISP standalone application
- Runing standalone applications

7.2 Software Instructions – Linux Software

Xylon provides Linux Framebuffer driver, Linux userspace ISP driver and logiISP example. Described chapters are:

- Xylon Linux userspace drivers and libs building
- Xylon Linux framebuffer driver
- Using the Linux binaries - logiISP

8 LOGIISP DEMO APPLICATION

The logiISP demo is the QT application that runs on Linux OS and can be fully controlled by the mouse. The demo control box occupies the left part of the application window (Figure 36). The video stream in the right part of the application window can be turned on and off by buttons "Video ON" and "Video OFF".

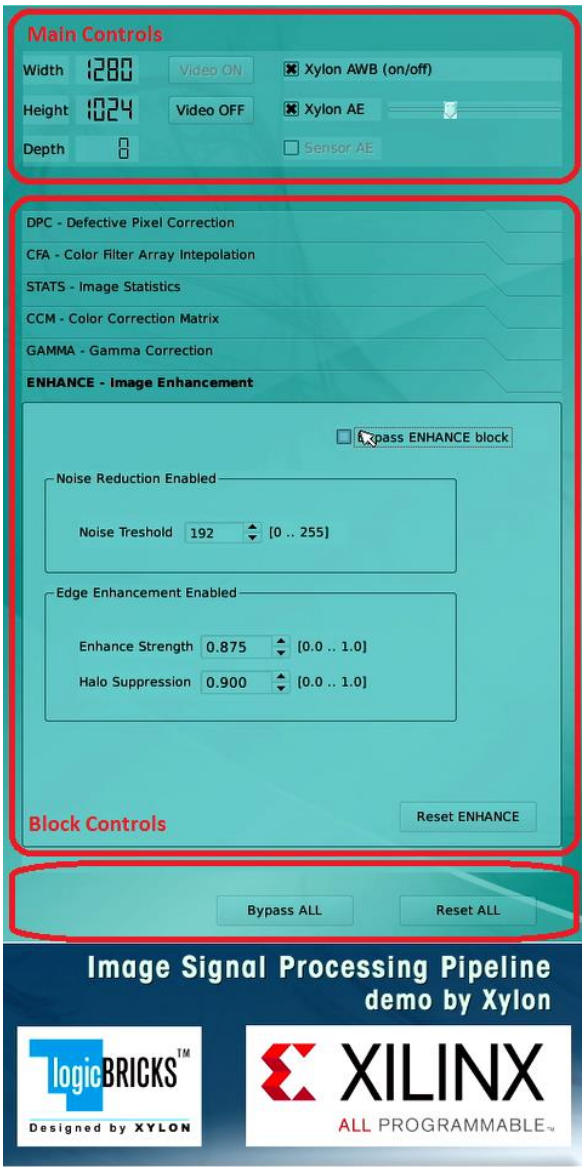


Figure 36: logiISP Demo – The Control Box

The Control box is divided in 3 parts: Main Controls, Block Controls and Bypass and Reset All.

8.1 Main Controls

- Main control frame displays the video resolution and video color depth (bits per pixel). Those three values are determined by the PYTHON-1300 Camera Module and can not be changed.
- Video ON and OFF buttons turn video input streaming on and off.
- Checkbox "Xylon AWB" – turns on/off Xylon Auto White Balance (AWB) algorithm, in which case the user can not manually program the Color Correction Matrix (CCM) values.
- Checkbox "Xylon AE" – turns on/off Xylon Auto Exposure (AE) control. The AE algorithm uses image statistic data and calculates the image brightness. The calculated image brightness is used by the processor-controlled algorithm that calculates sensor gain and exposure values.
- Target brightness slider – The checkbox AE muxt be turned to allow this slider to sets up the AE brightness target value.
- Check box "Sensor AE" - turns on the PYTHON-1300 Camera Module's built-in Auto Exposure Control (AEC).

8.2 Block Controls

Each ISP pipeline block can be independently reset or bypassed. User controllable options are briefly described in the following text. For more information about the logiISP customization options, please refere to the logiISP User's Manual distributed with the IP core.

8.2.1 DPC - Defective Pixel Correction Block

The DPC block menu displays the number of defective pixel candidates and the number of the detected defective pixels. Those values are updated every second.

Demo users can setup the following defective pixel calculation parameters: pixel age, spatial variance threshold and temporal variance threshold.

8.2.2 CFA – Color Filter Array Interpolation Block

Enables setup of the Bayer filter phase configuration, which is specified by the beginning pixel in the top-left corner of the Bayer sampling grid: Green, Red, or Blue Pixel.

8.2.3 STATS – Image Statistic Block

The Image Statistic Block cannot be turned off or bypassed. This block is here for a future development: displaying histograms, etc. Xylon Auto White Balance (AWB) and Auto Exposure (AE) control algorithms use the statistics data collected by this ISP block.

8.2.4 CCM – Color Correction Matrix Block

Demo users can setup the following CCM block parameters: the color correction matrix, color offsets, and clip and clamp values.

It is not possible to change the CCM matrix values while the AWB algorithm is turned on (checked in the Main Controls). Xylon AWB does not affect the color offsets, clip and clamp values.

8.2.5 GAMMA – Gamma Correction Block

The GAMMA block enables user to set gamma *value* (*γ)* for each color. The Gamma look-up tables (LUT) values are calculated by the software application and written in the logiISP IP core's LUTs.

The demonstrated logiISP configuration uses a separated Gamma LUT for each color.

8.2.6 Enhance – Image Enhancement Block

The Enhance block allows for noise reduction parameter (noise threshold) and enhance parameters (enhance strength and halo suppression) setup.

8.3 Bypass ALL and Reset ALL buttons

8.3.1 Bypass ALL Button

Demo users can bypass all ISP pipeline blocks and then gradually turn them (one by one) back to evaluate effects on the processed video stream.

8.3.2 Reset ALL Button

Resets all logiISP blocks to the initial state, turns off the Xylon AWB/AE algorithms and sets the default AE target value.

9 REVISION HISTORY

Version	Date	Author	Approved by	Note
1.00.a	December 15, 2014	G. Galic	G. Galic	Initial