32-BIT VMEBUS REPEATER

MODEL PT-VME902A

USER'S MANUAL

DRAWING NUMBER: 106A0102

REVISION CONTROL

Revision	ECN	Pages Effected	Approvals
00	-	All	
01	080A000017	Schematic Appendix Only	
02	080A000028	Schematic Appendix Only	

MODEL PT-VME902A 32-BIT VMEBUS REPEATER
USER'S MANUAL

NOTICE

This document presents information for users of the Performance Technologies, Incorporated' Model PT-VME902A 32 Bit VMEbus Repeater.

Although the information contained within this document is considered accurate and characteristic of the subject product, Performance Technologies, Incorporated reserves the right to make changes to this document and any products described herein to improve reliability, function, or design. Performance Technologies, Incorporated does not assume any liability arising out of the application or use of any product or circuit described herein.

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THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. AS TEMPORARILY PERMITTED BY REGULATION, IT HAS NOT BEEN TESTED FOR COMPLIANCE WITH THE LIMITS FOR CLASS A COMPUTING DEVICES PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE, IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES MAY BE REQUIRED TO CORRECT THE INTERFERENCE.

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SECTION 1 - GENERAL INFORMATION

1. SCOPE

This document provides support information for users of the Performance Technologies, Incorporated' 32 Bit VMEbus Repeater, Model PT-VME902A.

2. APPLICABLE DOCUMENTS

Reference to the following documents should be made in conjunction with this manual:

VMEbus Specification Manual (Revision C.1) -
IEC 821 Bus and IEEE P1014/D1.2,
VMEbus International Trade Association (VITA)

3. FEATURES

The Model PT-VME902A 32 Bit VMEbus Repeater has the following features:

* Buffered Interface That Supplies Drive For An Additional, Full Capacity VMEbus Load Configuration.

* Master/Slave Timing Compensation - VMEbus A32,D32 Compatible.

* Bidirectional Seven Level VMEbus Interrupt Channel - VMEbus IH(1-7) Compatible.

* Four Level VMEbus Arbitration - VMEbus PRI/RRS Compatible.

* VMEbus System Controller Functions Including A Bus Access Timeout Monitor On The Non-Host Side Of The Repeater.

* Supports Both "Star" And "Daisy-Chain" Configurations For Multiple VMEbus Card-Cage Systems.

* Supports A Software Controlled Isolation For Independent Card-Cage Operation And A Switch Controlled Isolation For Independent Card-Cage Powering-Up/Powering-Down.

* Conforms To VMEbus Specification - Revision C.1.

* Consists Of Two 32 Bit VMEbus Interface Boards With Standard Six Foot Long Interconnect Cables (20 Foot Absolute Maximum).

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SECTION 2 - INSTALLATION

1. UNPACKING AND INSPECTION

The PT-VME902A contains integrated circuits that may be damaged by electrostatic discharge. Precautions should be taken when handling and touching the PT-VME902A to minimize the risk of such static damage.

The shipping carton should be inspected for any possible damage that may have occurred during shipment. If such damage is noted, an agent of the shipping carrier should be present at any further unpacking and contents inspection.

Unpack contents from shipping carton and verify against packing list. Inspect the PT-VME902A assembly for any visible signs of shipping damage. If such damage is noted, report such damage to Performance Technologies, Incorporated and do not proceed with any further configuration and installation.

2. HARDWARE CONFIGURATION

The PT-VME902A has been configured at the factory to meet the needs of the majority of users. Your specific application may, however, require that the factory configuration be altered. In order to provide maximum flexibility, there are a large number of options that can present a confusing array of choices. For simplicity, the options should be considered in two groups. The first group, described in paragraphs 2.3 through 2.5 should be investigated if the factory configuration is not working and Software Isolation is not being used. The remainder of the options must be considered if the factory configuration is not working and Software Isolation is being used. It is recommended that the "Functional Element" descriptions in Section 3 of this manual be studied prior to altering any configuration options.

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2.1 HOST PCB CONFIGURATION OPTION LOCATION

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2.2 NON-HOST PCB CONFIGURATION OPTION LOCATION

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2.3 INTERRUPT HANDLER LOCATION SELECT

Switch U22, located on both the Host and the Non-Host PCBs, selects the direction in which interrupts are routed. The switches should be set so that interrupts are sent to the card cage (Host or Non-Host) in which the Interrupt Handler for that level is located.
"*" indicates factory configuration.

Interrupt Handler Level/Location	U22 Switch Positions	
*Level 1 (IRQ1) in Host	Host	U22-1 Off
	Non-Host	U22-1 On
Level 1 (IRQ1) in Non-Host	Host	U22-1 On
	Non-Host	U22-1 Off
*Level 2 (IRQ2) in Host	Host	U22-2 Off
	Non-Host	U22-2 On
Level 2 (IRQ2) in Non-Host	Host	U22-2 On
	Non-Host	U22-2 Off
*Level 3 (IRQ3) in Host	Host	U22-3 Off
	Non-Host	U22-3 On
Level 3 (IRQ3) in Non-Host	Host	U22-3 On
	Non-Host	U22-3 Off
*Level 4 (IRQ4) in Host	Host	U22-4 Off
	Non-Host	U22-4 On
Level 4 (IRQ4) in Non-Host	Host	U22-4 On
	Non-Host	U22-4 Off
*Level 5 (IRQ5) in Host	Host	U22-5 Off
	Non-Host	U22-5 On
Level 5 (IRQ5) in Non-Host	Host	U22-5 On
	Non-Host	U22-5 Off
*Level 6 (IRQ6) in Host	Host	U22-6 Off
	Non-Host	U22-6 On
Level 6 (IRQ6) in Non-Host	Host	U22-6 On
	Non-Host	U22-6 Off
*Level 7 (IRQ7) in Host	Host	U22-7 Off
	Non-Host	U22-7 On
Level 7 (IRQ7) in Non-Host	Host	U22-7 On
	Non-Host	U22-7 Off

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2.4 RELEASE-ON-REQUEST NON-HOST MASTER ENABLE/DISABLE

Jumper headers K5 on the Host PCB, and K6 on the Non-Host PCB are used to enable/disable the Non-Host master release-on-request feature. If this feature is enabled and isolation is disabled, Non-Host Bus Request Level 0 (BR0) will become the OR'ed condition of all four Host Bus Request Levels (BR0 through BR3) for Non-Host release-on-request (ROR) masters.

Non-Host Master R-O-R Mode	Jumpers IN, all others OUT		
*Enabled	Host	K5-1	to K5-2
	Non-Host	K6-1	to K6-2
Disabled	Host	K5-2	to K5-3
	Non-Host	K6-2	to K6-3

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2.5 ISOLATION CONTROL REGISTERS SLAVE ADDRESS SELECT

Switches U35, U38 located on the Host PCB, and U34, U37 located on the Non-Host PCB, are used to set the slave address (VMEbus A16 compatible) of the Isolation Control Registers. Since the Host isolation control register and Non-Host isolation control register are independent, each register may be configured to a different address. However, the same address may be used by both registers. The address is formed by setting the desired logic level for each bit. Note that, although this option pertains to Isolation, it is included in this option group since the slave address of the registers could conflict with other address assignments even if Isolation is not used.
"*" indicates factory configuration.

Address Bit	Condition	Host Slave Address Switch	Non-Host Slave Address Switch
AM2	User	U38-1 On	U37-1 On
	*Super	U38-1 Off	U37-1 Off
A01	*False	U38-2 On	U37-2 On
	True	U38-2 Off	U37-2 Off
A02	*False	U38-3 On	U37-3 On
	True	U38-3 Off	U37-3 Off
A03	*False	U38-4 On	U37-4 On
	True	U38-4 Off	U37-4 Off
A04	*False	U38-5 On	U37-5 On
	True	U38-5 Off	U37-5 Off
A05	*False	U38-6 On	U37-5 On
	True	U38-6 Off	U37-5 Off
A06	*False	U38-7 On	U37-7 On
	True	U38-7 Off	U37-7 Off
A07	*False	U38-8 On	U37-8 On
	True	U38-8 Off	U37-8 Off
A08	*False	U35-1 On	U34-1 On
	True	U35-1 Off	U34-1 Off
A09	*False	U35-2 On	U34-2 On
	True	U35-2 Off	U34-2 Off
A10	*False	U35-3 On	U34-3 On
	True	U35-3 Off	U34-3 Off
A11	*False	U35-4 On	U34-4 On
	True	U35-4 Off	U34-4 Off
A12	*False	U35-5 On	U34-5 On
	True	U35-5 Off	U34-5 Off
A13	*False	U35-6 On	U34-5 On
	True	U35-6 Off	U34-5 Off
A14	*False	U35-7 On	U34-7 On
	True	U35-7 Off	U34-7 Off
A15	*False	U35-8 On	U34-8 On
	True	U35-8 Off	U34-8 Off

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2.6 ISOLATION CONTROL BUS REQUEST/GRANT LEVEL

Jumper headers K1 and K2, on both the Host and Non-Host PCBs, provide the means of configuring the bus requester in the isolation control to one of four possible request/grant levels (BR0/BG0IN/BG0OUT through BR3/BG3IN/BG3OUT). On the Host, the bus requester is used to enable isolation and to issue interrupt acknowledge cycles from the Non-Host during software isolation. On the Non-Host, the bus requester is used to disable isolation and to issue interrupt acknowledge cycles from the Host during software isolation. Jumper configuration shown applies to both Host and Non-Host PCBs. "*" indicates factory configuration.

Bus Request/ Grant Level	Jumpers IN, all other K1,K2 OUT
BR0/BG0IN/BG0OUT	K1-1 to K1-2 K1-3 to K1-4 K1-6 to K1-7 K1-10 to K1-11 K1-14 to K1-15 K2-1 to K2-2
BR1/BG1IN/BG1OUT	K1-2 to K1-3 K1-5 to K1-6 K1-7 to K1-8 K1-10 to K1-11 K1-14 to K1-15 K2-3 to K2-4
BR2/BG2IN/BG2OUT	K1-2 to K1-3 K1-6 to K1-7 K1-9 to K1-10 K1-11 to K1-12 K1-14 to K1-15 K2-5 to K2-6
*BR3/BR3IN/BG3OUT	K1-2 To K1-3 K1-6 To K1-7 K1-10 To K1-11 K1-13 To K1-14 K1-15 To K1-16 K2-7 To K2-8

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2.7 SOFTWARE ISOLATION CONTROL BITS (B0-B1) INITIALIZATION

Jumper headers K3, K4 on the Host PCB and K4, K5 on the Non-Host PCB, provide the means of controlling the initialization state and software access of B0 and B1 in the isolation control registers. Using these jumpers, the bits can be initialized to a particular value and/or subsequent software write access to bits enabled/disabled. The Host and Non-Host isolation control register may be configured independently.
"*" indicates factory configuration.

State After Reset	Host Jumper IN, all other K3,K4 OUT	Non-Host Jumper IN, all other K4,K5 OUT
*B0=0, R/W	K4-1 to K4-3	K5-1 to K5-3
B0=1, R/W	K4-1 to K4-2	K5-1 to K5-2
B0=0, RO	K4-3 to K4-4	K5-3 to K5-4
B0-1, RO	K4-2 to K4-4	K5-2 to K5-4
*B1=0, R/W	K3-1 to K3-3	K4-1 to K4-3
B1=1, R/W	K3-1 to K3-2	K4-1 to K4-2
B1=0, RO	K3-3 to K3-4	K4-3 to K4-4
B1=1, RO	K3-2 to K3-4	K4-2 to K4-4

2.8 NON-HOST ISOLATION BUS ACCESS TIMEOUT MONITOR ENABLE/DISABLE

Jumper header K3, located on the Non-Host PCB, enables or disables the Non-Host bus access timeout monitor. If this option is enabled, the Bus Access Timeout Monitor Time Delay must also be set.
"*" indicates factory configuration.

Timeout Monitor State	Jumpers IN, all other K3 OUT
*Enabled	K3-1 to K3-2
Disabled	K3-2 to K3-3

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2.9 NON-HOST ISOLATION BUS ARBITER MODE SELECT

Jumper header K7, located on the Non-Host PCB, selects the operating mode of the Non-Host bus arbiter.
"*" indicates factory configuration.

Bus Arbiter Mode	Jumpers IN, all other K7 OUT
*Priority	K7-1 to K7-2
Round Robin	K7-2 to K7-3

2.10 NON-HOST ISOLATION BUS ACCESS TIMEOUT MONITOR TIME DELAY

Switch U56, located on the Non-Host PCB, is used to set the Non-Host Bus Access Timeout Monitor to 1 of 256 possible time delays in the range of 50 microseconds to 12.8 milliseconds. The time delay is calculated by using the equation (0.050 milliseconds + S1 + S2 + S3 + S4 + S5 + S6 + S7 + S8).
"*" indicates factory configuration.

Switch/ Delay Value	U56 Switch Position
*S1 / 0.5 milliseconds	U56-1 On
*S2 / 0.100 milliseconds	U56-2 On
*S3 / 0.200 milliseconds	U56-3 On
*S4 / 0.400 milliseconds	U56-4 On
*S5 / 0.800 milliseconds	U56-5 On
*S6 / 1.600 milliseconds	U56-6 On
*S7 / 3.200 milliseconds	U56-7 On
*S8 / 6.400 milliseconds	U56-8 On

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3. INSTALLATION

3.1 PRE-INSTALLATION PROCEDURE

Before proceeding with the PT-VME902A installation, a decision must be made as to which card-cage is to be the Host and which card-cage is to be the Non-Host. Use the following points for a basis to make this decision:

.1 The System Controller Board (bus arbiter) must be located in the Host card-cage.

.2 The direction of the System Reset (SYSRESET) signal and Power Fail (ACFAIL) signal are from the Host to the Non-Host, and the direction of the System Fail (SYSFAIL) signal is from the Non-Host to the Host.

Also, before installing the PT-VME902A, both boards should be configured as required, and the voltage levels supplied to both the Host and Non-Host card-cages into which the PT-VME902A is to be installed should be measured before installation to insure that they are within the specified range. Note that if the same power supply is not used for both the Host and Non-Host card-cages, a good common reference ground should be established between the two power supplies for proper operation of the PT-VME902A.

The PT-VME902A should never be inserted or removed from the Host and Non-Host card-cages while power is applied. Such insertion/removal with power applied could seriously damage the PT-VME902A components.

3.2 CARD-CAGE PREPARATION

The System Controller Board (bus arbiter), which is not part of the PT-VME902A, must be located in slot A01 of the Host card-cage. The Host side of the PT-VME902A may be installed in any slot on the VMEbus backplane in the Host card-cage keeping in mind that the interrupt acknowledge daisy-chain (IACKIN/IACKOUT) and the bus grant daisy-chains (BG0IN/BG0OUT through BG3IN/BG3OUT) must be used. The daisy-chain jumpers on the backplane must be removed for this slot. Note that multiple "first level" Non-Host card-cages may be added to a single Host card-cage by adding an extra PT-VME902A for every Non-Host card-cage added (star configuration).

The Non-Host side of the PT-VME902A must be installed in slot A01 on the VMEbus backplane in the Non-Host card-cage. The daisy-chain jumpers on the backplane must be removed for this slot. No System Controller Board should be installed into the Non-Host card-cage since all system controller functions are

handled by the PT-VME902A. Note that one or more "second level" Non-Host card-cages may be added to this "first level" Non-Host card-cage by installing the Host side of an additional PT-VME902A into any slot of the "first level" Non-Host card-cage (daisy-chain configuration).

3.3 CABLE INSTALLATION

.1 Unshielded Version

The unshielded version of the PT-VME902A uses four, industry standard, 50-pin flat cables as the board-to-board connection.

The unshielded cables must be connected before the boards are installed in the cardcage. To install the cables, remove the cable clamp by removing three M2.5 screws which secure it to the front panel. The cables are installed by matching the "J" numbers on the PCB silkscreen with the numbers stamped on the cables. After making the connections, reinstall the cable clamp using the three M2.5 screws.

.2 Shielded Version

The shielded version of the PT-VME902A uses four 50-pin shielded pair cables terminated with 50-pin "D" connectors as the board to board connection.

The shielded cables may be connected after the PT-VME902A is installed in the cardcage. To install the cables, simply match the "J" numbers on the front panel with the numbers on the cables.

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SECTION 3 - PRODUCT SPECIFICATION

1. GENERAL DESCRIPTION

The PT-VME902A 32 Bit VMEbus Repeater is a fully buffered and timing compensated interface for connecting two VMEbus compatible card-cages together. VMEbus masters, slaves, interrupt handlers and interrupters located on either side of the repeater functionally appear to be in the same cardcage. In addition, the switch and software controlled isolation give the PT-VME902A functionality and applications beyond the typical repeater.

The PT-VME902A supplies the electrical and physical means for interconnecting two VMEbus compatible subsystems, designated as Host and Non-Host, together. The Non-Host subsystem becomes an extension of the Host subsystem under the following guidelines:

.1 The system controller function, located in the Host cardcage, provides the bus arbitration and system reset for the Host and Non-Host when isolation is not selected.

.2 The direction of the System Reset and Power Fail signals are from the Host to the Non-Host, and the direction of the System Fail signal is from the Non-Host to the Host.

.3 Multiple VMEbus card-cages may be interconnected in a "star" or "daisy-chain" configuration, or a combination of the two, by adding a PT-VME902A for each additional VMEbus cardcage.

2. MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Characteristic	Specification
Ambient Temperature	0o to +55o C, operating -55o to +85o C, storage
Humidity	0% to 90% (non-condensing)
Mechanical	Per Board Dimensions For Two (2) Standard Double-Width VMEbus Boards:
	Width: 234 mm. (9.2 inches)
	Depth: 160 mm. (6.3 inches)
	Comp Height: 12.7 mm. (0.5 inches)
	Front Panel: 20.3 mm. (0.8 inches)
	Per Cable Dimensions For Four 50 conductor flat cables:
	Length: 1830 mm. (72 inches)

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3. ELECTRICAL SPECIFICATIONS

Characteristic	Specification	
Power Requirements (Per Board)	+5VDC (5%) at	3.8AMPs, typical. 5.8AMPs, maximum.
Total Signal Delay With 6 Foot Cables	AS (RD/WR)	- 170ns typ. - 190ns max.
	DSx (RD Cycle)	- 150ns typ. - 170ns max.
	DSx (WR Cycle)	- 225ns typ. - 250ns max.
	DTACK (RD Cycle)	- 120ns typ. - 140ns max.
	DTACK (WR Cycle)	- 35ns typ. - 50ns max.
Required Bus Timing	AS Cycle (false-to-true transition to false-to-true transition and/or true-to-false transition to true-to-false transition)	- 200ns min.
	AS Asserted (false-to-true transition to true-to-false transition)	- 140ns min.
+5VDC Monitor	Pulse Width	- 300 ms min.
	Trigger Voltage	- 4.4VDC min. - 4.7VDC max.

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4. FUNCTIONAL ELEMENTS

The PT-VME902A is made up of a Host and a Non-Host 32 Bit VMEbus Interface Board and uses the Extension Bus to interconnect them via four cables. The functional elements for the PT-VME902A are outlined in the following subsections.

4.1 DATA TRANSFER CONTROL

The data transfer control on the PT-VME902A is used by the VMEbus master to transfer data to/from an addressed slave in another VMEbus cardcage and used by a VMEbus interrupt handler to transfer the interrupt vector from an interrupter in another VMEbus cardcage. The data transfer control is VMEbus A32,D32 compatible and supports byte/word/longword aligned/unaligned data transfers, read-modify-write cycles, sequential block cycles and address pipelining. The added delay in the data transfer cycle incurred by the master when the slave is on the opposite side of the repeater, is the amount of time added for the Address Strobe/Data Strobes (AS/DS0/DS1) to be received by the slave plus the Data Transfer Acknowledge (DTACK) to be received by the master. A typical added delay of 290 nanoseconds is incurred for a READ cycle and 260 nanoseconds is incurred for a WRITE cycle.

When a data transfer is initiated in the Host or Non-Host by the bus master, the data transfer control on the PT-VME902A will initiate the same transfer on the other end of the repeater with compensation for any signal skew. If the addressed slave is located on the opposite side of the repeater relative to the bus master, the data transfer control will respond to the bus master in the same way that the slave responded.

During isolation, the data transfer control is disabled. However, during software controlled isolation only, the data transfer control will be temporarily enabled for an interrupt acknowledge cycle requested from the other side of the repeater if that direction of interrupt requests is specified by the isolation control registers.

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4.2 INTERRUPT CONTROL

The interrupt control on the PT-VME902A is used by a VMEbus interrupter to interrupt a VMEbus interrupt handler in another VMEbus cardcage. The interrupt control is VMEbus IH(1-7) compatible, supplies an IACK daisy-chain driver and supports interrupt requests/acknowledges across the repeater in both directions.

When an Interrupt Request (IRQ1-IRQ7) is issued in the Host or Non-Host by an interrupter and, if the interrupt request direction switch is set accordingly, for that interrupt request level, the interrupt control on the PT-VME902A will issue that Interrupt Request on the other end of the repeater. When the interrupt handler responds with an interrupt acknowledge cycle, the data transfer control on the PT-VME902A will initiate the same interrupt acknowledge cycle back on the other side of the repeater with compensation for any signal skew. The Interrupt Acknowledge daisy-chain (IACKIN/IACKOUT) will always originate in the Host and then branch to the first Non-Host cardcage or Host interrupter that is issuing an Interrupt Request on that level. However, during software controlled isolation only, the Interrupt Acknowledge daisy-chain will ignore the Host and originate in the Non-Host if the interrupt handler for an issued Interrupt Request is located in the Non-Host and there are no Interrupt Requests issued on that interrupt request level from the Host.

During software controlled isolation, the interrupt control is enabled in one direction as specified by the isolation control registers, and during the switch controlled isolation, the interrupt control is disabled.

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4.3 BUS ARBITRATION CONTROL

The bus arbitration control on the PT-VME902A is used by a Non-Host VMEbus master to gain control of the Host and Non-Host data transfer busses or to gain control of the Non-Host data transfer bus only during isolation. The bus arbitration control is VMEbus PRI/RRS compatible and supports Non-Host VMEbus arbitration and an optional Host VMEbus request for Non-Host VMEbus Release-On-Request (ROR) masters.

The Non-Host VMEbus arbitration is an extension of the Host VMEbus arbiter. However, during isolation, the Non-Host VMEbus arbitration is provided by a VMEbus arbiter on the PT-VME902A which has a jumper selectable Priority (PRI) or Round-Robin (RRS) arbitration mode). Note that the Round-Robin arbitration mode does not support Bus Clear (BCLR).

Since the VMEbus Requests (BR0-BR3) are buffered from the Non-Host to the Host, a Non-Host VMEbus Release-On-Request (ROR) master will not be able to sense when a Host VMEbus master is requesting the use of the Host and Non-Host data transfer busses. However, the Non-Host Bus Request level 0 (BR0) may be optionally jumpered on the PT-VME902A to be either buffered to the Host Bus Request level 0 (same as other levels) or an OR'ed condition of all the Host Bus Requests (BR0 through BR3) buffered to the Non-Host. The OR'ed condition has timing compensation so the Non-Host master will not sense its own Bus Request. Note that this function is disabled during isolation.

4.4 MAINTENANCE SIGNALS

The maintenance signals System Reset (SYSRESET) and AC Power Fail (ACFAIL) are buffered across the Extension Bus from the Host to the Non-Host, and the maintenance signal System Fail (SYSFAIL) is buffered across from the Non-Host to the Host. The Non-Host System Clock (SYSCLK) is generated by the PT-VME902A. However, during switch controlled isolation, the buffering of System Reset (SYSRESET), AC Power Fail (ACFAIL) and System Fail (SYSFAIL) are disabled.

On the Non-Host portion of the repeater, the +5VDC monitor and front panel RST button are used to maintain the system controller reset function in the Non-Host when either the Host or Non-Host ISO switch is set to ON. The red LED on the Non-Host front panel always indicates the status of the Non-Host System Fail signal. However, the red LED on the Host front panel only indicates the status of the corresponding Non-Host System Fail signal when there is no switch controlled isolation.

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4.5 BUS ACCESS TIMEOUT MONITOR

The Non-Host bus access timeout monitor provides a Bus Error (BERR) whenever Data Strobe 0 (DS0) and/or Data Strobe 1 (DS1) are asserted for a duration specified by a switch option without detecting a Data Transfer Acknowledge (DTACK). This function is only enabled during isolation and when selected by the jumper option.

4.6 ISOLATION CONTROL

The isolation control on the PT-VME902A is used to functionally separate the Non-Host cardcage from the Host cardcage in an organized manner so that both card-cages may continue normal operation independently. The isolation control supports software (address mapped registers) and hardware (switch/LED) controlled isolation as described in the following subsections.

.1 Isolation Control Registers

The two 8 bit (VMEbus D8(O) compatible) isolation control registers are used to control the software controlled isolation and to monitor the switch controlled isolation. One register is located on the Host portion of the repeater while the other register is located on the Non-Host portion of the repeater. Each register has a switch selectable 16 bit (VMEbus A16 compatible) address, and since the repeater only allows Host VMEbus masters to access the Host isolation control register and Non-Host VMEbus masters to access the Non-Host isolation control register, both registers may be configured with the same 16 bit address. The data bits in the Host and Non-Host isolation control registers are defined as follows:

B0 (R/W) = 0 Requests that isolation be turned off and interrupts be enabled from the Host to the Non-Host
1 Requests that isolation be turned on and interrupts be disabled from the Host to the Non-Host

B1 (R/W) = 0 Requests that isolation be turned off and interrupts be enabled from the Non-Host to the Host
1 Requests that isolation be turned on and interrupts be disabled from the Non-Host to the Host

Note that register bits B0 and B1 may be independently configured to be set to a "0" or a

"1" upon the issuance of a System Reset (R/W) or held to a "0" or a "1" continuously (R/O).

B2 (R/O) = 0 Indicates that the isolation control switch on the Host portion of the repeater is requesting that isolation be turned off
1 Indicates that the isolation control switch on the Host portion of the repeater is requesting that isolation be turned on

B3 (R/O) = 0 Indicates that the isolation control switch on the Non-Host portion of the repeater is requesting that isolation be turned off
1 Indicates that the isolation control switch on the Non-Host portion of the repeater is requesting that isolation be turned on

B4 (R/O) = 0 Indicates that this register is located on the Non-Host portion of the repeater
1 Indicates that this register is located on the Host portion of the repeater

B5 (R/O) = 0 Indicates that isolation has been turned off in response to B0 = 0 and B1 = 0 in the Host and/or Non-Host isolation control registers
1 Indicates that isolation has been turned on in response to B0 = 1 and/or B1 = 1 in the Host and Non-Host isolation control registers

B6 (R/O) = 0 Indicates that isolation has been turned off in response to the Host and Non-Host isolation control switches (B2 = 0 and B3 = 0)
1 Indicates that isolation has been turned on in response to the Host and/or Non-Host isolation control switches (B2 = 1 and/or B3 = 1)

B7 (R/O) = 0 Indicates that isolation is turned off (B5 = 0 and B6 = 0)
1 Indicates that isolation is turned on (B5 = 1 and/or B6 = 1)

R/W - Data bits that may be written and read
R/O - Data bits that are read only

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.2 Software Controlled Isolation

The software controlled isolation provides the ability to functionally disconnect the bus arbitration and data transfer portions of the Host VMEbus cardcage from the bus arbitration and data transfer portions of the Non-Host VMEbus cardcage. This allows the Host VMEbus masters to access Host VMEbus slaves without the contention of Non-Host VMEbus masters, and allows the Non-Host VMEbus masters to access Non-Host VMEbus slaves without the contention of Host VMEbus masters.

The maintenance signals are unaffected when the software controlled isolation is turned on, and the interrupts are disabled in one or both directions as specified by B0 and B1 in the isolation control registers. Note that when the interrupts are disabled in one or both directions by the repeater, there is no effect on interrupts generated and acknowledged within the same VMEbus cardcage.

a. Turning On Software Isolation

If isolation is not turned on and B0 has been set to a "1" in the Host and Non-Host isolation control registers or B1 has been set to a "1" in the Host and Non-Host isolation control registers, a Bus Request (BR0 - BR3) will be issued by the bus requester on the Host portion of the repeater. Once the requester receives a Bus Grant (BG0IN/BG0OUT - BG3IN/BG3OUT) from the Host bus arbiter on the system controller and has control of the Host and Non-Host bus arbitration, the bus arbitration control on the repeater will disconnect the Non-Host bus arbitration from the Host bus arbitration and enable a Non-Host bus arbiter located on the Non-Host portion of the repeater. Note that the Non-Host's Bus Requests (BR0 - BR3) will be removed from the Host within the 50 nanosecond window after the repeater's bus requester issues Bus Busy (BBSY) per the VMEbus specification.

Once the bus arbitration is disconnected between the Host and Non-Host and the last data transfer has been completed by the previous bus master, the data transfer control on the repeater will disconnect the Non-Host data transfer bus from the Host data transfer bus and enable a Non-Host bus access timeout monitor located on the Non-Host portion of the repeater.

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After the data transfer bus is disconnected, the Interrupt Request signals (IRQ1 - IRQ7) are disabled in the direction specified by the isolation control registers, and the interrupt acknowledge cycles are disabled in the opposite direction. If an interrupt acknowledge cycle is generated by an interrupt handler for the direction of interrupts still enabled and the Interrupt Request is being issued by an interrupter on the other side of the repeater, the bus requester on the interrupter's side of the repeater will issue a Bus Request (BR0 - BR3) to gain control of that data transfer bus temporarily so the interrupt control, utilizing the data transfer control, can fetch the interrupt vector from the interrupter. The bus requester will drop Bus Busy (BBSY) shortly after the Address Strobe (AS) is issued for this interrupt acknowledge cycle on the interrupter's data transfer bus.

b. Turning Off Software Isolation

If isolation is turned on and B0 has been set to a "0" in the Host or Non-Host isolation control registers and B1 has been set to a "0" in the Host or Non-Host isolation control registers, a Bus Request (BR0 - BR3) will be issued by the bus requester on the Non-Host portion of the repeater. Once the bus requester receives a Bus Grant (BG0IN/ BG0OUT - BG3IN/BG3OUT) from the Non-Host bus arbiter on the repeater and has control of the Non-Host bus arbitration, the bus arbitration control on the repeater will disable the Non-Host bus arbiter and connect the Non-Host bus arbitration to the Host bus arbitration.

Once the bus arbitration is connected between the Host and Non-Host and the last data transfer has been completed by the previous Non-Host bus master and the Host Address Strobe (AS) is false, the data transfer control on the repeater will disable the Non-Host bus access timeout monitor and connect the Non-Host data transfer bus to the Host data transfer bus.

After the data transfer bus is connected, the interrupt control will enable the interrupts in both directions.

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.3 Switch Controlled Isolation

The switch controlled isolation provides the ability to functionally disconnect the bus arbitration, data transfer, interrupt, and maintenance portions of the Host VMEbus cardcage from the Non-Host VMEbus cardcage. This allows the Host and Non-Host to operate totally independent of each other, and allows either the Host or Non-Host to be powered-down without affecting the operation of the other.

a. Turning On Switch Isolation

If the ISO switch on the front panel of the Host or Non-Host have been set to ON, the +5VDC monitor on the Non-Host portion of the repeater will be enabled and the software controlled isolation will be activated regardless of the software's request for isolation to be turned off in the isolation control registers. Once the bus arbitration and data transfer bus are disconnected between the Host and Non-Host, the interrupt and maintenance signals are disabled and the green LED on the Host and Non-Host front panel will turn ON to indicate that the two card-cages are disconnected. Note that the switch isolation request and switch isolation acknowledge may be monitored by the software in the isolation control registers.

b. Turning Off Switch Isolation

If the ISO switch on the front panel of the Host and Non-Host have been set to OFF, the maintenance signals will be enabled, the +5VDC monitor will be disabled and the green LED on the Host and Non-Host front panel will turn OFF. If the software is not requesting for isolation to be turned on in the isolation control registers, the software controlled isolation will be deactivated and the interrupt signals will be enabled. Note that the switch isolation request and switch isolation acknowledge may be monitored by the software in the isolation control registers.

4.7 EXTENSION BUS

The Extension Bus is used to interconnect the Host and Non-Host 32 Bit VMEbus Interface Boards together through four 50 conductor cables.

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