Using VHDL language, ALTERA Quartus II software and ALTERA DE2 board, you should design, simulate and implement a "4-bit up/down binary counter with reset button" circuit. The counter value must be automatically incremented/decremented by 1 every 1 second. The up counting or down counting is determined by the status of a push button on DE2 board (e.g. PUSHBUTTON[0]). If the push button is pressed, the counter should count down and vice versa. In the up counting mode, if the counter reaches "F" (hex), the
counter should go to "0" upon the next count. Similarly, in the down counting mode, when the counter reaches "0", it should go back to "F" (hex) upon the next count. The output of this circuit must be echoed in hex format on the 7-segment display unit of DE2 board (SEVEN SEGMENT Display). Use only one of the digits on 7-segment to display the counter value. The Reset will be determined by the other push button (e.g. PUSHBUTTON[1]). If the push button is pressed the counter should stop and the 7-segment display should reset to display "0". When pressed again, the counter will start counting. In this design you have to utilize the onboard oscillator as the source for clock signal (refer to "DE2 Board User Manual" to learn more about this signal).

Hints:

-This is a sequential logic circuit, where you must keep track of what state you are in.
-Declare libraries.
-Name of entity must match project name, declare ports of black box within entity, Architecture is where you should declare signals, write processes using sensitivity list, and assign signals to corresponding ports.
-You need to divide down the clock frequency from 50 MHz to 1 Hz.
-The push button on the DE2 board is already debounced by circuit on the board.
-It is highly recommended that each group writes at least some of the VHDL code BEFORE coming to the lab. This will save significant amount of their time.

Marking:
GAs will check the results of simulation and functionality of design on the
DE2 boards. Part marks will be given for all aspects.
35 percent for working simulation
35 percent for working implementation
30 percent individual oral questions
Extra time for project work can occur during G.A. office hours. Please make appointments through email. Late submissions will be penalized.