SAM3S Microcontroller Series
Schematic Check List

1. Introduction

This Application Note is a schematic review check list for systems embedding Atmel's SAM3S series of ARM® Cortex™-M3, Thumb®2-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the SAM3S Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This Application Note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify that the line item has been checked.

AT91 ARM Thumb-based Microcontrollers

Application Note

11061A–ATARM–28-Jul-10

2. Associated Documentation

Before going further into this Application Note, it is strongly recommended to check the latest documents for the SAM3S Series Microcontrollers on Atmel's Web site.

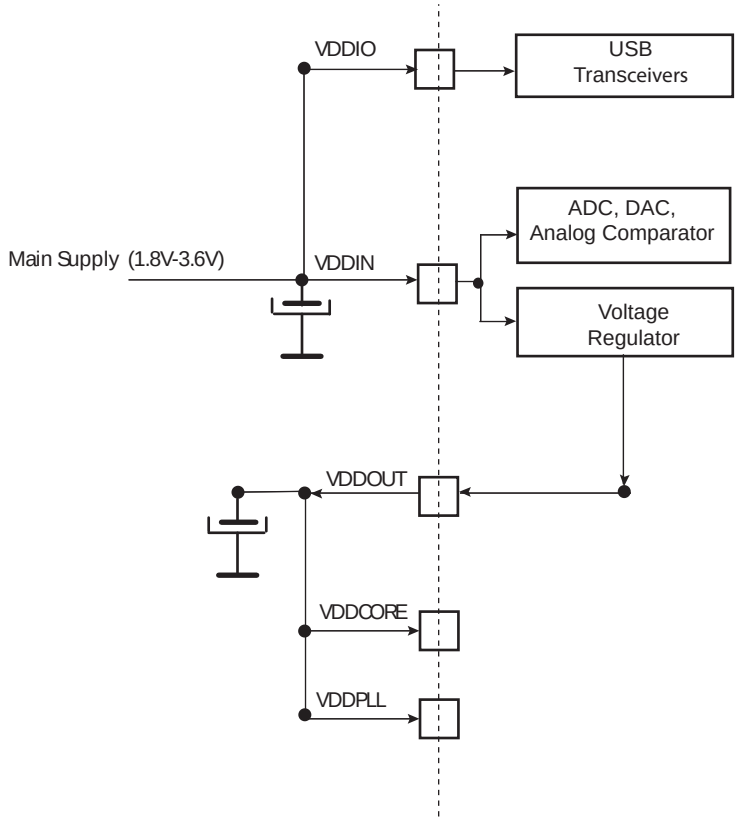
Table 2-1 gives the associated documentation needed to support full understanding of this application note.

Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	SAM3S Series Product Datasheet
Internal architecture of processor Thumb2 instruction sets Embedded in-circuit-emulator	This part is integrated and formated according to the core integration in the SAM3S series. This information is fully detailed in the SAM3S Series Product Datasheet. Cortex-M3 Technical Reference Manual (available from ARM Ltd.)
Evaluation Kit User Guide	SAM3S-EK Evaluation Board User Guide

3. Schematic Check List

Single Power Supply Strategy



Single Power Supply Schematic Example:

☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	1.8V to 3.6V Decoupling/Filtering capacitor (10µF or higher ceramic capacitor)(1)(2)	Powers the voltage regulator, ADC, DAC and Analog comparator power supply.
	VDDIO	1.62V to 3.6V Decoupling/Filtering capacitors (100 nF and 2.2µF)(1)(2)	Powers the peripheral I/Os, USB transceiver, Backup part, 32kHz crystal oscillator and oscillator pads. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning: At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V**
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2µF)(1)(2)	1.8V Output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	Must be connected directly to VDDOUT pin. 1.62V to 1.95V Decoupling capacitor (100 nF)(1)(2)	Power the Core, the embedded memories and the peripherals power supply.
	VDDPLL	1.62V to 1.95V Decoupling capacitor (100 nF)(1)(2)	Powers PLLA, PLLB, the Farst RC and the 3-20 MHz oscillator.
	GND	Ground	Ground pins GND are common to VDDIO, VDDPLL and VDDCORE

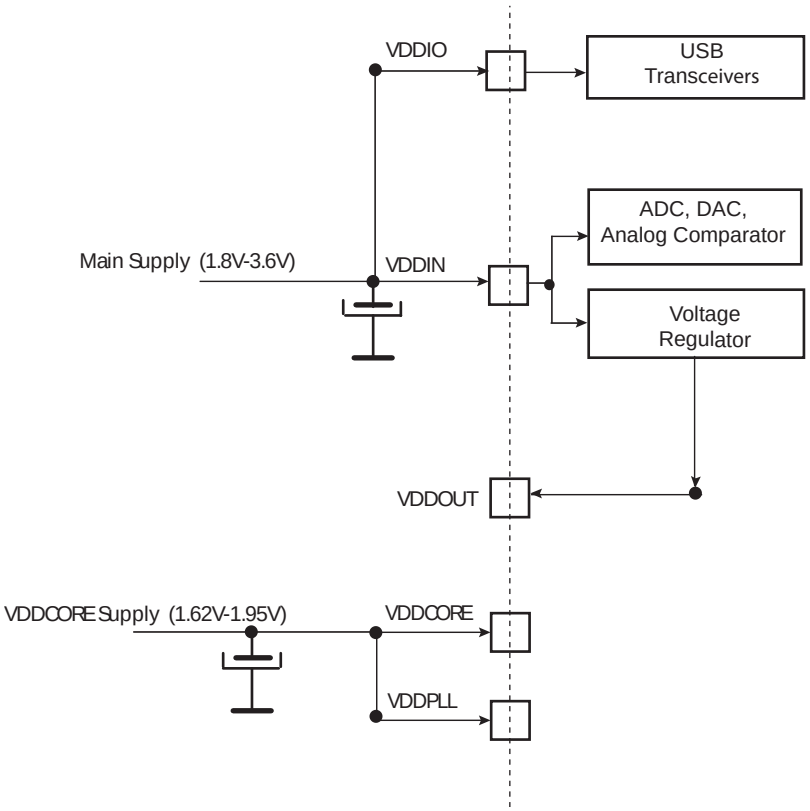
Note: Restrictions

With Main Supply < 2.0 V, USB and ADC/DAC and Analog comparator are not usable.

With Main Supply ≥ 2.0V and < 3V, USB is not usable.

With Main Supply ≥ 3V, all peripherals are usable.

Core Externally Supplied.



Core externally supplied Schematic Example:
Main Supply on VDDIO, and VDDIN (1.8V to 3.6V).
VDDCORE Supply is between 1.62V and 1.95V.

☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	1.8V to 3.6V Decoupling/Filtering capacitor (10µF or higher ceramic capacitor)(1)(2)	Powers the voltage regulator, ADC, DAC and Analog comparator power supply.
	VDDIO	1.62V to 3.6V Connected to Main Supply Decoupling/Filtering capacitors (100 nF and 2.2 µF)(1)(2)	Powers the peripheral I/Os. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning: At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V**
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2µF)(1)(2)	1.8V Output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.62V to 1.95V Connected to VDDCORE Supply Decoupling capacitor (100 nF and 2.2µF)(1)(2)	Core, embedded memories and peripherals power supply
	VDDPLL	1.62V to 1.95V Connected to VDDCORE Supply Decoupling capacitor (100 nF and 2.2µF)(1)(2)	Powers PLLA, PLLB, the Farst RC and the 3-20 MHz oscillator.
	GND	Ground	Ground pins GND are common to VDDIO, VDDPLL and VDDCORE

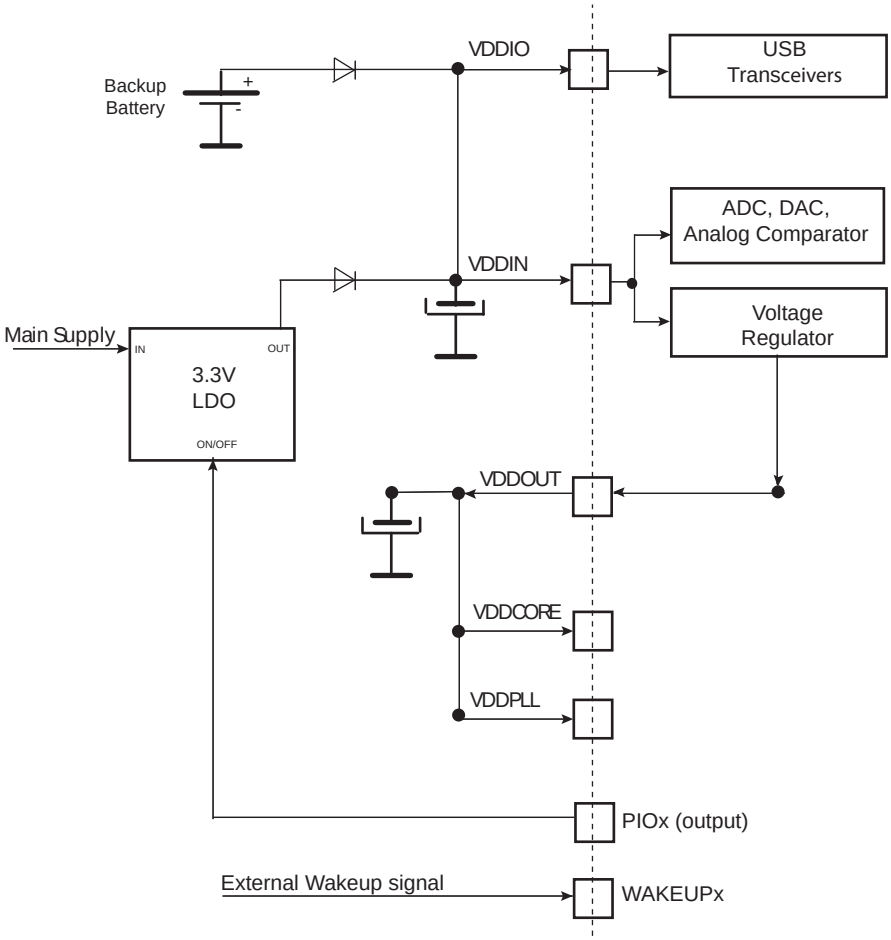
Note: Restrictions

With Main Supply < 2.0 V, USB and ADC/DAC and Analog comparator are not usable.

With Main Supply ≥ 2.0V and < 3V, USB is not usable.

With Main Supply ≥ 3V, all peripherals are usable.

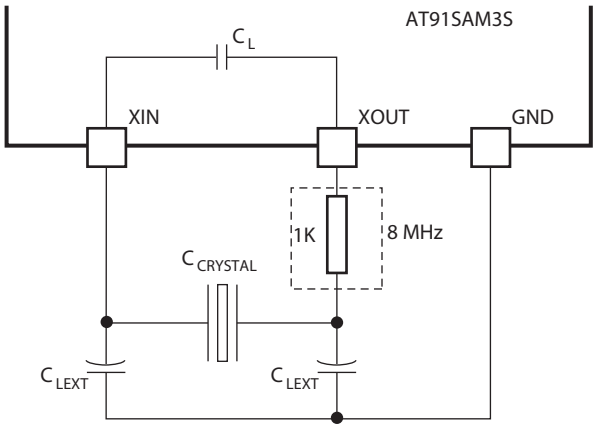
Backup Unit Externally Supplied

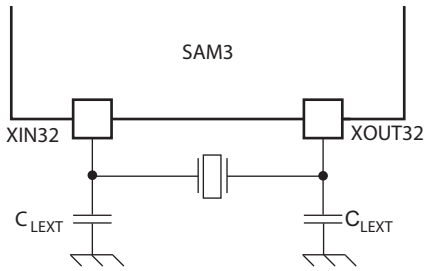


☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	1.8V to 3.6V Decoupling/Filtering capacitor (10µF or higher ceramic capacitor)(1)(2)	Powers the voltage regulator.
	VDDIO	1.62V to 3.6V Decoupling/Filtering capacitors (100 nF and 2.2 µF)(1)(2)	Powers the peripheral I/Os. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning: At power-up VDDIO needs to reach 0.6V before VDDIN reaches 1.0V**
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2µF)(1)(2)	1.8V Output of the main voltage regulator.

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.62V to 1.95V Connected to VDDOUT Supply Decoupling capacitor (100 nF)(1)(2)	Core, embedded memories and peripherals power supply
	VDDPLL	1.62V to 1.95V Connected to VDDOUT Supply Decoupling capacitor (100 nF)(1)(2)	Powers PLLA, PLLB, the Farst RC and the 3-20 MHz oscillator.
	GND	Ground	Ground pins GND are common to VDDIO, VDDPLL and VDDCORE

Note: The two diodes provide a "switchover circuit" (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

☑	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	PB9/XIN PB8/XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependant) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.	Internal Equivalent Load Capacitance (C_L): C_L = 9.5 pF Crystal Load Capacitance, ESR, Drive Level and Shunt Capacitance to validate.  The external load capacitance is calculated with the following formula: $C_{LEXT}=2*(C_{crystal}-C_L)$ Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM3S Series Datasheet. **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4 MHz.**
	PB9/XIN PB8/XOUT Main Oscillator in Bypass Mode	PB9/XIN: external clock source PB8/XOUT: can be left unconnected or used as GPIO.	1.62V to 3.6V Square wave signal (VDDIO)External Clock Source up to 50 MHz Duty Cycle: 45 to 55% **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4 MHz.**
	4/8/12MHz Fast Internal RC Oscillator	PB9/XIN and PB8/XOUT: can be left unconnected or used as GPIO	Powers up by VDDPLL 1.62V to 1.95V The output frequency is configurable through the PMC registers . The Fast RC oscillator is calibrated in production. The frequency can be trimmed by softtware Duty Cycle: 45 to 55% **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4 MHz.**

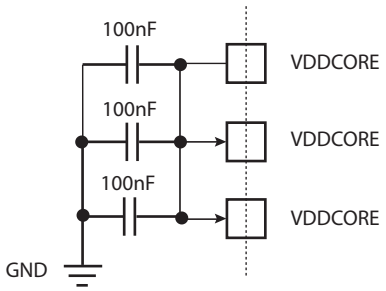
☑	Signal Name	Recommended Pin Connection	Description
	PA7/XIN32 PA8/XOUT32 32 kHz Crystal used	32.768 kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	Internal parasistic capacitance C_{para}=1pF Crystal Load Capacitance, ESR, Drive Level and Shunt Capacitance to validate. .  C_{LEXT}max=20pF C_{LEXT}= 2x($C_{crystal}$-C_{para}- C_{pcb}) Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM3S Series Datasheet. **By default at start-up the chip runs out of the embeded 32 kHz RC oscillator**
	PA7/XIN32 PA8/XOUT32 32 kHz Oscillator in bypass mode	PA7/XIN32: external clock source PA8/XOUT32: can be left unconnectde or use a GPIO.	1.62V to 3.6V Square wave signal (VDDIO) External Clock Source up to 44 kHz Duty Cycle: 45 to 55% **By default at start-up the chip runs out of the embeded 32 kHz RC oscillator**

☑	Signal Name	Recommended Pin Connection	Description
Serial Wire and JTAG[3]			
	TCK/SWCLK/PB7	Application dependant If debug mode is not required this pin can be use as GPIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TMS/SWDIO/PB6	Application dependant If debug mode is not required this pin can be use as GPIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDI/PB4	Application dependant If debug mode is not required this pin can be use as GPIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDO/ TRACESWO/PB5	Application dependant If debug mode is not required this pin can be use as GPIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	JTAGSEL	Application dependant. Must be tied to V_{VDDIO} to enter JTAG Boundary Scan. **In harsh environments, It is strongly recommended to tie this pin to GND.**	Permanent Internal pull-down resistor (15 kOhm).
Flash Memory			
	ERASE/PB12	Application dependant. If hardware erase is not required this pin can be use as GPIO	Internal pull-down resistor (100kOhm). Must be tied to V_{VDDIO} to erase the General Purpose NVM bits (GPNVMx), the whole Flash content and the security bit. Reset state: Erase Input, with a 100 kOhm Internal pull down and Schmitt trigger enabled Minimum debouncing time is 220 ms.
Reset/Test			
	NRST	Application dependant. Can be connected to a push button for hardware reset.	By default, the NRST pin is configured as an input Permanent internal pull-up resistor to V_{VDDIO} (15 kOhm).
	TST	**TST pin can be left unconnected in normal mode** To enter in FFPI mode TST pin must be tied to V_{VDDIO}. **In harsh environments, It is strongly recommended to tie this pin to GND.**	Permanent internal pull-down resistor (15 kOhm).

☑	Signal Name	Recommended Pin Connection	Description
PIO			
	PAx - PBx-PCx	Application Dependant (Pulled-up on V_{VDDIO})	At reset, all PIOs are in IO or System IO mode with Schmitt trigger inputs and internal pull-up enabled. To reduce power consumption, if not used, the concerned PIO can be configured as an output and driven at '0' with internal pull-up disabled.
Parallel Capture Mode			
	PIODC0-PIODC7	Application Dependant V_{VDDIO}	Parallel Mode capture Data
	PIODCCLK	Application Dependant V_{VDDIO}	Parallel Mode capture Clock
	PIODCEN1-2	Application Dependant V_{VDDIO}	Parallel Mode capture mode enable
Analog Reference			
	ADVREF	2.0V to V_{DDIO}(*) Decoupling capacitor(s). (*)2.0V is used for 10-bit ADC resolution only. In other case the minimum ADVREF value is 2.4V.	ADVREF is a pure analog input. ADVREF is the voltage reference for the ADC,DAC and Analog comparator. To reduce power consumption, if analog features are not used, connect ADVREF to GND.
12-bit ADC			
	AD0-AD14	0 to ADVREF.	ADC Channels
	ADTRG	V_{DDIO}.	ADC External Trigger input
10-bit ADC(4)			
	AD0-AD14	0 to ADVREF.	ADC Channels
	ADTRG	V_{DDIO}.	ADC External Trigger input
12-bit DAC			
	DAC0-DAC1	1/6* ADVREF to 5/6* ADVREF	
	DACTRG	V_{DDIO}.	DAC External Trigger input
USB Device (UDP)			
	DDP/PB10	Application dependent(3) If USB device support is not required this pin can be use as GPIO	Reset State: - USB Mode - Internal Pull-down
	DDM/PB11	Application dependent(3) If USB device support is not required this pin can be use as GPIO	IReset State: - USB Mode - Internal Pull-down

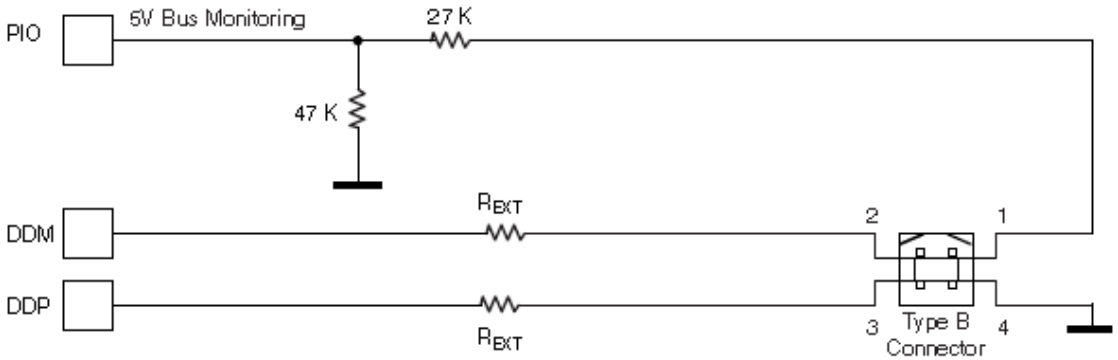
☑	Signal Name	Recommended Pin Connection	Description
Static Memory Controller (SMC)			
	D0-D15	Application dependent.	Data Bus (D0 to D15) *Note: Data bus lines are multiplexed with the PIOB controller. Their I/O line reset state is input with pull-up enabled.*
	A0-A23	Application dependent.	Address Bus (A0 to A23) *Note: Data bus lines are multiplexed with the PIOB & PIOC controllers. Their I/O line reset state is input with pull-up enabled.*
	NWAIT	Application dependent.	NWAIT pin is an active low input. *Note: NWAIT is multiplexed with PC18.*

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. USB Device Typical connection: copy of Figure 37-2 of the Datasheet

Figure 37-2. Board Schematic to Interface Device Peripheral



4. Note that the ADC voltages in 10-bit mode resolution (ADC 12-bit in low resolution) can descend to 2.0V. Only one ADC is available on the SAM3S series.

4. SAM3S Boot Program Hardware Constraints

See AT91SAM Boot Program section of the SAM3S Series Datasheet for more details on the boot program.

4.1 SAM-BA Boot

The SAM-BA® Boot Assistant supports serial communication via the UART or USB device port:

- UART0 Hardware Requirements: none.
- USB Device Hardware Requirements:

  External Crystal or External Clock(1) with frequency of:

  11,289 MHz

  12,000 MHz

  16,000 MHz

  18,432 MHz

Note: 1. Must be 2500 ppm and 1.8V Square Wave Signal

Table 4-1. Pins driven during SAM-BA Boot Program execution

Peripheral	Pin	PIO Line
UART0	URXD	PA9
UART0	UTXD	PA10

5. Revision History

Table 5-1. Revision History

Doc. Rev	Date	Comments	Change Request Ref.
11061A	28-Jul-10	First issue	

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